FUJITSU SEMICONDUCTOR
DATA SHEET

DS05-50207-1E

Stacked MCP (Multi-Chip Package) FLASH MEMORY & SRAM

CMOS

32M (× 8/×16) FLASH MEMORY & 8M (× 8/×16) STATIC RAM

MB84VD2228XEA-90/MB84VD2229XEA-90
MB84VD2228XEE-90/MB84VD2229XEE-90

■ FEATURES

- **Power supply voltage of 2.7 V to 3.3 V**
- **High performance**
  90 ns maximum access time (Flash)
  70 ns maximum access time (SRAM)
- **Operating Temperature**
  –25°C to +85°C
- **Package 71-ball BGA**

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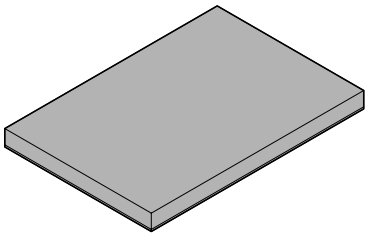
■ PRODUCT LINE UP

		Flash Memory	SRAM
Ordering Part No.	V_{CCf}, V_{CCS}= 3.0V $^{+0.3\ V}_{-0.3\ V}$	MB84VD2228XEA/EE-90/MB84VD2229XEA/EE-90	
Max. Address Access Time (ns)		90	70
Max. $\overline{CE}$ Access Time (ns)		90	70
Max. $\overline{OE}$ Access Time (ns)		40	35

■ PACKAGE

71-ball plastic FBGA



(BGA-71P-M01)

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1.FLASH MEMORY

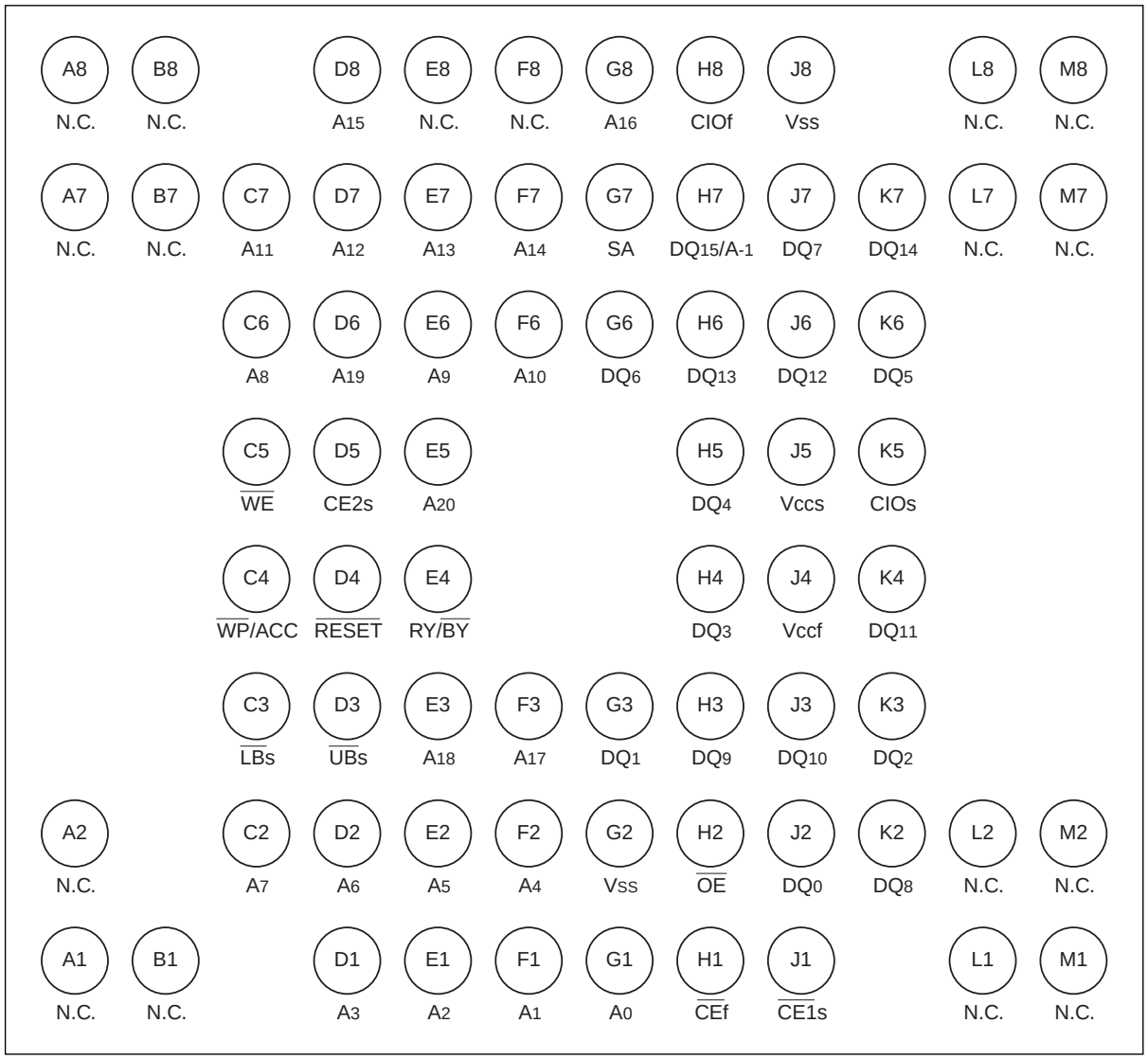
- **Simultaneous Read/Write operations (dual bank)**
  Multiple devices available with different bank sizes
  Host system can program or erase in one bank, then immediately and simultaneously read from the other bank
  Zero latency between read and write operations
  Read-while-erase
  Read-while-program
- **Minimum 100,000 write/erase cycles**
- **Sector erase architecture**
  Eight 4 K words and sixty three 32 K words.
  Any combination of sectors can be concurrently erased. Also supports full chip erase.
- **Boot Code Sector Architecture**
  MB84VD2228X: Top sector
  MB84VD2229X: Bottom sector
- **Embedded Erase™ Algorithms**
  Automatically pre-programs and erases the chip or any sector
- **Embedded Program™ Algorithms**
  Automatically writes and verifies data at specified address
- **$\overline{\text{Data}}$ Polling and Toggle Bit feature for detection of program or erase cycle completion**
- **Ready-Busy output (RY/$\overline{\text{BY}}$)**
  Hardware method for detection of program or erase cycle completion
- **Automatic sleep mode**
  When addresses remain stable, automatically switch themselves to low power mode.
- **Low V_{CC}f write inhibit ≤ 2.5 V**
- **Hidden ROM (Hi-ROM) region**
  64K byte of Hi-ROM, accessible through a new “Hi-ROM Enable” command sequence
  Factory serialized and protected to provide a secure electronic serial number (ESN)
- **$\overline{\text{WP}}$/ACC input pin**
  At V_{IL}, allows protection of boot sectors, regardless of sector protection/unprotection status
  (MB84VD2228XEA/EE:SA69,SA70 MB84VD2229XEA/EE:SA0,SA1)
  At V_{IH}, allows removal of boot sector protection
  At V_{ACC}, program time will reduse by 40%.
- **Erase Suspend/Resume**
  Suspends the erase operation to allow a read in another sector within the same device
- **Please refer to “MBM29DL32XTE/BE” data sheet in detailed function**

2.SRAM

- **Power dissipation**
  Operating : 50 mA max.
  Standby : 25 µA max.
- **Power down features using $\overline{\text{CE1}}$s and CE2s**
- **Data retention supply voltage: 1.5 V to 3.3 V**
- **$\overline{\text{CE1}}$s and CE2s Chip Select**
- **Byte data control: $\overline{\text{LB}}$s (DQ_0 to DQ_7), $\overline{\text{UB}}$s (DQ_8 to DQ_{15})**

■ PIN ASSIGNMENT

(Top View)
Marking side



(BGA-71P-M01)

■ PIN DESCRIPTION

Pin no.	Pin Name	Function	Input/Output
G1	A_0	Address Inputs (Common)	I
F1	A_1		
E1	A_2		
D1	A_3		
F2	A_4		
E2	A_5		
D2	A_6		
C2	A_7		
C6	A_8		
E6	A_9		
F6	A_{10}		
C7	A_{11}		
D7	A_{12}		
E7	A_{13}		
F7	A_{14}		
D8	A_{15}		
G8	A_{16}		
F3	A_{17}		
E3	A_{18}		
H7	A_{-1}	Address Input (Flash)	I
D6	A_{19}		
E5	A_{20}		
G7	SA	Address Input (SRAM)	I

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Pin no.	Pin Name	Function	Input/Output
J2	DQ_0	Data Inputs / Outputs (Common)	I/O
G3	DQ_1		
K3	DQ_2		
H4	DQ_3		
H5	DQ_4		
K6	DQ_5		
G6	DQ_6		
J7	DQ_7		
K2	DQ_8		
H3	DQ_9		
J3	DQ_{10}		
K4	DQ_{11}		
J6	DQ_{12}		
H6	DQ_{13}		
K7	DQ_{14}		
H7	DQ_{15}		
H1	$\overline{CE}$f	Chip Enable (Flash)	I
J1	$\overline{CE1}$s	Chip Enable (SRAM)	I
D5	CE2s	Chip Enable (SRAM)	I
H2	$\overline{OE}$	Output Enable (Common)	I
C5	$\overline{WE}$	Write Enable (Common)	I
E4	RY/$\overline{BY}$	Ready/Busy Outputs (Flash) Open Drain Output	O
D3	$\overline{UB}$s	Upper Byte Control (SRAM)	I
C3	$\overline{LB}$s	Lower Byte Control (SRAM)	I
H8	CIOf	I/O Configuration (Flash) CIOf=V_{CC}f is Word mode (×16), CIOf=V_{SS} is Byte mode (× 8)	I
K5	CIOs	I/O Configuration (SRAM) CIOs=V_{CC}s is Word mode (×16), CIOs=V_{SS} is Byte mode (× 8)	I
D4	$\overline{RESET}$	Hardware Reset Pin / Sector Protection Unlock (Flash)	I
C4	$\overline{WP}$/ACC	Write Protect / Acceleration (Flash)	I

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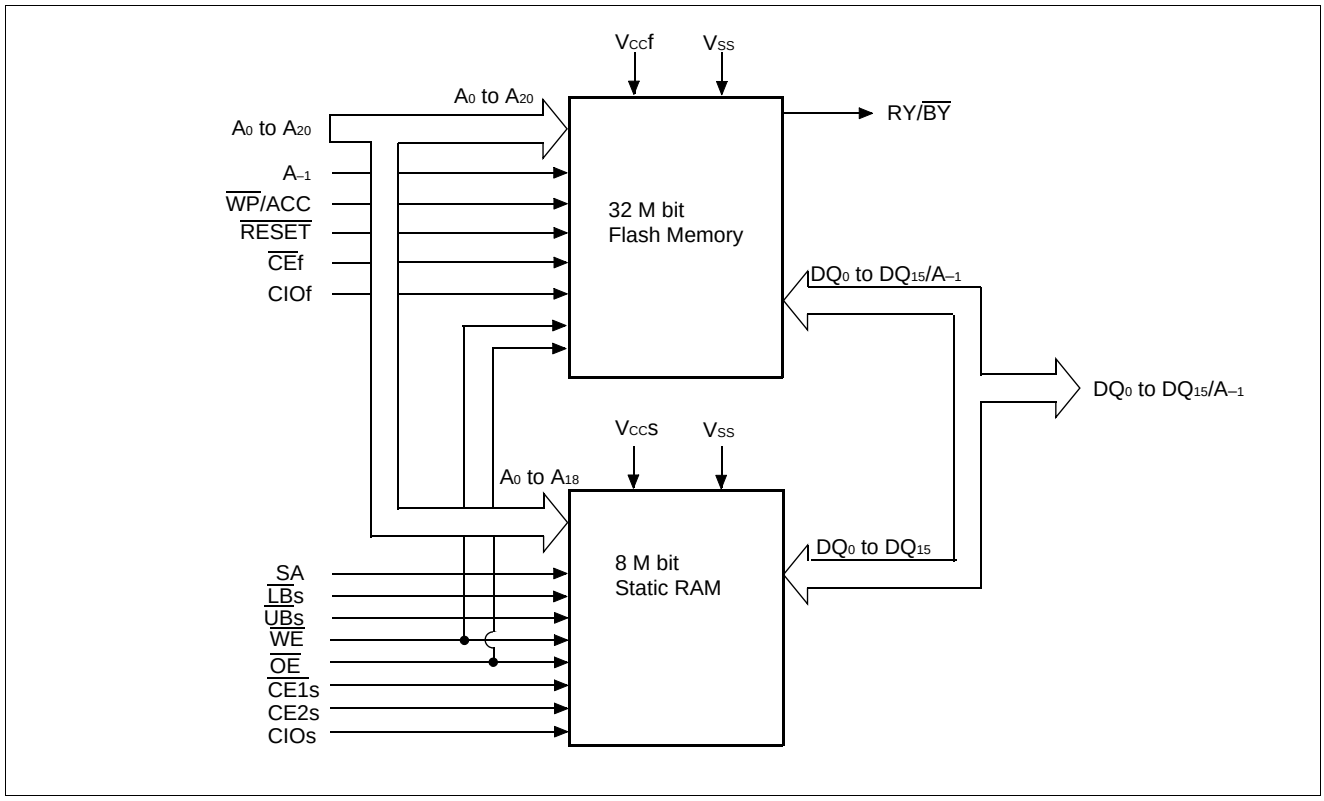
Pin no.	Pin Name	Function	Input/Output
A1,A2,A7,A8 B1,B7,B8, E8,F8, L1,L2,L7,L8, M1,M2,M7,M8	N.C.	No Internal Connection	—
J8,G2	V_{SS}	Device Ground (Common)	Power
J4	$V_{CC}f$	Device Power Supply (Flash)	Power
J5	$V_{CC}s$	Device Power Supply (SRAM)	Power

■ BLOCK DIAGRAM



■ DEVICE BUS OPERATIONS

Table 1. 1 User Bus Operations (Flash=Word mode; CIOf=V_{CC}f, SRAM=Word mode; CIOs=V_{CC}s)

Operation (1), (3)	$\overline{CE}$f	$\overline{CE1}$s	CE2s	$\overline{OE}$	$\overline{WE}$	SA (6)	$\overline{LB}$s	$\overline{UB}$s	DQ_0 to DQ_7	DQ_8 to DQ_{15}	$\overline{RESET}$	$\overline{WP}$/ ACC (5)
Full Standby	H	H	X	X	X	X	X	X	HIGH-Z	HIGH-Z	H	X
		X	L									
Output Disable	H	L	H	H	H	X	X	X	HIGH-Z	HIGH-Z	H	X
				X	X	X	H	H	HIGH-Z	HIGH-Z		
	L	H	X	H	H	X	X	X	HIGH-Z	HIGH-Z		
		X	L									
Read from Flash (2)	L	H	X	L	H	X	X	X	D_{OUT}	D_{OUT}	H	X
		X	L									
Write to Flash	L	H	X	H	L	X	X	X	D_{IN}	D_{IN}	H	X
		X	L									
Read from SRAM	H	L	H	L	H	X	L	L	D_{OUT}	D_{OUT}	H	X
							H	L	HIGH-Z	D_{OUT}		
							L	H	D_{OUT}	HIGH-Z		
Write to SRAM	H	L	H	X	L	X	L	L	D_{IN}	D_{IN}	H	X
							H	L	HIGH-Z	D_{IN}		
							L	H	D_{IN}	HIGH-Z		
Temporary Sector Group Unprotection(4)	X	X	X	X	X	X	X	X	X	X	V_{ID}	X
Flash Hardware Reset	X	H	X	X	X	X	X	X	HIGH-Z	HIGH-Z	L	X
		X	L									
Boot Block Sector Write Protection	X	X	X	X	X	X	X	X	X	X	X	L

Legend: L = V_{IL}, H = V_{IH}, X = V_{IL} or V_{IH}. See DC Characteristics for voltage levels.

Notes: 1. Other operations except for indicated this column are inhibited.
2. $\overline{WE}$ can be V_{IL} if $\overline{OE}$ is V_{IL}, $\overline{OE}$ at V_{IH} initiates the write operations.
3. Do not apply $\overline{CE}$f = V_{IL}, $\overline{CE1}$s = V_{IL} and CE2s = V_{IH} at a time.
4. It is also used for the extended sector group protections.
5. $\overline{WP}$/ACC = V_{IL}; protection of boot sectors.
$\overline{WP}$/ACC = V_{IH}; removal of boot sectors protection.
$\overline{WP}$/ACC = V_{ACC} (9V) ; Program time will reduce by 40%.
6. SA; Don't care or Open.

Table 1. 2 User Bus Operations (Flash=Word mode; CIOf=V_{CC}f, SRAM=Byte mode; CIOs=V_{SS})

Operation (1), (3)	$\overline{CE}$f	$\overline{CE1}$s	CE2s	$\overline{OE}$	$\overline{WE}$	SA	$\overline{LB}$s (6)	$\overline{UB}$s (6)	DQ_0 to DQ_7	DQ_8 to DQ_{15}	$\overline{RESET}$	$\overline{WP}$/ ACC (5)
Full Standby	H	H	X	X	X	X	X	X	HIGH-Z	HIGH-Z	H	X
		X	L									
Output Disable	H	L	H	H	H	X	X	X	HIGH-Z	HIGH-Z	H	X
				X	X	X	X	X	HIGH-Z	HIGH-Z		
	L	H	X	H	H	X	X	X	HIGH-Z	HIGH-Z		
		X	L									
Read from Flash (2)	L	H	X	L	H	X	X	X	D_{OUT}	D_{OUT}	H	X
		X	L									
Write to Flash	L	H	X	H	L	X	X	X	D_{IN}	D_{IN}	H	X
		X	L									
Read from SRAM	H	L	H	L	H	SA	X	X	D_{OUT}	HIGH-Z	H	X
Write to SRAM	H	L	H	X	L	SA	X	X	D_{IN}	HIGH-Z	H	X
Temporary Sector Group Unprotection(4)	X	X	X	X	X	X	X	X	X	X	V_{ID}	X
Flash Hardware Reset	X	H	X	X	X	X	X	X	HIGH-Z	HIGH-Z	L	X
		X	L									
Boot Block Sector Write Protection	X	X	X	X	X	X	X	X	X	X	X	L

Legend: L = V_{IL}, H = V_{IH}, X = V_{IL} or V_{IH}. See DC Characteristics for voltage levels.

Notes: 1. Other operations except for indicated this column are inhibited.
2. $\overline{WE}$ can be V_{IL} if $\overline{OE}$ is V_{IL}, $\overline{OE}$ at V_{IH} initiates the write operations.
3. Do not apply $\overline{CE}$f = V_{IL}, $\overline{CE1}$s = V_{IL} and CE2s = V_{IH} at a time.
4. It is also used for the extended sector group protections.
5. $\overline{WP}$/ACC = V_{IL}; protection of boot sectors.
$\overline{WP}$/ACC = V_{IH}; removal of boot sectors protection.
$\overline{WP}$/ACC = V_{ACC} (9V); Program time will reduce by 40%.
6. $\overline{LB}$s , $\overline{UB}$s; Don't care or Open.

Table 1. 3 User Bus Operations (Flash=Byte mode; CIOf=V_{SS}, SRAM=Byte mode; CIOs=V_{SS})

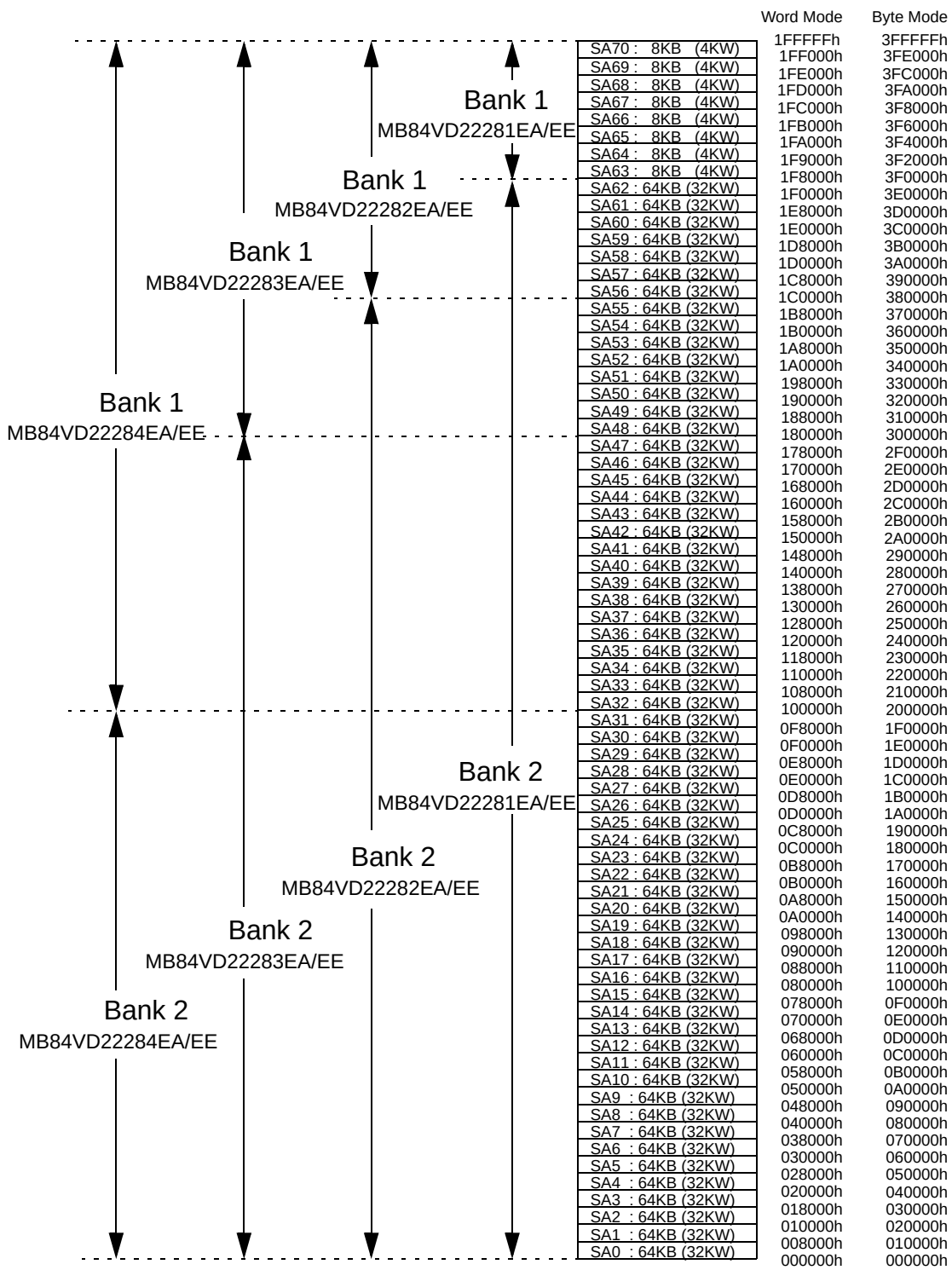
Operation (1), (3)	$\overline{CE}$f	$\overline{CE1}$s	CE2s	DQ_{15}/A_{-1}	$\overline{OE}$	$\overline{WE}$	SA	$\overline{LB}$s (6)	$\overline{UB}$s (6)	DQ_0 to DQ_7	DQ_8 to DQ_{14}	$\overline{RESET}$	$\overline{WP}$/ ACC (5)
Full Standby	H	H	X	X	X	X	X	X	X	HIGH-Z	HIGH-Z	H	X
		X	L										
Output Disable	H	L	H	X	H	H	X	X	X	HIGH-Z	HIGH-Z	H	X
				X	X	X	X	X	X	HIGH-Z	HIGH-Z		
	L	H	X	A_{-1}	H	H	X	X	X	HIGH-Z	HIGH-Z		
		X	L										
Read from Flash (2)	L	H	X	A_{-1}	L	H	X	X	X	D_{OUT}	X	H	X
		X	L										
Write to Flash	L	H	X	A_{-1}	H	L	X	X	X	D_{IN}	X	H	X
		X	L										
Read from SRAM	H	L	H	X	L	H	SA	X	X	D_{OUT}	HIGH-Z	H	X
Write to SRAM	H	L	H	X	X	L	SA	X	X	D_{IN}	HIGH-Z	H	X
Temporary Sector Group Unprotection(4)	X	X	X	X	X	X	X	X	X	X	X	V_{ID}	X
Flash Hardware Reset	X	H	X	X	X	X	X	X	X	HIGH-Z	HIGH-Z	L	X
		X	L										
Boot Block Sector Write Protection	X	X	X	X	X	X	X	X	X	X	X	X	L

Legend: L = V_{IL}, H = V_{IH}, X = V_{IL} or V_{IH}. See DC Characteristics for voltage levels.

Notes:
1. Other operations except for indicated this column are inhibited.
2. $\overline{WE}$ can be V_{IL} if $\overline{OE}$ is V_{IL}, $\overline{OE}$ at V_{IH} initiates the write operations.
3. Do not apply $\overline{CE}$f = V_{IL}, $\overline{CE1}$s = V_{IL} and CE2s = V_{IH} at a time.
4. It is also used for the extended sector group protections.
5. $\overline{WP}$/ACC = V_{IL}; protection of boot sectors.
   $\overline{WP}$/ACC = V_{IH}; removal of boot sectors protection.
   $\overline{WP}$/ACC = V_{ACC} (9V); Program time will reduce by 40%.
6. $\overline{LB}$s , $\overline{UB}$s; Don't care or Open.

■ FLEXIBLE SECTOR-ERASE ARCHITECTURE on FLASH MEMORY

- Eight 4 K words, and sixty three 32 K words.
- Individual-sector, multiple-sector, or bulk-erase capability.



	Word Mode	Byte Mode
SA70 : 8KB (4KW)	1FFFFFh	3FFFFFh
SA69 : 8KB (4KW)	1FF000h	3FE000h
SA68 : 8KB (4KW)	1FE000h	3FC000h
SA67 : 8KB (4KW)	1FD000h	3FA000h
SA66 : 8KB (4KW)	1FC000h	3F8000h
SA65 : 8KB (4KW)	1FB000h	3F6000h
SA64 : 8KB (4KW)	1FA000h	3F4000h
SA63 : 8KB (4KW)	1F9000h	3F2000h
SA62 : 64KB (32KW)	1F8000h	3F0000h
SA61 : 64KB (32KW)	1F0000h	3E0000h
SA60 : 64KB (32KW)	1E8000h	3D0000h
SA59 : 64KB (32KW)	1E0000h	3C0000h
SA58 : 64KB (32KW)	1D8000h	3B0000h
SA57 : 64KB (32KW)	1D0000h	3A0000h
SA56 : 64KB (32KW)	1C8000h	390000h
SA55 : 64KB (32KW)	1C0000h	380000h
SA54 : 64KB (32KW)	1B8000h	370000h
SA53 : 64KB (32KW)	1B0000h	360000h
SA52 : 64KB (32KW)	1A8000h	350000h
SA51 : 64KB (32KW)	1A0000h	340000h
SA50 : 64KB (32KW)	198000h	330000h
SA49 : 64KB (32KW)	190000h	320000h
SA48 : 64KB (32KW)	188000h	310000h
SA47 : 64KB (32KW)	180000h	300000h
SA46 : 64KB (32KW)	178000h	2F0000h
SA45 : 64KB (32KW)	170000h	2E0000h
SA44 : 64KB (32KW)	168000h	2D0000h
SA43 : 64KB (32KW)	160000h	2C0000h
SA42 : 64KB (32KW)	158000h	2B0000h
SA41 : 64KB (32KW)	150000h	2A0000h
SA40 : 64KB (32KW)	148000h	290000h
SA39 : 64KB (32KW)	140000h	280000h
SA38 : 64KB (32KW)	138000h	270000h
SA37 : 64KB (32KW)	130000h	260000h
SA36 : 64KB (32KW)	128000h	250000h
SA35 : 64KB (32KW)	120000h	240000h
SA34 : 64KB (32KW)	118000h	230000h
SA33 : 64KB (32KW)	110000h	220000h
SA32 : 64KB (32KW)	108000h	210000h
SA31 : 64KB (32KW)	100000h	200000h
SA30 : 64KB (32KW)	0F8000h	1F0000h
SA29 : 64KB (32KW)	0F0000h	1E0000h
SA28 : 64KB (32KW)	0E8000h	1D0000h
SA27 : 64KB (32KW)	0E0000h	1C0000h
SA26 : 64KB (32KW)	0D8000h	1B0000h
SA25 : 64KB (32KW)	0D0000h	1A0000h
SA24 : 64KB (32KW)	0C8000h	190000h
SA23 : 64KB (32KW)	0C0000h	180000h
SA22 : 64KB (32KW)	0B8000h	170000h
SA21 : 64KB (32KW)	0B0000h	160000h
SA20 : 64KB (32KW)	0A8000h	150000h
SA19 : 64KB (32KW)	0A0000h	140000h
SA18 : 64KB (32KW)	098000h	130000h
SA17 : 64KB (32KW)	090000h	120000h
SA16 : 64KB (32KW)	088000h	110000h
SA15 : 64KB (32KW)	080000h	100000h
SA14 : 64KB (32KW)	078000h	0F0000h
SA13 : 64KB (32KW)	070000h	0E0000h
SA12 : 64KB (32KW)	068000h	0D0000h
SA11 : 64KB (32KW)	060000h	0C0000h
SA10 : 64KB (32KW)	058000h	0B0000h
SA9 : 64KB (32KW)	050000h	0A0000h
SA8 : 64KB (32KW)	048000h	090000h
SA7 : 64KB (32KW)	040000h	080000h
SA6 : 64KB (32KW)	038000h	070000h
SA5 : 64KB (32KW)	030000h	060000h
SA4 : 64KB (32KW)	028000h	050000h
SA3 : 64KB (32KW)	020000h	040000h
SA2 : 64KB (32KW)	018000h	030000h
SA1 : 64KB (32KW)	010000h	020000h
SA0 : 64KB (32KW)	008000h	010000h
	000000h	000000h

MB84VD2228XEA/EE Sector Architecture (Top Boot Block)

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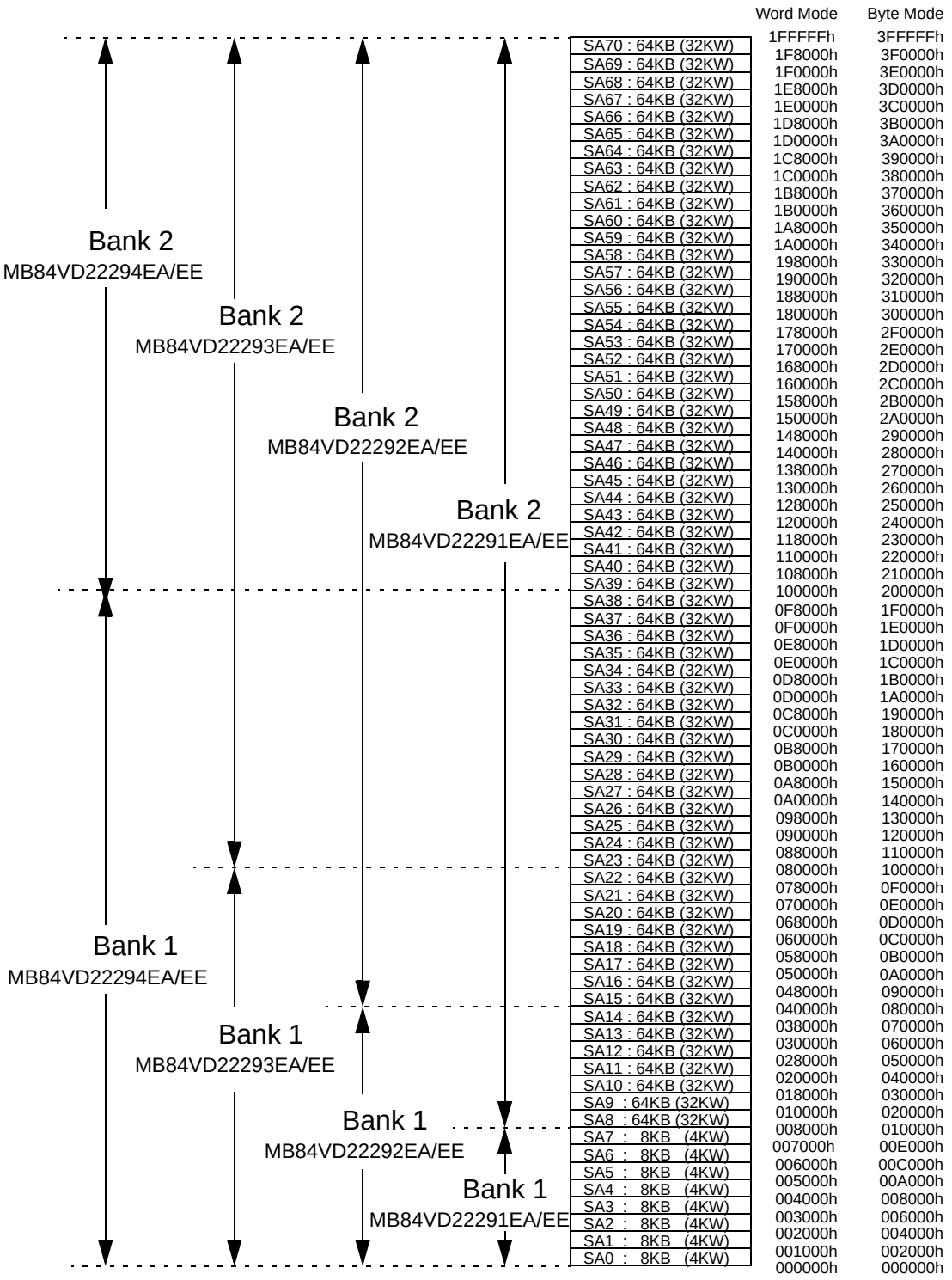

	Word Mode	Byte Mode
SA70 : 64KB (32KW)	1FFFFFh	3FFFFFh
SA69 : 64KB (32KW)	1F8000h	3F0000h
SA68 : 64KB (32KW)	1F0000h	3E0000h
SA67 : 64KB (32KW)	1E8000h	3D0000h
SA66 : 64KB (32KW)	1E0000h	3C0000h
SA65 : 64KB (32KW)	1D8000h	3B0000h
SA64 : 64KB (32KW)	1D0000h	3A0000h
SA63 : 64KB (32KW)	1C8000h	390000h
SA62 : 64KB (32KW)	1C0000h	380000h
SA61 : 64KB (32KW)	1B8000h	370000h
SA60 : 64KB (32KW)	1B0000h	360000h
SA59 : 64KB (32KW)	1A8000h	350000h
SA58 : 64KB (32KW)	1A0000h	340000h
SA57 : 64KB (32KW)	198000h	330000h
SA56 : 64KB (32KW)	190000h	320000h
SA55 : 64KB (32KW)	188000h	310000h
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SA51 : 64KB (32KW)	168000h	2D0000h
SA50 : 64KB (32KW)	160000h	2C0000h
SA49 : 64KB (32KW)	158000h	2B0000h
SA48 : 64KB (32KW)	150000h	2A0000h
SA47 : 64KB (32KW)	148000h	290000h
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SA44 : 64KB (32KW)	130000h	260000h
SA43 : 64KB (32KW)	128000h	250000h
SA42 : 64KB (32KW)	120000h	240000h
SA41 : 64KB (32KW)	118000h	230000h
SA40 : 64KB (32KW)	110000h	220000h
SA39 : 64KB (32KW)	108000h	210000h
SA38 : 64KB (32KW)	100000h	200000h
SA37 : 64KB (32KW)	0F8000h	1F0000h
SA36 : 64KB (32KW)	0F0000h	1E0000h
SA35 : 64KB (32KW)	0E8000h	1D0000h
SA34 : 64KB (32KW)	0E0000h	1C0000h
SA33 : 64KB (32KW)	0D8000h	1B0000h
SA32 : 64KB (32KW)	0D0000h	1A0000h
SA31 : 64KB (32KW)	0C8000h	190000h
SA30 : 64KB (32KW)	0C0000h	180000h
SA29 : 64KB (32KW)	0B8000h	170000h
SA28 : 64KB (32KW)	0B0000h	160000h
SA27 : 64KB (32KW)	0A8000h	150000h
SA26 : 64KB (32KW)	0A0000h	140000h
SA25 : 64KB (32KW)	098000h	130000h
SA24 : 64KB (32KW)	090000h	120000h
SA23 : 64KB (32KW)	088000h	110000h
SA22 : 64KB (32KW)	080000h	100000h
SA21 : 64KB (32KW)	078000h	0F0000h
SA20 : 64KB (32KW)	070000h	0E0000h
SA19 : 64KB (32KW)	068000h	0D0000h
SA18 : 64KB (32KW)	060000h	0C0000h
SA17 : 64KB (32KW)	058000h	0B0000h
SA16 : 64KB (32KW)	050000h	0A0000h
SA15 : 64KB (32KW)	048000h	090000h
SA14 : 64KB (32KW)	040000h	080000h
SA13 : 64KB (32KW)	038000h	070000h
SA12 : 64KB (32KW)	030000h	060000h
SA11 : 64KB (32KW)	028000h	050000h
SA10 : 64KB (32KW)	020000h	040000h
SA9 : 64KB (32KW)	018000h	030000h
SA8 : 64KB (32KW)	010000h	020000h
SA7 : 8KB (4KW)	008000h	010000h
SA6 : 8KB (4KW)	007000h	00E000h
SA5 : 8KB (4KW)	006000h	00C000h
SA4 : 8KB (4KW)	005000h	00A000h
SA3 : 8KB (4KW)	004000h	008000h
SA2 : 8KB (4KW)	003000h	006000h
SA1 : 8KB (4KW)	002000h	004000h
SA0 : 8KB (4KW)	001000h	002000h
	000000h	000000h

MB84VD2229XEA/EE Sector Architecture (Bottom Boot Block)

Table 2. 1 Sector Address Tables (MB84VD22281EA/EE)

Bank	Sector	Sector Address										Address Range (BYTE mode)	Address Range (WORD mode)
		Bank Address											
		A_{20}	A_{19}	A_{18}	A_{17}	A_{16}	A_{15}	A_{14}	A_{13}	A_{12}	A_{11}		
Bank 2	SA0	0	0	0	0	0	0	X	X	X	X	000000h to 00FFFFh	000000h to 007FFFh
	SA1	0	0	0	0	0	1	X	X	X	X	010000h to 01FFFFh	008000h to 00FFFFh
	SA2	0	0	0	0	1	0	X	X	X	X	020000h to 02FFFFh	010000h to 017FFFh
	SA3	0	0	0	0	1	1	X	X	X	X	030000h to 03FFFFh	018000h to 01FFFFh
	SA4	0	0	0	1	0	0	X	X	X	X	040000h to 04FFFFh	020000h to 027FFFh
	SA5	0	0	0	1	0	1	X	X	X	X	050000h to 05FFFFh	028000h to 02FFFFh
	SA6	0	0	0	1	1	0	X	X	X	X	060000h to 06FFFFh	030000h to 037FFFh
	SA7	0	0	0	1	1	1	X	X	X	X	070000h to 07FFFFh	038000h to 03FFFFh
	SA8	0	0	1	0	0	0	X	X	X	X	080000h to 08FFFFh	040000h to 047FFFh
	SA9	0	0	1	0	0	1	X	X	X	X	090000h to 09FFFFh	048000h to 04FFFFh
	SA10	0	0	1	0	1	0	X	X	X	X	0A0000h to 0AFFFFh	050000h to 057FFFh
	SA11	0	0	1	0	1	1	X	X	X	X	0B0000h to 0BFFFFh	058000h to 05FFFFh
	SA12	0	0	1	1	0	0	X	X	X	X	0C0000h to 0CFFFFh	060000h to 067FFFh
	SA13	0	0	1	1	0	1	X	X	X	X	0D0000h to 0DFFFFh	068000h to 06FFFFh
	SA14	0	0	1	1	1	0	X	X	X	X	0E0000h to 0EFFFFh	070000h to 077FFFh
	SA15	0	0	1	1	1	1	X	X	X	X	0F0000h to 0FFFFFh	078000h to 07FFFFh
	SA16	0	1	0	0	0	0	X	X	X	X	100000h to 10FFFFh	080000h to 087FFFh
	SA17	0	1	0	0	0	1	X	X	X	X	110000h to 11FFFFh	088000h to 08FFFFh
	SA18	0	1	0	0	1	0	X	X	X	X	120000h to 12FFFFh	090000h to 097FFFh
	SA19	0	1	0	0	1	1	X	X	X	X	130000h to 13FFFFh	098000h to 09FFFFh
	SA20	0	1	0	1	0	0	X	X	X	X	140000h to 14FFFFh	0A0000h to 0A7FFFh
	SA21	0	1	0	1	0	1	X	X	X	X	150000h to 15FFFFh	0A8000h to 0AFFFFh
	SA22	0	1	0	1	1	0	X	X	X	X	160000h to 16FFFFh	0B0000h to 0B7FFFh
	SA23	0	1	0	1	1	1	X	X	X	X	170000h to 17FFFFh	0B8000h to 0BFFFFh
	SA24	0	1	1	0	0	0	X	X	X	X	180000h to 18FFFFh	0C0000h to 0C7FFFh
	SA25	0	1	1	0	0	1	X	X	X	X	190000h to 19FFFFh	0C8000h to 0CFFFFh
	SA26	0	1	1	0	1	0	X	X	X	X	1A0000h to 1AFFFFh	0D0000h to 0D7FFFh
	SA27	0	1	1	0	1	1	X	X	X	X	1B0000h to 1BFFFFh	0D8000h to 0DFFFFh
	SA28	0	1	1	1	0	0	X	X	X	X	1C0000h to 1CFFFFh	0E0000h to 0E7FFFh
	SA29	0	1	1	1	0	1	X	X	X	X	1D0000h to 1DFFFFh	0E8000h to 0EFFFFh
	SA30	0	1	1	1	1	0	X	X	X	X	1E0000h to 1EFFFFh	0F0000h to 0F7FFFh
	SA31	0	1	1	1	1	1	X	X	X	X	1F0000h to 1FFFFFh	0F8000h to 0FFFFFh

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Bank	Sector	Sector Address										Address Range (BYTE mode)	Address Range (WORD mode)
		Bank Address											
		A_{20}	A_{19}	A_{18}	A_{17}	A_{16}	A_{15}	A_{14}	A_{13}	A_{12}	A_{11}		
Bank 2	SA32	1	0	0	0	0	0	X	X	X	X	200000h to 20FFFFh	100000h to 107FFFh
	SA33	1	0	0	0	0	1	X	X	X	X	210000h to 21FFFFh	108000h to 10FFFFh
	SA34	1	0	0	0	1	0	X	X	X	X	220000h to 22FFFFh	110000h to 117FFFh
	SA35	1	0	0	0	1	1	X	X	X	X	230000h to 23FFFFh	118000h to 11FFFFh
	SA36	1	0	0	1	0	0	X	X	X	X	240000h to 24FFFFh	120000h to 127FFFh
	SA37	1	0	0	1	0	1	X	X	X	X	250000h to 25FFFFh	128000h to 12FFFFh
	SA38	1	0	0	1	1	0	X	X	X	X	260000h to 26FFFFh	130000h to 137FFFh
	SA39	1	0	0	1	1	1	X	X	X	X	270000h to 27FFFFh	138000h to 13FFFFh
	SA40	1	0	1	0	0	0	X	X	X	X	280000h to 28FFFFh	140000h to 147FFFh
	SA41	1	0	1	0	0	1	X	X	X	X	290000h to 29FFFFh	148000h to 14FFFFh
	SA42	1	0	1	0	1	0	X	X	X	X	2A0000h to 2AFFFFh	150000h to 157FFFh
	SA43	1	0	1	0	1	1	X	X	X	X	2B0000h to 2BFFFFh	158000h to 15FFFFh
	SA44	1	0	1	1	0	0	X	X	X	X	2C0000h to 2CFFFFh	160000h to 167FFFh
	SA45	1	0	1	1	0	1	X	X	X	X	2D0000h to 2DFFFFh	168000h to 16FFFFh
	SA46	1	0	1	1	1	0	X	X	X	X	2E0000h to 2EFFFFh	170000h to 177FFFh
	SA47	1	0	1	1	1	1	X	X	X	X	2F0000h to 2FFFFFh	178000h to 17FFFFh
	SA48	1	1	0	0	0	0	X	X	X	X	300000h to 30FFFFh	180000h to 187FFFh
	SA49	1	1	0	0	0	1	X	X	X	X	310000h to 31FFFFh	188000h to 18FFFFh
	SA50	1	1	0	0	1	0	X	X	X	X	320000h to 32FFFFh	190000h to 197FFFh
	SA51	1	1	0	0	1	1	X	X	X	X	330000h to 33FFFFh	198000h to 19FFFFh
	SA52	1	1	0	1	0	0	X	X	X	X	340000h to 34FFFFh	1A0000h to 1A7FFFh
	SA53	1	1	0	1	0	1	X	X	X	X	350000h to 35FFFFh	1A8000h to 1AFFFFh
	SA54	1	1	0	1	1	0	X	X	X	X	360000h to 36FFFFh	1B0000h to 1B7FFFh
	SA55	1	1	0	1	1	1	X	X	X	X	370000h to 37FFFFh	1B8000h to 1BFFFFh
	SA56	1	1	1	0	0	0	X	X	X	X	380000h to 38FFFFh	1C0000h to 1C7FFFh
	SA57	1	1	1	0	0	1	X	X	X	X	390000h to 39FFFFh	1C8000h to 1CFFFFh
	SA58	1	1	1	0	1	0	X	X	X	X	3A0000h to 3AFFFFh	1D0000h to 1D7FFFh
	SA59	1	1	1	0	1	1	X	X	X	X	3B0000h to 3BFFFFh	1D8000h to 1DFFFFh
	SA60	1	1	1	1	0	0	X	X	X	X	3C0000h to 3CFFFFh	1E0000h to 1E7FFFh
	SA61	1	1	1	1	0	1	X	X	X	X	3D0000h to 3DFFFFh	1E8000h to 1EFFFFh
	SA62	1	1	1	1	1	0	X	X	X	X	3E0000h to 3EFFFFh	1F0000h to 1F7FFFh
Bank 1	SA63	1	1	1	1	1	1	0	0	0	X	3F0000h to 3F1FFFh	1F8000h to 1F8FFFh
	SA64	1	1	1	1	1	1	0	0	1	X	3F2000h to 3F3FFFh	1F9000h to 1F9FFFh
	SA65	1	1	1	1	1	1	0	1	0	X	3F4000h to 3F5FFFh	1FA000h to 1FAFFFh
	SA66	1	1	1	1	1	1	0	1	1	X	3F6000h to 3F7FFFh	1FB000h to 1FBFFFh
	SA67	1	1	1	1	1	1	1	0	0	X	3F8000h to 3F9FFFh	1FC000h to 1FCFFFh
	SA68	1	1	1	1	1	1	1	0	1	X	3FA000h to 3FAFFFh	1FD000h to 1FDFFFh
	SA69	1	1	1	1	1	1	1	1	0	X	3FC000h to 3FCFFFh	1FE000h to 1FEFFFh
	SA70	1	1	1	1	1	1	1	1	1	X	3FE000h to 3FFFFFh	1FF000h to 1FFFFFh

Table 2. 2 Sector Address Tables (MB84VD22291EA/EE)

Bank	Sector	Sector Address										Address Range (BYTE mode)	Address Range (WORD mode)
		Band Address											
		A_{20}	A_{19}	A_{18}	A_{17}	A_{16}	A_{15}	A_{14}	A_{13}	A_{12}	A_{11}		
Bank 1	SA0	0	0	0	0	0	0	0	0	0	X	000000h to 001FFFh	000000h to 000FFFh
	SA1	0	0	0	0	0	0	0	0	1	X	002000h to 003FFFh	001000h to 001FFFh
	SA2	0	0	0	0	0	0	0	1	0	X	004000h to 005FFFh	002000h to 002FFFh
	SA3	0	0	0	0	0	0	0	1	1	X	006000h to 007FFFh	003000h to 003FFFh
	SA4	0	0	0	0	0	0	1	0	0	X	008000h to 009FFFh	004000h to 004FFFh
	SA5	0	0	0	0	0	0	1	0	1	X	00A000h to 00BFFFh	005000h to 005FFFh
	SA6	0	0	0	0	0	0	1	1	0	X	00C000h to 00DFFFh	006000h to 006FFFh
	SA7	0	0	0	0	0	0	1	1	1	X	00E000h to 00FFFFh	007000h to 007FFFh
Bank 2	SA8	0	0	0	0	0	1	X	X	X	X	010000h to 01FFFFh	008000h to 00FFFFh
	SA9	0	0	0	0	1	0	X	X	X	X	020000h to 02FFFFh	010000h to 017FFFh
	SA10	0	0	0	0	1	1	X	X	X	X	030000h to 03FFFFh	018000h to 01FFFFh
	SA11	0	0	0	1	0	0	X	X	X	X	040000h to 04FFFFh	020000h to 027FFFh
	SA12	0	0	0	1	0	1	X	X	X	X	050000h to 05FFFFh	028000h to 02FFFFh
	SA13	0	0	0	1	1	0	X	X	X	X	060000h to 06FFFFh	030000h to 037FFFh
	SA14	0	0	0	1	1	1	X	X	X	X	070000h to 07FFFFh	038000h to 03FFFFh
	SA15	0	0	1	0	0	0	X	X	X	X	080000h to 08FFFFh	040000h to 047FFFh
	SA16	0	0	1	0	0	1	X	X	X	X	090000h to 09FFFFh	048000h to 04FFFFh
	SA17	0	0	1	0	1	0	X	X	X	X	0A0000h to 0AFFFFh	050000h to 057FFFh
	SA18	0	0	1	0	1	1	X	X	X	X	0B0000h to 0BFFFFh	058000h to 05FFFFh
	SA19	0	0	1	1	0	0	X	X	X	X	0C0000h to 0CFFFFh	060000h to 067FFFh
	SA20	0	0	1	1	0	1	X	X	X	X	0D0000h to 0DFFFFh	068000h to 06FFFFh
	SA21	0	0	1	1	1	0	X	X	X	X	0E0000h to 0EFFFFh	070000h to 077FFFh
	SA22	0	0	1	1	1	1	X	X	X	X	0F0000h to 0FFFFFh	078000h to 07FFFFh
	SA23	0	1	0	0	0	0	X	X	X	X	100000h to 10FFFFh	080000h to 087FFFh
	SA24	0	1	0	0	0	1	X	X	X	X	110000h to 11FFFFh	088000h to 08FFFFh
	SA25	0	1	0	0	1	0	X	X	X	X	120000h to 12FFFFh	090000h to 097FFFh
	SA26	0	1	0	0	1	1	X	X	X	X	130000h to 13FFFFh	098000h to 09FFFFh
	SA27	0	1	0	1	0	0	X	X	X	X	140000h to 14FFFFh	0A0000h to 0A7FFFh
	SA28	0	1	0	1	0	1	X	X	X	X	150000h to 15FFFFh	0A8000h to 0AFFFFh
	SA29	0	1	0	1	1	0	X	X	X	X	160000h to 16FFFFh	0B0000h to 0B7FFFh
	SA30	0	1	0	1	1	1	X	X	X	X	170000h to 17FFFFh	0B8000h to 0BFFFFh
	SA31	0	1	1	0	0	0	X	X	X	X	180000h to 18FFFFh	0C0000h to 0C7FFFh
	SA32	0	1	1	0	0	1	X	X	X	X	190000h to 19FFFFh	0C8000h to 0CFFFFh
	SA33	0	1	1	0	1	0	X	X	X	X	1A0000h to 1AFFFFh	0D0000h to 0D7FFFh
	SA34	0	1	1	0	1	1	X	X	X	X	1B0000h to 1BFFFFh	0D8000h to 0DFFFFh
	SA35	0	1	1	1	0	0	X	X	X	X	1C0000h to 1CFFFFh	0E0000h to 0E7FFFh

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Bank	Sector	Sector Address										Address Range (BYTE mode)	Address Range (WORD mode)
		Bank Address											
		A_{20}	A_{19}	A_{18}	A_{17}	A_{16}	A_{15}	A_{14}	A_{13}	A_{12}	A_{11}		
Bank 2	SA36	0	1	1	1	0	1	X	X	X	X	1D0000h to 1DFFFFh	0E8000h to 0EFFFFh
	SA37	0	1	1	1	1	0	X	X	X	X	1E0000h to 1EFFFFh	0F0000h to 0F7FFFh
	SA38	0	1	1	1	1	1	X	X	X	X	1F0000h to 1FFFFFh	0F8000h to 0FFFFFh
	SA39	1	0	0	0	0	0	X	X	X	X	200000h to 20FFFFh	100000h to 107FFFh
	SA40	1	0	0	0	0	1	X	X	X	X	210000h to 21FFFFh	108000h to 10FFFFh
	SA41	1	0	0	0	1	0	X	X	X	X	220000h to 22FFFFh	110000h to 117FFFh
	SA42	1	0	0	0	1	1	X	X	X	X	230000h to 23FFFFh	118000h to 11FFFFh
	SA43	1	0	0	1	0	0	X	X	X	X	240000h to 24FFFFh	120000h to 127FFFh
	SA44	1	0	0	1	0	1	X	X	X	X	250000h to 25FFFFh	128000h to 12FFFFh
	SA45	1	0	0	1	1	0	X	X	X	X	260000h to 26FFFFh	130000h to 137FFFh
	SA46	1	0	0	1	1	1	X	X	X	X	270000h to 27FFFFh	138000h to 13FFFFh
	SA47	1	0	1	0	0	0	X	X	X	X	280000h to 28FFFFh	140000h to 147FFFh
	SA48	1	0	1	0	0	1	X	X	X	X	290000h to 29FFFFh	148000h to 14FFFFh
	SA49	1	0	1	0	1	0	X	X	X	X	2A0000h to 2AFFFFh	150000h to 157FFFh
	SA50	1	0	1	0	1	1	X	X	X	X	2B0000h to 2BFFFFh	158000h to 15FFFFh
	SA51	1	0	1	1	0	0	X	X	X	X	2C0000h to 2CFFFFh	160000h to 167FFFh
	SA52	1	0	1	1	0	1	X	X	X	X	2D0000h to 2DFFFFh	168000h to 16FFFFh
	SA53	1	0	1	1	1	0	X	X	X	X	2E0000h to 2EFFFFh	170000h to 177FFFh
	SA54	1	0	1	1	1	1	X	X	X	X	2F0000h to 2FFFFFh	178000h to 17FFFFh
	SA55	1	1	0	0	0	0	X	X	X	X	300000h to 30FFFFh	180000h to 187FFFh
	SA56	1	1	0	0	0	1	X	X	X	X	310000h to 31FFFFh	188000h to 18FFFFh
	SA57	1	1	0	0	1	0	X	X	X	X	320000h to 32FFFFh	190000h to 197FFFh
	SA58	1	1	0	0	1	1	X	X	X	X	330000h to 33FFFFh	198000h to 19FFFFh
	SA59	1	1	0	1	0	0	X	X	X	X	340000h to 34FFFFh	1A0000h to 1A7FFFh
	SA60	1	1	0	1	0	1	X	X	X	X	350000h to 35FFFFh	1A8000h to 1AFFFFh
	SA61	1	1	0	1	1	0	X	X	X	X	360000h to 36FFFFh	1B0000h to 1B7FFFh
	SA62	1	1	0	1	1	1	X	X	X	X	370000h to 37FFFFh	1B8000h to 1BFFFFh
	SA63	1	1	1	0	0	0	X	X	X	X	380000h to 38FFFFh	1C0000h to 1C7FFFh
	SA64	1	1	1	0	0	1	X	X	X	X	390000h to 39FFFFh	1C8000h to 1CFFFFh
	SA65	1	1	1	0	1	0	X	X	X	X	3A0000h to 3AFFFFh	1D0000h to 1D7FFFh
	SA66	1	1	1	0	1	1	X	X	X	X	3B0000h to 3BFFFFh	1D8000h to 1DFFFFh
	SA67	1	1	1	1	0	0	X	X	X	X	3C0000h to 3CFFFFh	1E0000h to 1E7FFFh
	SA68	1	1	1	1	0	1	X	X	X	X	3D0000h to 3DFFFFh	1E8000h to 1EFFFFh
	SA69	1	1	1	1	1	0	X	X	X	X	3E0000h to 3EFFFFh	1F0000h to 1F7FFFh
	SA70	1	1	1	1	1	1	X	X	X	X	3F0000h to 3FFFFFh	1F8000h to 1FFFFFh

Table 2. 3 Sector Address Tables (MB84VD22282EA/EE)

Bank	Sector	Sector Address										Address Range (BYTE mode)	Address Range (WORD mode)
		Bank Address											
		A_{20}	A_{19}	A_{18}	A_{17}	A_{16}	A_{15}	A_{14}	A_{13}	A_{12}	A_{11}		
Bank 2	SA0	0	0	0	0	0	0	X	X	X	X	000000h to 00FFFFh	000000h to 007FFFh
	SA1	0	0	0	0	0	1	X	X	X	X	010000h to 01FFFFh	008000h to 00FFFFh
	SA2	0	0	0	0	1	0	X	X	X	X	020000h to 02FFFFh	010000h to 017FFFh
	SA3	0	0	0	0	1	1	X	X	X	X	030000h to 03FFFFh	018000h to 01FFFFh
	SA4	0	0	0	1	0	0	X	X	X	X	040000h to 04FFFFh	020000h to 027FFFh
	SA5	0	0	0	1	0	1	X	X	X	X	050000h to 05FFFFh	028000h to 02FFFFh
	SA6	0	0	0	1	1	0	X	X	X	X	060000h to 06FFFFh	030000h to 037FFFh
	SA7	0	0	0	1	1	1	X	X	X	X	070000h to 07FFFFh	038000h to 03FFFFh
	SA8	0	0	1	0	0	0	X	X	X	X	080000h to 08FFFFh	040000h to 047FFFh
	SA9	0	0	1	0	0	1	X	X	X	X	090000h to 09FFFFh	048000h to 04FFFFh
	SA10	0	0	1	0	1	0	X	X	X	X	0A0000h to 0AFFFFh	050000h to 057FFFh
	SA11	0	0	1	0	1	1	X	X	X	X	0B0000h to 0BFFFFh	058000h to 05FFFFh
	SA12	0	0	1	1	0	0	X	X	X	X	0C0000h to 0CFFFFh	060000h to 067FFFh
	SA13	0	0	1	1	0	1	X	X	X	X	0D0000h to 0DFFFFh	068000h to 06FFFFh
	SA14	0	0	1	1	1	0	X	X	X	X	0E0000h to 0EFFFFh	070000h to 077FFFh
	SA15	0	0	1	1	1	1	X	X	X	X	0F0000h to 0FFFFFh	078000h to 07FFFFh
	SA16	0	1	0	0	0	0	X	X	X	X	100000h to 10FFFFh	080000h to 087FFFh
	SA17	0	1	0	0	0	1	X	X	X	X	110000h to 11FFFFh	088000h to 08FFFFh
	SA18	0	1	0	0	1	0	X	X	X	X	120000h to 12FFFFh	090000h to 097FFFh
	SA19	0	1	0	0	1	1	X	X	X	X	130000h to 13FFFFh	098000h to 09FFFFh
	SA20	0	1	0	1	0	0	X	X	X	X	140000h to 14FFFFh	0A0000h to 0A7FFFh
	SA21	0	1	0	1	0	1	X	X	X	X	150000h to 15FFFFh	0A8000h to 0AFFFFh
	SA22	0	1	0	1	1	0	X	X	X	X	160000h to 16FFFFh	0B0000h to 0B7FFFh
	SA23	0	1	0	1	1	1	X	X	X	X	170000h to 17FFFFh	0B8000h to 0BFFFFh
	SA24	0	1	1	0	0	0	X	X	X	X	180000h to 18FFFFh	0C0000h to 0C7FFFh
	SA25	0	1	1	0	0	1	X	X	X	X	190000h to 19FFFFh	0C8000h to 0CFFFFh
	SA26	0	1	1	0	1	0	X	X	X	X	1A0000h to 1AFFFFh	0D0000h to 0D7FFFh
	SA27	0	1	1	0	1	1	X	X	X	X	1B0000h to 1BFFFFh	0D8000h to 0DFFFFh
	SA28	0	1	1	1	0	0	X	X	X	X	1C0000h to 1CFFFFh	0E0000h to 0E7FFFh
	SA29	0	1	1	1	0	1	X	X	X	X	1D0000h to 1DFFFFh	0E8000h to 0EFFFFh
	SA30	0	1	1	1	1	0	X	X	X	X	1E0000h to 1EFFFFh	0F0000h to 0F7FFFh
	SA31	0	1	1	1	1	1	X	X	X	X	1F0000h to 1FFFFFh	0F8000h to 0FFFFFh

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Bank	Sector	Sector Address										Address Range (BYTE mode)	Address Range (WORD mode)
		Bank Address											
		A_{20}	A_{19}	A_{18}	A_{17}	A_{16}	A_{15}	A_{14}	A_{13}	A_{12}	A_{11}		
Bank 2	SA32	1	0	0	0	0	0	X	X	X	X	200000h to 20FFFFh	100000h to 107FFFh
	SA33	1	0	0	0	0	1	X	X	X	X	210000h to 21FFFFh	108000h to 10FFFFh
	SA34	1	0	0	0	1	0	X	X	X	X	220000h to 22FFFFh	110000h to 117FFFh
	SA35	1	0	0	0	1	1	X	X	X	X	230000h to 23FFFFh	118000h to 11FFFFh
	SA36	1	0	0	1	0	0	X	X	X	X	240000h to 24FFFFh	120000h to 127FFFh
	SA37	1	0	0	1	0	1	X	X	X	X	250000h to 25FFFFh	128000h to 12FFFFh
	SA38	1	0	0	1	1	0	X	X	X	X	260000h to 26FFFFh	130000h to 137FFFh
	SA39	1	0	0	1	1	1	X	X	X	X	270000h to 27FFFFh	138000h to 13FFFFh
	SA40	1	0	1	0	0	0	X	X	X	X	280000h to 28FFFFh	140000h to 147FFFh
	SA41	1	0	1	0	0	1	X	X	X	X	290000h to 29FFFFh	148000h to 14FFFFh
	SA42	1	0	1	0	1	0	X	X	X	X	2A0000h to 2AFFFFh	150000h to 157FFFh
	SA43	1	0	1	0	1	1	X	X	X	X	2B0000h to 2BFFFFh	158000h to 15FFFFh
	SA44	1	0	1	1	0	0	X	X	X	X	2C0000h to 2CFFFFh	160000h to 167FFFh
	SA45	1	0	1	1	0	1	X	X	X	X	2D0000h to 2DFFFFh	168000h to 16FFFFh
	SA46	1	0	1	1	1	0	X	X	X	X	2E0000h to 2EFFFFh	170000h to 177FFFh
	SA47	1	0	1	1	1	1	X	X	X	X	2F0000h to 2FFFFFh	178000h to 17FFFFh
	SA48	1	1	0	0	0	0	X	X	X	X	300000h to 30FFFFh	180000h to 187FFFh
	SA49	1	1	0	0	0	1	X	X	X	X	310000h to 31FFFFh	188000h to 18FFFFh
	SA50	1	1	0	0	1	0	X	X	X	X	320000h to 32FFFFh	190000h to 197FFFh
	SA51	1	1	0	0	1	1	X	X	X	X	330000h to 33FFFFh	198000h to 19FFFFh
	SA52	1	1	0	1	0	0	X	X	X	X	340000h to 34FFFFh	1A0000h to 1A7FFFh
	SA53	1	1	0	1	0	1	X	X	X	X	350000h to 35FFFFh	1A8000h to 1AFFFFh
	SA54	1	1	0	1	1	0	X	X	X	X	360000h to 36FFFFh	1B0000h to 1B7FFFh
	SA55	1	1	0	1	1	1	X	X	X	X	370000h to 37FFFFh	1B8000h to 1BFFFFh
Bank 1	SA56	1	1	1	0	0	0	X	X	X	X	380000h to 38FFFFh	1C0000h to 1C7FFFh
	SA57	1	1	1	0	0	1	X	X	X	X	390000h to 39FFFFh	1C8000h to 1CFFFFh
	SA58	1	1	1	0	1	0	X	X	X	X	3A0000h to 3AFFFFh	1D0000h to 1D7FFFh
	SA59	1	1	1	0	1	1	X	X	X	X	3B0000h to 3BFFFFh	1D8000h to 1DFFFFh
	SA60	1	1	1	1	0	0	X	X	X	X	3C0000h to 3CFFFFh	1E0000h to 1E7FFFh
	SA61	1	1	1	1	0	1	X	X	X	X	3D0000h to 3DFFFFh	1E8000h to 1EFFFFh
	SA62	1	1	1	1	1	0	X	X	X	X	3E0000h to 3EFFFFh	1F0000h to 1F7FFFh
	SA63	1	1	1	1	1	1	0	0	0	X	3F0000h to 3F1FFFh	1F8000h to 1F8FFFh
	SA64	1	1	1	1	1	1	0	0	1	X	3F2000h to 3F3FFFh	1F9000h to 1F9FFFh
	SA65	1	1	1	1	1	1	0	1	0	X	3F4000h to 3F5FFFh	1FA000h to 1FAFFFh
	SA66	1	1	1	1	1	1	0	1	1	X	3F6000h to 3F7FFFh	1FB000h to 1FBFFFh
	SA67	1	1	1	1	1	1	1	0	0	X	3F8000h to 3F9FFFh	1FC000h to 1FCFFFh
	SA68	1	1	1	1	1	1	1	0	1	X	3FA000h to 3FAFFFh	1FD000h to 1FDFFFh
	SA69	1	1	1	1	1	1	1	1	0	X	3FC000h to 3FCFFFh	1FE000h to 1FEFFFh
	SA70	1	1	1	1	1	1	1	1	1	X	3FE000h to 3FFFFFh	1FF000h to 1FFFFFh

Table 2. 4 Sector Address Tables (MB84VD22292EA/EE)

Bank	Sector	Sector Address										Address Range (BYTE mode)	Address Range (WORD mode)
		Bank Address											
		A_{20}	A_{19}	A_{18}	A_{17}	A_{16}	A_{15}	A_{14}	A_{13}	A_{12}	A_{11}		
Bank 1	SA0	0	0	0	0	0	0	0	0	0	X	000000h to 001FFFh	000000h to 000FFFh
	SA1	0	0	0	0	0	0	0	0	1	X	002000h to 003FFFh	001000h to 001FFFh
	SA2	0	0	0	0	0	0	0	1	0	X	004000h to 005FFFh	002000h to 002FFFh
	SA3	0	0	0	0	0	0	0	1	1	X	006000h to 007FFFh	003000h to 003FFFh
	SA4	0	0	0	0	0	0	1	0	0	X	008000h to 009FFFh	004000h to 004FFFh
	SA5	0	0	0	0	0	0	1	0	1	X	00A000h to 00BFFFh	005000h to 005FFFh
	SA6	0	0	0	0	0	0	1	1	0	X	00C000h to 00DFFFh	006000h to 006FFFh
	SA7	0	0	0	0	0	0	1	1	1	X	00E000h to 00FFFFh	007000h to 007FFFh
	SA8	0	0	0	0	0	1	X	X	X	X	010000h to 01FFFFh	008000h to 00FFFFh
	SA9	0	0	0	0	1	0	X	X	X	X	020000h to 02FFFFh	010000h to 017FFFh
	SA10	0	0	0	0	1	1	X	X	X	X	030000h to 03FFFFh	018000h to 01FFFFh
	SA11	0	0	0	1	0	0	X	X	X	X	040000h to 04FFFFh	020000h to 027FFFh
	SA12	0	0	0	1	0	1	X	X	X	X	050000h to 05FFFFh	028000h to 02FFFFh
	SA13	0	0	0	1	1	0	X	X	X	X	060000h to 06FFFFh	030000h to 037FFFh
	SA14	0	0	0	1	1	1	X	X	X	X	070000h to 07FFFFh	038000h to 03FFFFh
Bank 2	SA15	0	0	1	0	0	0	X	X	X	X	080000h to 08FFFFh	040000h to 047FFFh
	SA16	0	0	1	0	0	1	X	X	X	X	090000h to 09FFFFh	048000h to 04FFFFh
	SA17	0	0	1	0	1	0	X	X	X	X	0A0000h to 0AFFFFh	050000h to 057FFFh
	SA18	0	0	1	0	1	1	X	X	X	X	0B0000h to 0BFFFFh	058000h to 05FFFFh
	SA19	0	0	1	1	0	0	X	X	X	X	0C0000h to 0CFFFFh	060000h to 067FFFh
	SA20	0	0	1	1	0	1	X	X	X	X	0D0000h to 0DFFFFh	068000h to 06FFFFh
	SA21	0	0	1	1	1	0	X	X	X	X	0E0000h to 0EFFFFh	070000h to 077FFFh
	SA22	0	0	1	1	1	1	X	X	X	X	0F0000h to 0FFFFFh	078000h to 07FFFFh
	SA23	0	1	0	0	0	0	X	X	X	X	100000h to 10FFFFh	080000h to 087FFFh
	SA24	0	1	0	0	0	1	X	X	X	X	110000h to 11FFFFh	088000h to 08FFFFh
	SA25	0	1	0	0	1	0	X	X	X	X	120000h to 12FFFFh	090000h to 097FFFh
	SA26	0	1	0	0	1	1	X	X	X	X	130000h to 13FFFFh	098000h to 09FFFFh
	SA27	0	1	0	1	0	0	X	X	X	X	140000h to 14FFFFh	0A0000h to 0A7FFFh
	SA28	0	1	0	1	0	1	X	X	X	X	150000h to 15FFFFh	0A8000h to 0AFFFFh
	SA29	0	1	0	1	1	0	X	X	X	X	160000h to 16FFFFh	0B0000h to 0B7FFFh
	SA30	0	1	0	1	1	1	X	X	X	X	170000h to 17FFFFh	0B8000h to 0BFFFFh
	SA31	0	1	1	0	0	0	X	X	X	X	180000h to 18FFFFh	0C0000h to 0C7FFFh
	SA32	0	1	1	0	0	1	X	X	X	X	190000h to 19FFFFh	0C8000h to 0CFFFFh
	SA33	0	1	1	0	1	0	X	X	X	X	1A0000h to 1AFFFFh	0D0000h to 0D7FFFh
	SA34	0	1	1	0	1	1	X	X	X	X	1B0000h to 1BFFFFh	0D8000h to 0DFFFFh
	SA35	0	1	1	1	0	0	X	X	X	X	1C0000h to 1CFFFFh	0E0000h to 0E7FFFh

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Bank	Sector	Sector Address										Address Range (BYTE mode)	Address Range (WORD mode)
		Bank Address											
		A_{20}	A_{19}	A_{18}	A_{17}	A_{16}	A_{15}	A_{14}	A_{13}	A_{12}	A_{11}		
Bank 2	SA36	0	1	1	1	0	1	X	X	X	X	1D0000h to 1DFFFFh	0E8000h to 0EFFFFh
	SA37	0	1	1	1	1	0	X	X	X	X	1E0000h to 1EFFFFh	0F0000h to 0F7FFFh
	SA38	0	1	1	1	1	1	X	X	X	X	1F0000h to 1FFFFFh	0F8000h to 0FFFFFh
	SA39	1	0	0	0	0	0	X	X	X	X	200000h to 20FFFFh	100000h to 107FFFh
	SA40	1	0	0	0	0	1	X	X	X	X	210000h to 21FFFFh	108000h to 10FFFFh
	SA41	1	0	0	0	1	0	X	X	X	X	220000h to 22FFFFh	110000h to 117FFFh
	SA42	1	0	0	0	1	1	X	X	X	X	230000h to 23FFFFh	118000h to 11FFFFh
	SA43	1	0	0	1	0	0	X	X	X	X	240000h to 24FFFFh	120000h to 127FFFh
	SA44	1	0	0	1	0	1	X	X	X	X	250000h to 25FFFFh	128000h to 12FFFFh
	SA45	1	0	0	1	1	0	X	X	X	X	260000h to 26FFFFh	130000h to 137FFFh
	SA46	1	0	0	1	1	1	X	X	X	X	270000h to 27FFFFh	138000h to 13FFFFh
	SA47	1	0	1	0	0	0	X	X	X	X	280000h to 28FFFFh	140000h to 147FFFh
	SA48	1	0	1	0	0	1	X	X	X	X	290000h to 29FFFFh	148000h to 14FFFFh
	SA49	1	0	1	0	1	0	X	X	X	X	2A0000h to 2AFFFFh	150000h to 157FFFh
	SA50	1	0	1	0	1	1	X	X	X	X	2B0000h to 2BFFFFh	158000h to 15FFFFh
	SA51	1	0	1	1	0	0	X	X	X	X	2C0000h to 2CFFFFh	160000h to 167FFFh
	SA52	1	0	1	1	0	1	X	X	X	X	2D0000h to 2DFFFFh	168000h to 16FFFFh
	SA53	1	0	1	1	1	0	X	X	X	X	2E0000h to 2EFFFFh	170000h to 177FFFh
	SA54	1	0	1	1	1	1	X	X	X	X	2F0000h to 2FFFFFh	178000h to 17FFFFh
	SA55	1	1	0	0	0	0	X	X	X	X	300000h to 30FFFFh	180000h to 187FFFh
	SA56	1	1	0	0	0	1	X	X	X	X	310000h to 31FFFFh	188000h to 18FFFFh
	SA57	1	1	0	0	1	0	X	X	X	X	320000h to 32FFFFh	190000h to 197FFFh
	SA58	1	1	0	0	1	1	X	X	X	X	330000h to 33FFFFh	198000h to 19FFFFh
	SA59	1	1	0	1	0	0	X	X	X	X	340000h to 34FFFFh	1A0000h to 1A7FFFh
	SA60	1	1	0	1	0	1	X	X	X	X	350000h to 35FFFFh	1A8000h to 1AFFFFh
	SA61	1	1	0	1	1	0	X	X	X	X	360000h to 36FFFFh	1B0000h to 1B7FFFh
	SA62	1	1	0	1	1	1	X	X	X	X	370000h to 37FFFFh	1B8000h to 1BFFFFh
	SA63	1	1	1	0	0	0	X	X	X	X	380000h to 38FFFFh	1C0000h to 1C7FFFh
	SA64	1	1	1	0	0	1	X	X	X	X	390000h to 39FFFFh	1C8000h to 1CFFFFh
	SA65	1	1	1	0	1	0	X	X	X	X	3A0000h to 3AFFFFh	1D0000h to 1D7FFFh
	SA66	1	1	1	0	1	1	X	X	X	X	3B0000h to 3BFFFFh	1D8000h to 1DFFFFh
	SA67	1	1	1	1	0	0	X	X	X	X	3C0000h to 3CFFFFh	1E0000h to 1E7FFFh
	SA68	1	1	1	1	0	1	X	X	X	X	3D0000h to 3DFFFFh	1E8000h to 1EFFFFh
	SA69	1	1	1	1	1	0	X	X	X	X	3E0000h to 3EFFFFh	1F0000h to 1F7FFFh
	SA70	1	1	1	1	1	1	X	X	X	X	3F0000h to 3FFFFFh	1F8000h to 1FFFFFh

Table 2. 5 Sector Address Tables (MB84VD22283EA/EE)

Bank	Sector	Sector Address										Address Range (BYTE mode)	Address Range (WORD mode)
		Bank Address											
		A_{20}	A_{19}	A_{18}	A_{17}	A_{16}	A_{15}	A_{14}	A_{13}	A_{12}	A_{11}		
Bank 2	SA0	0	0	0	0	0	0	X	X	X	X	000000h to 00FFFFh	000000h to 007FFFh
	SA1	0	0	0	0	0	1	X	X	X	X	010000h to 01FFFFh	008000h to 00FFFFh
	SA2	0	0	0	0	1	0	X	X	X	X	020000h to 02FFFFh	010000h to 017FFFh
	SA3	0	0	0	0	1	1	X	X	X	X	030000h to 03FFFFh	018000h to 01FFFFh
	SA4	0	0	0	1	0	0	X	X	X	X	040000h to 04FFFFh	020000h to 027FFFh
	SA5	0	0	0	1	0	1	X	X	X	X	050000h to 05FFFFh	028000h to 02FFFFh
	SA6	0	0	0	1	1	0	X	X	X	X	060000h to 06FFFFh	030000h to 037FFFh
	SA7	0	0	0	1	1	1	X	X	X	X	070000h to 07FFFFh	038000h to 03FFFFh
	SA8	0	0	1	0	0	0	X	X	X	X	080000h to 08FFFFh	040000h to 047FFFh
	SA9	0	0	1	0	0	1	X	X	X	X	090000h to 09FFFFh	048000h to 04FFFFh
	SA10	0	0	1	0	1	0	X	X	X	X	0A0000h to 0AFFFFh	050000h to 057FFFh
	SA11	0	0	1	0	1	1	X	X	X	X	0B0000h to 0BFFFFh	058000h to 05FFFFh
	SA12	0	0	1	1	0	0	X	X	X	X	0C0000h to 0CFFFFh	060000h to 067FFFh
	SA13	0	0	1	1	0	1	X	X	X	X	0D0000h to 0DFFFFh	068000h to 06FFFFh
	SA14	0	0	1	1	1	0	X	X	X	X	0E0000h to 0EFFFFh	070000h to 077FFFh
	SA15	0	0	1	1	1	1	X	X	X	X	0F0000h to 0FFFFFh	078000h to 07FFFFh
	SA16	0	1	0	0	0	0	X	X	X	X	100000h to 10FFFFh	080000h to 087FFFh
	SA17	0	1	0	0	0	1	X	X	X	X	110000h to 11FFFFh	088000h to 08FFFFh
	SA18	0	1	0	0	1	0	X	X	X	X	120000h to 12FFFFh	090000h to 097FFFh
	SA19	0	1	0	0	1	1	X	X	X	X	130000h to 13FFFFh	098000h to 09FFFFh
	SA20	0	1	0	1	0	0	X	X	X	X	140000h to 14FFFFh	0A0000h to 0A7FFFh
	SA21	0	1	0	1	0	1	X	X	X	X	150000h to 15FFFFh	0A8000h to 0AFFFFh
	SA22	0	1	0	1	1	0	X	X	X	X	160000h to 16FFFFh	0B0000h to 0B7FFFh
	SA23	0	1	0	1	1	1	X	X	X	X	170000h to 17FFFFh	0B8000h to 0BFFFFh
	SA24	0	1	1	0	0	0	X	X	X	X	180000h to 18FFFFh	0C0000h to 0C7FFFh
	SA25	0	1	1	0	0	1	X	X	X	X	190000h to 19FFFFh	0C8000h to 0CFFFFh
	SA26	0	1	1	0	1	0	X	X	X	X	1A0000h to 1AFFFFh	0D0000h to 0D7FFFh
	SA27	0	1	1	0	1	1	X	X	X	X	1B0000h to 1BFFFFh	0D8000h to 0DFFFFh
	SA28	0	1	1	1	0	0	X	X	X	X	1C0000h to 1CFFFFh	0E0000h to 0E7FFFh
	SA29	0	1	1	1	0	1	X	X	X	X	1D0000h to 1DFFFFh	0E8000h to 0EFFFFh
	SA30	0	1	1	1	1	0	X	X	X	X	1E0000h to 1EFFFFh	0F0000h to 0F7FFFh
	SA31	0	1	1	1	1	1	X	X	X	X	1F0000h to 1FFFFFh	0F8000h to 0FFFFFh

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Bank	Sector	Sector Address										Address Range (BYTE mode)	Address Range (WORD mode)
		Bank Address											
		A_{20}	A_{19}	A_{18}	A_{17}	A_{16}	A_{15}	A_{14}	A_{13}	A_{12}	A_{11}		
Bank 2	SA32	1	0	0	0	0	0	X	X	X	X	200000h to 20FFFFh	100000h to 107FFFh
	SA33	1	0	0	0	0	1	X	X	X	X	210000h to 21FFFFh	108000h to 10FFFFh
	SA34	1	0	0	0	1	0	X	X	X	X	220000h to 22FFFFh	110000h to 117FFFh
	SA35	1	0	0	0	1	1	X	X	X	X	230000h to 23FFFFh	118000h to 11FFFFh
	SA36	1	0	0	1	0	0	X	X	X	X	240000h to 24FFFFh	120000h to 127FFFh
	SA37	1	0	0	1	0	1	X	X	X	X	250000h to 25FFFFh	128000h to 12FFFFh
	SA38	1	0	0	1	1	0	X	X	X	X	260000h to 26FFFFh	130000h to 137FFFh
	SA39	1	0	0	1	1	1	X	X	X	X	270000h to 27FFFFh	138000h to 13FFFFh
	SA40	1	0	1	0	0	0	X	X	X	X	280000h to 28FFFFh	140000h to 147FFFh
	SA41	1	0	1	0	0	1	X	X	X	X	290000h to 29FFFFh	148000h to 14FFFFh
	SA42	1	0	1	0	1	0	X	X	X	X	2A0000h to 2AFFFFh	150000h to 157FFFh
	SA43	1	0	1	0	1	1	X	X	X	X	2B0000h to 2BFFFFh	158000h to 15FFFFh
	SA44	1	0	1	1	0	0	X	X	X	X	2C0000h to 2CFFFFh	160000h to 167FFFh
	SA45	1	0	1	1	0	1	X	X	X	X	2D0000h to 2DFFFFh	168000h to 16FFFFh
	SA46	1	0	1	1	1	0	X	X	X	X	2E0000h to 2EFFFFh	170000h to 177FFFh
	SA47	1	0	1	1	1	1	X	X	X	X	2F0000h to 2FFFFFh	178000h to 17FFFFh
Bank 1	SA48	1	1	0	0	0	0	X	X	X	X	300000h to 30FFFFh	180000h to 187FFFh
	SA49	1	1	0	0	0	1	X	X	X	X	310000h to 31FFFFh	188000h to 18FFFFh
	SA50	1	1	0	0	1	0	X	X	X	X	320000h to 32FFFFh	190000h to 197FFFh
	SA51	1	1	0	0	1	1	X	X	X	X	330000h to 33FFFFh	198000h to 19FFFFh
	SA52	1	1	0	1	0	0	X	X	X	X	340000h to 34FFFFh	1A0000h to 1A7FFFh
	SA53	1	1	0	1	0	1	X	X	X	X	350000h to 35FFFFh	1A8000h to 1AFFFFh
	SA54	1	1	0	1	1	0	X	X	X	X	360000h to 36FFFFh	1B0000h to 1B7FFFh
	SA55	1	1	0	1	1	1	X	X	X	X	370000h to 37FFFFh	1B8000h to 1BFFFFh
	SA56	1	1	1	0	0	0	X	X	X	X	380000h to 38FFFFh	1C0000h to 1C7FFFh
	SA57	1	1	1	0	0	1	X	X	X	X	390000h to 39FFFFh	1C8000h to 1CFFFFh
	SA58	1	1	1	0	1	0	X	X	X	X	3A0000h to 3AFFFFh	1D0000h to 1D7FFFh
	SA59	1	1	1	0	1	1	X	X	X	X	3B0000h to 3BFFFFh	1D8000h to 1DFFFFh
	SA60	1	1	1	1	0	0	X	X	X	X	3C0000h to 3CFFFFh	1E0000h to 1E7FFFh
	SA61	1	1	1	1	0	1	X	X	X	X	3D0000h to 3DFFFFh	1E8000h to 1EFFFFh
	SA62	1	1	1	1	1	0	X	X	X	X	3E0000h to 3EFFFFh	1F0000h to 1F7FFFh
	SA63	1	1	1	1	1	1	0	0	0	X	3F0000h to 3F1FFFh	1F8000h to 1F8FFFh
	SA64	1	1	1	1	1	1	0	0	1	X	3F2000h to 3F3FFFh	1F9000h to 1F9FFFh
	SA65	1	1	1	1	1	1	0	1	0	X	3F4000h to 3F5FFFh	1FA000h to 1FAFFFh
	SA66	1	1	1	1	1	1	0	1	1	X	3F6000h to 3F7FFFh	1FB000h to 1FBFFFh
	SA67	1	1	1	1	1	1	1	0	0	X	3F8000h to 3F9FFFh	1FC000h to 1FCFFFh
	SA68	1	1	1	1	1	1	1	0	1	X	3FA000h to 3FAFFFh	1FD000h to 1FDFFFh
	SA69	1	1	1	1	1	1	1	1	0	X	3FC000h to 3FCFFFh	1FE000h to 1FEFFFh
	SA70	1	1	1	1	1	1	1	1	1	X	3FE000h to 3FFFFFh	1FF000h to 1FFFFFh

Table 2. 6 Sector Address Tables (MB84VD22293EA/EE)

Bank	Sector	Sector Address										Address Range (BYTE mode)	Address Range (WORD mode)
		Bank Address											
		A_{20}	A_{19}	A_{18}	A_{17}	A_{16}	A_{15}	A_{14}	A_{13}	A_{12}	A_{11}		
Bank 1	SA0	0	0	0	0	0	0	0	0	0	X	000000h to 001FFFh	000000h to 000FFFh
	SA1	0	0	0	0	0	0	0	0	1	X	002000h to 003FFFh	001000h to 001FFFh
	SA2	0	0	0	0	0	0	0	1	0	X	004000h to 005FFFh	002000h to 002FFFh
	SA3	0	0	0	0	0	0	0	1	1	X	006000h to 007FFFh	003000h to 003FFFh
	SA4	0	0	0	0	0	0	1	0	0	X	008000h to 009FFFh	004000h to 004FFFh
	SA5	0	0	0	0	0	0	1	0	1	X	00A000h to 00BFFFh	005000h to 005FFFh
	SA6	0	0	0	0	0	0	1	1	0	X	00C000h to 00DFFFh	006000h to 006FFFh
	SA7	0	0	0	0	0	0	1	1	1	X	00E000h to 00FFFFh	007000h to 007FFFh
	SA8	0	0	0	0	0	1	X	X	X	X	010000h to 01FFFFh	008000h to 00FFFFh
	SA9	0	0	0	0	1	0	X	X	X	X	020000h to 02FFFFh	010000h to 017FFFh
	SA10	0	0	0	0	1	1	X	X	X	X	030000h to 03FFFFh	018000h to 01FFFFh
	SA11	0	0	0	1	0	0	X	X	X	X	040000h to 04FFFFh	020000h to 027FFFh
	SA12	0	0	0	1	0	1	X	X	X	X	050000h to 05FFFFh	028000h to 02FFFFh
	SA13	0	0	0	1	1	0	X	X	X	X	060000h to 06FFFFh	030000h to 037FFFh
	SA14	0	0	0	1	1	1	X	X	X	X	070000h to 07FFFFh	038000h to 03FFFFh
	SA15	0	0	1	0	0	0	X	X	X	X	080000h to 08FFFFh	040000h to 047FFFh
	SA16	0	0	1	0	0	1	X	X	X	X	090000h to 09FFFFh	048000h to 04FFFFh
	SA17	0	0	1	0	1	0	X	X	X	X	0A0000h to 0AFFFFh	050000h to 057FFFh
	SA18	0	0	1	0	1	1	X	X	X	X	0B0000h to 0BFFFFh	058000h to 05FFFFh
	SA19	0	0	1	1	0	0	X	X	X	X	0C0000h to 0CFFFFh	060000h to 067FFFh
	SA20	0	0	1	1	0	1	X	X	X	X	0D0000h to 0DFFFFh	068000h to 06FFFFh
	SA21	0	0	1	1	1	0	X	X	X	X	0E0000h to 0EFFFFh	070000h to 077FFFh
	SA22	0	0	1	1	1	1	X	X	X	X	0F0000h to 0FFFFFh	078000h to 07FFFFh
Bank 2	SA23	0	1	0	0	0	0	X	X	X	X	100000h to 10FFFFh	080000h to 087FFFh
	SA24	0	1	0	0	0	1	X	X	X	X	110000h to 11FFFFh	088000h to 08FFFFh
	SA25	0	1	0	0	1	0	X	X	X	X	120000h to 12FFFFh	090000h to 097FFFh
	SA26	0	1	0	0	1	1	X	X	X	X	130000h to 13FFFFh	098000h to 09FFFFh
	SA27	0	1	0	1	0	0	X	X	X	X	140000h to 14FFFFh	0A0000h to 0A7FFFh
	SA28	0	1	0	1	0	1	X	X	X	X	150000h to 15FFFFh	0A8000h to 0AFFFFh
	SA29	0	1	0	1	1	0	X	X	X	X	160000h to 16FFFFh	0B0000h to 0B7FFFh
	SA30	0	1	0	1	1	1	X	X	X	X	170000h to 17FFFFh	0B8000h to 0BFFFFh
	SA31	0	1	1	0	0	0	X	X	X	X	180000h to 18FFFFh	0C0000h to 0C7FFFh
	SA32	0	1	1	0	0	1	X	X	X	X	190000h to 19FFFFh	0C8000h to 0CFFFFh
	SA33	0	1	1	0	1	0	X	X	X	X	1A0000h to 1AFFFFh	0D0000h to 0D7FFFh
	SA34	0	1	1	0	1	1	X	X	X	X	1B0000h to 1BFFFFh	0D8000h to 0DFFFFh
	SA35	0	1	1	1	0	0	X	X	X	X	1C0000h to 1CFFFFh	0E0000h to 0E7FFFh

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Bank	Sector	Sector Address										Address Range (BYTE mode)	Address Range (WORD mode)
		Bank Address											
		A_{20}	A_{19}	A_{18}	A_{17}	A_{16}	A_{15}	A_{14}	A_{13}	A_{12}	A_{11}		
Bank 2	SA36	0	1	1	1	0	1	X	X	X	X	1D0000h to 1DFFFFh	0E8000h to 0EFFFFh
	SA37	0	1	1	1	1	0	X	X	X	X	1E0000h to 1EFFFFh	0F0000h to 0F7FFFh
	SA38	0	1	1	1	1	1	X	X	X	X	1F0000h to 1FFFFFh	0F8000h to 0FFFFFh
	SA39	1	0	0	0	0	0	X	X	X	X	200000h to 20FFFFh	100000h to 107FFFh
	SA40	1	0	0	0	0	1	X	X	X	X	210000h to 21FFFFh	108000h to 10FFFFh
	SA41	1	0	0	0	1	0	X	X	X	X	220000h to 22FFFFh	110000h to 117FFFh
	SA42	1	0	0	0	1	1	X	X	X	X	230000h to 23FFFFh	118000h to 11FFFFh
	SA43	1	0	0	1	0	0	X	X	X	X	240000h to 24FFFFh	120000h to 127FFFh
	SA44	1	0	0	1	0	1	X	X	X	X	250000h to 25FFFFh	128000h to 12FFFFh
	SA45	1	0	0	1	1	0	X	X	X	X	260000h to 26FFFFh	130000h to 137FFFh
	SA46	1	0	0	1	1	1	X	X	X	X	270000h to 27FFFFh	138000h to 13FFFFh
	SA47	1	0	1	0	0	0	X	X	X	X	280000h to 28FFFFh	140000h to 147FFFh
	SA48	1	0	1	0	0	1	X	X	X	X	290000h to 29FFFFh	148000h to 14FFFFh
	SA49	1	0	1	0	1	0	X	X	X	X	2A0000h to 2AFFFFh	150000h to 157FFFh
	SA50	1	0	1	0	1	1	X	X	X	X	2B0000h to 2BFFFFh	158000h to 15FFFFh
	SA51	1	0	1	1	0	0	X	X	X	X	2C0000h to 2CFFFFh	160000h to 167FFFh
	SA52	1	0	1	1	0	1	X	X	X	X	2D0000h to 2DFFFFh	168000h to 16FFFFh
	SA53	1	0	1	1	1	0	X	X	X	X	2E0000h to 2EFFFFh	170000h to 177FFFh
	SA54	1	0	1	1	1	1	X	X	X	X	2F0000h to 2FFFFFh	178000h to 17FFFFh
	SA55	1	1	0	0	0	0	X	X	X	X	300000h to 30FFFFh	180000h to 187FFFh
	SA56	1	1	0	0	0	1	X	X	X	X	310000h to 31FFFFh	188000h to 18FFFFh
	SA57	1	1	0	0	1	0	X	X	X	X	320000h to 32FFFFh	190000h to 197FFFh
	SA58	1	1	0	0	1	1	X	X	X	X	330000h to 33FFFFh	198000h to 19FFFFh
	SA59	1	1	0	1	0	0	X	X	X	X	340000h to 34FFFFh	1A0000h to 1A7FFFh
	SA60	1	1	0	1	0	1	X	X	X	X	350000h to 35FFFFh	1A8000h to 1AFFFFh
	SA61	1	1	0	1	1	0	X	X	X	X	360000h to 36FFFFh	1B0000h to 1B7FFFh
	SA62	1	1	0	1	1	1	X	X	X	X	370000h to 37FFFFh	1B8000h to 1BFFFFh
	SA63	1	1	1	0	0	0	X	X	X	X	380000h to 38FFFFh	1C0000h to 1C7FFFh
	SA64	1	1	1	0	0	1	X	X	X	X	390000h to 39FFFFh	1C8000h to 1CFFFFh
	SA65	1	1	1	0	1	0	X	X	X	X	3A0000h to 3AFFFFh	1D0000h to 1D7FFFh
	SA66	1	1	1	0	1	1	X	X	X	X	3B0000h to 3BFFFFh	1D8000h to 1DFFFFh
	SA67	1	1	1	1	0	0	X	X	X	X	3C0000h to 3CFFFFh	1E0000h to 1E7FFFh
	SA68	1	1	1	1	0	1	X	X	X	X	3D0000h to 3DFFFFh	1E8000h to 1EFFFFh
	SA69	1	1	1	1	1	0	X	X	X	X	3E0000h to 3EFFFFh	1F0000h to 1F7FFFh
	SA70	1	1	1	1	1	1	X	X	X	X	3F0000h to 3FFFFFh	1F8000h to 1FFFFFh

Table 2. 7 Sector Address Tables (MB84VD22284EA/EE)

Bank	Sector	Sector Address										Address Range (BYTE mode)	Address Range (WORD mode)
		Bank Address											
		A_{20}	A_{19}	A_{18}	A_{17}	A_{16}	A_{15}	A_{14}	A_{13}	A_{12}	A_{11}		
Bank 2	SA0	0	0	0	0	0	0	X	X	X	X	000000h to 00FFFFh	000000h to 007FFFh
	SA1	0	0	0	0	0	1	X	X	X	X	010000h to 01FFFFh	008000h to 00FFFFh
	SA2	0	0	0	0	1	0	X	X	X	X	020000h to 02FFFFh	010000h to 017FFFh
	SA3	0	0	0	0	1	1	X	X	X	X	030000h to 03FFFFh	018000h to 01FFFFh
	SA4	0	0	0	1	0	0	X	X	X	X	040000h to 04FFFFh	020000h to 027FFFh
	SA5	0	0	0	1	0	1	X	X	X	X	050000h to 05FFFFh	028000h to 02FFFFh
	SA6	0	0	0	1	1	0	X	X	X	X	060000h to 06FFFFh	030000h to 037FFFh
	SA7	0	0	0	1	1	1	X	X	X	X	070000h to 07FFFFh	038000h to 03FFFFh
	SA8	0	0	1	0	0	0	X	X	X	X	080000h to 08FFFFh	040000h to 047FFFh
	SA9	0	0	1	0	0	1	X	X	X	X	090000h to 09FFFFh	048000h to 04FFFFh
	SA10	0	0	1	0	1	0	X	X	X	X	0A0000h to 0AFFFFh	050000h to 057FFFh
	SA11	0	0	1	0	1	1	X	X	X	X	0B0000h to 0BFFFFh	058000h to 05FFFFh
	SA12	0	0	1	1	0	0	X	X	X	X	0C0000h to 0CFFFFh	060000h to 067FFFh
	SA13	0	0	1	1	0	1	X	X	X	X	0D0000h to 0DFFFFh	068000h to 06FFFFh
	SA14	0	0	1	1	1	0	X	X	X	X	0E0000h to 0EFFFFh	070000h to 077FFFh
	SA15	0	0	1	1	1	1	X	X	X	X	0F0000h to 0FFFFFh	078000h to 07FFFFh
	SA16	0	1	0	0	0	0	X	X	X	X	100000h to 10FFFFh	080000h to 087FFFh
	SA17	0	1	0	0	0	1	X	X	X	X	110000h to 11FFFFh	088000h to 08FFFFh
	SA18	0	1	0	0	1	0	X	X	X	X	120000h to 12FFFFh	090000h to 097FFFh
	SA19	0	1	0	0	1	1	X	X	X	X	130000h to 13FFFFh	098000h to 09FFFFh
	SA20	0	1	0	1	0	0	X	X	X	X	140000h to 14FFFFh	0A0000h to 0A7FFFh
	SA21	0	1	0	1	0	1	X	X	X	X	150000h to 15FFFFh	0A8000h to 0AFFFFh
	SA22	0	1	0	1	1	0	X	X	X	X	160000h to 16FFFFh	0B0000h to 0B7FFFh
	SA23	0	1	0	1	1	1	X	X	X	X	170000h to 17FFFFh	0B8000h to 0BFFFFh
	SA24	0	1	1	0	0	0	X	X	X	X	180000h to 18FFFFh	0C0000h to 0C7FFFh
	SA25	0	1	1	0	0	1	X	X	X	X	190000h to 19FFFFh	0C8000h to 0CFFFFh
	SA26	0	1	1	0	1	0	X	X	X	X	1A0000h to 1AFFFFh	0D0000h to 0D7FFFh
	SA27	0	1	1	0	1	1	X	X	X	X	1B0000h to 1BFFFFh	0D8000h to 0DFFFFh
	SA28	0	1	1	1	0	0	X	X	X	X	1C0000h to 1CFFFFh	0E0000h to 0E7FFFh
	SA29	0	1	1	1	0	1	X	X	X	X	1D0000h to 1DFFFFh	0E8000h to 0EFFFFh
	SA30	0	1	1	1	1	0	X	X	X	X	1E0000h to 1EFFFFh	0F0000h to 0F7FFFh
	SA31	0	1	1	1	1	1	X	X	X	X	1F0000h to 1FFFFFh	0F8000h to 0FFFFFh

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Bank	Sector	Sector Address										Address Range (BYTE mode)	Address Range (WORD mode)
		Bank Address											
		A_{20}	A_{19}	A_{18}	A_{17}	A_{16}	A_{15}	A_{14}	A_{13}	A_{12}	A_{11}		
Bank 1	SA32	1	0	0	0	0	0	X	X	X	X	200000h to 20FFFFh	100000h to 107FFFh
	SA33	1	0	0	0	0	1	X	X	X	X	210000h to 21FFFFh	108000h to 10FFFFh
	SA34	1	0	0	0	1	0	X	X	X	X	220000h to 22FFFFh	110000h to 117FFFh
	SA35	1	0	0	0	1	1	X	X	X	X	230000h to 23FFFFh	118000h to 11FFFFh
	SA36	1	0	0	1	0	0	X	X	X	X	240000h to 24FFFFh	120000h to 127FFFh
	SA37	1	0	0	1	0	1	X	X	X	X	250000h to 25FFFFh	128000h to 12FFFFh
	SA38	1	0	0	1	1	0	X	X	X	X	260000h to 26FFFFh	130000h to 137FFFh
	SA39	1	0	0	1	1	1	X	X	X	X	270000h to 27FFFFh	138000h to 13FFFFh
	SA40	1	0	1	0	0	0	X	X	X	X	280000h to 28FFFFh	140000h to 147FFFh
	SA41	1	0	1	0	0	1	X	X	X	X	290000h to 29FFFFh	148000h to 14FFFFh
	SA42	1	0	1	0	1	0	X	X	X	X	2A0000h to 2AFFFFh	150000h to 157FFFh
	SA43	1	0	1	0	1	1	X	X	X	X	2B0000h to 2BFFFFh	158000h to 15FFFFh
	SA44	1	0	1	1	0	0	X	X	X	X	2C0000h to 2CFFFFh	160000h to 167FFFh
	SA45	1	0	1	1	0	1	X	X	X	X	2D0000h to 2DFFFFh	168000h to 16FFFFh
	SA46	1	0	1	1	1	0	X	X	X	X	2E0000h to 2EFFFFh	170000h to 177FFFh
	SA47	1	0	1	1	1	1	X	X	X	X	2F0000h to 2FFFFFh	178000h to 17FFFFh
	SA48	1	1	0	0	0	0	X	X	X	X	300000h to 30FFFFh	180000h to 187FFFh
	SA49	1	1	0	0	0	1	X	X	X	X	310000h to 31FFFFh	188000h to 18FFFFh
	SA50	1	1	0	0	1	0	X	X	X	X	320000h to 32FFFFh	190000h to 197FFFh
	SA51	1	1	0	0	1	1	X	X	X	X	330000h to 33FFFFh	198000h to 19FFFFh
	SA52	1	1	0	1	0	0	X	X	X	X	340000h to 34FFFFh	1A0000h to 1A7FFFh
	SA53	1	1	0	1	0	1	X	X	X	X	350000h to 35FFFFh	1A8000h to 1AFFFFh
	SA54	1	1	0	1	1	0	X	X	X	X	360000h to 36FFFFh	1B0000h to 1B7FFFh
	SA55	1	1	0	1	1	1	X	X	X	X	370000h to 37FFFFh	1B8000h to 1BFFFFh
	SA56	1	1	1	0	0	0	X	X	X	X	380000h to 38FFFFh	1C0000h to 1C7FFFh
	SA57	1	1	1	0	0	1	X	X	X	X	390000h to 39FFFFh	1C8000h to 1CFFFFh
	SA58	1	1	1	0	1	0	X	X	X	X	3A0000h to 3AFFFFh	1D0000h to 1D7FFFh
	SA59	1	1	1	0	1	1	X	X	X	X	3B0000h to 3BFFFFh	1D8000h to 1DFFFFh
	SA60	1	1	1	1	0	0	X	X	X	X	3C0000h to 3CFFFFh	1E0000h to 1E7FFFh
	SA61	1	1	1	1	0	1	X	X	X	X	3D0000h to 3DFFFFh	1E8000h to 1EFFFFh
	SA62	1	1	1	1	1	0	X	X	X	X	3E0000h to 3EFFFFh	1F0000h to 1F7FFFh
	SA63	1	1	1	1	1	1	0	0	0	X	3F0000h to 3F1FFFh	1F8000h to 1F8FFFh
	SA64	1	1	1	1	1	1	0	0	1	X	3F2000h to 3F3FFFh	1F9000h to 1F9FFFh
	SA65	1	1	1	1	1	1	0	1	0	X	3F4000h to 3F5FFFh	1FA000h to 1FAFFFh
	SA66	1	1	1	1	1	1	0	1	1	X	3F6000h to 3F7FFFh	1FB000h to 1FBFFFh
	SA67	1	1	1	1	1	1	1	0	0	X	3F8000h to 3F9FFFh	1FC000h to 1FCFFFh
	SA68	1	1	1	1	1	1	1	0	1	X	3FA000h to 3FAFFFh	1FD000h to 1FDFFFh
	SA69	1	1	1	1	1	1	1	1	0	X	3FC000h to 3FCFFFh	1FE000h to 1FEFFFh
	SA70	1	1	1	1	1	1	1	1	1	X	3FE000h to 3FFFFFh	1FF000h to 1FFFFFh

Table 2. 8 Sector Address Tables (MB84VD22294EA/EE)

Bank	Sector	Sector Address										Address Range (BYTE mode)	Address Range (WORD mode)
		Bank Address											
		A_{20}	A_{19}	A_{18}	A_{17}	A_{16}	A_{15}	A_{14}	A_{13}	A_{12}	A_{11}		
Bank 1	SA0	0	0	0	0	0	0	0	0	0	X	000000h to 001FFFh	000000h to 000FFFh
	SA1	0	0	0	0	0	0	0	0	1	X	002000h to 003FFFh	001000h to 001FFFh
	SA2	0	0	0	0	0	0	0	1	0	X	004000h to 005FFFh	002000h to 002FFFh
	SA3	0	0	0	0	0	0	0	1	1	X	006000h to 007FFFh	003000h to 003FFFh
	SA4	0	0	0	0	0	0	1	0	0	X	008000h to 009FFFh	004000h to 004FFFh
	SA5	0	0	0	0	0	0	1	0	1	X	00A000h to 00BFFFh	005000h to 005FFFh
	SA6	0	0	0	0	0	0	1	1	0	X	00C000h to 00DFFFh	006000h to 006FFFh
	SA7	0	0	0	0	0	0	1	1	1	X	00E000h to 00FFFFh	007000h to 007FFFh
	SA8	0	0	0	0	0	1	X	X	X	X	010000h to 01FFFFh	008000h to 00FFFFh
	SA9	0	0	0	0	1	0	X	X	X	X	020000h to 02FFFFh	010000h to 017FFFh
	SA10	0	0	0	0	1	1	X	X	X	X	030000h to 03FFFFh	018000h to 01FFFFh
	SA11	0	0	0	1	0	0	X	X	X	X	040000h to 04FFFFh	020000h to 027FFFh
	SA12	0	0	0	1	0	1	X	X	X	X	050000h to 05FFFFh	028000h to 02FFFFh
	SA13	0	0	0	1	1	0	X	X	X	X	060000h to 06FFFFh	030000h to 037FFFh
	SA14	0	0	0	1	1	1	X	X	X	X	070000h to 07FFFFh	038000h to 03FFFFh
	SA15	0	0	1	0	0	0	X	X	X	X	080000h to 08FFFFh	040000h to 047FFFh
	SA16	0	0	1	0	0	1	X	X	X	X	090000h to 09FFFFh	048000h to 04FFFFh
	SA17	0	0	1	0	1	0	X	X	X	X	0A0000h to 0AFFFFh	050000h to 057FFFh
	SA18	0	0	1	0	1	1	X	X	X	X	0B0000h to 0BFFFFh	058000h to 05FFFFh
	SA19	0	0	1	1	0	0	X	X	X	X	0C0000h to 0CFFFFh	060000h to 067FFFh
	SA20	0	0	1	1	0	1	X	X	X	X	0D0000h to 0DFFFFh	068000h to 06FFFFh
	SA21	0	0	1	1	1	0	X	X	X	X	0E0000h to 0EFFFFh	070000h to 077FFFh
	SA22	0	0	1	1	1	1	X	X	X	X	0F0000h to 0FFFFFh	078000h to 07FFFFh
	SA23	0	1	0	0	0	0	X	X	X	X	100000h to 10FFFFh	080000h to 087FFFh
	SA24	0	1	0	0	0	1	X	X	X	X	110000h to 11FFFFh	088000h to 08FFFFh
	SA25	0	1	0	0	1	0	X	X	X	X	120000h to 12FFFFh	090000h to 097FFFh
	SA26	0	1	0	0	1	1	X	X	X	X	130000h to 13FFFFh	098000h to 09FFFFh
	SA27	0	1	0	1	0	0	X	X	X	X	140000h to 14FFFFh	0A0000h to 0A7FFFh
	SA28	0	1	0	1	0	1	X	X	X	X	150000h to 15FFFFh	0A8000h to 0AFFFFh
	SA29	0	1	0	1	1	0	X	X	X	X	160000h to 16FFFFh	0B0000h to 0B7FFFh
	SA30	0	1	0	1	1	1	X	X	X	X	170000h to 17FFFFh	0B8000h to 0BFFFFh
	SA31	0	1	1	0	0	0	X	X	X	X	180000h to 18FFFFh	0C0000h to 0C7FFFh
	SA32	0	1	1	0	0	1	X	X	X	X	190000h to 19FFFFh	0C8000h to 0CFFFFh
	SA33	0	1	1	0	1	0	X	X	X	X	1A0000h to 1AFFFFh	0D0000h to 0D7FFFh
	SA34	0	1	1	0	1	1	X	X	X	X	1B0000h to 1BFFFFh	0D8000h to 0DFFFFh

(Continued)

(Continued)

Bank	Sector	Sector Address										Address Range (BYTE mode)	Address Range (WORD mode)
		Bank Address											
		A_{20}	A_{19}	A_{18}	A_{17}	A_{16}	A_{15}	A_{14}	A_{13}	A_{12}	A_{11}		
Bank 1	SA35	0	1	1	1	0	0	X	X	X	X	1C0000h to 1CFFFFh	0E0000h to 0E7FFFh
	SA36	0	1	1	1	0	1	X	X	X	X	1D0000h to 1DFFFFh	0E8000h to 0EFFFFh
	SA37	0	1	1	1	1	0	X	X	X	X	1E0000h to 1EFFFFh	0F0000h to 0F7FFFh
	SA38	0	1	1	1	1	1	X	X	X	X	1F0000h to 1FFFFFh	0F8000h to 0FFFFFh
Bank 2	SA39	1	0	0	0	0	0	X	X	X	X	200000h to 20FFFFh	100000h to 107FFFh
	SA40	1	0	0	0	0	1	X	X	X	X	210000h to 21FFFFh	108000h to 10FFFFh
	SA41	1	0	0	0	1	0	X	X	X	X	220000h to 22FFFFh	110000h to 117FFFh
	SA42	1	0	0	0	1	1	X	X	X	X	230000h to 23FFFFh	118000h to 11FFFFh
	SA43	1	0	0	1	0	0	X	X	X	X	240000h to 24FFFFh	120000h to 127FFFh
	SA44	1	0	0	1	0	1	X	X	X	X	250000h to 25FFFFh	128000h to 12FFFFh
	SA45	1	0	0	1	1	0	X	X	X	X	260000h to 26FFFFh	130000h to 137FFFh
	SA46	1	0	0	1	1	1	X	X	X	X	270000h to 27FFFFh	138000h to 13FFFFh
	SA47	1	0	1	0	0	0	X	X	X	X	280000h to 28FFFFh	140000h to 147FFFh
	SA48	1	0	1	0	0	1	X	X	X	X	290000h to 29FFFFh	148000h to 14FFFFh
	SA49	1	0	1	0	1	0	X	X	X	X	2A0000h to 2AFFFFh	150000h to 157FFFh
	SA50	1	0	1	0	1	1	X	X	X	X	2B0000h to 2BFFFFh	158000h to 15FFFFh
	SA51	1	0	1	1	0	0	X	X	X	X	2C0000h to 2CFFFFh	160000h to 167FFFh
	SA52	1	0	1	1	0	1	X	X	X	X	2D0000h to 2DFFFFh	168000h to 16FFFFh
	SA53	1	0	1	1	1	0	X	X	X	X	2E0000h to 2EFFFFh	170000h to 177FFFh
	SA54	1	0	1	1	1	1	X	X	X	X	2F0000h to 2FFFFFh	178000h to 17FFFFh
	SA55	1	1	0	0	0	0	X	X	X	X	300000h to 30FFFFh	180000h to 187FFFh
	SA56	1	1	0	0	0	1	X	X	X	X	310000h to 31FFFFh	188000h to 18FFFFh
	SA57	1	1	0	0	1	0	X	X	X	X	320000h to 32FFFFh	190000h to 197FFFh
	SA58	1	1	0	0	1	1	X	X	X	X	330000h to 33FFFFh	198000h to 19FFFFh
	SA59	1	1	0	1	0	0	X	X	X	X	340000h to 34FFFFh	1A0000h to 1A7FFFh
	SA60	1	1	0	1	0	1	X	X	X	X	350000h to 35FFFFh	1A8000h to 1AFFFFh
	SA61	1	1	0	1	1	0	X	X	X	X	360000h to 36FFFFh	1B0000h to 1B7FFFh
	SA62	1	1	0	1	1	1	X	X	X	X	370000h to 37FFFFh	1B8000h to 1BFFFFh
	SA63	1	1	1	0	0	0	X	X	X	X	380000h to 38FFFFh	1C0000h to 1C7FFFh
	SA64	1	1	1	0	0	1	X	X	X	X	390000h to 39FFFFh	1C8000h to 1CFFFFh
	SA65	1	1	1	0	1	0	X	X	X	X	3A0000h to 3AFFFFh	1D0000h to 1D7FFFh
	SA66	1	1	1	0	1	1	X	X	X	X	3B0000h to 3BFFFFh	1D8000h to 1DFFFFh
	SA67	1	1	1	1	0	0	X	X	X	X	3C0000h to 3CFFFFh	1E0000h to 1E7FFFh
	SA68	1	1	1	1	0	1	X	X	X	X	3D0000h to 3DFFFFh	1E8000h to 1EFFFFh
	SA69	1	1	1	1	1	0	X	X	X	X	3E0000h to 3EFFFFh	1F0000h to 1F7FFFh
	SA70	1	1	1	1	1	1	X	X	X	X	3F0000h to 3FFFFFh	1F8000h to 1FFFFFh

Table 3. 1 Sector Group Addresses (MB84VD2228XEA/EE)
(Top Boot Block)

Sector Group	A_{20}	A_{19}	A_{18}	A_{17}	A_{16}	A_{15}	A_{14}	A_{13}	A_{12}	Sectors
SGA0	0	0	0	0	0	0	X	X	X	SA0
SGA1	0	0	0	0	0	1	X	X	X	SA1 to SA3
					1	0				
					1	1				
SGA2	0	0	0	1	X	X	X	X	X	SA4 to SA7
SGA3	0	0	1	0	X	X	X	X	X	SA8 to SA11
SGA4	0	0	1	1	X	X	X	X	X	SA12 to SA15
SGA5	0	1	0	0	X	X	X	X	X	SA16 to SA19
SGA6	0	1	0	1	X	X	X	X	X	SA20 to SA23
SGA7	0	1	1	0	X	X	X	X	X	SA24 to SA27
SGA8	0	1	1	1	X	X	X	X	X	SA28 to SA31
SGA9	1	0	0	0	X	X	X	X	X	SA32 to SA35
SGA10	1	0	0	1	X	X	X	X	X	SA36 to SA39
SGA11	1	0	1	0	X	X	X	X	X	SA40 to SA43
SGA12	1	0	1	1	X	X	X	X	X	SA44 to SA47
SGA13	1	1	0	0	X	X	X	X	X	SA48 to SA51
SGA14	1	1	0	1	X	X	X	X	X	SA52 to SA55
SGA15	1	1	1	0	X	X	X	X	X	SA56 to SA59
SGA16	1	1	1	1	0	0	X	X	X	SA60 to SA62
					0	1				
					1	0				
SGA17	1	1	1	1	1	1	0	0	0	SA63
SGA18	1	1	1	1	1	1	0	0	1	SA64
SGA19	1	1	1	1	1	1	0	1	0	SA65
SGA20	1	1	1	1	1	1	0	1	1	SA66
SGA21	1	1	1	1	1	1	1	0	0	SA67
SGA22	1	1	1	1	1	1	1	0	1	SA68
SGA23	1	1	1	1	1	1	1	1	0	SA69
SGA24	1	1	1	1	1	1	1	1	1	SA70

Table 3. 2 Sector Group Addresses (MB84VD2229XEA/EE)
(Bottom Boot Block)

Sector Group	A_{20}	A_{19}	A_{18}	A_{17}	A_{16}	A_{15}	A_{14}	A_{13}	A_{12}	Sectors
SGA0	0	0	0	0	0	0	0	0	0	SA0
SGA1	0	0	0	0	0	0	0	0	1	SA1
SGA2	0	0	0	0	0	0	0	1	0	SA2
SGA3	0	0	0	0	0	0	0	1	1	SA3
SGA4	0	0	0	0	0	0	1	0	0	SA4
SGA5	0	0	0	0	0	0	1	0	1	SA5
SGA6	0	0	0	0	0	0	1	1	0	SA6
SGA7	0	0	0	0	0	0	1	1	1	SA7
SGA8	0	0	0	0	0	1	X	X	X	SA8 to SA10
					1	0				
					1	1				
SGA9	0	0	0	1	X	X	X	X	X	SA11 to SA14
SGA10	0	0	1	0	X	X	X	X	X	SA15 to SA18
SGA11	0	0	1	1	X	X	X	X	X	SA19 to SA22
SGA12	0	1	0	0	X	X	X	X	X	SA23 to SA26
SGA13	0	1	0	1	X	X	X	X	X	SA27 to SA30
SGA14	0	1	1	0	X	X	X	X	X	SA31 to SA34
SGA15	0	1	1	1	X	X	X	X	X	SA35 to SA38
SGA16	1	0	0	0	X	X	X	X	X	SA39 to SA42
SGA17	1	0	0	1	X	X	X	X	X	SA43 to SA46
SGA18	1	0	1	0	X	X	X	X	X	SA47 to SA50
SGA19	1	0	1	1	X	X	X	X	X	SA51 to SA54
SGA20	1	1	0	0	X	X	X	X	X	SA55 to SA58
SGA21	1	1	0	1	X	X	X	X	X	SA59 to SA62
SGA22	1	1	1	0	X	X	X	X	X	SA63 to SA66
SGA23	1	1	1	1	0	0	X	X	X	SA67 to SA69
					0	1				
					1	0				
SGA24	1	1	1	1	1	1	X	X	X	SA70

Table 4 Flash Memory Autoselect Codes

Type			A_{12} to A_{19}	A_6	A_1	A_0	A_{-1}*1	Code (HEX)
Manufacturer's Code			X	V_{IL}	V_{IL}	V_{IL}	V_{IL}	04h
Device Code	MB84VD22281EA MB84VD22281EE	Byte	X	V_{IL}	V_{IL}	V_{IH}	V_{IL}	59h
		Word					X	2259h
	MB84VD22291EA MB84VD22291EE	Byte	X	V_{IL}	V_{IL}	V_{IH}	V_{IL}	5Ah
		Word					X	225Ah
	MB84VD22282EA MB84VD22282EE	Byte	X	V_{IL}	V_{IL}	V_{IH}	V_{IL}	55h
		Word					X	2255h
	MB84VD22292EA MB84VD22292EE	Byte	X	V_{IL}	V_{IL}	V_{IH}	V_{IL}	56h
		Word					X	2256h
	MB84VD22283EA MB84VD22283EE	Byte	X	V_{IL}	V_{IL}	V_{IH}	V_{IL}	50h
		Word					X	2250h
	MB84VD22293EA MB84VD22293EE	Byte	X	V_{IL}	V_{IL}	V_{IH}	V_{IL}	53h
		Word					X	2253h
	MB84VD22284EA MB84VD22284EE	Byte	X	V_{IL}	V_{IL}	V_{IH}	V_{IL}	5Ch
		Word					X	225Ch
	MB84VD22294EA MB84VD22294EE	Byte	X	V_{IL}	V_{IL}	V_{IH}	V_{IL}	5Fh
		Word					X	225Fh
Sector Group protect			Sector Group Address	V_{IL}	V_{IH}	V_{IL}	V_{IL}	01h*2

*1: A_{-1} is for Byte mode.
*2: Output 01h at protected sector address and output 00h at unprotected sector address.

Table 5 Flash Memory Command Definitions

Command Sequence		Bus Write Cycles Req'd	First Bus Write Cycle		Second Bus Write Cycle		Third Bus Write Cycle		Fourth Bus Read/Write Cycle		Fifth Bus Write Cycle		Sixth Bus Write Cycle	
			Addr.	Data	Addr.	Data	Addr.	Data	Addr.	Data	Addr.	Data	Addr.	Data
Read/Reset (Note 1)		1	XXXh	F0h	—	—	—	—	—	—	—	—	—	—
Read/Reset (Note 1)	Word	3	555h	AAh	2AAh	55h	555h	F0h	RA	RD	—	—	—	—
	Byte		AAAh		555h		AAAh							
Autoselect	Word	3	555h	AAh	2AAh	55h	(BA) 555h	90h	—	—	—	—	—	—
	Byte		AAAh		555h		(BA) AAAh							
Program	Word	4	555h	AAh	2AAh	55h	555h	A0h	PA	PD	—	—	—	—
	Byte		AAAh		555h		AAAh							
Chip Erase	Word	6	555h	AAh	2AAh	55h	555h	80h	555h	AAh	2AAh	55h	555h	10h
	Byte		AAAh		555h		AAAh		AAAh		555h		AAAh	
Sector Erase	Word	6	555h	AAh	2AAh	55h	555h	80h	555h	AAh	2AAh	55h	SA	30h
	Byte		AAAh		555h		AAAh		AAAh		555h			
Sector Erase Suspend		1	BA	B0h	—	—	—	—	—	—	—	—	—	—
Sector Erase Resume		1	BA	30h	—	—	—	—	—	—	—	—	—	—
Set to Fast Mode	Word	3	555h	AAh	2AAh	55h	555h	20h	—	—	—	—	—	—
	Byte		AAAh		555h		AAAh							
Fast Program (Note 2)	Word	2	XXXh	A0h	PA	PD	—	—	—	—	—	—	—	—
	Byte													
Reset from Fast Mode (Note 2)	Word	2	BA	90h	XXXh	F0h (Note6)	—	—	—	—	—	—	—	—
	Byte													
Extended Sector Group Protection (Note 3)	Word	4	XXXh	60h	SPA	60h	SPA	40h	SPA	SD	—	—	—	—
	Byte													
Query (Note 4)	Word	1	55h	98h	—	—	—	—	—	—	—	—	—	—
	Byte		AAh											
Hi-ROM Entry	Word	3	555h	AAh	2AAh	55h	555h	88h	—	—	—	—	—	—
	Byte		AAAh		555h		AAAh							
Hi-ROM Program (Note 5)	Word	4	555h	AAh	2AAh	55h	555h	A0h	PA	PD	—	—	—	—
	Byte		AAAh		555h		AAAh							
Hi-ROM Erase (Note 5)	Word	6	555h	AAh	2AAh	55h	555h	80h	555h	AAh	2AAh	55h	HRA	30h
	Byte		AAAh		555h		AAAh		AAAh		555h			
Hi-ROM Exit (Note 5)	Word	4	555h	AAh	2AAh	55h	(HRBA) 555h	90h	XXXh	00h	—	—	—	—
	Byte		AAAh		555h		(HRBA) AAAh							

Notes: 1. Both Read/Reset commands are functionally equivalent, resetting the device to the read mode.
2. This command is valid while Fast Mode.
3. This command is valid while $\overline{RESET}=V_{ID}$.
4. The valid Address is A_0 to A_6.

5: This command is valid while Hi-ROM mode.
6: The data “00h” is also acceptable.

Address bits A_{11} to A_{20} = X = “H” or “L” for all address commands except for Program Address (PA), Sector Address (SA),and Bank Address (BA).
Bus operations are defined in Table 2 "User Bus Operations".
RA = Address of the memory location to be read.
PA = Address of the memory location to be programmed.
Addresses are latched on the falling edge of the write pulse.

SA = Address of the sector to be erased. The combination of A_{20}, A_{19}, A_{18}, A_{17}, A_{16}, A_{15}, A_{14}, A_{13}, and A_{12} will uniquely select any sector.
BA = Bank address (A_{15} to A_{20})
SPA = Sector group address to be protected. Set sector group address (SGA) and (A_6, A_1, A_0) = (0, 1, 0).
HRA= Address of the Hidden-ROM area.
MB84VD2228XEA/EE (Top Boot Type) Word mode: 1F8000h to 1FFFFFh
Byte mode: 3F0000h to 3FFFFFh
MB84VD2229XEA/EE (Bottom Boot Type) Word mode: 000000h to 007FFFh
Byte mode: 000000h to 00FFFFh
HRBA = Bank address of the Hidden-ROM area
MB84VD2228XEA/EE (Top Boot Type) : $A_{15} = A_{16} = A_{17} = A_{18} = A_{19} = A_{20} = 1$
MB84VD2229XEA/EE (Bottom Boot Type) : $A_{15} = A_{16} = A_{17} = A_{18} = A_{19} = A_{20} = 0$
RD = Data read from location RA during read operation.
PD = Data to be programmed at location PA.
SD = Sector protection verify data. Output 01h at protected sector addresses and output 00h at unprotectedsector addresses.

The system should generate the following address patterns;
Word mode : 555h or 2AAh to addresses A_0 to A_{10}
Byte mode : AAAh or 555h to addresses A_{-1} and A_0 to A_{10}

■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating		Unit
		Min.	Max.	
Storage Temperature	Tstg	–55	+125	°C
Ambient Temperature with Power Applied	T_A	–25	+85	°C
Voltage with Respect to Ground All pins except A_9, $\overline{OE}$, $\overline{RESET}$, $\overline{WP}$/ACC (Note 1)	V_{IN}, V_{OUT}	–0.3	$V_{CC}f$ +0.3	V
			$V_{CC}s$ +0.4	V
$V_{CC}f$/$V_{CC}s$ Supply (Note 1)	$V_{CC}f$,$V_{CC}s$	–0.3	+4.0	V
A_9 and $\overline{OE}$ (Note2)	V_{IN}	–0.3	+13.0	V
$\overline{RESET}$ (Note 2)	V_{IN}	–0.5	+ 13.0	V
$\overline{WP}$/ACC (Note 3)	V_{IN}	–0.5	+10.5	V

Notes: 1. Minimum DC voltage on input or I/O pins is –0.3 V. During voltage transitions, input or I/O pins may undershoot V_{SS} to –2.0 V for periods of up to 20 ns. Maximum DC voltage on input or I/O pins is $V_{CC}f$ +0.3 V or $V_{CC}s$+0.4 V. During voltage transitions, input or I/O pins may overshoot to $V_{CC}f$+2.0 V or $V_{CC}s$+2.0 V for periods of up to 20 ns.

2. Minimum DC input voltage on A_9 and $\overline{OE}$ pin is –0.3 V. Minimum DC input voltage on $\overline{RESET}$ pin is –0.5 V. During voltage transitions, A_9, $\overline{OE}$, and $\overline{RESET}$ pins may undershoot V_{SS} to –2.0 V for periods of up to 20 ns.
   Voltage difference between input and supply voltage (VIN-$V_{CC}f$ or $V_{CC}s$) does not exceed 9.0 V.
   Maximum DC input voltage on A_9, $\overline{OE}$, and $\overline{RESET}$ pins is +13.0 V which may overshoot to +14.0 V for periods of up to 20 ns.

3. Minimum DC input voltage on $\overline{WP}$/ACC pin is –0.5 V. During voltage transitions, $\overline{WP}$/ACC pin may undershoot Vss to –2.0 V for periods of up to 20 ns. Maximum DC input voltage on $\overline{WP}$/ACC pin is +10.5 V which may overshoot to +12.0 V for periods of up to 20 ns, when $V_{CC}f$ is applied.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value		Unit
		Min.	Max.	
Ambient Temperature	T_A	–25	+85	°C
$V_{CC}f$/$V_{CC}s$ Supply Voltages	Vccf, Vccs	+2.7	+3.3	V

Note: Operating ranges define those limits between which the functionality of the device is guaranteed.

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within the recommended operating conditions. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representative beforehand.

■ ELECTRICAL CHARACTERISTICS

1. DC Characteristics

Parameter Symbol	Parameter Description	Test Conditions			Min.	Typ.	Max.	Unit
I_{LI}	Input Leakage Current	V_{IN} = V_{SS} to V_{CCf}, V_{CCS}			–1.0	—	+1.0	µA
I_{LO}	Output Leakage Current	V_{OUT} = V_{SS} to V_{CCf}, V_{CCS}			–1.0	—	+1.0	µA
I_{LIT}	$\overline{RESET}$ Inputs Leakage Current	V_{CCf} = V_{CCf} Max., V_{CCS} = V_{CCS} Max., $\overline{RESET}$ = 12.5V			—	—	35	µA
I_{LIA}	ACC Input Leakage Current	V_{CCf} = V_{CCf} Max., V_{CCS} = V_{CCS} Max., $\overline{WP}$/A_{CC} = V_{ACC} Max			—	—	20	mA
I_{CC1f}	Flash V_{CC} Active Current (Read) (Note 1)	$\overline{CE}f$ = V_{IL}, $\overline{OE}$ = V_{IH}	t_{CYCLE} = 5 MHz	Byte	—	—	16	mA
			t_{CYCLE} = 5 MHz	Word	—	—	18	
			t_{CYCLE} = 1 MHz	Byte	—	—	7	mA
			t_{CYCLE} = 1 MHz	Word	—	—	7	
I_{CC2f}	Flash V_{CC} Active Current (Program/Erase) (Note 2)	$\overline{CE}f$ = V_{IL}, $\overline{OE}$ = V_{IH}			—	—	35	mA
I_{CC3f}	Flash V_{CC} Active Current (Read-While-Program) (Note 5)	$\overline{CE}f$ = V_{IL}, $\overline{OE}$ = V_{IH}		Byte	—	—	51	mA
				Word	—	—	53	
I_{CC4f}	Flash V_{CC} Active Current (Read-While-Erase) (Note 5)	$\overline{CE}f$ = V_{IL}, $\overline{OE}$ = V_{IH}		Byte	—	—	51	mA
				Word	—	—	53	
I_{CC5f}	Flash V_{CC} Active Current (Erase-Suspend-Program)	$\overline{CE}f$ = V_{IL}, $\overline{OE}$ = V_{IH}			—	—	35	mA
I_{CC1S}	SRAM V_{CC} Active Current	V_{CCS} = V_{CC} Max., $\overline{CE1}s$ = V_{IL}, $CE2s$ = V_{IH}	t_{CYCLE} =10 MHz		—	—	50	mA
I_{CC2S}	SRAM V_{CC} Active Current	$\overline{CE1}s$ = 0.2 V, $CE2s$ = V_{CCS} – 0.2 V	t_{CYCLE} = 10 MHz		—	—	50	mA
			t_{CYCLE} = 1 MHz		—	—	8	mA
I_{SB1f}	Flash V_{CC} Standby Current	V_{CCf} = V_{CC} Max., $\overline{CE}f$ = V_{CCf} ± 0.3 V $\overline{RESET}$ = V_{CCf} ± 0.3 V, $\overline{WP}$/A_{CC} = V_{CCf}± 0.3 V			—	1	5	µA
I_{SB2f}	Flash V_{CC} Standby Current ($\overline{RESET}$)	V_{CCf} = V_{CC} Max., $\overline{RESET}$ = V_{SS} ± 0.3 V, $\overline{WP}$/A_{CC} = V_{CCf}± 0.3 V			—	1	5	µA
I_{SB3f}	Flash V_{CC} Current (Automatic Sleep Mode) (Note 3)	V_{CCf} = V_{CC} Max., $\overline{CE}f$ = V_{SS} ± 0.3 V $\overline{RESET}$ = V_{CCf} ± 0.3 V, $\overline{WP}$/A_{CC} = V_{CCf}± 0.3 V V_{IN} = V_{CCf}± 0.3 V or V_{SS} ± 0.3 V			—	1	5	µA
I_{SB1S}	SRAM V_{CC} Standby Current	$\overline{CE1}s \geq V_{CCS}$ – 0.2 V, $CE2s \geq V_{CCS}$ – 0.2 V			—	—	25	µA
I_{SB2S}	SRAM V_{CC} Standby Current	$CE2s \leq$ 0.2 V			—	—	25	µA

(Continued)

(Continued)

Parameter Symbol	Parameter Description	Test Conditions	Min.	Typ.	Max.	Unit
V_{IL}	Input Low Level	—	–0.3	—	0.5	V
V_{IH}	Input High Level	—	2.4	—	V_{CC}+0.3*	V
V_{ID}	Voltage for Sector Protection, and Temporary Sector Unprotection ($\overline{RESET}$) (Note 4)	—	11.5	—	12.5	V
V_{ACC}	Voltage for Program Acceleration ($\overline{WP}$/ACC) (Note4)	—	8.5	9.0	9.5	V
V_{OL}	Output Low Voltage Level	$V_{CC}f$ = $V_{CC}f$ Min., $V_{CC}s$ = $V_{CC}s$ Min., I_{OL}=1.0 mA	—	—	0.4	V
V_{OH}	Output High Voltage Level	$V_{CC}f$ = $V_{CC}f$ Min., $V_{CC}s$ = $V_{CC}s$ Min., I_{OH}=–0.5 mA	2.4	—	—	V
V_{LKO}	Flash Low $V_{CC}f$ Lock-Out Voltage	—	2.3	—	2.5	V

*: V_{CC} indicates lower of $V_{CC}f$ or $V_{CC}s$.

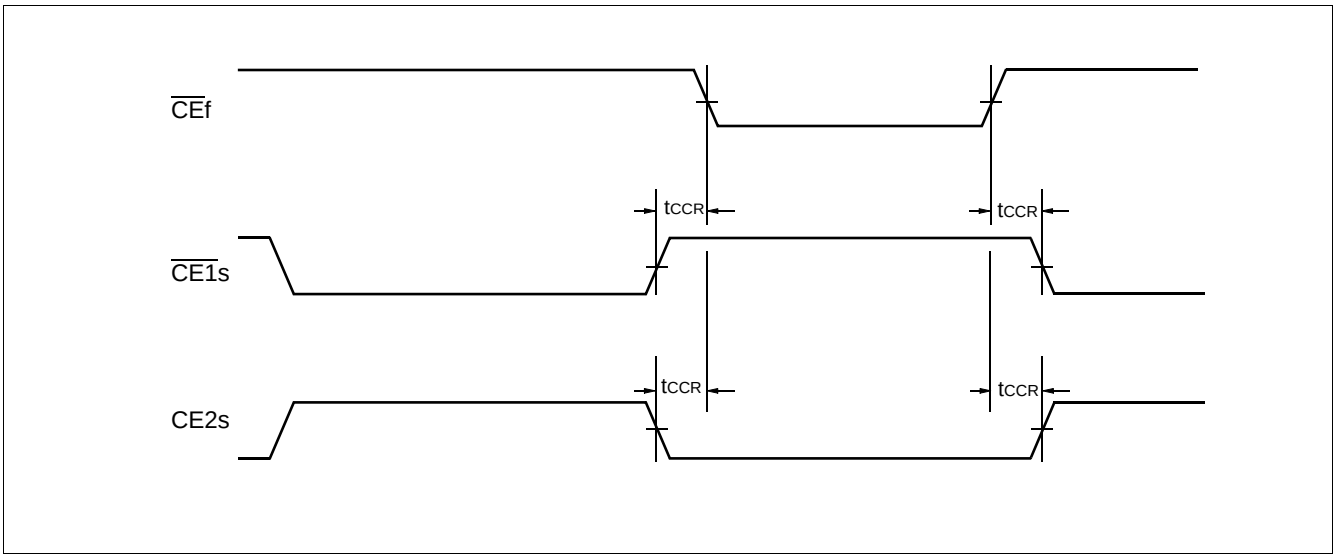
Notes: 1. The I_{CC} current listed includes both the DC operating current and the frequency dependent component.
2. I_{CC} active while Embedded Algorithm (program or erase) is in progress.
3. Automatic sleep mode enables the low power mode when address remain stable for 150 ns.
4. Applicable for only $V_{CC}f$ applying.
5. Embedded Alogorithm (program or erase) is in progress. (@5 MHz)

2. AC Characteristics

- **$\overline{CE}$ Timing**

Parameter Symbols		Description	Test Setup		-90	Unit
JEDEC	Standard					
—	t_{CCR}	$\overline{CE}$ Recover Time	—	Min.	0	ns

- **Timing Diagram for alternating SRAM to Flash**

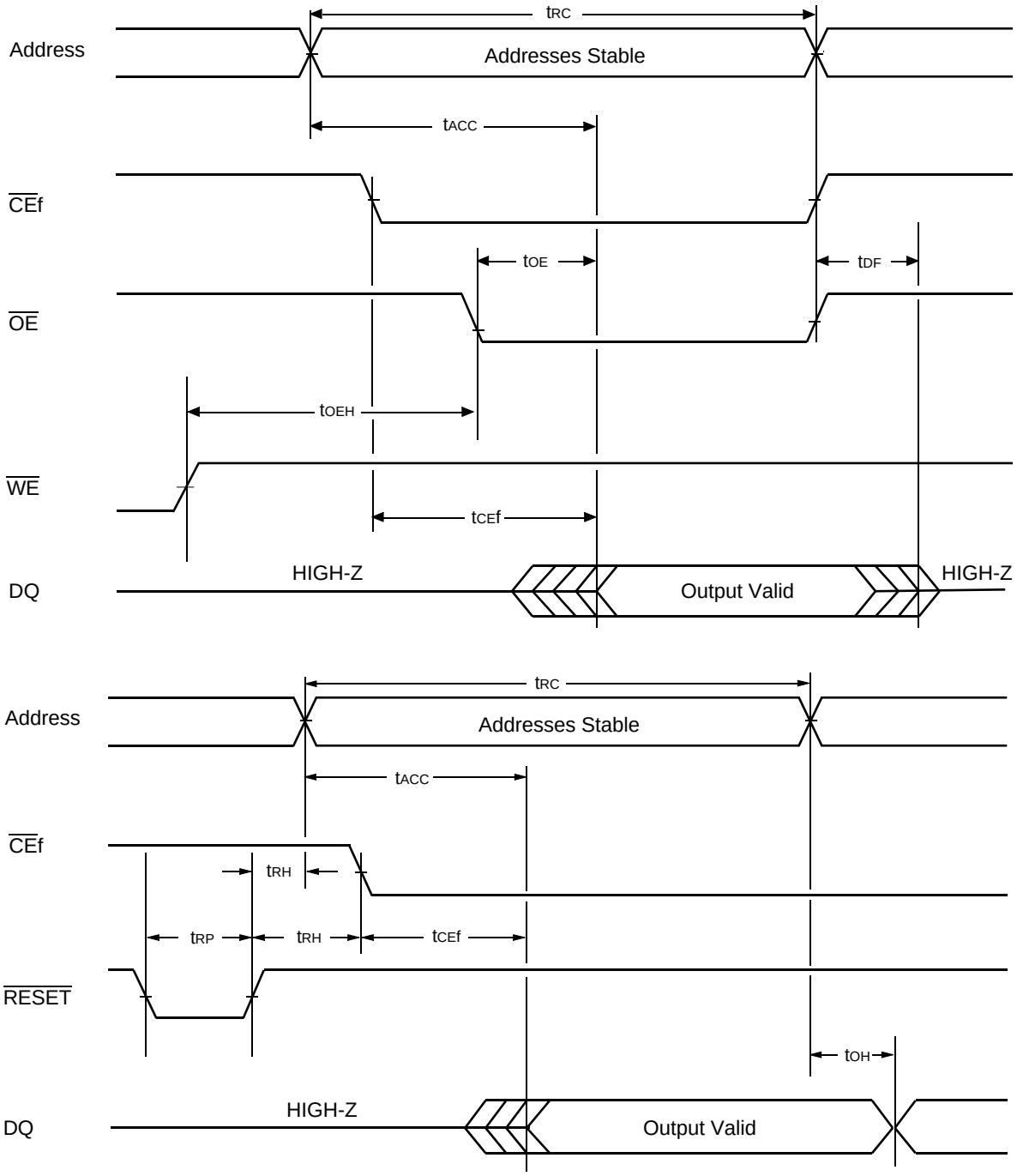


- **Read Only Operations Characteristics (Flash)**

Parameter Symbols		Description	Test Setup	-90 (Note)		Unit
JEDEC	Standard			Min.	Max.	
t_{AVAV}	t_{RC}	Read Cycle Time	—	90	—	ns
t_{AVQV}	t_{ACC}	Address to Output Delay	$\overline{CE}f = V_{IL}$ $\overline{OE} = V_{IL}$	—	90	ns
t_{ELQV}	$t_{CE}f$	Chip Enable to Output Delay	$\overline{OE} = V_{IL}$	—	90	ns
t_{GLQV}	t_{OE}	Output Enable to Output Delay	—	—	40	ns
t_{EHQZ}	t_{DF}	Chip Enable to Output High-Z	—	—	30	ns
t_{GHQZ}	t_{DF}	Output Enable to Output High-Z	—	—	30	ns
t_{AXQX}	t_{OH}	Output Hold Time From Addresses, $\overline{CE}f$ or $\overline{OE}$, Whichever Occurs First	—	0	—	ns
—	t_{READY}	$\overline{RESET}$ Pin Low to Read Mode	—	—	20	µs

Note: Test Conditions–Output Load: 1 TTL gate and 30 pF
Input rise and fall times: 5 ns
Input pulse levels: 0.0 V to 3.0 V
Timing measurement reference level
Input: 1.5 V
Output: 1.5 V

- **Read Cycle (Flash)**



• **Erase/Program Operations (Flash)**

Parameter Symbols		Description		-90			Unit
JEDEC	Standard			Min.	Typ.	Max.	
t_{AVAV}	t_{WC}	Write Cycle Time		90	—	—	ns
t_{AVWL}	t_{AS}	Address Setup Time ($\overline{WE}$ to Addr.)		0	—	—	ns
—	t_{ASO}	Address Setup Time to $\overline{CE}$ Low During Toggle Bit Polling		15	—	—	ns
t_{WLAX}	t_{AH}	Address Hold Time ($\overline{WE}$ to Addr.)		45	—	—	ns
—	t_{AHT}	Address Hold Time from $\overline{CE}$ or $\overline{OE}$ High During Toggle Bit Polling		0	—	—	ns
t_{DVWH}	t_{DS}	Data Setup Time		35	—	—	ns
t_{WHDX}	t_{DH}	Data Hold Time		0	—	—	ns
—	t_{OES}	Output Enable Setup Time		0	—	—	ns
—	t_{OEH}	Output Enable Hold Time	Read	0	—	—	ns
			Toggle and $\overline{Data}$ Polling	10	—	—	ns
—	t_{CEPH}	$\overline{CE}$ High During Toggle Bit Polling		20	—	—	ns
—	t_{OEPH}	$\overline{OE}$ High During Toggle Bit Polling		20	—	—	ns
t_{GHEL}	t_{GHEL}	Read Recover Time Before Write ($\overline{OE}$ to $\overline{CE}$f)		0	—	—	ns
t_{GHWL}	t_{GHWL}	Read Recover Time Before Write ($\overline{OE}$ to $\overline{WE}$)		0	—	—	ns
t_{WLEL}	t_{WS}	$\overline{WE}$ Setup Time ($\overline{CE}$f to $\overline{WE}$)		0	—	—	ns
t_{ELWL}	t_{CS}	$\overline{CE}$f Setup Time ($\overline{WE}$ to $\overline{CE}$f)		0	—	—	ns
t_{EHWH}	t_{WH}	$\overline{WE}$ Hold Time ($\overline{CE}$f to $\overline{WE}$)		0	—	—	ns
t_{WHEH}	t_{CH}	$\overline{CE}$f Hold Time ($\overline{WE}$ to $\overline{CE}$f)		0	—	—	ns
t_{WLWH}	t_{WP}	Write Pulse Width		35	—	—	ns
t_{ELEH}	t_{CP}	$\overline{CE}$f Pulse Width		35	—	—	ns
t_{WHWL}	t_{WPH}	Write Pulse Width High		30	—	—	ns
t_{EHEL}	t_{CPH}	$\overline{CE}$f Pulse Width High		30	—	—	ns
t_{WHWH1}	t_{WHWH1}	Byte Programming Operation		—	8	—	µs
		Word Programming Operation		—	16	—	µs
t_{WHWH2}	t_{WHWH2}	Sector Erase Operation (Note 1)		—	1	—	s

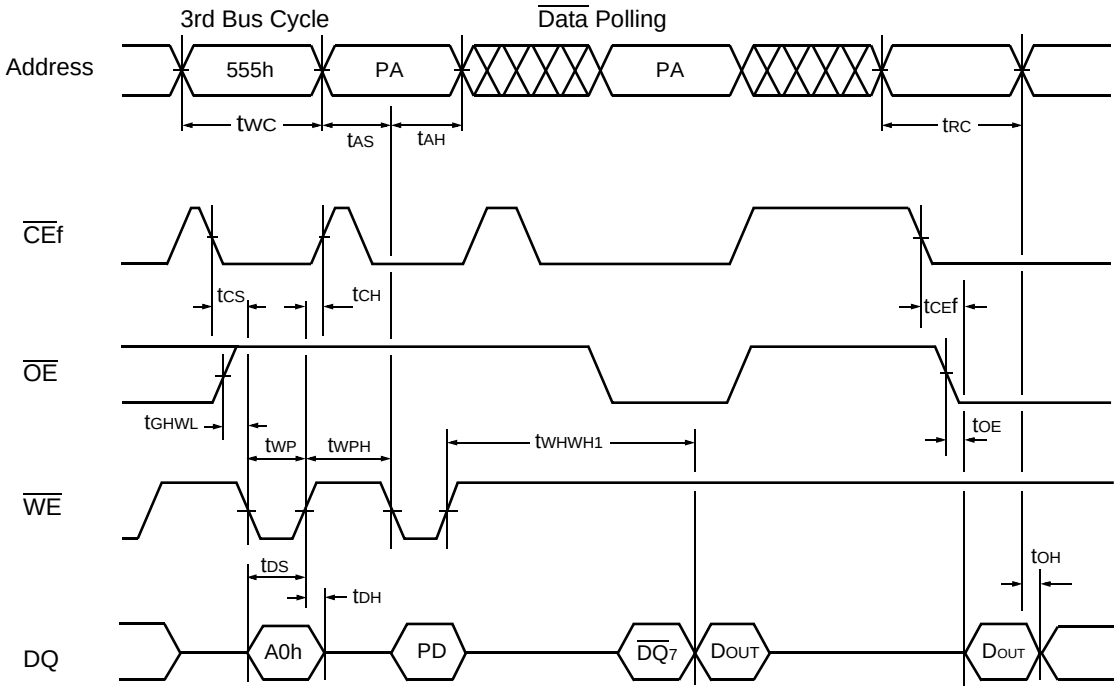
(Continued)

(Continued)

Parameter Symbols		Description	-90			Unit
JEDEC	Standard		Min.	Typ.	Max.	
—	t_{VCS}	V_{CC}f Setup Time	50	—	—	µs
—	t_{VLHT}	Voltage Transition Time (Note 2)	4	—	—	µs
—	t_{VIDR}	Rise Time to V_{ID} (Note 2)	500	—	—	ns
—	t_{VACCR}	Rise Time to V_{ACC}	500	—	—	ns
—	t_{RB}	Recover Time from RY/$\overline{BY}$	0	—	—	ns
—	t_{RP}	$\overline{RESET}$ Pulse Width	500	—	—	ns
—	t_{EOE}	Delay Time from Embedded Output Enable	—	—	90	ns
—	t_{RH}	$\overline{RESET}$ High Level Period Before Read	200	—	—	ns
—	t_{BUSY}	Program/Erase Valid to RY/$\overline{BY}$ Delay	—	—	90	ns
—	t_{TOW}	Erase Time-out Time (Note 3)	50	—	—	µs
—	t_{SPD}	Erase Suspend Transition Time (Note 4)	—	—	20	µs

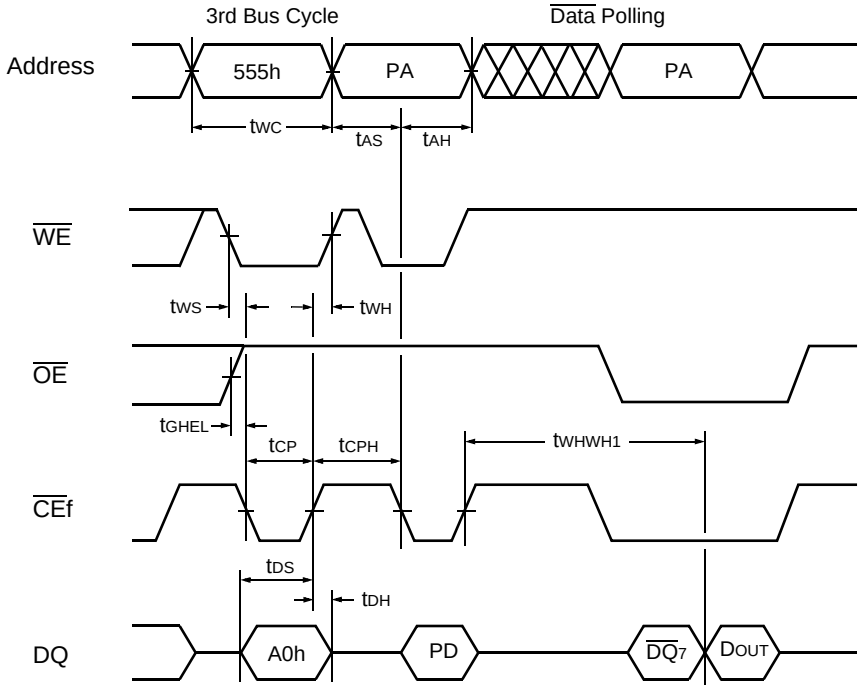
Notes: 1. This does not include the preprogramming time.
2. This timing is for Sector Protection Operation.
3. The time between writes must be less than "t_{TOW}" otherwise that command will not be accepted and erasure will start. A time-out or "t_{TOW}" from the rising edge of last $\overline{CE}$ or $\overline{WE}$ whichever happens first will initiate the execution of the Sector Erase command(s).
4. When the Erase Suspend command is written during the Sector Erase operation, the device will take a maximum of "t_{SPD}" to suspend the erase operation.

- **Write Cycle ($\overline{WE}$ control) (Flash)**



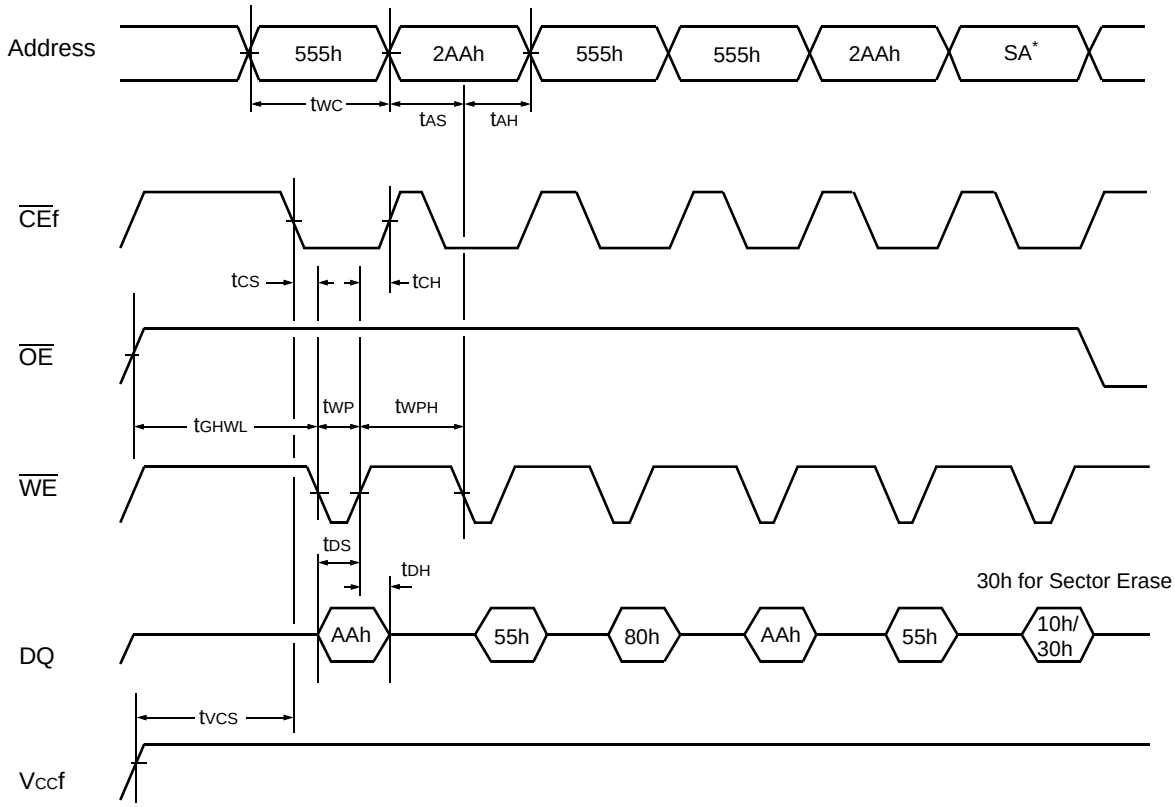
Notes:
- PA is address of the memory location to be programmed.
- PD is data to be programmed at byte address.
- $\overline{DQ}_7$ is the output of the complement of the data written to the device.
- D_{OUT} is the output of the data written to the device.
- Figure indicates last two bus cycles out of four bus cycle sequence.
- These waveforms are for the ×16 mode. (The addresses differ from ×8 mode.)

- **Write Cycle ($\overline{CE}$f control) (Flash)**



Notes:
- PA is address of the memory location to be programmed.
- PD is data to be programmed at byte address.
- $\overline{DQ}_7$ is the output of the complement of the data written to the device.
- D_{OUT} is the output of the data written to the device.
- Figure indicates last two bus cycles out of four bus cycle sequence.
- These waveforms are for the ×16 mode. (The addresses differ from ×8 mode.)

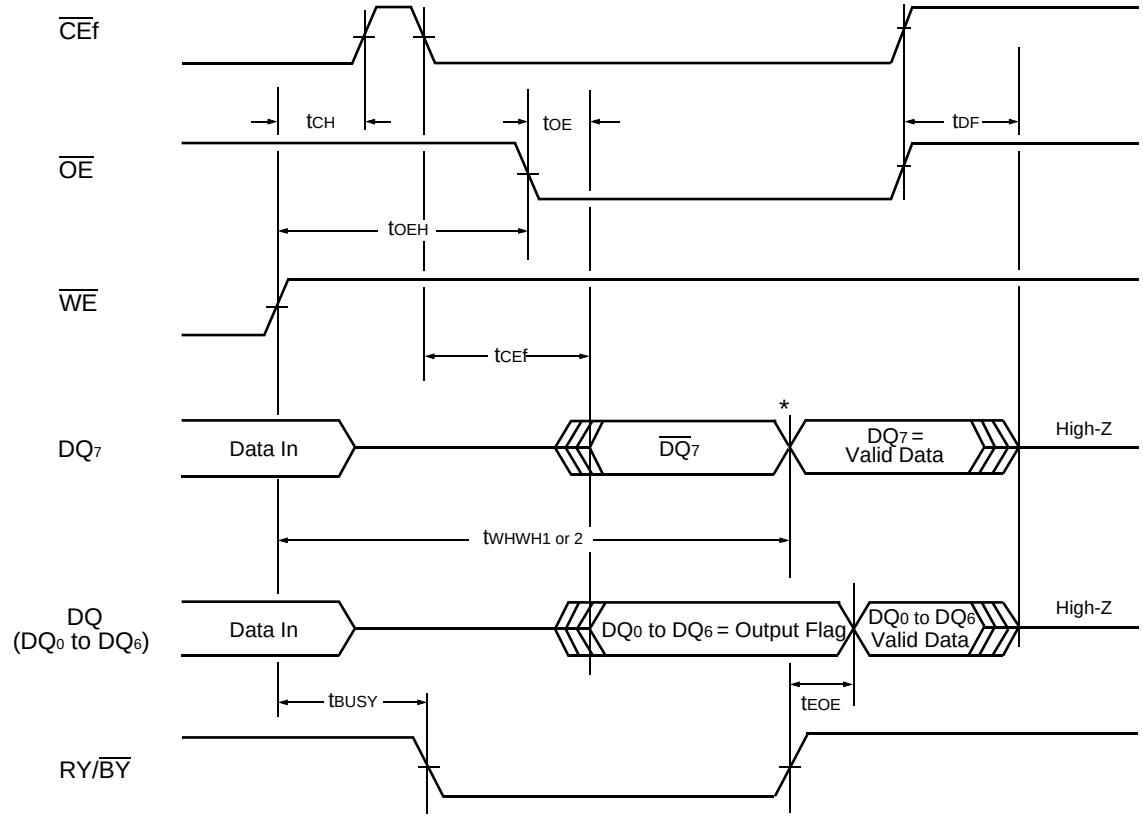
- **AC Waveforms Chip/Sector Erase Operations (Flash)**



*: SA is the sector address for Sector Erase. Addresses = 555h for Chip Erase.

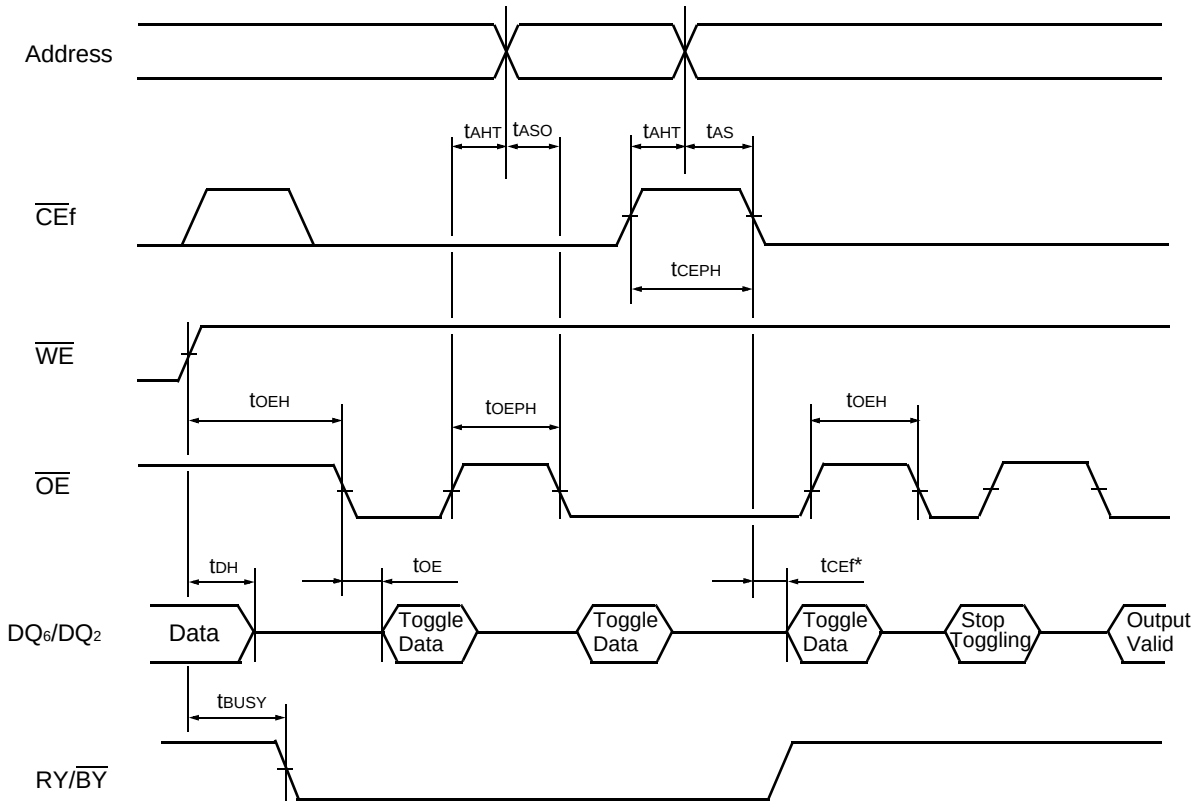
Note: These waveforms are for the ×16 mode. (The addresses differ from ×8 mode.)

- **AC Waveforms for $\overline{\text{Data}}$ Polling during Embedded Algorithm Operations (Flash)**



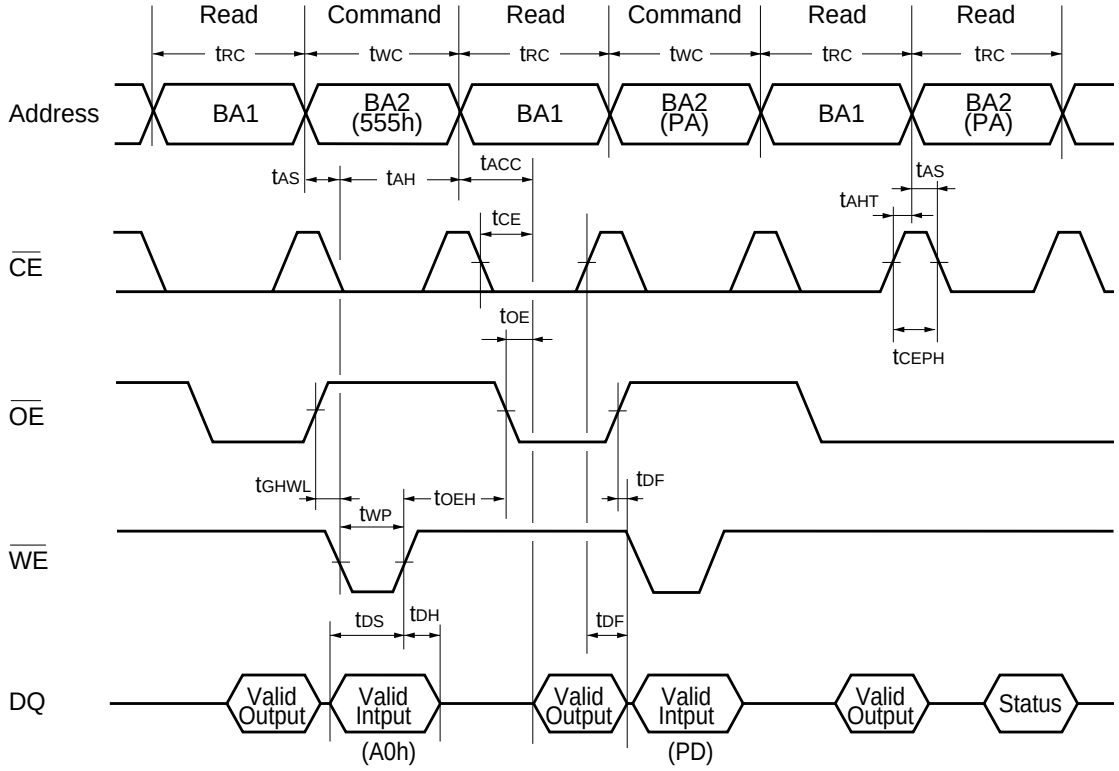
*: DQ_7 = Valid Data (The device has completed the Embedded operation.)

- **AC Waveforms for Toggle Bit during Embedded Algorithm Operations (Flash)**



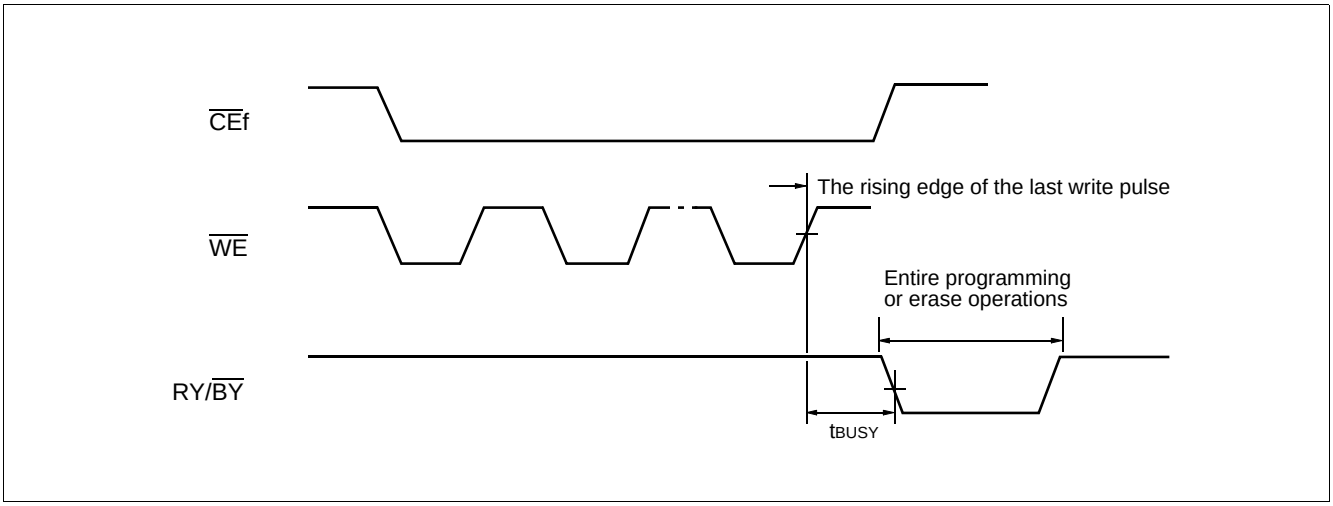
* : DQ_6 stops toggling (The device has completed the Embedded operation).

- **Back-to-back Read/Write Timing Diagram (Flash)**

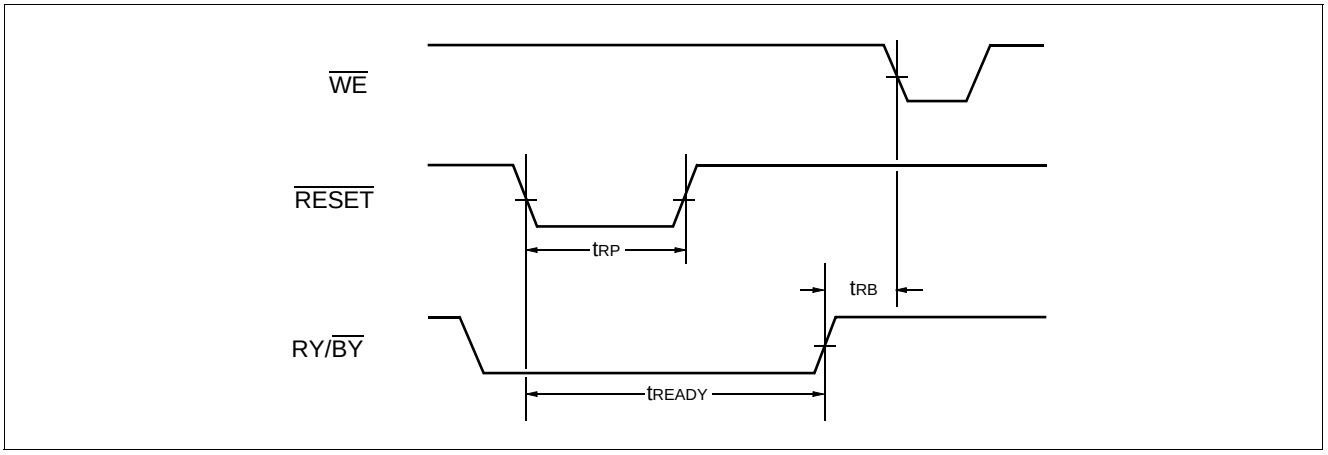


Note: This is example of Read for Bank 1 and Embedded Algorithm (program) for Bank 2.
BA1: Address of Bank 1.
BA2: Address of Bank 2.

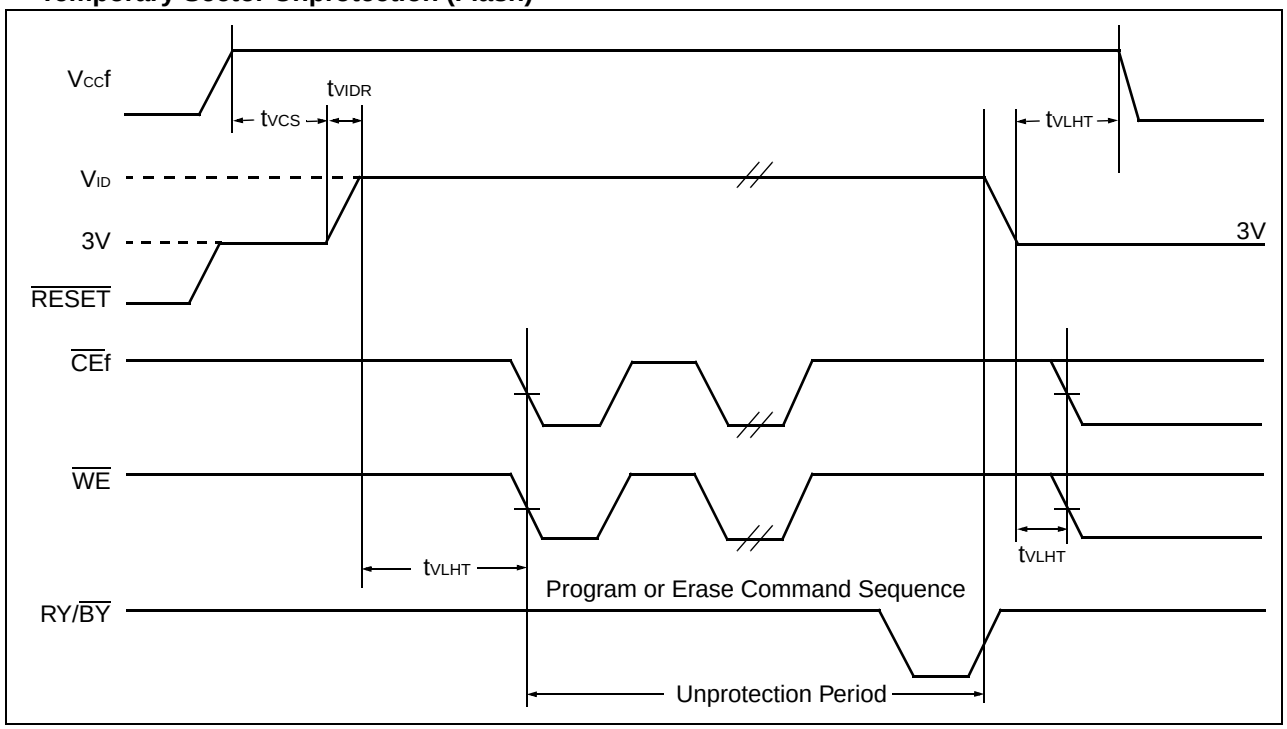
- **RY/$\overline{BY}$ Timing Diagram during Write/Erase Operations (Flash)**



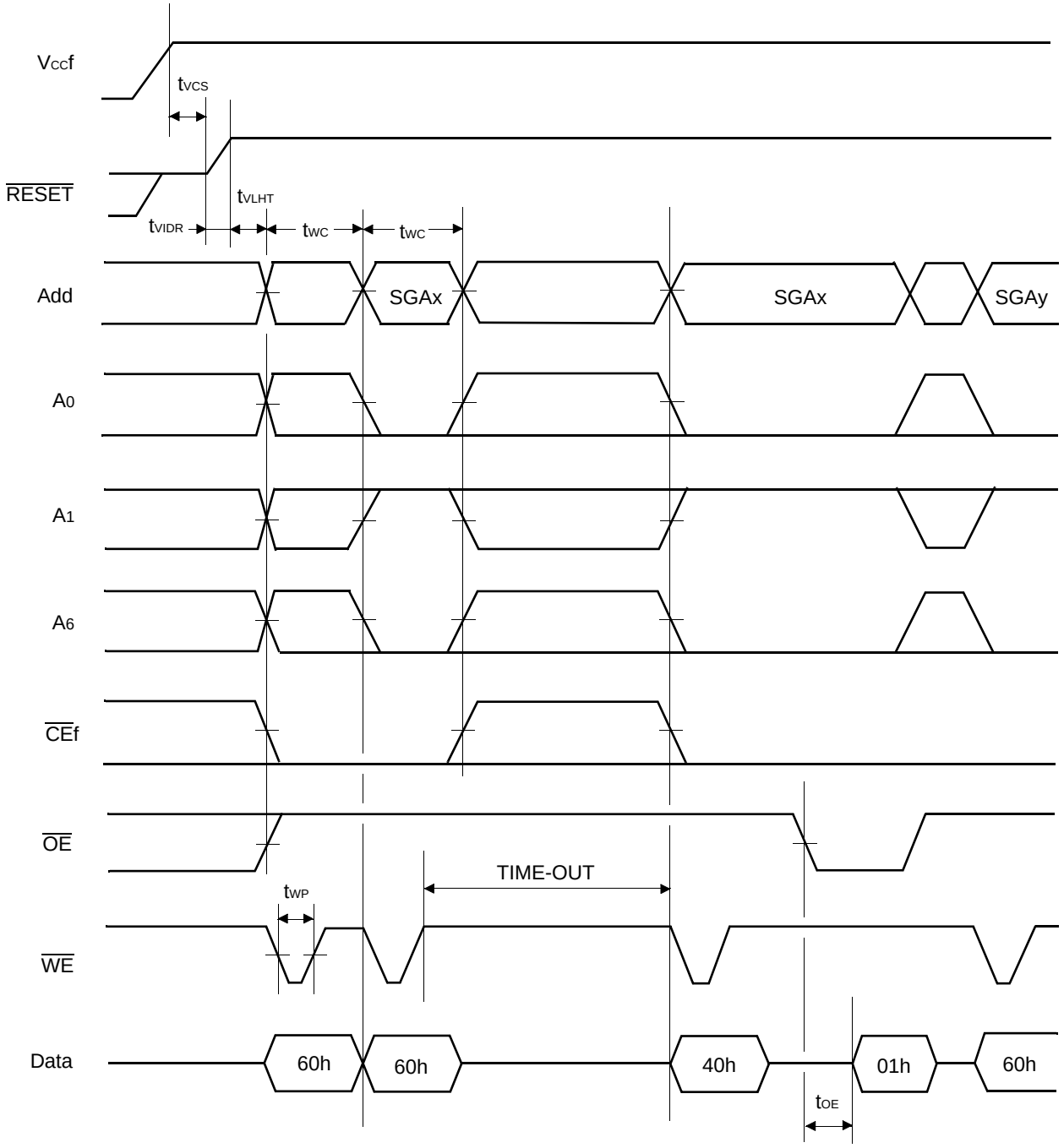
- **$\overline{RESET}$, RY/$\overline{BY}$ Timing Diagram (Flash)**



- **Temporary Sector Unprotection (Flash)**

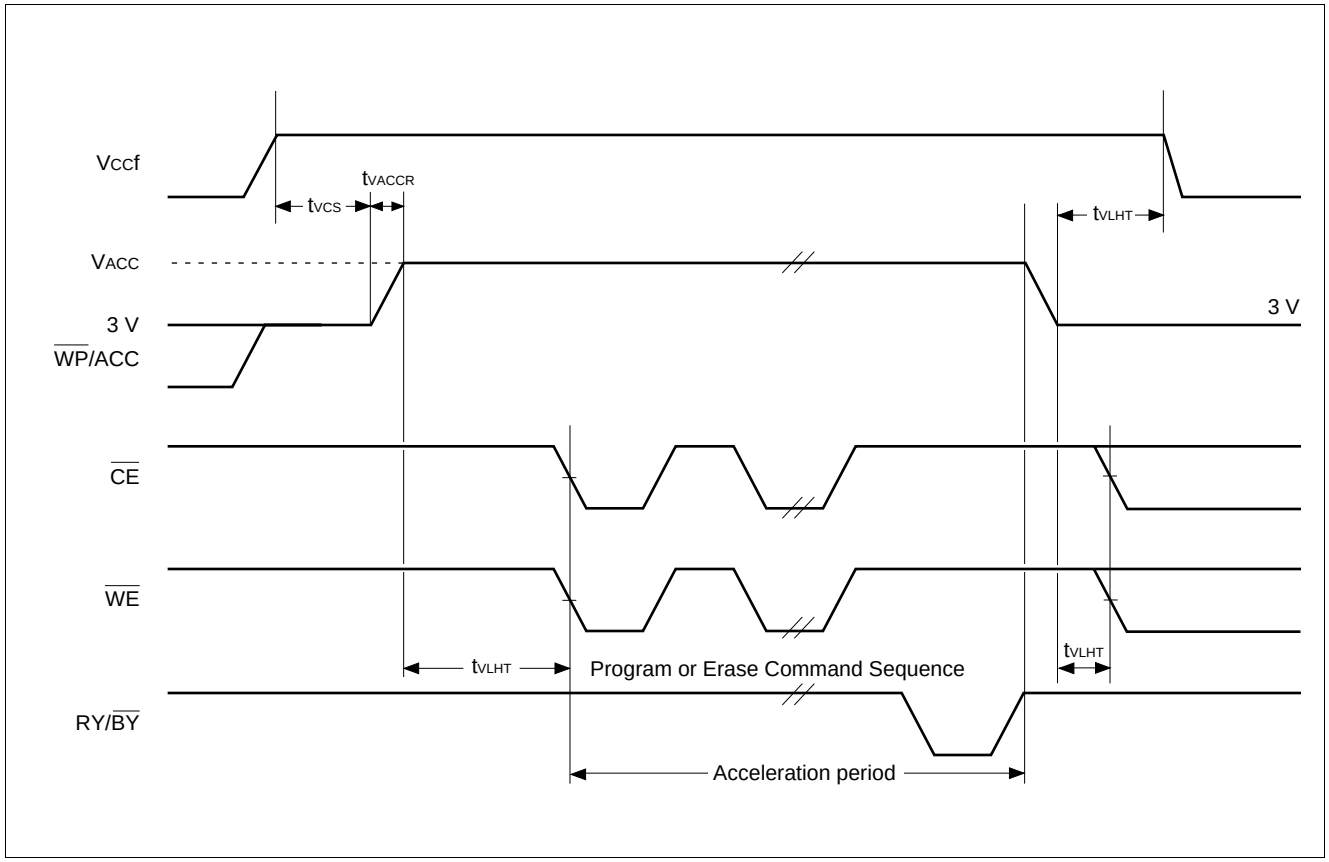


- **Extended Sector Protection (Flash)**



SGAx: Sector Group Address to be protected
SGAy : Next Group Sector Address to be protected
TIME-OUT : Time-Out window = 250 μs (Min.)

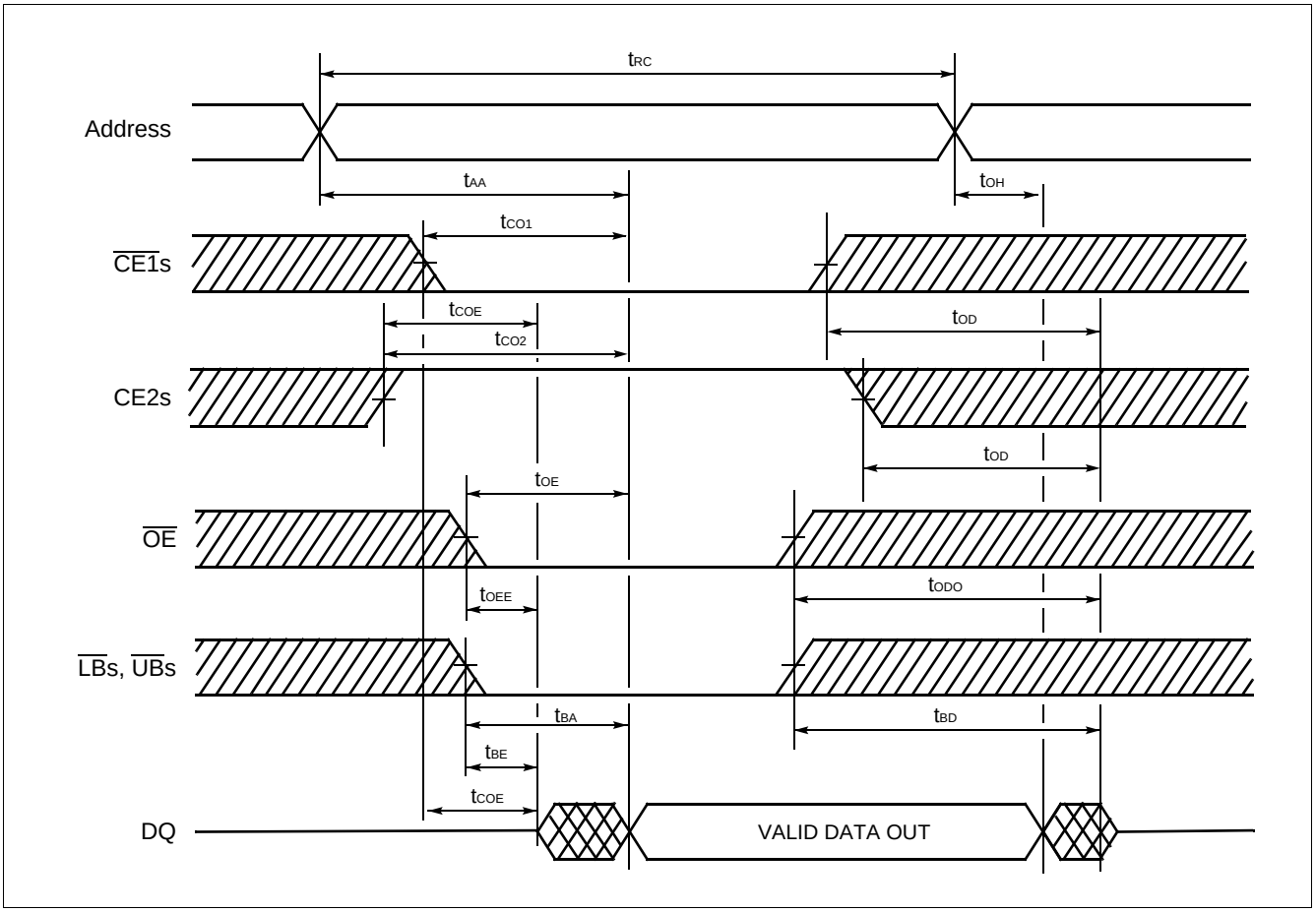
- **Accelerated Program (Flash)**



- **Read Cycle (SRAM)**

Parameter Symbol	Parameter Description	Min.	Max.	Unit
t_{RC}	Read Cycle Time	70	—	ns
t_{AA}	Address Access Time	—	70	ns
t_{CO1}	Chip Enable ($\overline{CE1}$s) Access Time	—	70	ns
t_{CO2}	Chip Enable (CE2s) Access Time	—	70	ns
t_{OE}	Output Enable Access Time	—	35	ns
t_{BA}	$\overline{LB}$, $\overline{UB}$ to Output Valid	—	70	ns
t_{COE}	Chip Enable ($\overline{CE1}$s Low and CE2s High) to Output Active	5	—	ns
t_{OEE}	Output Enable Low to Output Active	0	—	ns
t_{BE}	$\overline{UB}$, $\overline{LB}$ Enable Low to Output Active	0	—	ns
t_{OD}	Chip Enable ($\overline{CE1}$s High or CE2s Low) to Output High-Z	—	25	ns
t_{ODO}	Output Enable High to Output High-Z	—	25	ns
t_{BD}	$\overline{UB}$, $\overline{LB}$ Output Enable to Output High-Z	—	25	ns
t_{OH}	Output Data Hold Time	10	—	ns

- **Read Cycle (Note 1) (SRAM)**

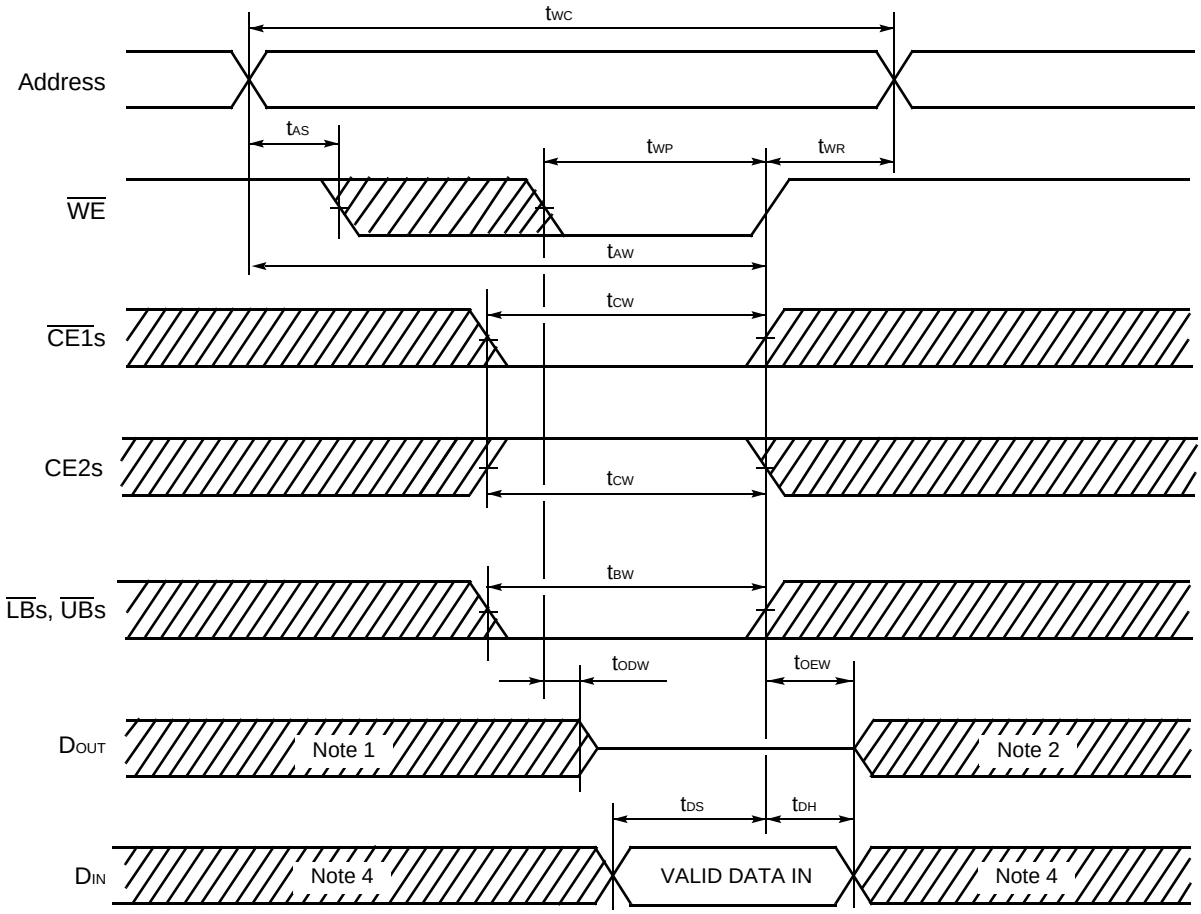


Note: $\overline{WE}$ remains HIGH for the read cycle.

- **Write Cycle (SRAM)**

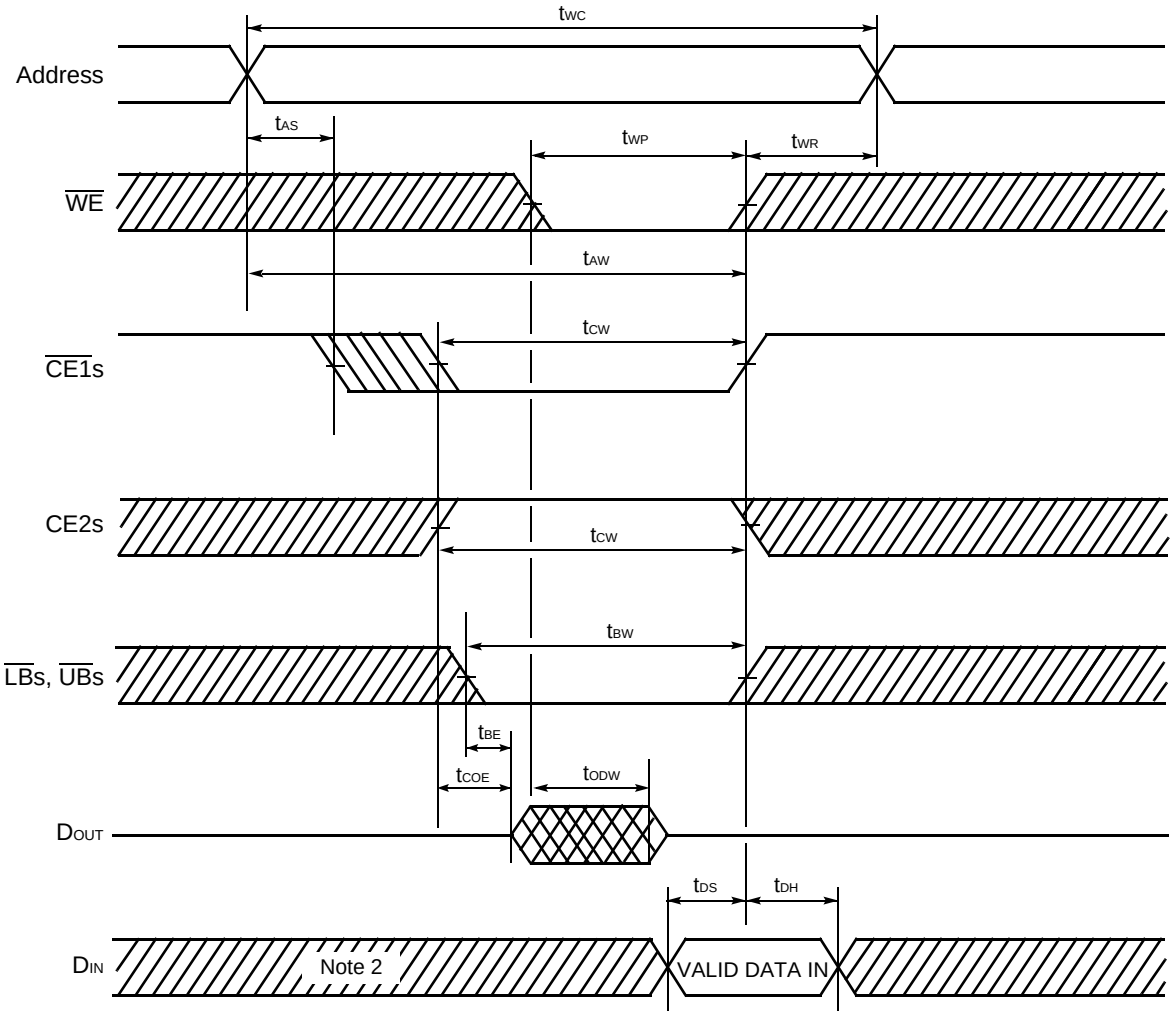
Parameter Symbol	Parameter Description	Min.	Max.	Unit
t_{WC}	Write Cycle Time	70	—	ns
t_{WP}	Write Pulse Width	55	—	ns
t_{CW}	Chip Enable to End of Write	60	—	ns
t_{AW}	Address valid to End of Write	60	—	ns
t_{BW}	$\overline{UB}$, $\overline{LB}$ to End of Write	60	—	ns
t_{AS}	Address Setup Time	0	—	ns
t_{WR}	Write Recovery Time	0	—	ns
t_{ODW}	$\overline{WE}$ Low to Output High-Z	—	25	ns
t_{OEW}	$\overline{WE}$ High to Output Active	0	—	ns
t_{DS}	Data Setup Time	30	—	ns
t_{DH}	Data Hold Time	0	—	ns

- **Write Cycle (Note 3) ($\overline{WE}$ control) (SRAM)**



Notes:
1. If $\overline{CE1}$s goes LOW (or CE2s goes HIGH) coincident with or after $\overline{WE}$ goes LOW, the output will remain at high impedance.
2. If $\overline{CE1}$s goes HIGH (or CE2s goes LOW) coincident with or before $\overline{WE}$ goes HIGH, the output will remain at high impedance.
3. If $\overline{OE}$ is HIGH during the write cycle, the outputs will remain at high impedance.
4. Because I/O signals may be in the output state at this time, input signals of reverse polarity must not be applied.

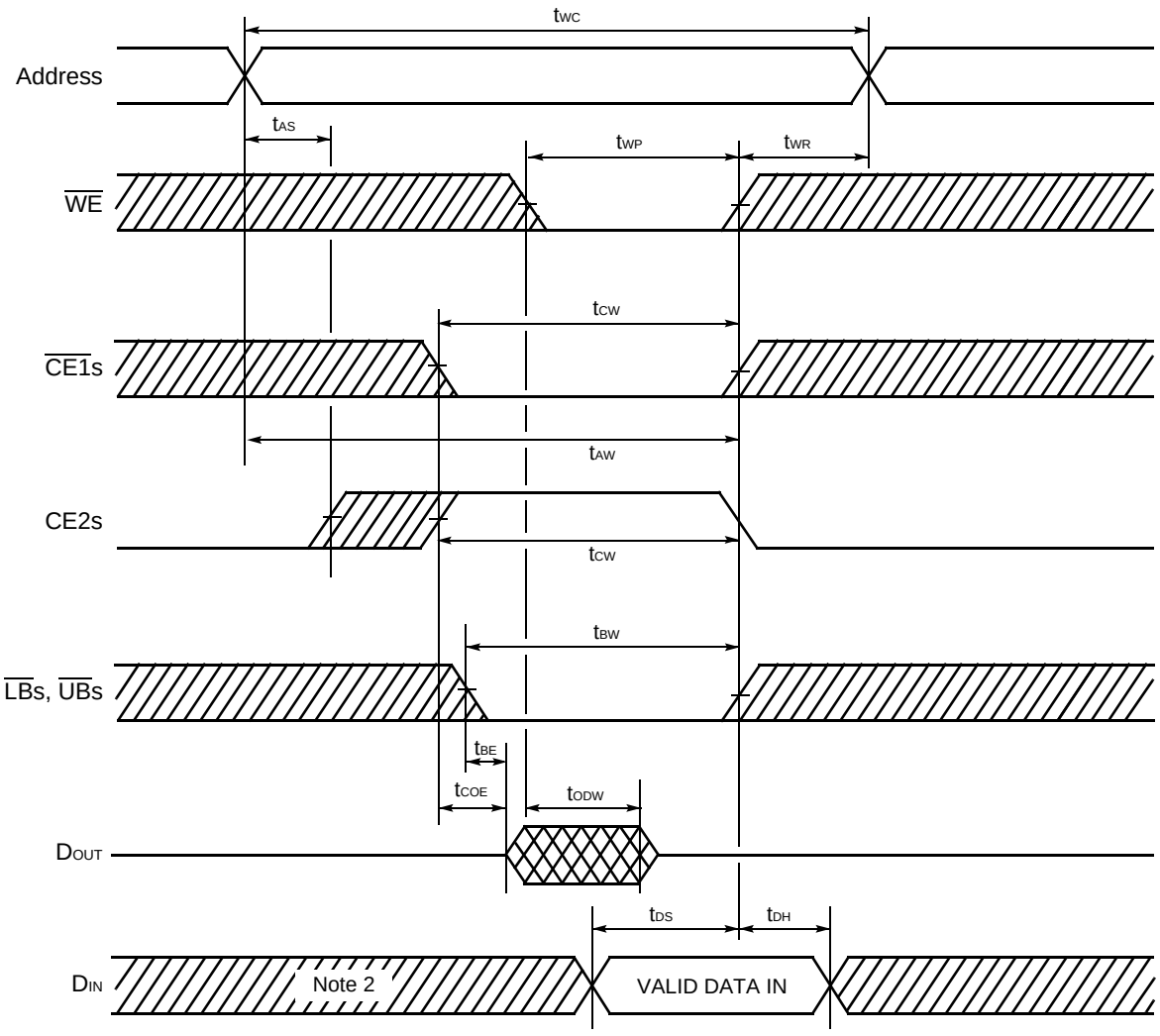
- **Write Cycle (Note 1) ($\overline{CE}$1s control) (SRAM)**



Notes: 1. If $\overline{OE}$ is HIGH during the write cycle, the outputs will remain at high impedance.

2. Because I/O signals may be in the output state at this time, input signals of reverse polarity must not be applied.

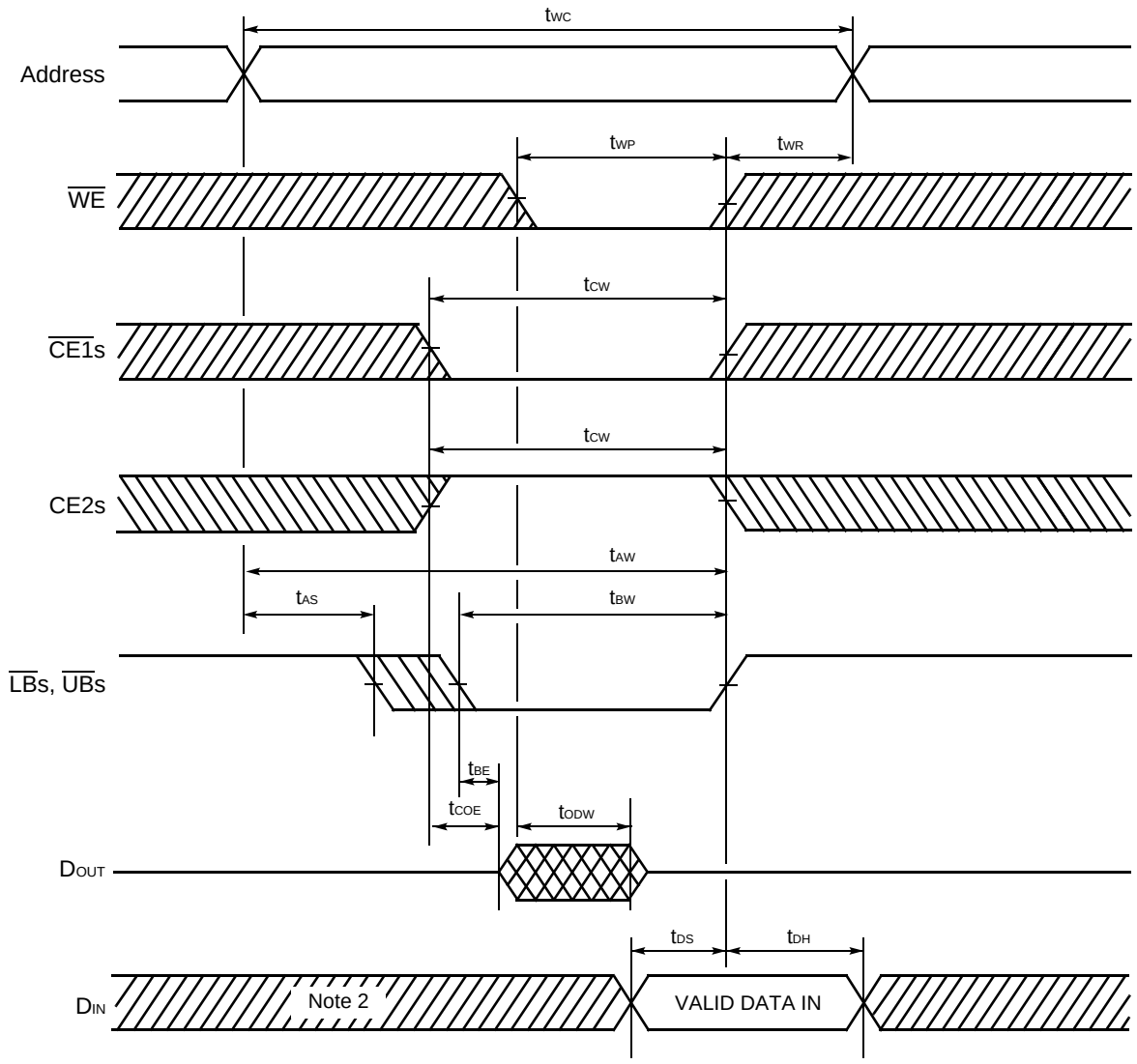
- **Write Cycle (Note 1) (CE2s Control) (SRAM)**



Notes: 1. If $\overline{OE}$ is HIGH during the write cycle, the outputs will remain at high impedance.

2. Because I/O signals may be in the output state at this time, input signals of reverse polarity must not be applied.

- **Write Cycle (Note 1) ($\overline{LB}$, $\overline{UB}$ Control) (SRAM)**



Notes: 1. If $\overline{OE}$ is HIGH during the write cycle, the outputs will remain at high impedance.

2. Because I/O signals may be in the output state at this time, input signals of reverse polarity must not be applied.

■ ERASE AND PROGRAMMING PERFORMANCE (Flash)

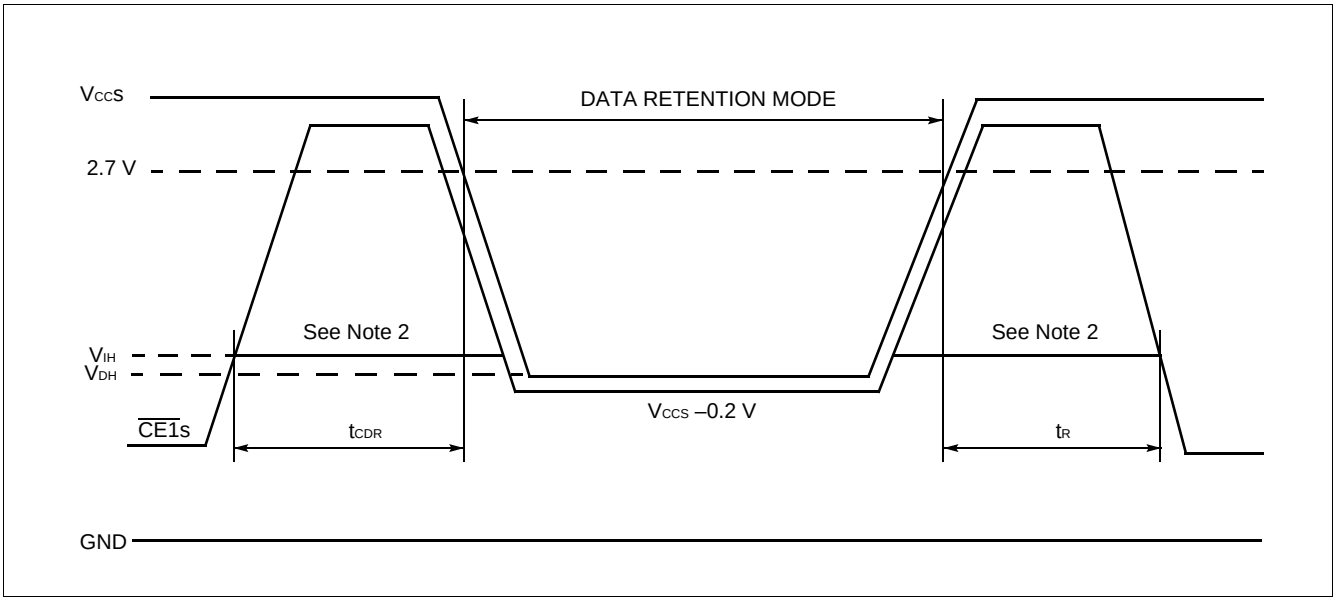
Parameter	Limits			Unit	Comment
	Min.	Typ.	Max.		
Sector Erase Time	—	1	10	s	Excludes programming time prior to erasure
Byte Programming Time	—	8	300	µs	Excludes system-level overhead
Word Programming Time	—	16	360	µs	Excludes system-level overhead
Chip Programming Time	—	—	100	s	Excludes system-level overhead
Erase/Program Cycle	100,000	—	—	cycle	

■ DATA RETENTION CHARACTERISTICS (SRAM)

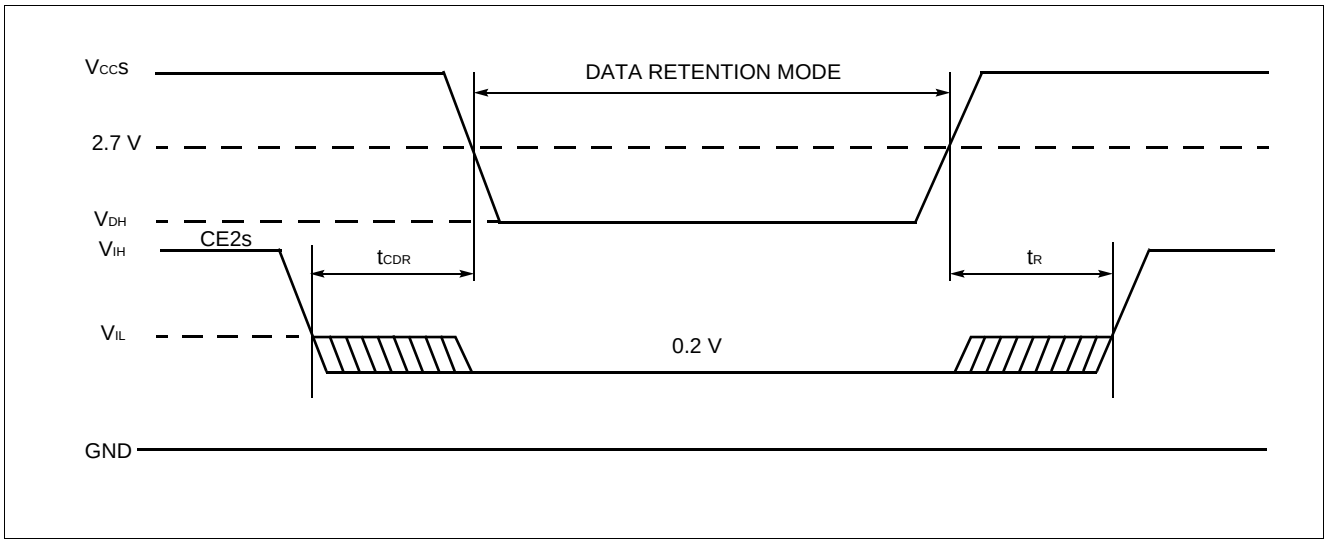
Parameter Symbol	Parameter Description		Min.	Typ.	Max.	Unit
V_{DH}	Data Retention Supply Voltage		1.5	—	3.3	V
I_{DDS2}	Standby Current	V_{DH} = 3.0 V	—	TBD	TBD	µA
t_{CDR}	Chip Deselect to Data Retention Mode Time		0	—	—	ns
t_R	Recovery Time		t_{RC}	—	—	ns

Note: t_{RC}: Read cycle time

- **$\overline{CE1}$s Controlled Data Retention Mode (Note 1)**



- **CE2s Controlled Data Retention Mode (Note 3)**



Notes: 1. In $\overline{CE1}$s controlled data retention mode, input level of CE2s should be fixed Vccs to Vccs–0.2 V or Vss to 0.2 V during data retention mode. Other input and input/output pins can be used between –0.3 V to Vccs+0.3 V.
2. When $\overline{CE1}$s is operating at the V_{IH} min. level (2.2 V), the standby current is given by I_{SB1}s during the transition of V_{CC}s from 3.6 to 2.2 V.
3. In CE2s controlled data retention mode, input and input/output pins can be used between –0.3 V to Vccs+0.3 V.

■ PIN CAPACITANCE

Parameter Symbol	Parameter Description	Test Setup	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0	11	14	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0	12	16	pF
C_{IN2}	Control Pin Capacitance	V_{IN} = 0	14	16	pF
C_{IN3}	$\overline{WP}$/ACC Pin Capacitance	V_{IN} = 0	21.5	26	pF

Note: Test conditions T_A = 25°C, f = 1.0 MHz

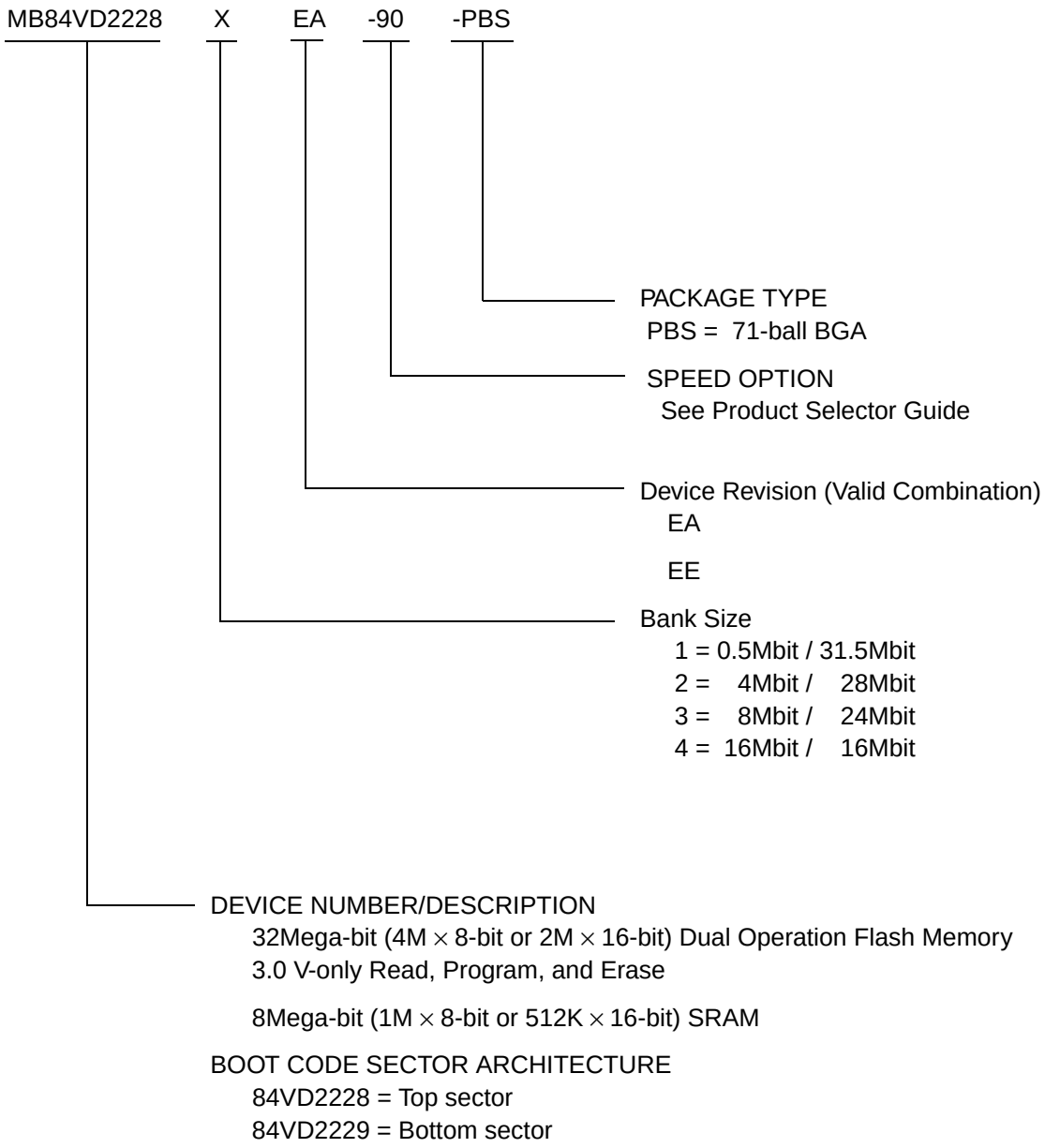
■ HANDLING OF PACKAGE

Please handle this package carefully since the sides of packages are right angle.

■ CAUTION

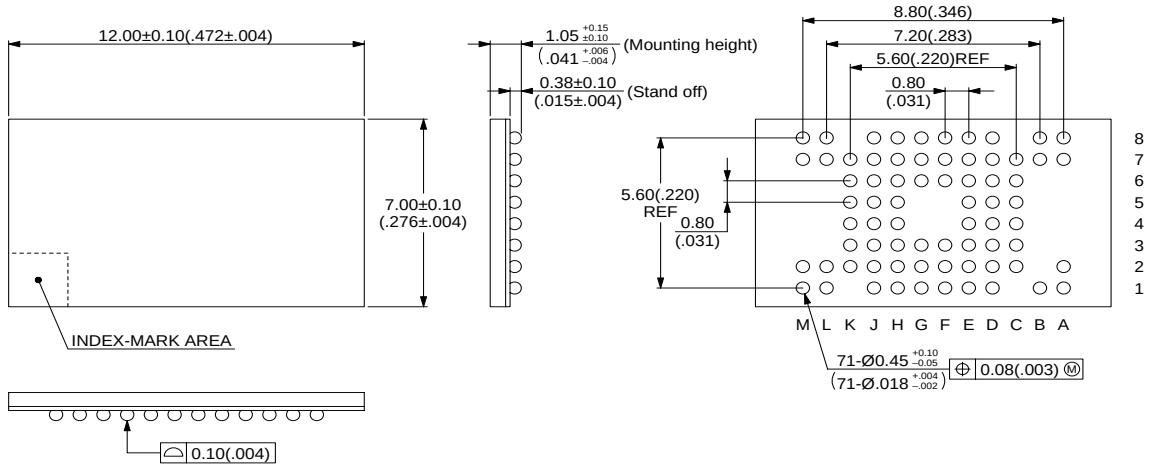
1) The high voltage (V_{ID}) can not apply to address pins and control pins except $\overline{RESET}$. Therefore, it can not use autoselect and sector protect function by applying the high voltage (V_{ID}) to specific pins.
2) For the sector protection, since the high voltage (V_{ID}) can be applied to the $\overline{RESET}$, it can be protected the sector useing “Extended sector protect” command.

■ ORDERING INFORMATION



■ PACKAGE DIMENSION

71-ball plastic FBGA
(BGA-71P-M01)



Dimensions in mm (inches)

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