Monolithic Digital IC



LB1817W

FDD Spindle Motor Driver

Overview

The LB1817W is a spindle motor driver for low-profile floppy disk drives.

Functions and Features

- Three-phase full-wave linear drive (with external PNP transistor)
- Low saturation voltage
- Built-in digital speed control
- Start/stop circuit (Low active)
- Switchable rotation speed
- Current limiter circuit
- Built-in index processing circuit
- Index timing adjustable by VR
- AGC circuit
- Thermal protection circuit

Package Dimensions

unit: mm

3163A-SQFP48



Specifications

Absolute Maximum Ratings at $Ta = 25^{\circ}C$

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V _{CC} max		7.0	V
Maximum output current	I _{CC} max1	t ≤ 0.5s	1.5	А
Maximum constant output current	I _O max2		1.0	А
Allowable power dissipation	Pd max1	IC only	0.45	W
Operating temperature	Topr		-20 to +80	°C
Storage temperature	Tstg		-40 to +150	°C

Allowable Operating Ranges at $Ta = 25^{\circ}C$

Parameter	Symbol	Conditions	Ratings	Unit
Power supply voltage	V _{CC}		4.2 to 6.5	V

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SANYO Electric Co., Ltd. Semiconductor Company TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO, 110-8534 JAPAN

Electrical Characteristics at Ta = 25°C, V_{CC} = 5V

Demonster	Quarteral	O a sultitude		Ratings		
Parameter	Symbol	Conditions	min	typ	max	Unit
Current drain	Icco	S/S = 5V (Standby)		70	100	μA
		S/S = 0V (Normal)		25	35	mA
MS1 bias current		$V_{MC}1 = 5V$		180	270	μA
MS1 Low input voltage	VMc1L		0.0		0.8	V
MS1 High input voltage	V _M S ¹		2		Vee	V
MS2 bias current	MS ^{III}	1/1 = 2 - 5/1	-	90	135	μΔ
MS2 Low input voltage	MS ²	* MS2 = 0 *	0.0		0.8	V
MS2 High input voltage	V 2H		0.0		0.0 V	V
MS2 high input voltage	MS ²¹¹	$\sqrt{2-5}$	2	00	VCC 125	v
MS3 bias current	MS ³	V _{MS} 3 = 3V	0.0	90	133	μΑ
MC2 List input voltage	V _{MS} SL		0.0		0.8	V
NIS3 High input voltage	V _{MS} 3H		2		VCC	V
S/S bias current	I _{S/S}				20	μΑ
S/S Low voltage	V _{S/SL}		0.0		0.8	V
S/S High voltage	V _{S/SH}		2		V _{CC}	V
Hall amplifier input bias current	I _{HB}				15	μA
Common mode input voltage range	Vh		2.0		V _{CC} -0.7	V
Differential input voltage range	Vdif		50		200	mVp-p
Input offset voltage	Vho	*			±10	mV
Hall bias output voltage	V _H	I _H = 5 mA	0.5	0.8	1.1	V
Leakage current	V _{HL}	S/S = 5V			±10	μΑ
Output saturation voltage	V(sat)	$I_{O} = 0.8A$		0.45	0.64	V
Output leakage current	I _{OI}				1	mA
Current limiter	Ilim	$R_F = 3 k\Omega, R_{OUT} = 100\Omega$	6.3	7.5	8.7	mA
Control amplifier voltage gain	G _C		-7.5	-5.5	-3.5	dB
Voltage gain phase differential	ΔG _C				±1	dB
V/I conversion source current	C		19	28	37	μA
V/I conversion sink current	-		-19	-28	-37	uА
V/I conversion current ratio	+/ -		0.8	1.0	1.2	
DSC buffer input current	1000				1	μА
EG amplifier input voltage	VEO	f = 300 Hz	2		20	m\/n-n
FG amplifier voltage gain	Geo	Open loop*	-	60	20	dB
FG amplifier input offset	V	*		00	+10	m\/
EG amplifier internal reference voltage	V FGO		2.2	2.5	29	111V V
EC Sobmitt by storogic width	VFGB	High s low*	2.2	2.5	2.0	v m\/
		l light -> LOW		25		m)/
Concept discrimination equat				20		mv
Speed discriminator count		*		1390/2		N 41 1-
Discriminator operating frequency	FD				1.1	MHZ
Oscillator frequency	Fosc				1.1	MHZ
Oscillator frequency tolerance					±0.2	%
Index output Low voltage	V _{IDL}	I _O = 2 mA			0.4	V
Index output leakage current	I _{IDL}				±10	μΑ
Index amplifier common mode input voltage range	VI		0.2		V _{CC} -0.7	V
Index amplifier differential input voltage range	V _{DIF}	Hysteresis width < 25 mA	25		100	mV
Index amplifier hysteresis set current	I _{HYS}		2.9	4.2	5.5	μΑ
Timing adjustment at High level	V _{TH}	MS1 = L	1.15	1.26	1.35	V
Timing adjustment at Low level	V _{TL}	MS1 = L	0.40	0.52	0.60	V
Timing adjustment ratio	T _{HL}	V _{TH} (MS1 = L) / V _{TH} (MS1 = H)		1.148		
Reference voltage	V _{REF} 1		2.20	2.50	2.80	V
	V _{REF} 2		1.85	2.15	2.45	V
Thermal protection operating temperature	TSD	*	150	180		°C
Hysteresis width	∆TSD	*		10		°C

Note: Items shown to be "*" are not measured.

Pin Assignment



Block Diagram



Pin Descriptions

Pin number	Pin name	Pin voltage	Equivalent circuit	Pin function
1, 5	NC			Pins not used
12, 13				
14, 19				
24, 25				
31, 36				
37, 47				
48				
2	V _{REF} 1	2.5V typ		 V_{REF}1 pin. Used as power supply for external CR serving for index timing adjustment.
3	V _{REF} 2	2.15V typ	○ Vcc → ↓ ↓ ↓ → → → → → → → → → → → → → → → →	 V_{REF}2 pin. Used as bias pin for external index sensor.
4	I/D		A A A A A A A A A A A A A A A A A A A	Index pulse output pin.
6	SG			Signal ground pin. Connect to ground together with pin 21.
7	MS3	H: 2.0V min L: 0.8V max		 FG switching pin. High: FG set to through Low: FG set to 1-stage division
8	MS2	H: 2.0V min L: 0.8V max	Ο Vcc	 CLK switching pin. High: Clock set to through Low: Clock set to 1-stage division

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Pin number	Pin name	Pin voltage	Equivalent circuit	Pin function
9	MS1	H: 2.0V min		Rotation speed switching pin.
		L: 0.8V max		High: 360 rpm
				Low: 300 rpm
				For details, see rotation speed switching
				table.
			\mathbf{I} \mathbf{I} \mathbf{I} \mathbf{I} \mathbf{I} \mathbf{I} \mathbf{I}	
10	S/S	H: 2.0V min		 Start/stop switching pin.
		L: 0.8V max		Low: active
			10 × 10	
			7// 7//	
44	1-			- Estematicales, incut sin
11	1			External index – input pin.
10	1.			 External index + input pin. When I = pip in High constant current 11
				flows When nin is Low constant current
				11 is cut off
				Resistor externally connected to I ⁻ pin
				determines hysteresis width.
16	X1			Reference clock generator pin.
			400Ω ≥	
47	V0			
17	λZ			
18	FC			• Frequency characteristics compensation
				pin.
				To prevent current control loop oscillation,
				insert a capacitor between this pin and
				V _{CC} .

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Pin number	Pin name	Pin voltage	Equivalent circuit	Pin function
20	RF			• Output current detection pin. To detect output current as a voltage, insert a resistor R_f between this pin and V_{CC} . The voltage is used for the current limiter. The detection level is about 1/50 of the output current.
21	PG			Output transistor ground pin. Connect to ground together with pin 6.
22 23	FG ⁺ FG ⁻	2.5V typ	200Ω 12kΩ % 12kΩ % 100Ω	 FG amplifier + pin FG amplifier – pin
26	FGout			• FG amplifier output pin.
27 28 29 30 32 33	U _{OUT} U _{PB} Vout V _{PB} Wout W _{PB}		$V_{CC} \circ $	 U phase output pin. U phase external PNP transistor base connection. V phase output pin. V phase external PNP transistor base connection. W phase output pin. W phase external PNP transistor base connection.
34 35 38 39 40 41	U _{IN} 2 U _{IN} 1 V _{IN} 2 V _{IN} 1 W _{IN} 2 W _{IN} 1		35 39 41 30 30 41 30 30 30 30 30 30 30 30 30 30 30 30 30	 U phase Hall input pin. Logic High means U_{IN}1 > U_{IN}2. V phase Hall input pin. Logic High means V_{IN}1 > V_{IN}2. W phase Hall input pin. Logic High means W_{IN}1 > W_{IN}2.

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Pin number	Pin name	Pin voltage	Equivalent circuit	Pin function
42	HB			Hall bias negative-side pin.
				In stop mode, the pin is open and Hall
				bias is cut off.
40	N (Deveneration
43	VCC			Power supply pin. The violation of the this pin must be
				the voltage supplied to this pin must be
				noises from inputting to this pin
44	AGC			AGC nin
	100		○ Vcc	Controls the Hall amplifier gain according
				to Hall input amplitude.
				An external capacitor is used.
			(44)	
45	DSC			 Speed discriminator pin.
46	СТ			Timing adjustment nin
40	01			External CR for time constant circuit is
				connected here.

Truth Table

	Courses . Cials	Hall input				
	Source -> Sink	U	V	W		
1	V phase -> W phase	Н	Н	L		
2	V phase -> U phase	L	Н	L		
3	W phase -> U phase	L	Н	Н		
4	W phase -> V phase	L	L	Н		
5	U phase -> V phase	Н	L	Н		
6	U phase -> W phase	Н	L	Ĺ		

Hall input pin High means $U_{IN}1 > U_{IN}2$ $V_{IN}1 > V_{IN}2$ $W_{IN}1 > W_{IN}2$

Rotation Speed Select Table

f _{OSC}	_C = 1 MHz	<u>.</u>						
MS1	Н	L	Н	L	Н	L	Н	L
MS2	H		l	_	Н		L	
MS3	ŀ	1	l	-	l	-	ŀ	1
f _{FG} [Hz]	720	600	720	600	1440	1200	360	300



Index and Timing Chart



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