INTERSIL

AO05
The ICL8007 — A High Performance FET — Input Operational Amplifier

INTRODUCTION

During the last 10 years the Field Effect Transistor has become the accepted device for amplifying low level currents. Until recently, however, high performance FET amplifiers have been available in only relatively expensive module or discrete form. With the introduction of the ICL8007, the first inexpensive high performance FET input OPAMP, Intersil has provided a device for use in those applications previously considered impossible due to cost factors. It is extremely easy to use, is a pin for pin replacement for the popular 741 (Ref 1), has internal compensation, and is short circuit protected. The ICL8007 is available in a hermetic TO5 type package and is ideally suited to both military and commercial applications.

CIRCUIT DESCRIPTION

Input Stage Design

Figure 1 shows a simplified schematic of the ICL8007. It is a two stage-circuit with a class AB complementary output and internal phase compensation.

The input stage consists of two bootstrapped FET source followers driving a lateral PNP emitter coupled pair. By using the FET's in the source follower mode, run to run variations of g_m have no influence on the stability. The bootstrap serves a dual purpose: it ensures excellent common mode rejection, and also prevents excessive gate currents. The latter problem is frequently seen in FET amplifiers, where at one end of the common mode range the FET sees large drain to source voltages.

Another feature of the input design which deserves comment is the method of offset adjustment. To minimize the temperature coefficient of the input offset voltage, it is imperative that the current through the two FET's be closely matched. Any attempt to compensate for initial offset by mismatching the FET drain currents will result in excessive temperature drift. The best place to implement the offset nulling is in the PNP stage, provided that Q_3 and Q_4 are fed from a low temperature coefficient current source; zeroing the offset will have no detrimental effect on the drift.

Input Current

The input current of the ICL8007 is typically less than 3 pA; it is selected for an input current of 1 pA maximum at 25° C. As with any junction FET input amplifier, this current approximately doubles for every 10° C increase in temperature, as shown in Figure 2.

Summary of Characteristics (Typ. at 25° C)

	ICL8007M	ICL8007C	ICL8007AM & ICL8007AC	UNITS
Input Offset Voltage	10	20	15	mV
Input Bias Current	2.0	3.0	0.5	pA
Input Resistance	10^6	10^6	10^6	MΩ
Common Mode Rejection	90	90	95	dB
Input Voltage Range	±12	±12	±12	V
Slew Rate	6.0	6.0	6.0	V/μs
Unity Gain Bandwidth	1.0	1.0	1.0	MHz

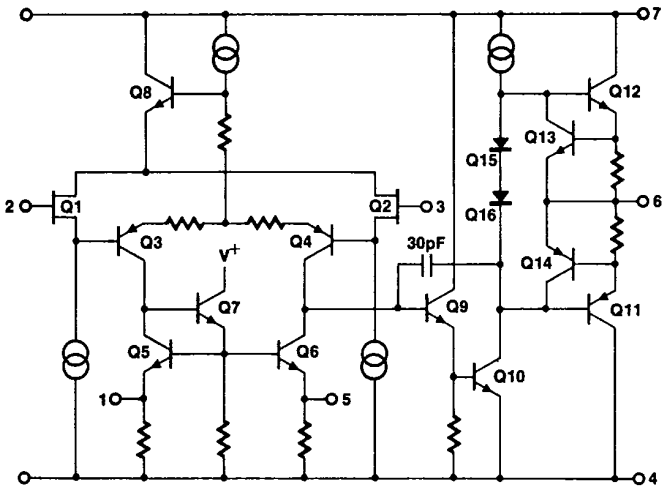

Figure 1: ICL8007 Simplified Schematic

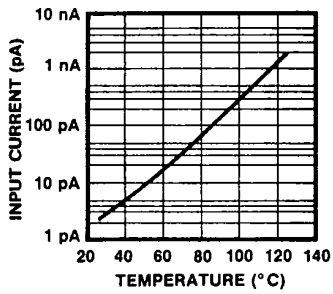

Figure 2: Input Bias Current as a Function of Temperature

Input Offset Voltage Drift

The input offset voltage drift of an FET amplifier is inherently worse than that of a well-designed bipolar circuit. The ICL8007M and ICL8007C are guaranteed to have temperature coefficients of less than 75μV/°C, while the ICL8007AM and ICL8007AC are specified at 50μV/°C maximum. Practically the whole of the manufacturing distribution falls within these limits, and it is straight forward to screen for tighter limits on a custom basis.

Noise Performance

The total mean square noise of an operational amplifier for a bandwidth $\Delta f = f_2 - f_1$ is given by

$$e_T^2 = \int \frac{f_2}{f_1}(e_n)^2\,df + R_S^2 \int \frac{f_2}{f_1}(i_n)^2\,df + 4kTR_S\,\Delta f \quad (1)$$

where R_S is the source resistance, e_n is the input-referred noise voltage generator, and i_n is the input-referred noise current generator. Typical values for e_n and i_n are compared with the 741 in the table below.

	e_n (at 10 Hz)	i_n (at 10 Hz)
8007	200 nV/√Hz	< 0.1 pA/√Hz
741	25 nV/√Hz	0.7 pA/√Hz

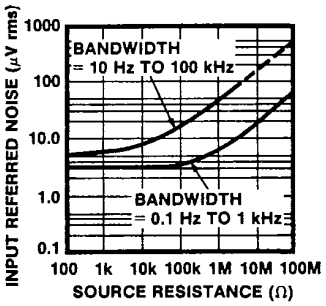

Figure 3: Wideband Noise as a Function of Source Resistance

It is clear that for high source resistances (R_S> 1MΩ) where i_n dominates, the FET input is superior to a general purpose bipolar design such as the 741. The input-referred current noise in the ICL8007 is so low that accurate measurement is difficult. For source impedances between 1MΩ and 50MΩ, the total noise shown in equation 1 is dominated by the third term, the thermal noise of the feedback and source resistors. This is of course independent of the amplifier itself.

The total input-referred noise is shown as a function of source resistance in Figure 3.

APPLICATIONS

1) Log and Antilog Amplifiers

An application which illustrates the advantages of low input current is the log circuit of Figure 4 and its antilog counterpart, Figure 5.

These circuits make use of the well known logarithmic relationship between the base-emitter voltage and the collector current in a transistor (equation 2):

$$V_{BE} = \left(\frac{mkT}{q}\right)\ell n\,\frac{I_C}{I_S} \quad (2)$$

Hence $$\Delta V_{BE} = \left(\frac{mkT}{q}\right)\ell n\,\frac{I_{C1}}{I_{C2}} \quad (3)$$

at 25°C $$\Delta V_{BE} = 60\,\log_{10}\frac{I_{C1}}{I_{C2}}\ \text{mV} \quad (4)$$

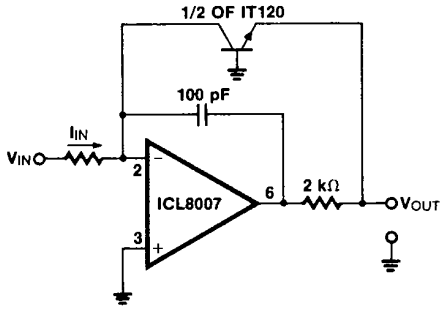

Figure 4: Basic Log Amplifier

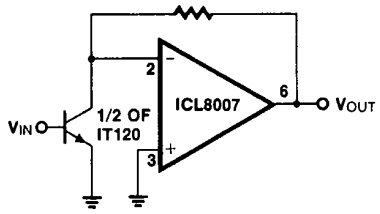

Figure 5: Basic Antilog Amplifier

It can be seen from equation 4 that each factor of ten change in collector current produces a 60mV change in V_{BE}. For a low leakage silicon transistor such as the IT120, this relationship holds true over a surprisingly wide dynamic range: 10 decades (0.1 pA to 1 mA) is quite common. Ref (3) contains an excellent discussion of the principles and limitations of this type of log amplifier.

At the low current end of the range, the accuracy of the circuit in Figure 4 is primarily dependent on the amplifier input current, making the FET input type an obvious choice. At high currents, accuracy is finally limited by base resistance and current crowding effects in the "log" transistor. Figure 6 shows the input/output characteristics of such an amplifier.

In the majority of applications where the logarithm function is used, the antilogarithm is subsequently derived. In such applications, the temperature dependence of equation 3 is usually unimportant, provided the log and antilog transistors are in good thermal contact. A monolithic transistor pair such as the IT120 will ensure the required thermal tracking. However there are occasions when direct readout of a log function is called for, and unless compensated, the temperature dependence of equation 3 becomes a serious limitation. Ref 4 contains a more detailed discussion of this problem, and outlines some temperature compensation techniques. One of these is used in the photo cell amplifier which follows.

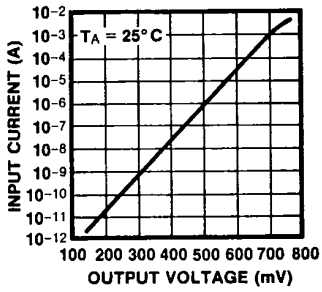

Figure 6: Transfer Characteristic of a Log Amplifier

2) Photocell Amplifier

Figure 7 shows a light meter which directly displays the log of the light intensity as an Exposure Value.* The silicon cell is operated at zero voltage to minimize leakage errors. R_1 and R_2 form a temperature sensitive gainblock, thus compensating the kT/q term in equation 3. The output reads EV −3 to EV +18 (@ ASA 100) on a 500μA meter.

3) Peak Detector

Both peak detectors and sample & hold circuits benefit from the use of an FET input amplifier since the capacitor discharge rate is a function of the amplifier input current. Two long time constant peak detectors are shown. Figure 8 shows a circuit having an input resistance of around 40MΩ and provides an output in phase with the input; figure 9 shows an inverting version of the same circuit. Although the input resistance is reduced to 10KΩ, there are no common mode errors due to the 741 since it is operating as a virtual ground amplifier. Note that in both cases the initial offset of the ICL8007 is automatically nulled out. The typical output voltage decay rate for either circuit is less than 1mV/min.

*This is a photographic term. Each unit change of EV corresponds to a factor of two change in light intensity.

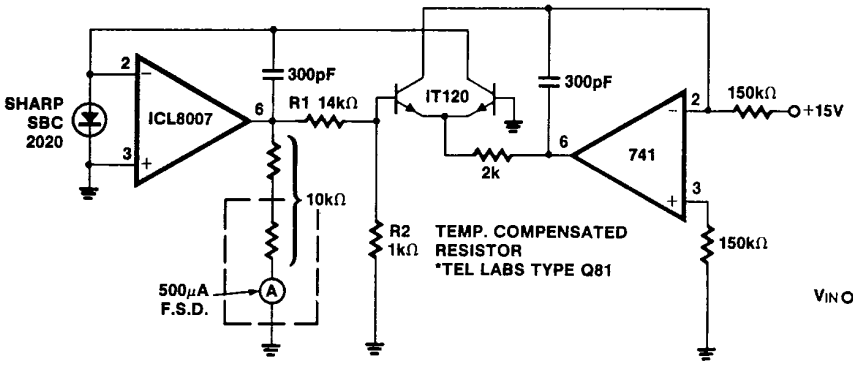

Figure 7: Sensitive Photometer

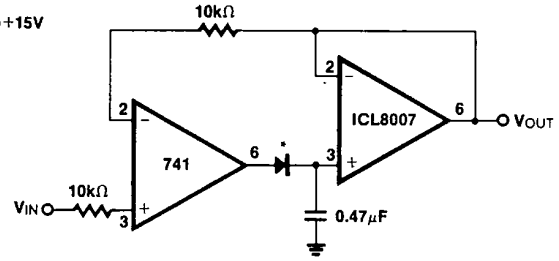

Figure 8: Non-Inverting Peak Detector

4) Sample & Hold Circuits

A straightforward sample & hold circuit using the DG139A analog switch (Ref 5) is shown in Figure 10. During the hold mode, the input amplifier is connected in unity gain to avoid output saturation.

A sample and hold with input multiplexing can also be designed using low cost Intersil analog switches. In Figure 11, one channel of the IH5009 (Ref 6) is used to control the sample and hold, while the other 3 channels control the input multiplexing. Output voltage decay rates of about 5mV/sec can be achieved with this circuit.

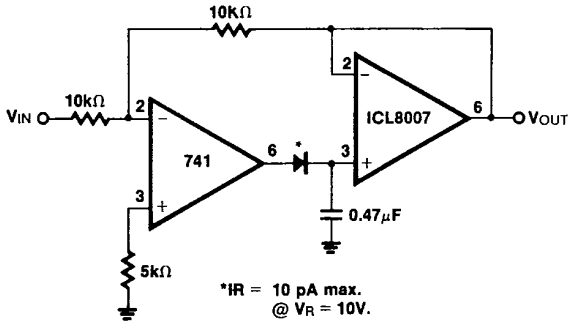

Figure 9: Inverting Peak Detector

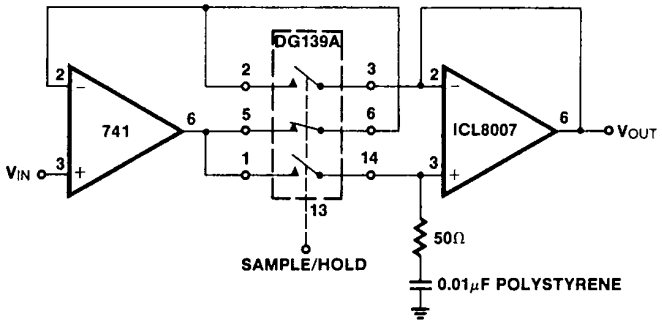

Figure 10: Sample and Hold Circuit

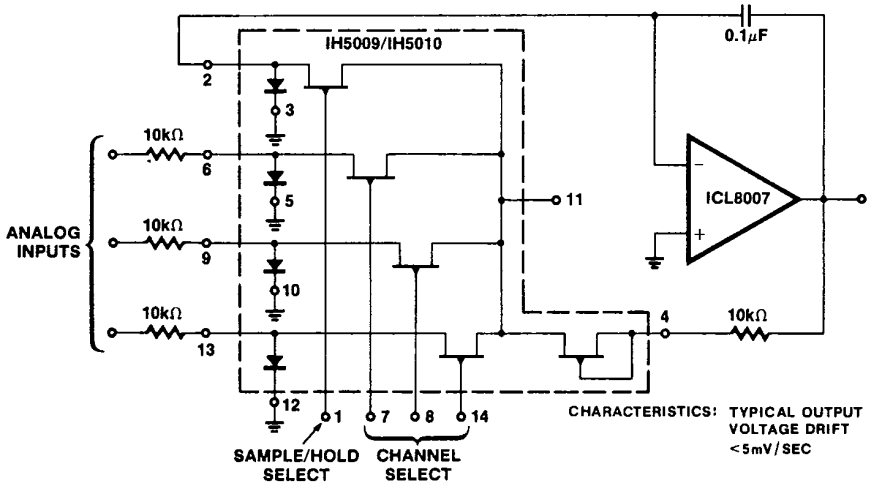

Figure 11: Sample and Hold With Input Multiplexing

A----00005-3X

5) High Impedance Buffer

Figure 12 shows a high impedance follower in which the output of the amplifier is used to drive a shielded cable. This circuit is used by Intersil to measure the performance of MOSFET's at wafer sort. Since the amplifiers are situated some distance from the probe tips, shielded cable is used. The reduction in test speed normally associated with high capacitance coax is eliminated by driving the shield in phase with the input.

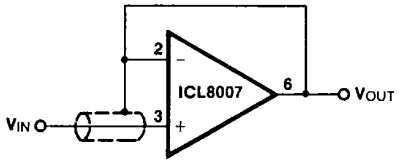

Figure 12: Buffer with Screen Drive

6) Wein Bridge Oscillator

In many oscillator and other large signal applications, the high slew rate of the ICL8007 may be used to advantage. When using general purpose amplifiers, such as the 741, to process signals with amplitudes greater than about 100mV, the slew rate determines the upper operating frequency. This frequency is substantially less than the 1MHz small signal bandwidth. It can easily be shown that for a sinusoidal waveform described by equation 5 the maximum rate of change of voltage is given by equation 6.

$$V = Vo \sin\omega t \quad (5)$$

$$\frac{dv}{dt}(max) = 2\pi fVo \quad (6)$$

If the amplifier slew rate is less than dv/dt (max), distortion will occur. An amplifier with 0.6V/μs slew rate will not handle 20V p-p signals above about 10kHz.

The ICL8007 has a typical slew rate of 6V/μs, thus extending the large signal operating frequency range by a factor of 10 compared with the 741. The undistorted output voltage swing as a function of frequency is shown in Figure 13. Figure 14 illustrates the large signal pulse response characteristics.

The Wein Bridge Oscillator of Figure 15 makes use of the high slew rate to provide a 20V peak to peak output at 40kHz. The amplitude may be controlled by R_4; for smaller output swings correspondingly higher frequencies can be obtained.

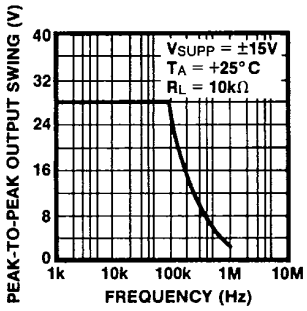

Figure 13: Output Voltage Swing as a Function of Frequency

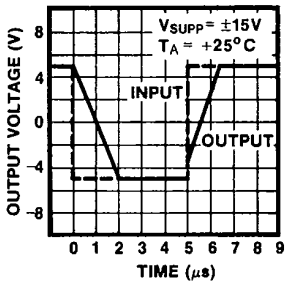

Figure 14: Voltage Follower Large-Signal Pulse Response

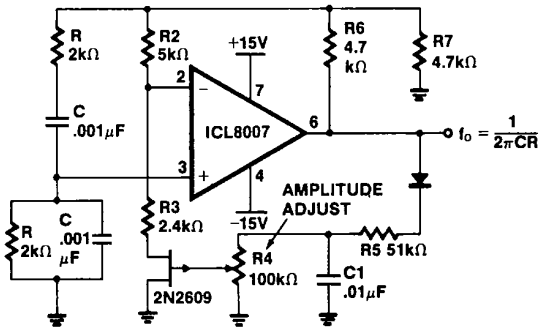

Figure 15: Wein Bridge Oscillator

REFERENCES

(1) D. Fullagar, *"A New High Performance Monolithic Operational Amplifier"*, Fairchild Semiconductor Application Brief, May, 1968.

(2) W. L. Paterson, *"Multiplication and Logarithmic Conversion by Operational Amplifier-Transistor Circuits"*, The Review of Scientific Instruments, Volume 34, Number 12, December, 1963.

(3) R. Dobkin, *"Logarithmic Converters"*, National Semiconductor Application Note AN-30, November, 1969.

(4) Intersil Application Note A003, *"Understanding and Applying the Analog Switch"*.

(5) Intersil Application Note A004. *"The IH5009 Series of Low Cost Analog Switches"*.

INTERSIL 10710 N. Tantau Ave., Cupertino, CA 95014 (408) 996-5000 TWX: 910-338-0171