

Recording/Playback Equalizer Amplifier

Description

The CXA1898Q is an IC developed for analog signal processing in tape recorders. Processing for both the recording and playback systems is achieved on one chip.

Features

- Recording equalizer Gp and Fp can be adjusted externally.
- Recording mute function
- AGC (Automatic Gain Control)
- Comparator for AMS (Automatic Music Sensor)
- Recording/playback equalizer amplifier with 1.7 times speed switching
- 11-bit serial data interface

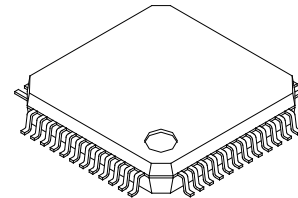
Absolute Maximum Ratings

- | | | | |
|-------------------------------|------------------|-------------|----|
| • Supply voltage | V _{CC} | 12 | V |
| • Operating temperature | T _{opr} | -20 to +75 | °C |
| • Storage temperature | T _{stg} | -65 to +150 | °C |
| • Allowable power dissipation | P _D | 735 | mW |

Operating Conditions

- | | | | |
|----------------|-----------------|-------------|---|
| Supply voltage | V _{CC} | 6.5 to 10.0 | V |
|----------------|-----------------|-------------|---|

48 pin QFP (Plastic)



Structure

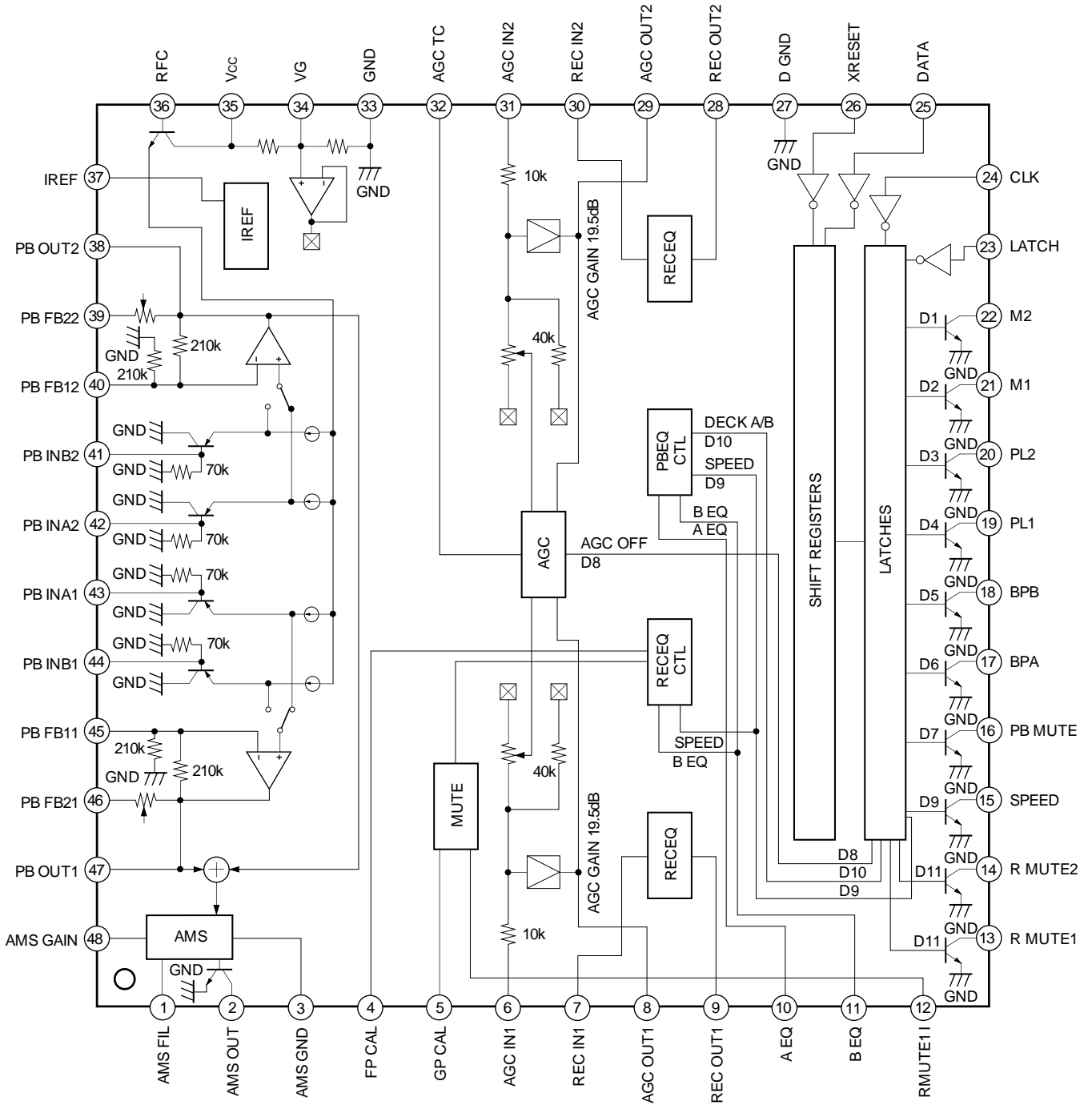
Bipolar silicon monolithic IC

Applications

All analog signal processing in the cassette decks of tape recorders and compact music centers
(Applicable to Sankyo Seiki mfg. Co., Ltd.
YK47R-KF202 R/P head or equivalent)

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Block Diagram and Pin Configuration (Top View)



Pin Description

Pin No.	Symbol	DC voltage	I/O	I/O resistance	Equivalent circuit	Description
6 31	AGC IN1 AGC IN2	4.0V	I	50kΩ		AGC signal input. Input resistance changes between 47kΩ and 3kΩ
7 30	REC IN1 REC IN2	4.0V	I	50kΩ		Recording equalizer input.
8 29	AGC OUT1 AGC OUT2	4.0V	O	147Ω		AGC output pin. AGC is applied at -11dBm or more.
9 28	REC OUT1 REC OUT2	4.0V	O	147Ω		Recording equalizer output.

Pin No.	Symbol	DC voltage	I/O	I/O resistance	Equivalent circuit	Description
10	A EQ	—	I	—		A deck equalizer switch. Low: 120μs EQ High: 70μs EQ
11	B EQ	2.5V (when open)	I	53kΩ		B deck equalizer switch. Low: Normal Tape, 120μs EQ High: CrO ₂ Tape, 70μs EQ Medium: Metal Tape, 70μs EQ
12	RMUTE1 I	—	I	—		Recording mute ON/OFF switch. Low: Mute OFF High: Mute ON * Fader function is realized by the external time constant circuit. Connects Pin 13 (RMUTE1).
13 14	R MUTE1 R MUTE2	5.0V (when reset) (when Pin 25 (DATA) is set to high)	O	—		Output for recording mute ON/OFF switch control signal. Outputs D11 from Pin 25 (DATA).
15	SPEED					Output for recording/playback equalizer speed switch control signal. Outputs D9 from Pin 25 (DATA). Low: Normal Speed High: High Speed (1.7 times)
16	PB MUTE					Output pin for playback mute ON/OFF switch control signal. Outputs D7 from Pin 25 (DATA). Connects a resistor to VDD for Pins 13 to 16.

Pin No.	Symbol	DC voltage	I/O	I/O resistance	Equivalent circuit	Description
17	BPA	5.0V (when reset) (when Pin 25 (DATA) is set to high)	O	—		Outputs D6 from Pin 25 (DATA).
18	BPB					Outputs D5 from Pin 25 (DATA).
19	PL1					Outputs D4 from Pin 25 (DATA).
20	PL2					Outputs D3 from Pin 25 (DATA).
21	M1					Outputs D2 from Pin 25 (DATA).
22	M2					Outputs D1 from Pin 25 (DATA).
23	LATCH	—	I	—		Serial data interface latch input.
26	XRESET					Serial data interface reset input. Low: Reset. At this time serial data outputs (Pins 13 to 22) are all open (high).
24	CLK					Serial data interface clock input.
25	DATA	—	I	—		Serial data interface serial data input.
32	AGC TC	0.0V	—	—		Connects a resistor and capacitor for determining AGC attack/recovery time constants.

Pin No.	Symbol	DC voltage	I/O	I/O resistance	Equivalent circuit	Description
34	VG	4.0V	—	60kΩ		Signal reference voltage. Connects a capacitor for ripple rejection.
35	Vcc	8.0V	—	—		Power supply.
36	RFC	8.0V	—	—		Connects a resistor and capacitor for obtaining stable voltage with power supply ripple rejected.
38 47	PB OUT2 PB OUT1	2.8V	O	147Ω		Playback equalizer output.

Pin No.	Symbol	DC voltage	I/O	I/O resistance	Equivalent circuit	Description
39 46	PB FB22 PB FB21	2.8V	—	—		Connects a capacitor for determining playback equalizer time constants, such as 120μs and 70μs.
40 45	PB FB12 PB FB11	1.4V	—	105kΩ		Playback equalizer negative feedback.
41 42 43 44	PB INB2 PB INA2 PB INA1 PB INB1	0.0V	I	70kΩ		Playback equalizer input.
48	AMS GAIN	3.5V	—	—		Connects a resistor for determining AMS signal detection level and a capacitor for determining HPF cut-off frequency.

Note)

The resistance of open collector outputs (Pins 2 and 13 to 22) can be also connected to Vcc.

Electrical Characteristics

(Ta = 25°C, Vcc = 8.0V, VDD = 5.0V, refer to Electrical Characteristics Measurement Circuit)

Item	Measurement conditions	Min.	Typ.	Max.	Unit	
Operating voltage	Vcc	6.5	8.0	10.0	V	
Current consumption	NORM-NS, Vcc = 8V, No signal	13.5	18.0	22.5	mA	
AGC	AGC ON output level	Pin 32 external R300kΩ/ /C47μF f = 1kHz, Vin = -25dBm	-13.0	-11.0	-9.0	dBm
	AGC ON channel balance	Pin 32 external R300kΩ/ /C47μF f = 1kHz, Vin = -15dBm	-2.0	0.0	2.0	dB
	AGC ON distortion	Pin 32 external R300kΩ/ /C47μF f = 1kHz, Vin = 0dBm	—	0.3	1.5	%
	AGC OFF output level	Pin 32 external R300kΩ/ /C 47μF f = 1kHz, Vin = -25dBm	-7.5	-5.5	-3.5	dBm
AMS	No signal detection threshold level	Pin 48 external R9.1kΩ, C0.015μF Pin 1 external R100kΩ/ /C0.1μF f = 5kHz, 0dB = -21dBm (at PBEQ reference output level)	-11.5	-8.2	—	dB
Playback equalizer amplifier block	120μs-NS frequency response	f = 315Hz, Vin = -70dBm Reference for frequency response	-23.0	-21.0	-19.0	dBm
	120μs-NS frequency response	f = 2.7kHz, Vin = -58.5dBm at 120μs-NS, 315Hz	-0.1	1.3	2.9	dB
	70μs-NS frequency response	f = 4.5kHz, Vin = -53.8dBm at 120μs-NS, 315Hz	-0.1	1.7	2.9	
	120μs-HS frequency response	f = 5.3kHz, Vin = -52.5dBm at 120μs-NS, 315Hz	1.8	3.0	4.8	
	70μs-HS frequency response	f = 9.1kHz, Vin = -47.8dBm at 120μs-NS, 315Hz	2.1	3.6	5.1	
	Signal handling	120μs-NS, RL = 2.7kΩ f = 1kHz, THD + N = 1%	-10.0	-6.0	—	
	Total harmonic distortion	120μs-NS, RL = 2.7kΩ f = 1kHz, Vin = -56.4dBm	—	0.3	0.7	%
	S/N ratio	120μs-NS, Rg = 2.2kΩ "A" weighting filter	55.0	62.0	—	dB
	Output offset voltage	120μs-NS, Rg = 70kΩ	2.4	2.7	3.2	V

Item	Measurement conditions	Min.	Typ.	Max.	Unit
Reference input level	NORM-NS, 315Hz, input level at which reference output can be obtained	-29.4	-27.9	-26.4	dBm
	Reference output level	NORM-NS, 315Hz	—	-10.0	
Channel balance	NORM-NS, 315Hz, Output difference 1ch-2ch for -27.9dBm input	-1.5	0.0	1.5	dB
NORM-NS frequency response	f = 3kHz at NORM-NS, 315Hz, reference output -20dB	-1.3	-0.2	1.1	
NORM-NS frequency response	f = 8kHz at NORM-NS, 315Hz, reference output -20dB	3.7	5.7	7.3	
NORM-NS frequency response	f = 12kHz at NORM-NS, 315Hz, reference output -20dB	10.4	13.4	16.4	
CrO ₂ -NS frequency response	f = 3kHz at NORM-NS, 315Hz, reference output -20dB	1.8	3.0	4.2	
CrO ₂ -NS frequency response	f = 8kHz at NORM-NS, 315Hz, reference output -20dB	6.7	8.4	9.7	
CrO ₂ -NS frequency response	f = 12kHz at NORM-NS, 315Hz, reference output -20dB	13.2	15.8	18.2	
METAL-NS frequency response	f = 3kHz at NORM-NS, 315Hz, reference output -20dB	3.3	4.5	5.7	
METAL-NS frequency response	f = 8kHz at NORM-NS, 315Hz, reference output -20dB	5.9	7.4	8.9	
METAL-NS frequency response	f = 12kHz at NORM-NS, 315Hz, reference output -20dB	11.3	13.7	15.8	
NORM-HS frequency response	f = 5kHz at NORM-NS, 315Hz, reference output -20dB	-0.7	0.2	1.7	
NORM-HS frequency response	f = 15kHz at NORM-NS, 315Hz, reference output -20dB	8.3	10.5	12.3	
NORM-HS frequency response	f = 20kHz at NORM-NS, 315Hz, reference output -20dB	13.5	16.7	19.5	
CrO ₂ -HS frequency response	f = 5kHz at NORM-NS, 315Hz, reference output -20dB	3.6	4.9	6.0	
CrO ₂ -HS frequency response	f = 15kHz at NORM-NS, 315Hz, reference output -20dB	12.0	14.2	16.0	
CrO ₂ -HS frequency response	f = 20kHz at NORM-NS, 315Hz, reference output -20dB	17.0	20.0	22.5	
METAL-HS frequency response	f = 5kHz at NORM-NS, 315Hz, reference output -20dB	4.9	6.1	7.3	
METAL-HS frequency response	f = 15kHz at NORM-NS, 315Hz, reference output -20dB	10.5	12.4	14.0	
METAL-HS frequency response	f = 20kHz at NORM-NS, 315Hz, reference output -20dB	14.7	17.4	19.7	

Recording equalizer amplifier block

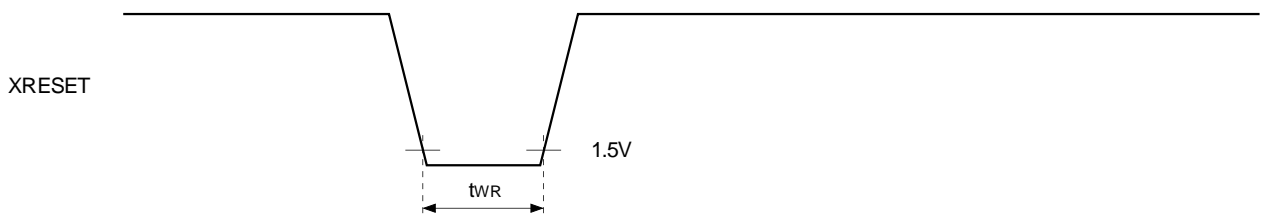
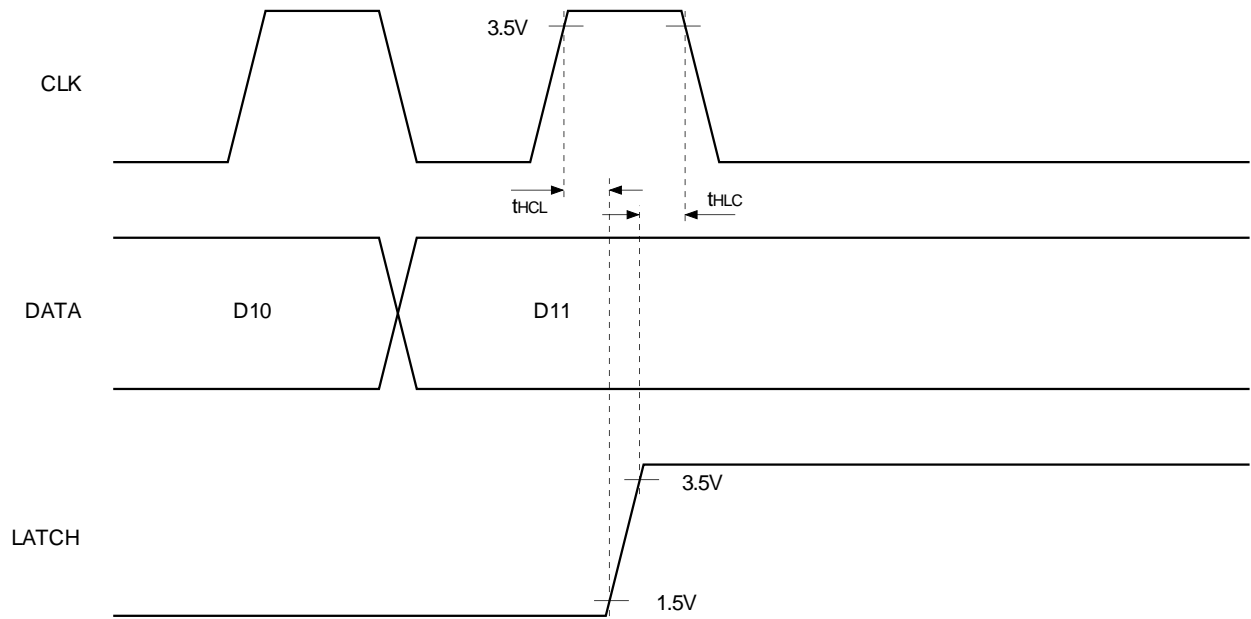
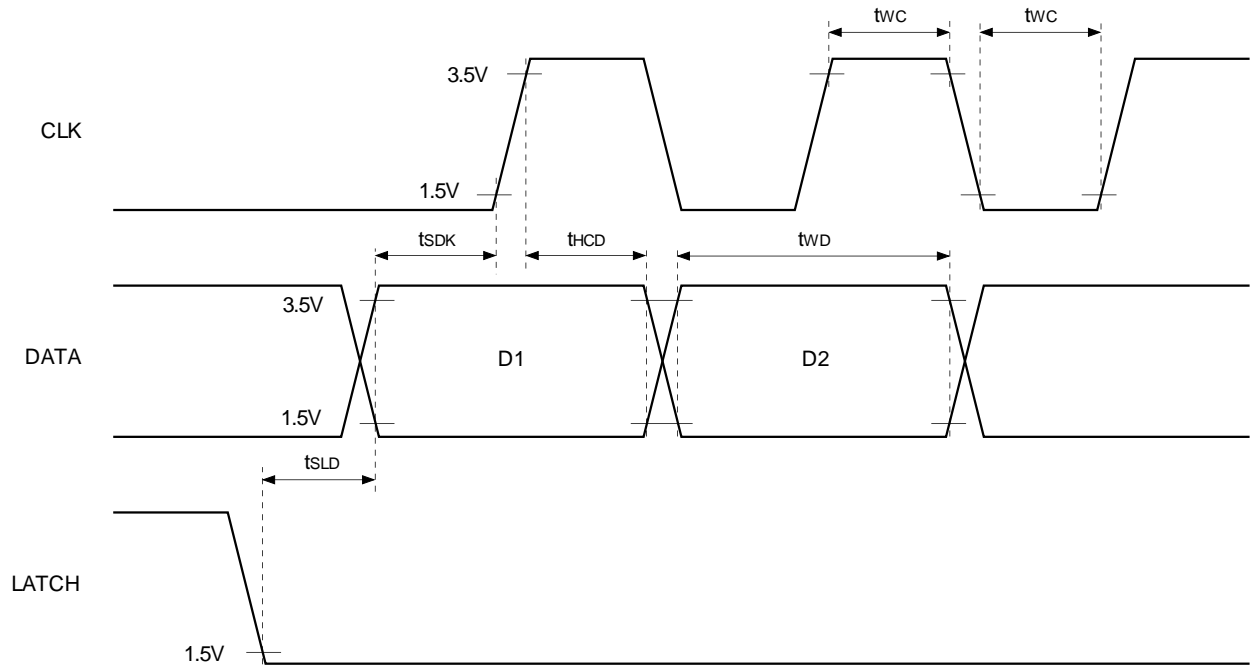
Item		Measurement conditions	Min.	Typ.	Max.	Unit
Recording equalizer amplifier block	Signal handling	NORM-NS, R _L 2.7kΩ f = 1kHz, THD = 1%	8.0	8.8	—	dB
	Total harmonic distortion	NORM-NS, R _L 2.7kΩ f = 1kHz, 0dB	—	0.2	0.5	%
	S/N ratio	NORM-NS, R _g = 5.1kΩ "A" weighting filter	57.0	60.6	—	dB
	Output offset voltage	NORM-NS	3.6	4.0	4.4	V
	Mute characteristics 1	NORM-NS, f = 1kHz 8dB, Pin 12 = 3.5V	—	-100	-80	dB
	Mute characteristics 2	NORM-NS, f = 1kHz 8dB, Pin 12 = 2.0V	-8.3	-7.0	-4.3	
Control voltage low level 1	A-EQ (Pin 10)	0.0	—	0.5	V	
Control voltage high level 1	A-EQ (Pin 10)	2.5	—	V _{cc}		
Control voltage low level 2	B-EQ (Pin 11)	0.0	—	0.5		
Control voltage medium level 1	B-EQ (Pin 11)	2.2	—	2.8		
Control voltage high level 2	B-EQ (Pin 11)	4.2	—	V _{cc}		
Control voltage low level 3	RMUTE1-I (Pin 12)	0.0	—	0.5		
Control voltage high level 3	RMUTE1-I (Pin 12)	3.5	—	V _{cc}		

Note) NORM-NS : NORMAL TAPE-NORMAL SPEED
 NORM-HS : NORMAL TAPE-HIGH SPEED
 CrO₂-NS : CrO₂ TAPE-NORMAL SPEED
 CrO₂-HS : CrO₂ TAPE-HIGH SPEED
 METAL-NS : METAL TAPE-NORMAL SPEED
 METAL-HS : METAL TAPE-HIGH SPEED
 120μs-NS : EQ = 120μs-NORMAL SPEED
 120μs-HS : EQ = 120μs-HIGH SPEED
 70μs-NS : EQ = 70μs-NORMAL SPEED
 70μs-HS : EQ = 70μs-HIGH SPEED

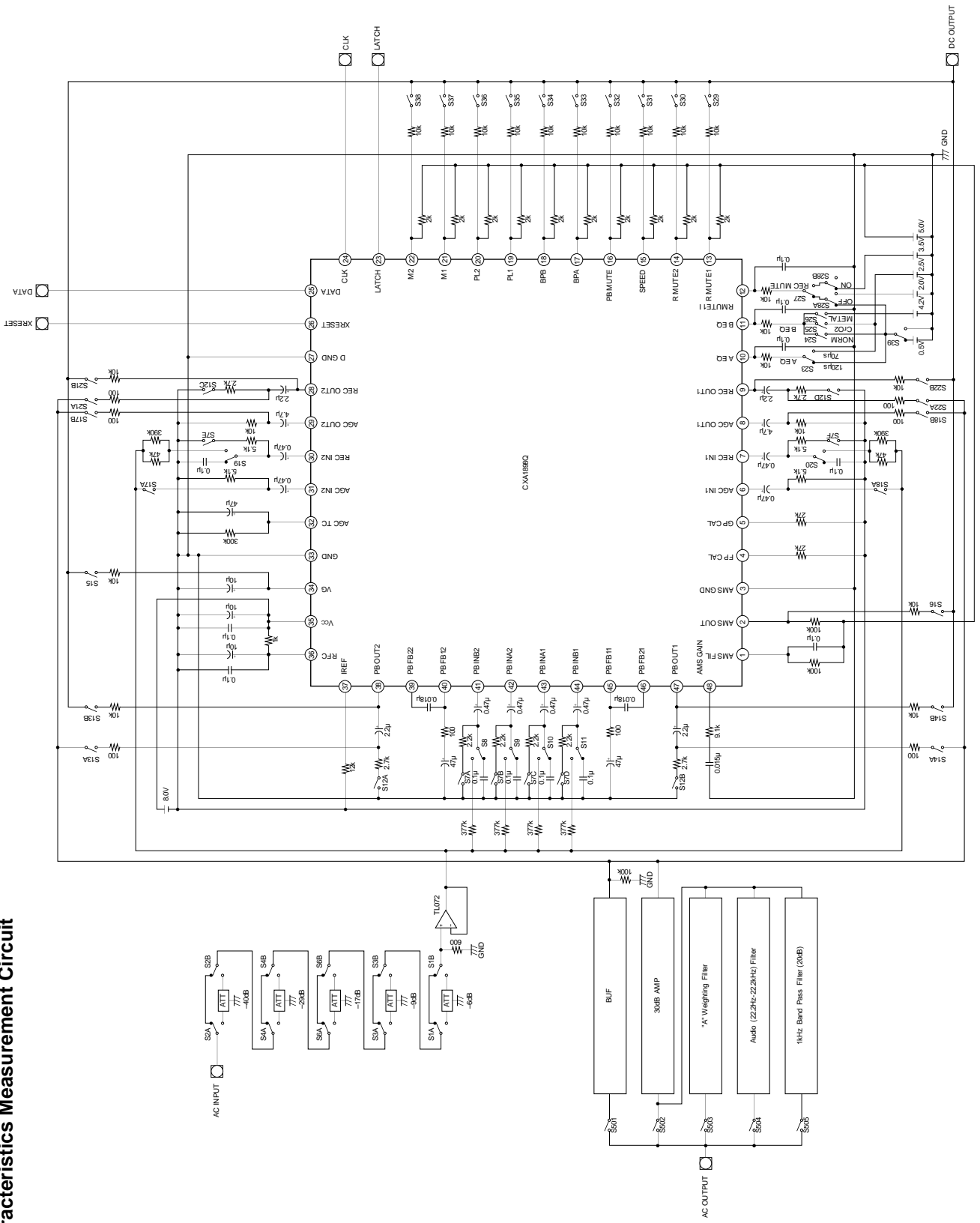
Item		Measurement conditions	Min.	Typ.	Max.	Unit
11-bit serial data interface block	Low level input voltage	V_{IL} (LATCH/CLK/DATA/XRESET) (Pins 23, 24, 25, 26)	0.0	—	1.5	V
	High level input voltage	V_{IH} (LATCH/CLK/DATA/XRESET) (Pins 23, 24, 25, 26)	3.5	—	V_{DD}	
	Low level output voltage	V_{OL} , $I_{OL} = 2\text{mA}$ (max) (Pins 13, 14, 15, 16, 17, 18, 19, 20, 21, 22)	0.0	—	0.5	
	High level output off-leak current	I_{OZ} Leak current which flows to the output pin when I_{OZ} output is open; applied voltage is 10V.	—	—	1.0	μA
	Maximum clock frequency	(1) f_{CK}	500	—	—	kHz
	Minimum clock pulse width	(2) t_{WC}	—	—	1.0	μs
	Minimum reset pulse width	(3) t_{WR}	—	—	1.0	
	Minimum data setup time	(4) t_{SDK} (DATA → CLK)	—	—	1.0	
	Minimum data hold time	(5) t_{HCD} (CLK → DATA)	—	—	1.0	
	Minimum data pulse width	(6) t_{WD}	—	—	2.0	
	Minimum latch setup time	(7) t_{SLD} (LATCH → DATA)	—	—	1.0	
	Minimum latch hold time	(8) t_{HCL} (CLK → LATCH)	—	—	1.0	
Minimum clock hold time	(9) t_{HLC} (LATCH → CLK)	—	—	1.0		

- Note)**
- V_{DD} is CPU supply voltage 5.0V.
 - The maximum value for V_{DD} is Pin 35 (V_{CC}) voltage.
 - For high level output off leak current, V_{CC} is 10.0V.

Timing Chart for 11-bit Serial Data Interface



Electrical Characteristics Measurement Circuit



1. System control mode

Playback and recording equalizer

(1) Playback equalizer (120 μ s/70 μ s)

		A-EQ (Pin 10)		B-EQ (Pin 11)	
		L	H	L	M/H
DECK-AB (serial data D10 (Pin 25))	L	120 μ s (A DECK)	70 μ s (A DECK)	According to A EQ control	
	H	According to B EQ control		120 μ s (B DECK)	70 μ s (B DECK)

(2) Recording equalizer (Normal, CrO₂, Metal)

B-EQ (Pin 11)	L	M	H
REC MODE	Normal (Type I)	CrO ₂ (Type II)	Metal (Type IV)

(3) Recording mute (Pin 12)

Rec Mute	Mute OFF	-7dB attenuation	Mute ON
Control voltage	$GND \leq V_{CL} \leq 0.5V$	2.0V	$3.5V \leq V_{CH} \leq V_{CC}$

Muting is achieved by varying the recording equalizer amplifier gain just like an electronic volume, according to the DC voltage applied to the REC MUTE pin.

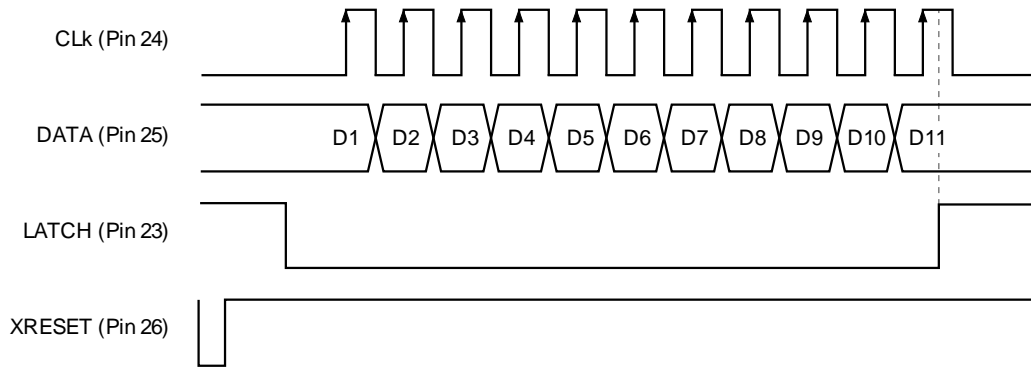
(4) FP CAL (Pin 4)

The standard resistor setting is 27k Ω , but when resistance value is larger, fo (Hz) is low, and when resistance value is smaller, fo (Hz) is high.

(5) Gp Cal (Pin 5)

The standard resistor setting is 27k Ω , but when resistance value is larger, gain is larger, and when resistance value is smaller, gain is smaller.

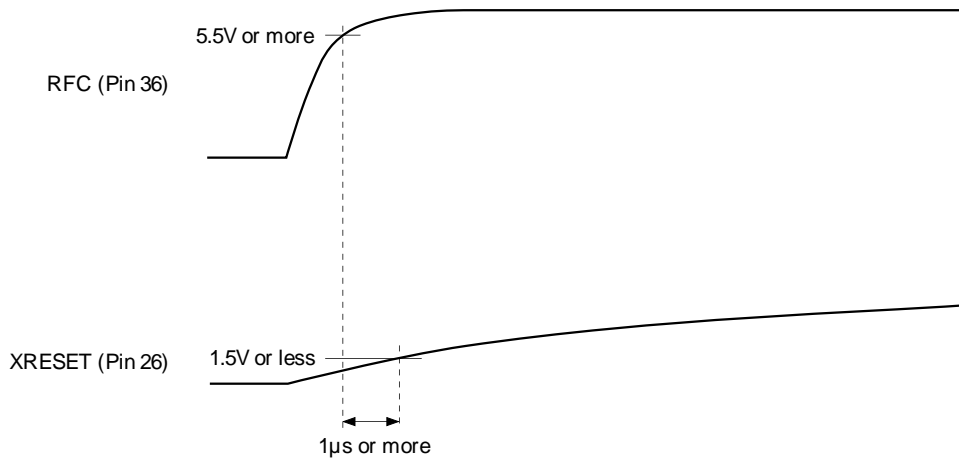
2. 11-bit serial data interface



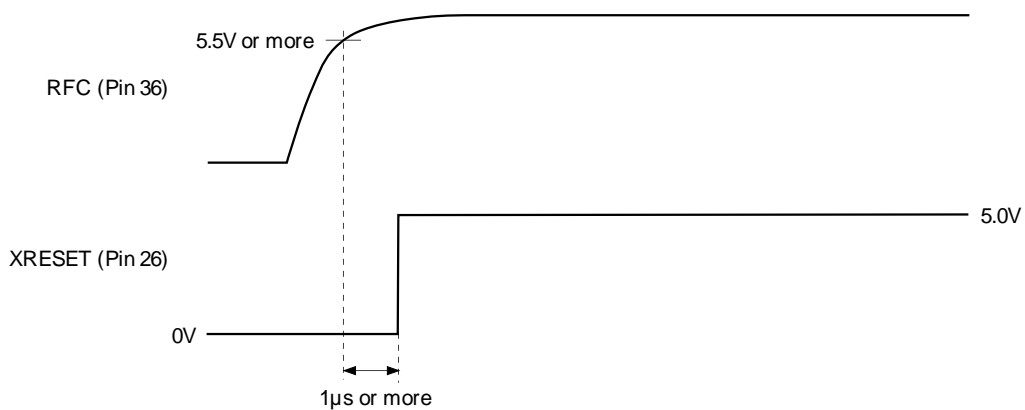
- The DATA signal is taken in at the rising edge of the CLK signal.
- The DATA signal is taken in to the internal shift register when the LATCH signal is low.
(Outputs (Pins 13 to 22) hold the previous value while the LATCH signal is low.)
- The internal shift register data is latched and output in parallel at the rising edge of the LATCH signal.
(Internal shift register data is loaded while the LATCH signal is high.)
- The CLK signal of 11th bit should fall after the LATCH signal rises.
- Reset is done when the XRESET pin is low. (asynchronous method)
Outputs (Pins 13 to 22) are all high (open) during reset.

DATA (Pin 25)	Control signal	Output		
		Output pin	Input set at low	Input set at high
D1	M2	Pin 22	L	H (OPEN)
D2	M1	Pin 21	L	H (OPEN)
D3	PL2	Pin 20	L	H (OPEN)
D4	PL1	Pin 19	L	H (OPEN)
D5	BPB	Pin 18	L	H (OPEN)
D6	BPA	Pin 17	L	H (OPEN)
D7	PB-MUTE	Pin 16	L	H (OPEN)
D8	AGC-OFF	—	AGC function stops	AGC function operates
D9	SPEED	Pin 15	Low, normal speed	High (open) 1.7
D10	DECK-AB	—	A DECK selected	B DECK selected
D11	REC-MUTE	Pin 14/Pin 13	Low mute OFF	High (open) mute ON

- Make sure that RFC is 5.5V or more and XRESET is 1.5V or less, and 1 μ s or more when resetting by applying CR time constant to XRESET (Pin 26) and turning power ON.

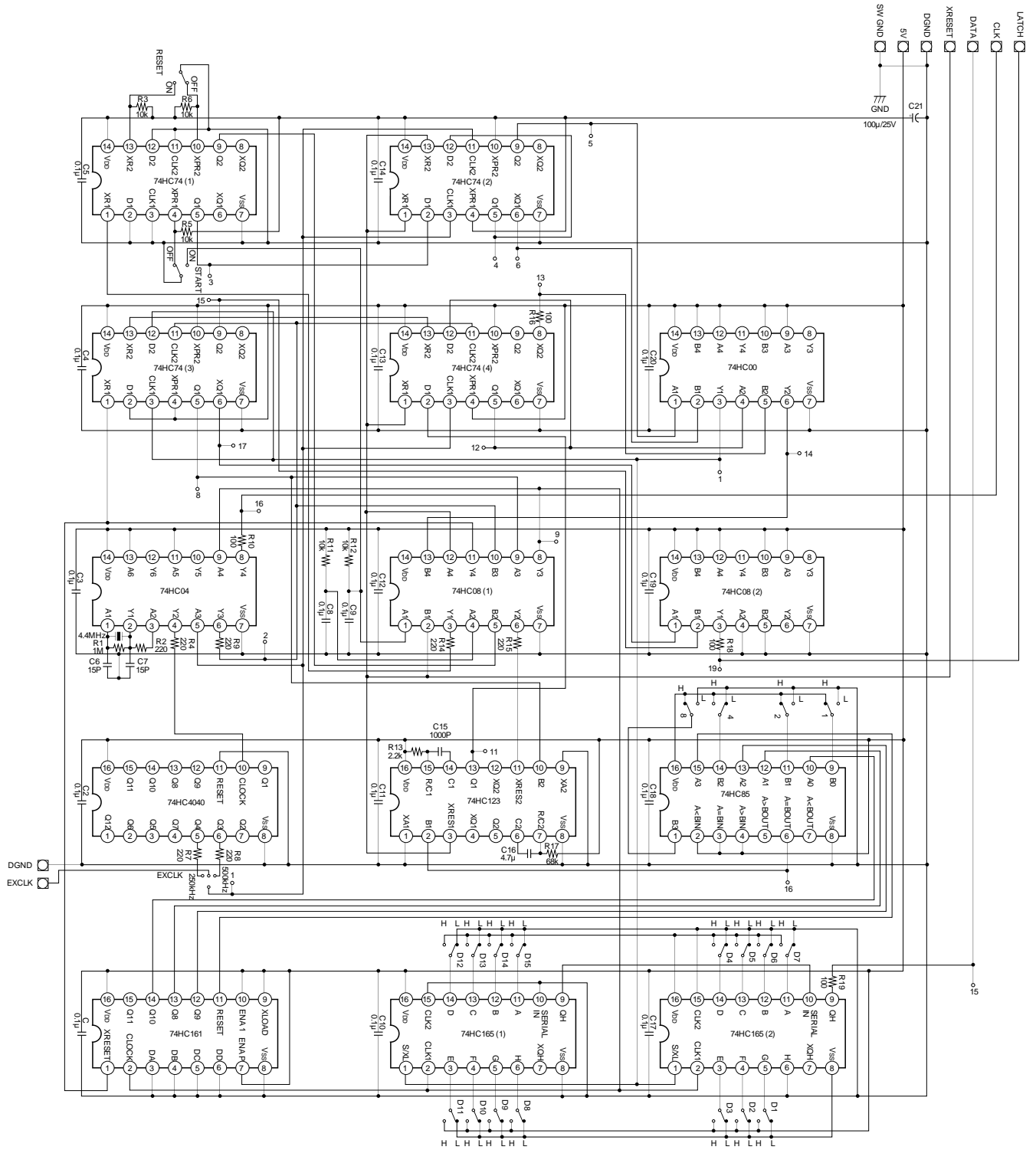


- When resetting with CPU or other when power is turned ON

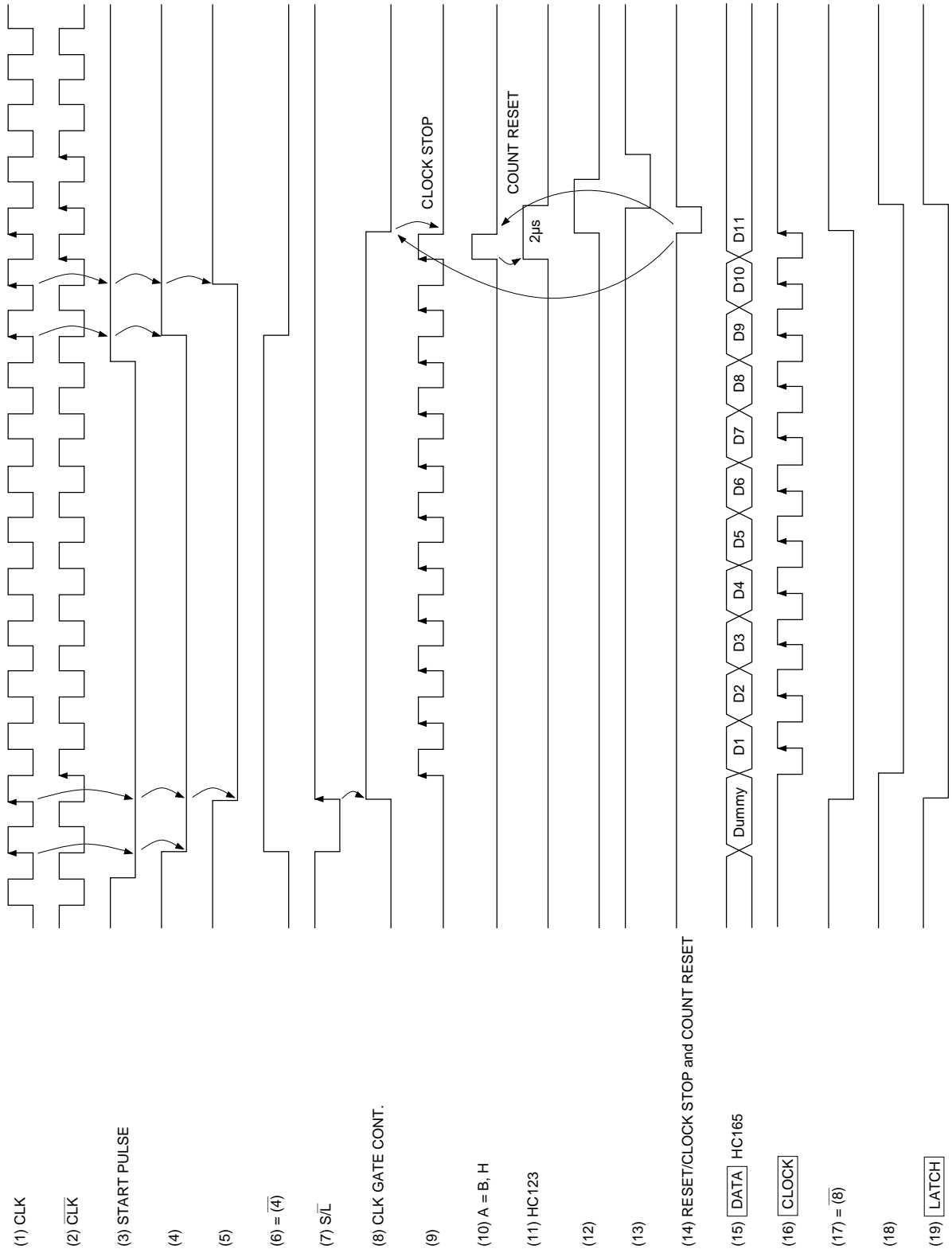


- Examples of AGC control during timer recording
 - (1) Resets when power is turned ON (AGC function operates).
 - (2) AGC is turned OFF after AGC inputs (Pins 6 and 31) rise.
(External capacitor charge of AGC TC is discharged.)
 - (3) AGC is turned ON and timer recording begins.

Circuit Diagram for 11-bit Serial Data Transfer Evaluation Tool



Timing Chart for 11-bit Serial Data Transfer Evaluation Tool



3. AMS

(1) AMS output logic

Detection status	Signal detection	No signal detection
AMS OUT (Pin 2)	L	H

AMS OUT (Pin 2) is an open collector output pin. When a 2.2kΩ resistor is connected to V_{DD}:

Low : approximately 0.5V (I_{OL} = 2mA (max.))

High : V_{DD}

Fig. 1 shows the AMS block diagram.

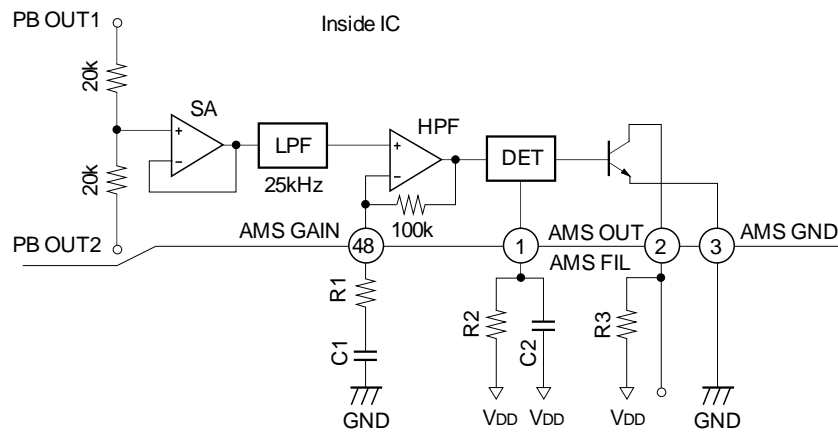


Fig. 1 AMS Block Diagram

Fig. 2 shows the frequency response of the signal output from HPF.

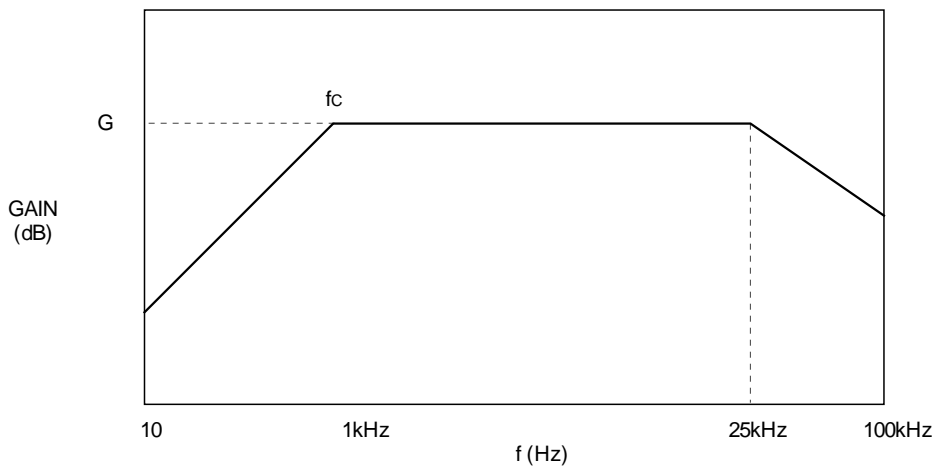


Fig. 2 Frequency Response

(2) AMS level setting

The AMS level is set by adjusting HPF gain and cut-off frequency with the external resistor and capacitor at Pin 48.

G and f_c in Fig. 2 are obtained from the following formula.

$$G = 20\log(1 + 100k/R) \quad [\text{dB}] - (1)$$

$$f_c = 1 / (2 \cdot \pi \cdot C \cdot R) \quad [\text{Hz}]$$

Full-wave rectifier is applied for the signal at DET.

Signal detection time is set by the time constant of Pin 1 external resistor and capacitor.

DET signal detection level:

$$= -7.5\text{dBm (typ.)}$$

$$= \text{playback equalizer reference output level} + \text{AMS level} + \text{HPF gain} - (2)$$

Playback equalizer reference output level of -21dBm is 0dB .

Ex.)

To set AMS level at -25dB , determine and set the constant for Pin 48 external resistor.

(Calculate assuming $\text{PBOUT1} = \text{PBOUT2}$)

First, get the required HPF gain from formula (2).

$$-7.5\text{dBm} = -21\text{dBm} + (-25\text{dB}) + \text{HPF gain},$$

so HPF gain = 38.5dB .

Next, get Pin 48 external resistance from formula (1).

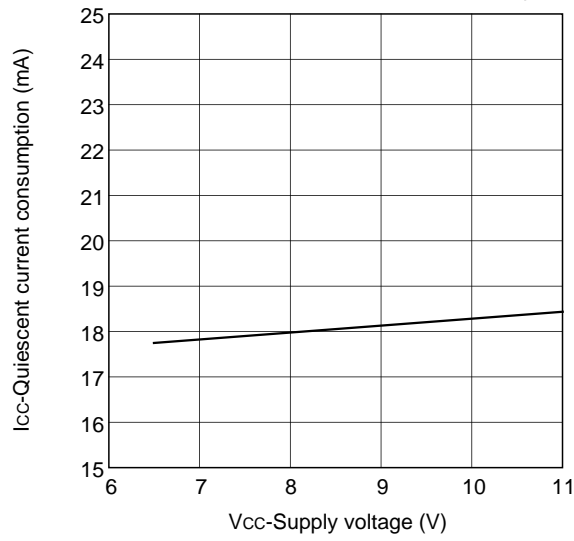
$$38.5\text{dB} = 20\log(1 + 100k/R),$$

so $R \approx 1.2\text{k}\Omega$,

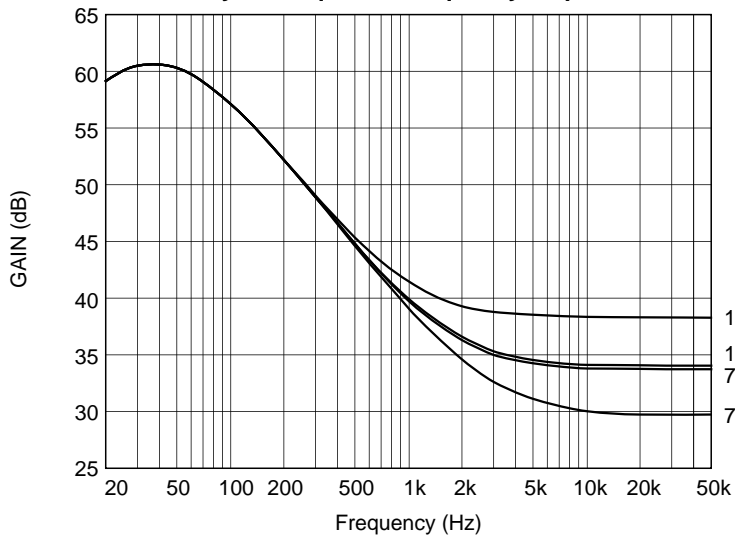
and external resistance is $1.2\text{k}\Omega$.

Example of Representative Characteristics

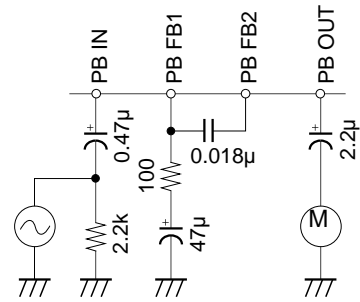
Quiescent current consumption vs. Supply voltage

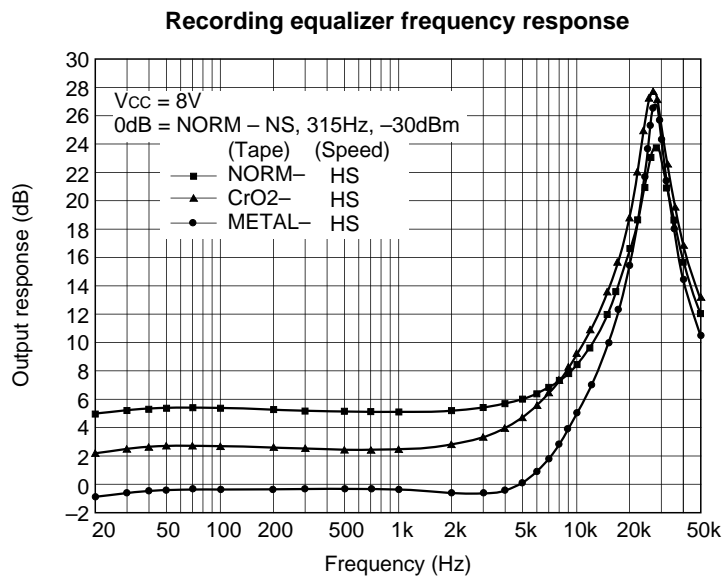
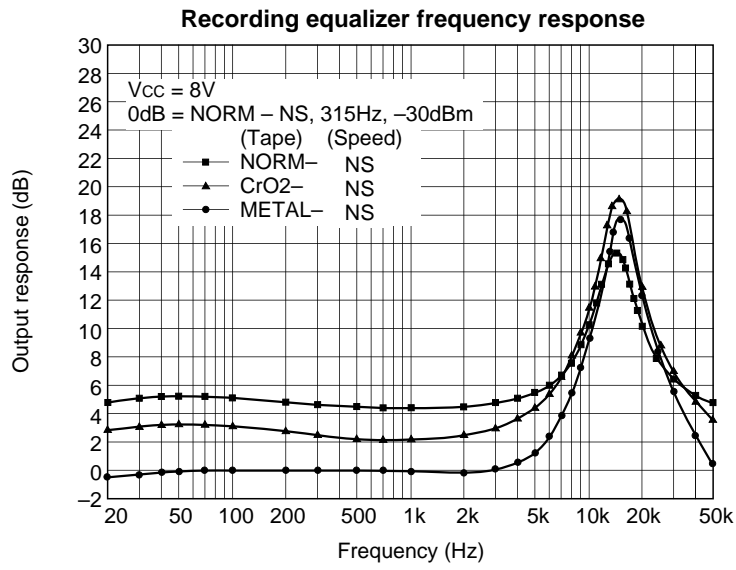


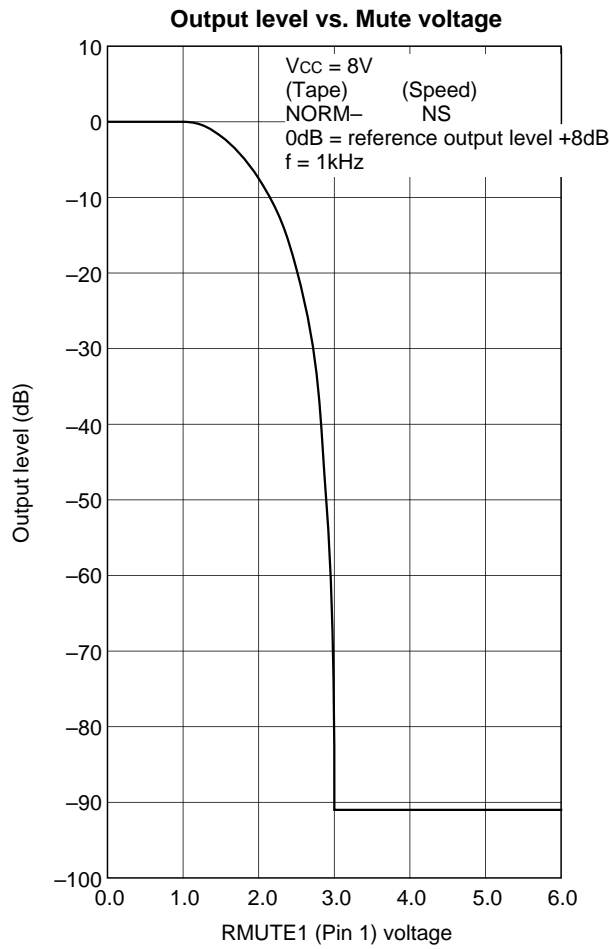
Playback equalizer frequency response



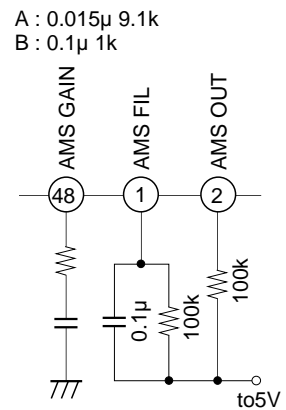
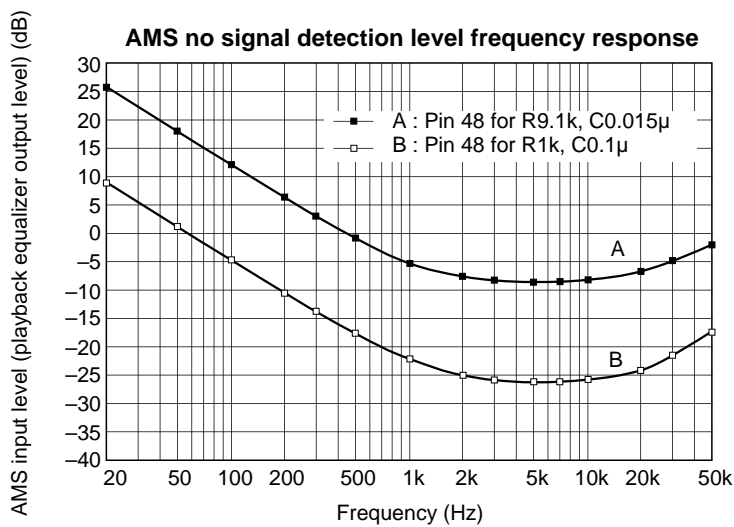
Vcc = 8V



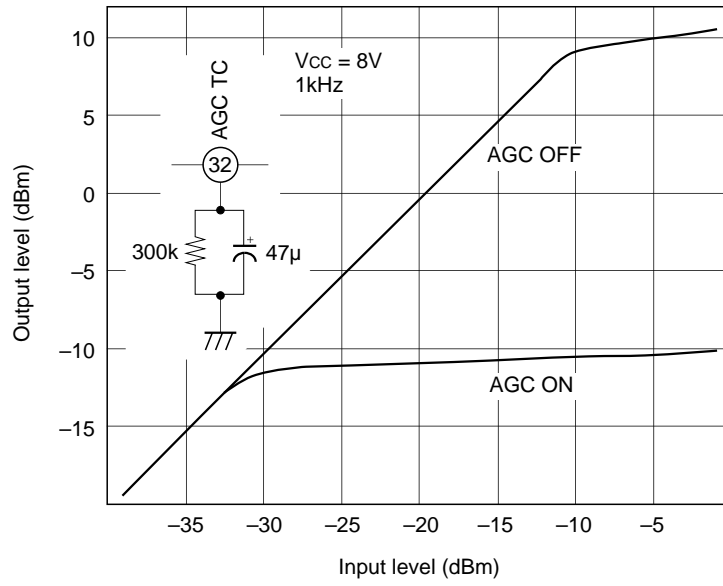




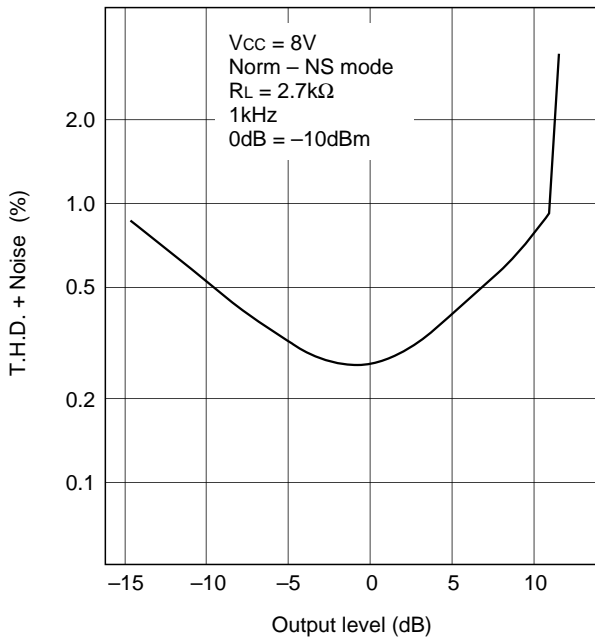
$V_{CC} = 8V$
 $120\mu s - NS$
 AMS OUT 5V
 0dB = -21dBm, 315Hz (playback equalizer reference output level)



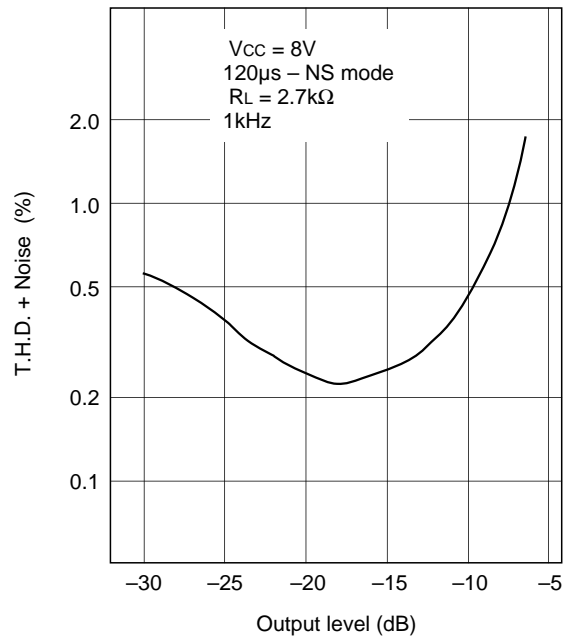
AGC Output response



Recording equalizer total harmonic distortion

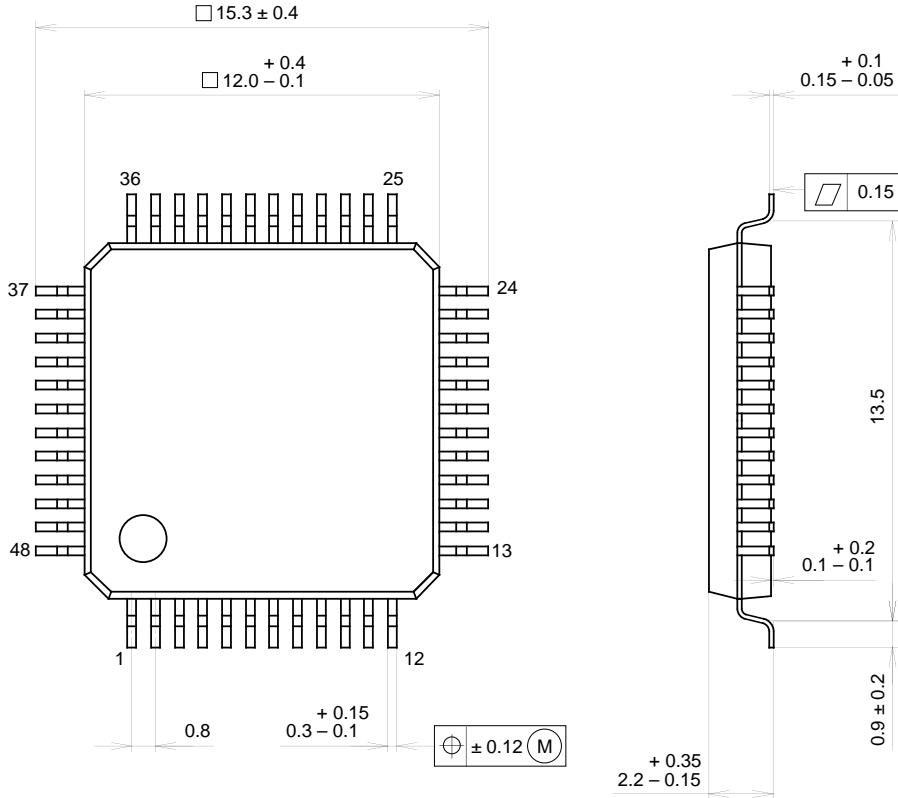


Playback equalizer total harmonic distortion



Package Outline Unit: mm

48PIN QFP (PLASTIC)



PACKAGE STRUCTURE

SONY CODE	QFP-48P-L04
EIAJ CODE	*QFP048-P-1212-B
JEDEC CODE	_____

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER / PALLADIUM PLATING
LEAD MATERIAL	COPPER / 42 ALLOY
PACKAGE WEIGHT	0.7g

NOTE : PALLADIUM PLATING
 This product uses S-PdPPF (Sony Spec.-Palladium Pre-Plated Lead Frame).