DATA SHEET

BF1201; BF1201R; BF1201WR
N-channel dual-gate PoLo MOS-FETs

Product specification
Supersedes data of 1999 Dec 01

2000 Mar 29

Philips Semiconductors

PHILIPS

N-channel dual-gate PoLo MOS-FETs

BF1201; BF1201R; BF1201WR

FEATURES

- Short channel transistor with high forward transfer admittance to input capacitance ratio
- Low noise gain controlled amplifier
- Partly internal self-biasing circuit to ensure good cross-modulation performance during AGC and good DC stabilization.

APPLICATIONS

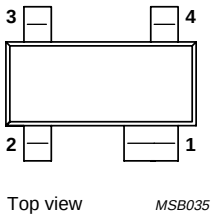
- VHF and UHF applications with 3 to 9 V supply voltage, such as digital and analogue television tuners and professional communications equipment.

DESCRIPTION

Enhancement type N-channel field-effect transistor with source and substrate interconnected. Integrated diodes between gates and source protect against excessive input voltage surges. The BF1201, BF1201R and BF1201WR are encapsulated in the SOT143B, SOT143R and SOT343R plastic packages respectively.

PINNING

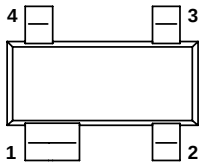
PIN	DESCRIPTION
1	source
2	drain
3	gate 2
4	gate 1



Top view MSB035

BF1201R marking code: LBp

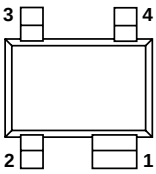
Fig.2 Simplified outline (SOT143R).



Top view MSB014

BF1201 marking code: LAp.

Fig.1 Simplified outline (SOT143B).



Top view MSB842

BF1201WR marking code: LA

Fig.3 Simplified outline (SOT343R).

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DS}	drain-source voltage		–	–	10	V
I_D	drain current		–	–	30	mA
P_{tot}	total power dissipation		–	–	200	mW
$\lvert y_{fs} \rvert$	forward transfer admittance		23	28	35	mS
$C_{ig1\text{-}ss}$	input capacitance at gate 1		–	2.6	3.1	pF
C_{rss}	reverse transfer capacitance	f = 1 MHz	–	15	30	fF
F	noise figure	f = 400 MHz	–	1	1.8	dB
X_{mod}	cross-modulation	input level for k = 1% at 40 dB AGC	105	–	–	dBµV
T_j	operating junction temperature		–	–	150	°C

CAUTION

This product is supplied in anti-static packing to prevent damage caused by electrostatic discharge during transport and handling. For further information, refer to Philips specs.: SNW-EQ-608, SNW-FQ-302A and SNW-FQ-302B.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

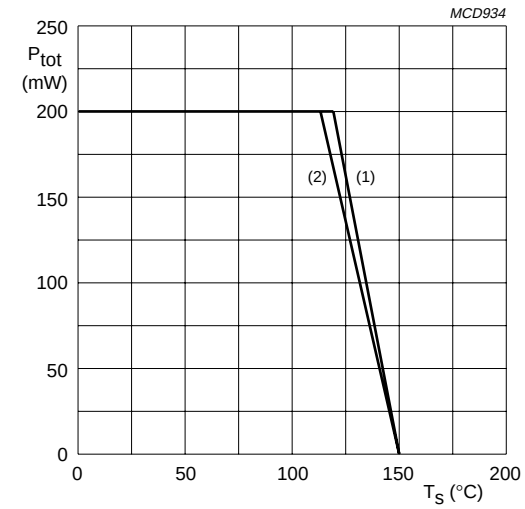
SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	10	V
I_D	drain current (DC)		–	30	mA
I_{G1}	gate 1 current		–	±10	mA
I_{G2}	gate 2 current		–	±10	mA
P_{tot}	total power dissipation				
	BF1201; BF1201R	$T_s \leq 113$ °C; note 1	–	200	mW
	BF1201WR	$T_s \leq 109$ °C; note 1	–	200	mW
T_{stg}	storage temperature		–65	+150	°C
T_j	operating junction temperature		–	150	°C

Note

1. T_s is the temperature of the soldering point of the source lead.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}s}$	thermal resistance from junction to soldering point		
	BF1201; BF1201R	185	K/W
	BF1201WR	155	K/W



(1) BF1201WR.
(2) BF1201 and BF1201R.

Fig.4 Power derating curve.

STATIC CHARACTERISTICS

T_j = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	$V_{G1-S} = V_{G2-S} = 0$; I_D = 10 μA	10	–	V
$V_{(BR)G1-SS}$	gate 1-source breakdown voltage	$V_{G2-S} = V_{DS} = 0$; I_{G1-S} = 10 mA	6	–	V
$V_{(BR)G2-SS}$	gate 2-source breakdown voltage	$V_{G1-S} = V_{DS} = 0$; I_{G2-S} = 10 mA	6	–	V
$V_{(F)S-G1}$	forward source-gate 1 voltage	$V_{G2-S} = V_{DS} = 0$; I_{S-G1} = 10 mA	0.5	1.5	V
$V_{(F)S-G2}$	forward source-gate 2 voltage	$V_{G1-S} = V_{DS} = 0$; I_{S-G2} = 10 mA	0.5	1.5	V
$V_{G1-S(th)}$	gate 1-source threshold voltage	V_{G2-S} = 4 V; V_{DS} = 5 V; I_D = 100 μA	0.3	1.0	V
$V_{G2-S(th)}$	gate 2-source threshold voltage	$V_{G1-S} = V_{DS}$ = 5 V; I_D = 100 μA	0.3	1.2	V
I_{DSX}	drain-source current	V_{G2-S} = 4 V; V_{DS} = 5 V; R_{G1} = 62 kΩ; note 1	11	19	mA
I_{G1-SS}	gate 1 cut-off current	$V_{G2-S} = V_{DS} = 0$; V_{G1-S} = 5 V	–	50	nA
I_{G2-SS}	gate 2 cut-off current	$V_{G1-S} = V_{DS} = 0$; V_{G2-S} = 4 V	–	20	nA

Note

1. R_{G1} connects G_1 to V_{GG} = 5 V.

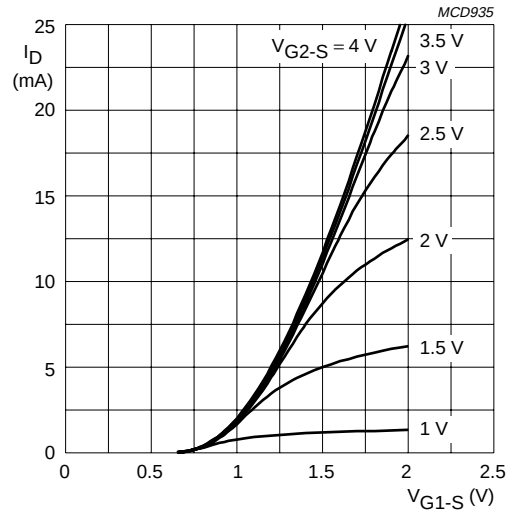
DYNAMIC CHARACTERISTICS

Common source; T_{amb} = 25 °C; V_{G2-S} = 4 V; V_{DS} = 5 V; I_D = 15 mA; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$\lvert y_{fs} \rvert$	forward transfer admittance	pulsed; T_j = 25 °C	23	28	35	mS
C_{ig1-ss}	input capacitance at gate 1	f = 1 MHz	–	2.6	3.1	pF
C_{ig2-ss}	input capacitance at gate 2	f = 1 MHz	–	1.1	–	pF
C_{oss}	output capacitance	f = 1 MHz	–	0.9	–	pF
C_{rss}	reverse transfer capacitance	f = 1 MHz	–	15	30	fF
F	noise figure	f = 10.7 MHz; G_S = 20 mS; B_S = 0	–	5	7	dB
		f = 400 MHz; $Y_S = Y_{S\ opt}$	–	1	1.8	dB
		f = 800 MHz; $Y_S = Y_{S\ opt}$	–	1.9	2.5	dB
G_{tr}	power gain	f = 200 MHz; G_S = 2 mS; $B_S = B_{S\ opt}$; G_L = 0.5 mS; $B_L = B_{L\ opt}$;	–	33.5	–	dB
		f = 400 MHz; G_S = 2 mS; $B_S = B_{S\ opt}$; G_L = 1 mS; $B_L = B_{L\ opt}$;	–	29	–	dB
		f = 800 MHz; G_S = 3.3 mS; $B_S = B_{S\ opt}$; G_L = 1 mS; $B_L = B_{L\ opt}$;	–	24	–	dB
X_{mod}	cross-modulation	input level for k = 1%; f_w = 50 MHz; f_{unw} = 60 MHz; note 1				
		at 0 dB AGC	90	–	–	dBμV
		at 10 dB AGC	–	95	–	dBμV
		at 40 dB AGC	105	–	–	dBμV

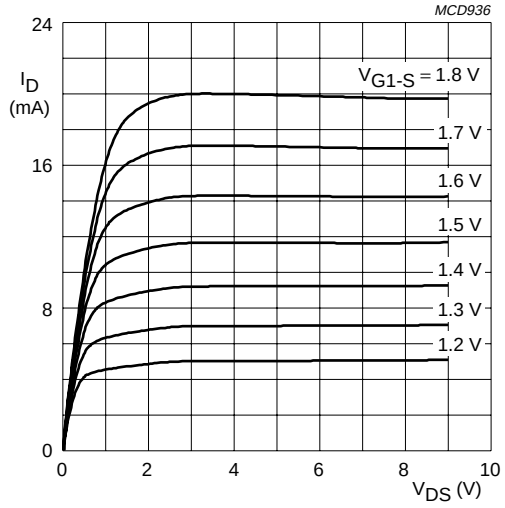
Note

1. Measured in Fig.21 test circuit.



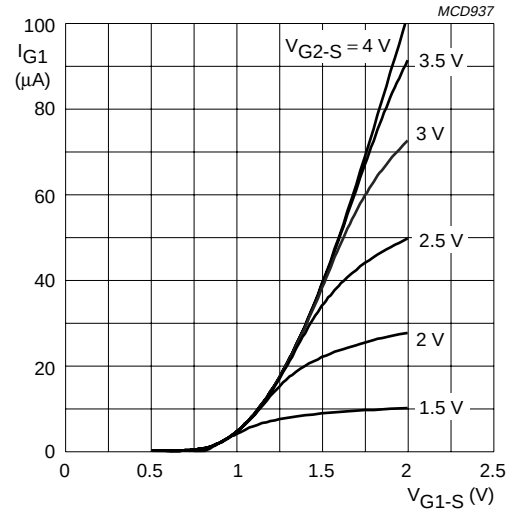
V_{DS} = 5 V.
T_j = 25 °C.

Fig.5 Transfer characteristics; typical values.



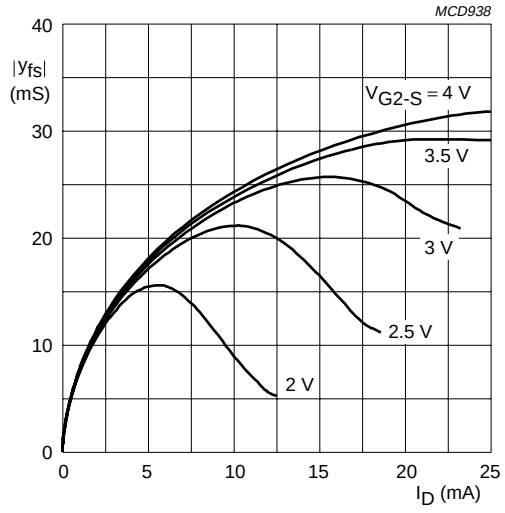
V_{G2-S} = 4 V.
T_j = 25 °C.

Fig.6 Output characteristics; typical values.



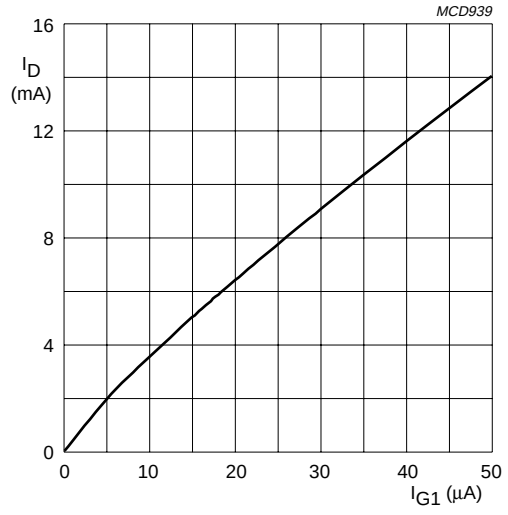
V_{DS} = 5 V.
T_j = 25 °C.

Fig.7 Gate 1 current as a function of gate 1 voltage; typical values.



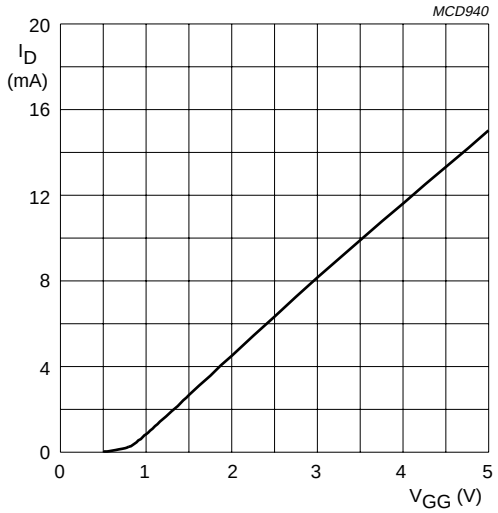
V_{DS} = 5 V.
T_j = 25 °C.

Fig.8 Forward transfer admittance as a function of drain current; typical values.



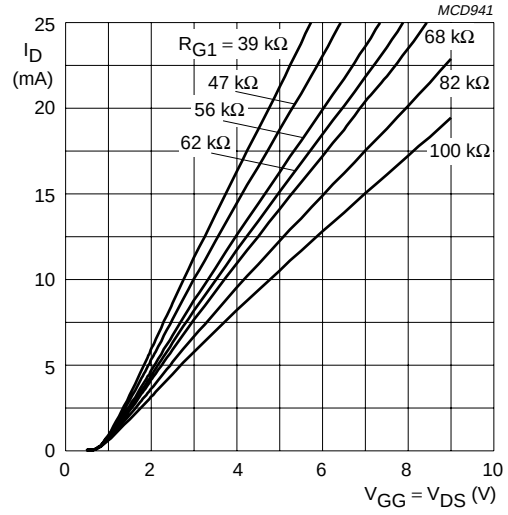
V_{DS} = 5 V; $V_{G2\text{-}S}$ = 4 V.
T_j = 25 °C.

Fig.9 Drain current as a function of gate 1 current; typical values.



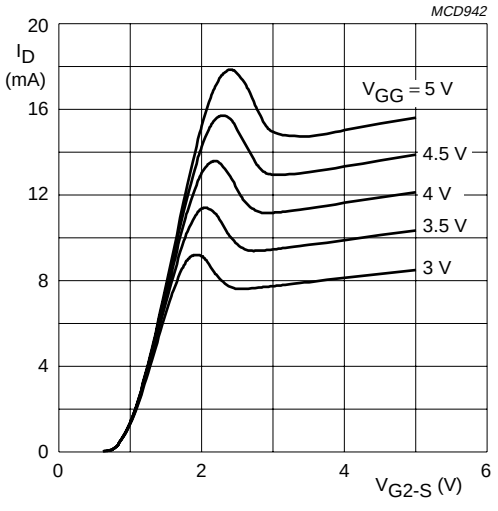
V_{DS} = 5 V; $V_{G2\text{-}S}$ = 4 V; T_j = 25 °C.
R_{G1} = 62 kΩ (connected to V_{GG}); see Fig.21.

Fig.10 Drain current as a function of gate 1 supply voltage (= V_{GG}); typical values.



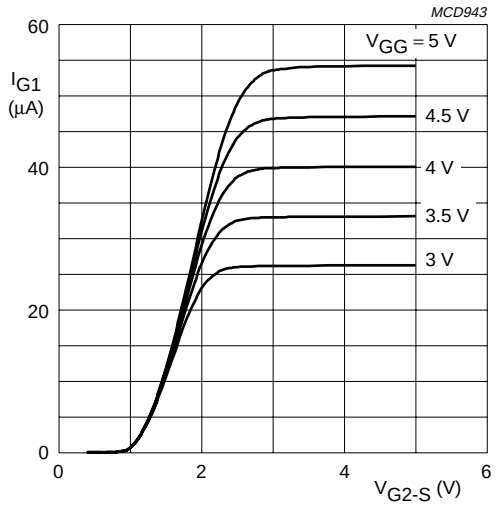
$V_{G2\text{-}S}$ = 4 V; T_j = 25 °C.
R_{G1} connected to V_{GG}; see Fig.21.

Fig.11 Drain current as a function of gate 1 (= V_{GG}) and drain supply voltage; typical values.



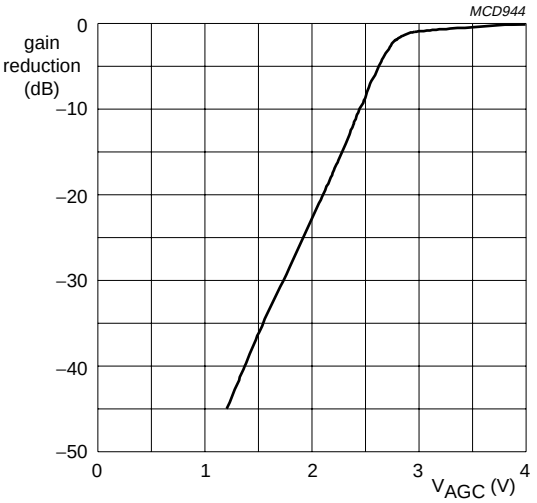
V_{DS} = 5 V; T_j = 25 °C.
R_{G1} = 62 kΩ (connected to V_{GG}); see Fig.21.

Fig.12 Drain current as a function of gate 2 voltage; typical values.



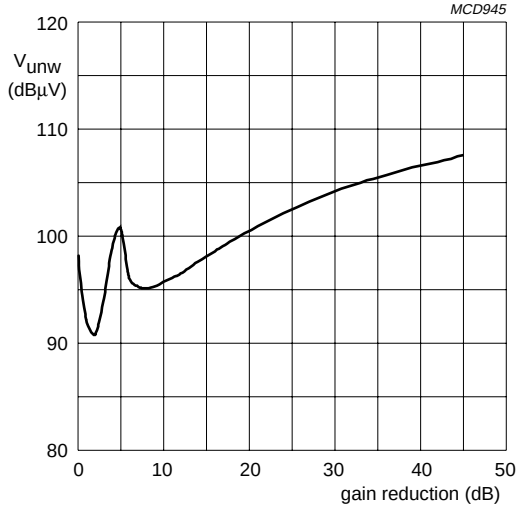
V_{DS} = 5 V; T_j = 25 °C.
R_{G1} = 62 kΩ (connected to V_{GG}); see Fig.21.

Fig.13 Gate 1 current as a function of gate 2 voltage; typical values.



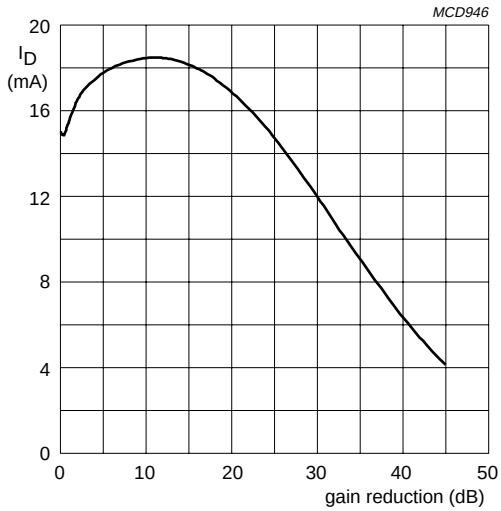
V_{DS} = 5 V; V_{GG} = 5 V; R_{G1} = 62 kΩ;
f = 50 MHz; T_{amb} = 25 °C.

Fig.14 Typical gain reduction as a function of the AGC voltage; see Fig.21.



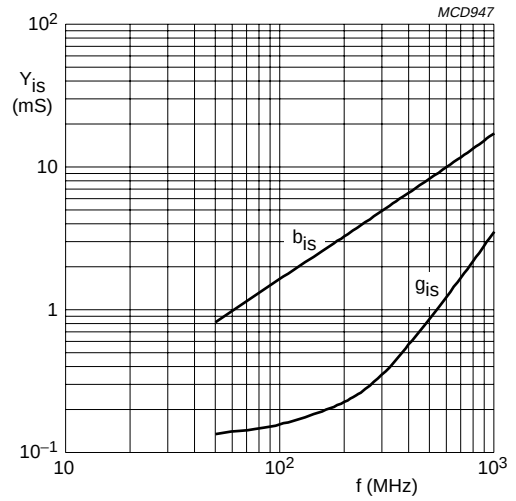
V_{DS} = 5 V; V_{GG} = 5 V; R_{G1} = 62 kΩ; f = 50 MHz;
f_{unw} = 60 MHz; T_{amb} = 25 °C.

Fig.15 Unwanted voltage for 1% cross-modulation as a function of gain reduction; typical values; see Fig.21.



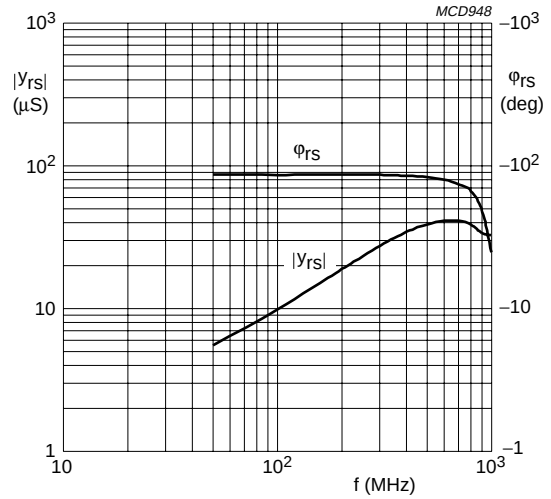
V_{DS} = 5 V; V_{GG} = 5 V; R_{G1} = 62 kΩ;
f = 50 MHz; T_{amb} = 25 °C.

Fig.16 Drain current as a function of gain reduction; typical values; see Fig.21.



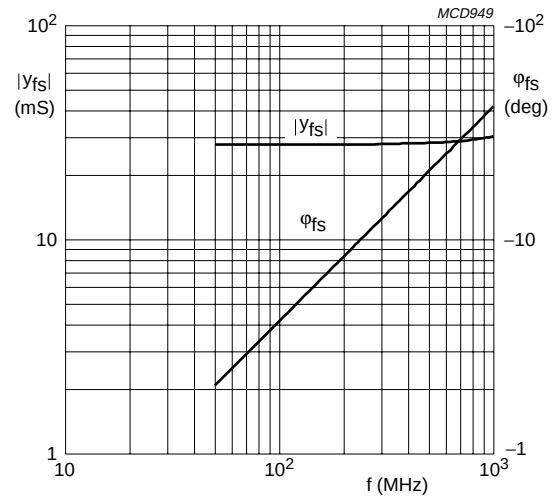
V_{DS} = 5 V; V_{G2} = 4 V.
I_D = 15 mA; T_{amb} = 25 °C.

Fig.17 Input admittance as a function of frequency; typical values.



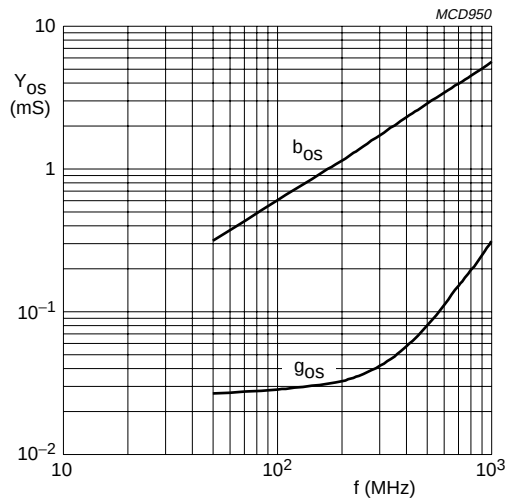
V_{DS} = 5 V; V_{G2} = 4 V.
I_D = 15 mA; T_{amb} = 25 °C.

Fig.18 Reverse transfer admittance and phase as a function of frequency; typical values.



V_{DS} = 5 V; V_{G2} = 4 V.
I_D = 15 mA; T_{amb} = 25 °C.

Fig.19 Forward transfer admittance and phase as a function of frequency; typical values.



V_{DS} = 5 V; V_{G2} = 4 V.
I_D = 15 mA; T_{amb} = 25 °C.

Fig.20 Output admittance as a function of frequency; typical values.

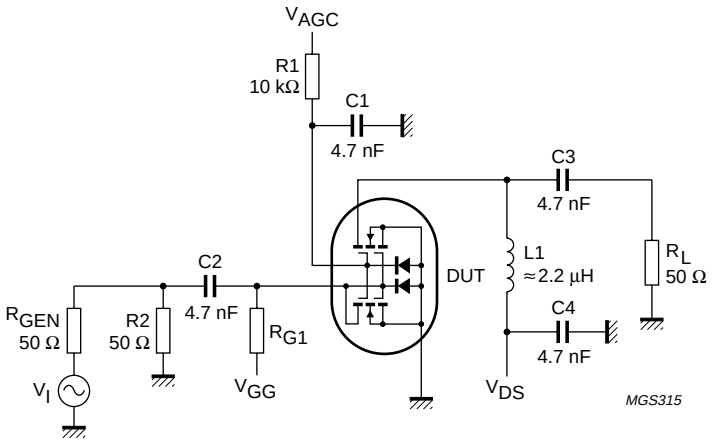


Fig.21 Cross-modulation test set-up.

Table 1 Scattering parameters: V_{DS} = 5 V; V_{G2-S} = 4 V; I_D = 15 mA; T_{amb} = 25 °C

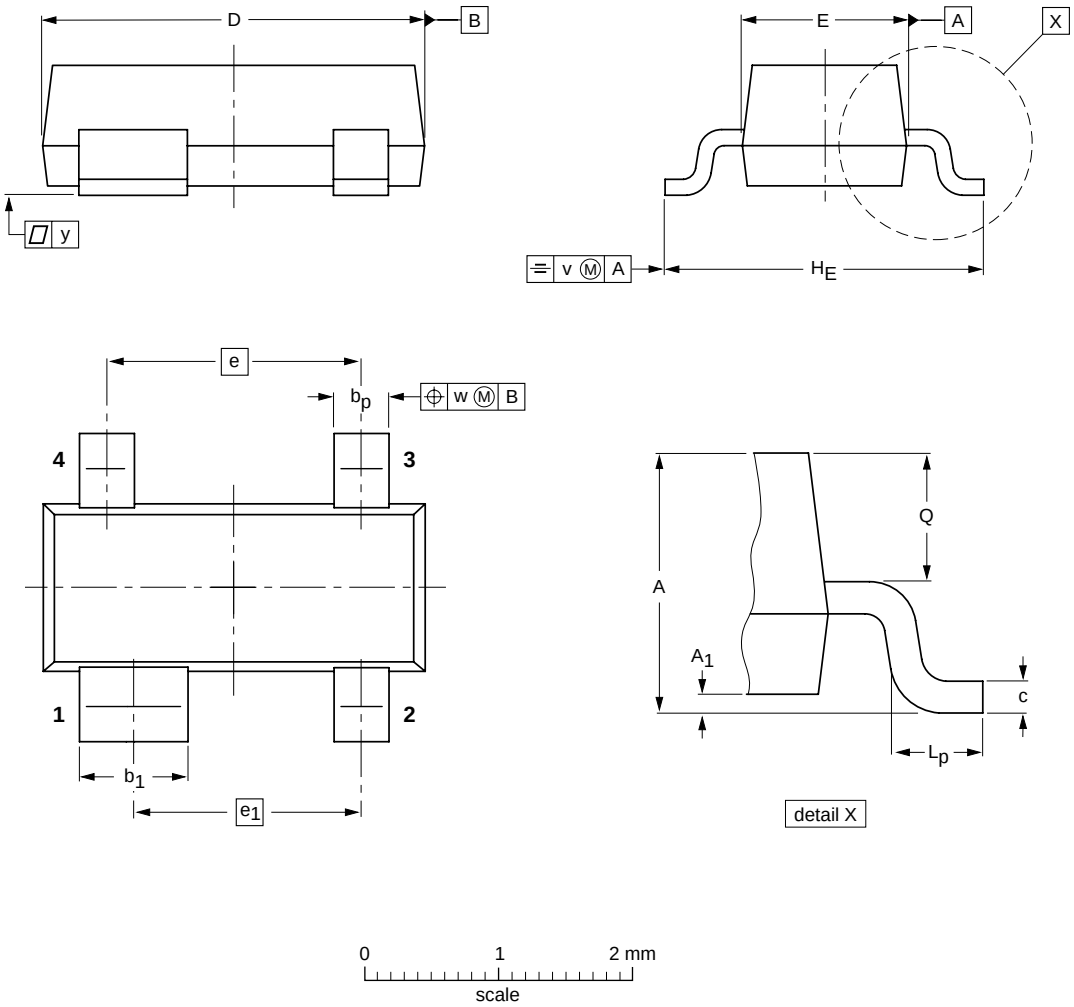
f (MHz)	s_{11}		s_{21}		s_{12}		s_{22}	
	MAGNITUDE (ratio)	ANGLE (deg)	MAGNITUDE (ratio)	ANGLE (deg)	MAGNITUDE (ratio)	ANGLE (deg)	MAGNITUDE (ratio)	ANGLE (deg)
50	0.987	–4.72	2.775	174.6	0.0006	88.8	0.997	–1.84
100	0.985	–9.39	2.774	169.5	0.0010	86.7	0.997	–3.37
200	0.978	–18.59	2.731	159.1	0.0019	79.7	0.996	–6.72
300	0.976	–27.74	2.671	148.8	0.0026	74.2	0.994	–10.02
400	0.949	–36.59	2.599	138.8	0.0032	69.9	0.992	–13.33
500	0.928	–45.08	2.501	129.1	0.0035	65.9	0.989	–16.55
600	0.905	–53.26	2.400	119.8	0.0035	64.6	0.986	–19.64
700	0.882	–61.07	2.297	110.9	0.0033	65.7	0.982	–22.63
800	0.860	–68.48	2.199	102.4	0.0029	69.1	0.979	–25.54
900	0.838	–75.55	2.096	94.2	0.0024	83.3	0.975	–28.44
1000	0.818	–82.23	1.997	86.3	0.0021	103.8	0.971	–31.42

Table 2 Noise data: V_{DS} = 5 V; V_{G2-S} = 4 V; I_D = 15 mA; T_{amb} = 25 °C

f (MHz)	F_{min} (dB)	Γ_{opt}		R_n (Ω)
		(ratio)	(deg)	
400	1	0.825	38.93	50
800	1.9	0.753	70.65	38.75

PACKAGE OUTLINES

Plastic surface mounted package; 4 leads **SOT143B**

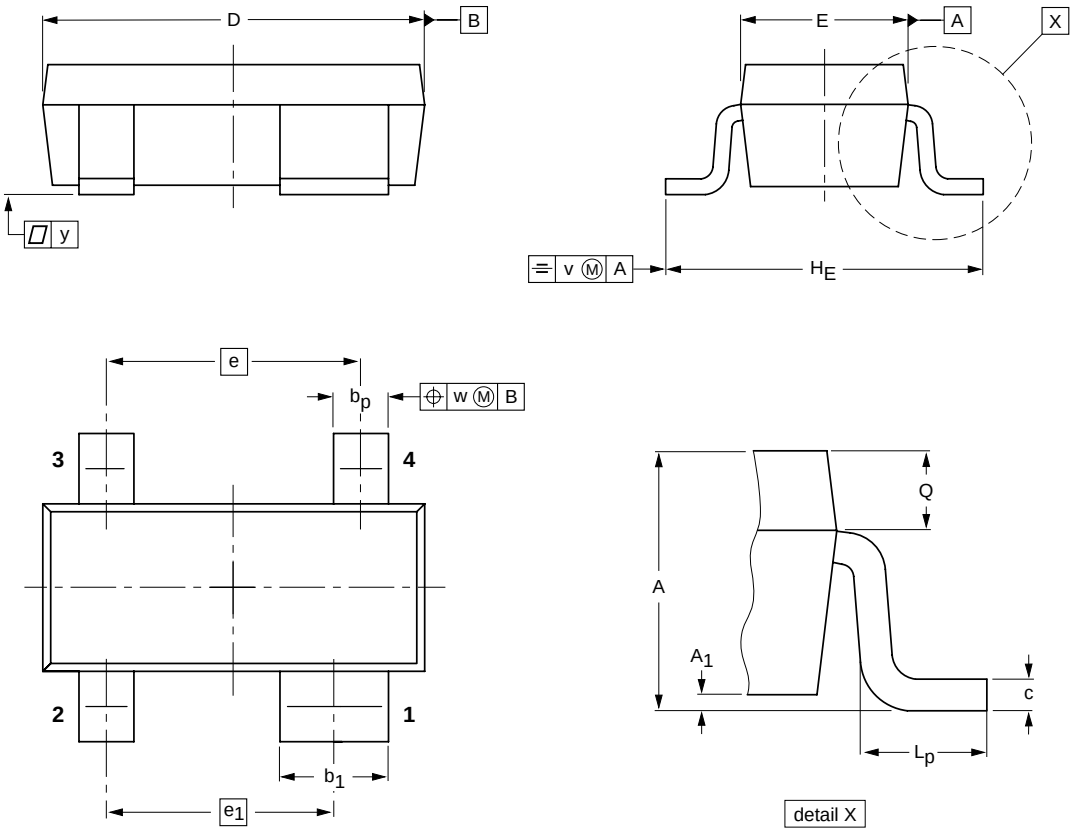


DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1 max	b_p	b_1	c	D	E	e	e_1	H_E	L_p	Q	v	w	y
mm	1.1 0.9	0.1	0.48 0.38	0.88 0.78	0.15 0.09	3.0 2.8	1.4 1.2	1.9	1.7	2.5 2.1	0.45 0.15	0.55 0.45	0.2	0.1	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT143B						97-02-28

Plastic surface mounted package; reverse pinning; 4 leads **SOT143R**

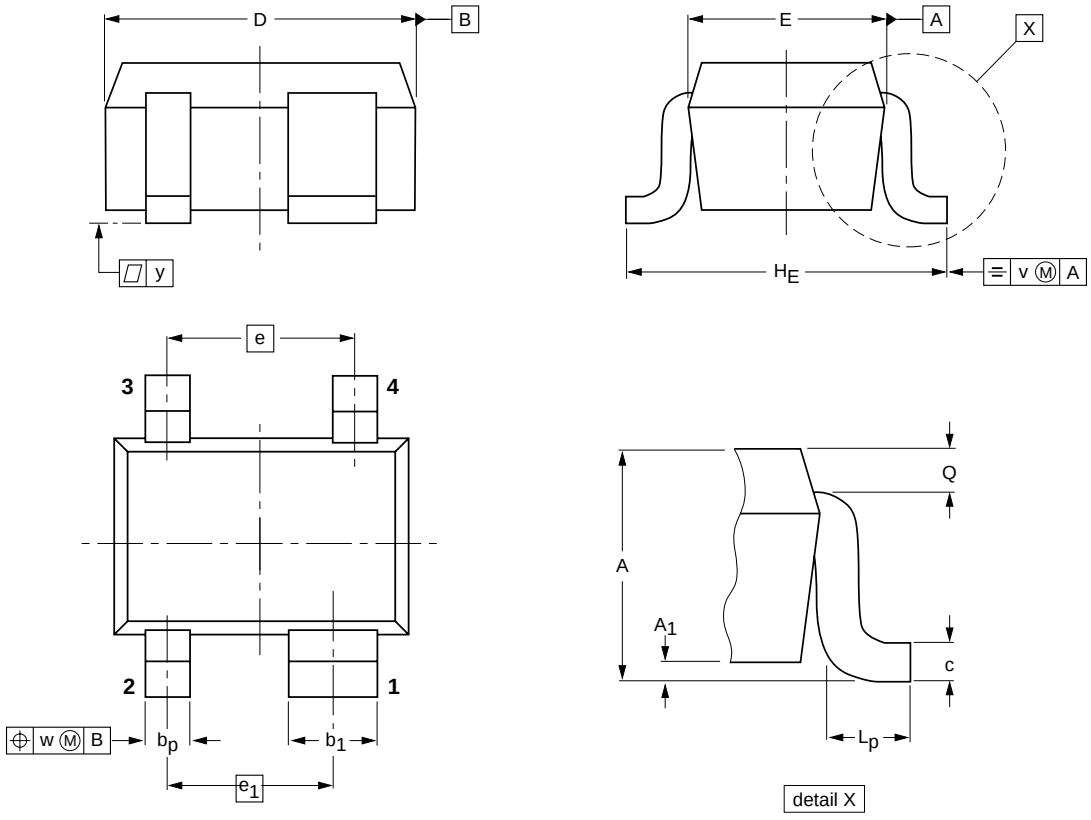


DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1 max	b_p	b_1	c	D	E	e	e_1	H_E	L_p	Q	v	w	y
mm	1.1 0.9	0.1	0.48 0.38	0.88 0.78	0.15 0.09	3.0 2.8	1.4 1.2	1.9	1.7	2.5 2.1	0.55 0.25	0.45 0.25	0.2	0.1	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT143R			SC-61B			~~97-03-10~~ 99-09-13

Plastic surface mounted package; reverse pinning; 4 leads **SOT343R**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1 max	b_p	b_1	c	D	E	e	e_1	H_E	L_p	Q	v	w	y
mm	1.1 0.8	0.1	0.4 0.3	0.7 0.5	0.25 0.10	2.2 1.8	1.35 1.15	1.3	1.15	2.2 2.0	0.45 0.15	0.23 0.13	0.2	0.2	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT343R						97-05-21

DATA SHEET STATUS

DATA SHEET STATUS	PRODUCT STATUS	DEFINITIONS [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product specification	Production	This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

Note

1. Please consult the most recently issued data sheet before initiating or completing a design.

DEFINITIONS

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

Application information — Applications that are described herein for any of these products are for illustrative purposes only. Philips Semiconductors make no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

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