RF/IF 34dB Gain Range VGA with AGC Detector

Preliminary Technical Data

AD8368

FEATURES

Analog Variable Gain Range: -12 to 22dB
Linear-in-dB Scaling: 40dB/V
3dB Bandwidth: 800 MHz
Integrated RMS Detector
Output 1dB Compression: 17 dBm
Output IP3: 33.7 dBm
Minimum Noise Figure: 9 dB
Input and Output Impedances: 50 ohms
Single Supply Voltages from 4.5 – 5.5 V
RoHS Compliant 24-lead LFCSP Package

APPLICATIONS

Complete IF AGC Amplifiers
Gain Trimming and Leveling
Cellular base station
Point-to-Point Radio links
RF Instrumentation

FUNCTIONAL BLOCK DIAGRAM

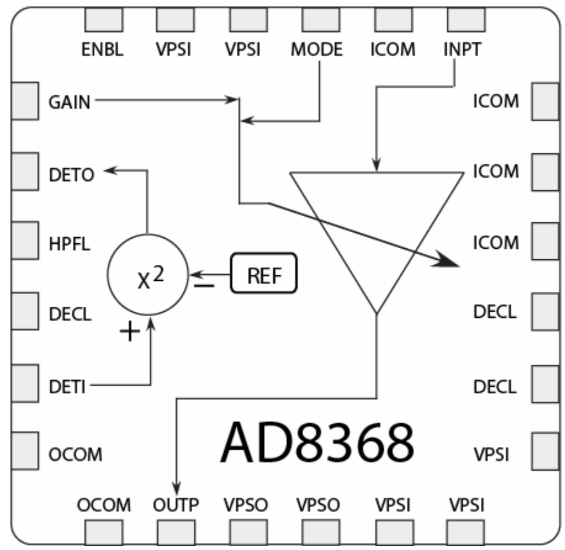

Figure 1.

GENERAL DESCRIPTION

The AD8368 is a variable gain amplifier with analog linear-in-dB gain control that can be used from low frequencies to beyond 1 GHz. Its excellent gain range, conformance and flatness are attributed to Analog Devices' X-AMP ™ architecture, an innovative technique for implementing high performance variable gain-control.

The gain range of -12 to 22 dB is scaled accurately to 40 dB/V with excellent conformance error. The AD8368 has a 3-dB bandwidth of 800 MHz that is independent of gain setting. At 70 MHz, the OIP3 and P1dB are 33.7 dBm and 17 dBm, respectively. The output noise floor is –143 dBm/Hz, which corresponds to 9 dB noise figure at maximum gain. The single-ended input and output impedances are nominally 50 ohms.

The gain of the AD8368 can be configured to be an increasing or decreasing function of the gain control voltage depending on whether the MODE pin is pulled to the positive supply or to ground, respectively. When MODE is pulled high, the gain increases with gain control voltage and the AD8368 operates as a typical VGA. When MODE is pulled low, the gain decreases with gain control voltage. This second mode allows the AD8368 to be used in AGC systems with power detectors whose outputs increase with received signal level.

The AD8368 contains an accurate stand-alone RMS detector that enables versatile AGC operation. To form a complete AGC loop, the MODE pin is pulled low and the detector output pin is directly connected to the GAIN pin and an integrating capacitor. Then, by connecting the VGA output OUTP directly to the detector input DETI, the output is leveled to the set-point of 63 mV_{rms} or -11 dBm referenced to 50 Ω. This reference level can be raised by dividing down the output signal before applying it to DETI. The detector can level the AD8368 output or any other point in the signal chain depending on where the detector pins DETI and DETO are connected.

The AD8368 operates from a supply voltage of 4.5 to 5.5 V and consumes 54 mA of current. It can be fully powered down to <1mA by grounding the ENBL pin. The AD8368 is fabricated in Analog Devices' proprietary SiGe SOI complementary bipolar IC process. It is available in a 24 pin CSP and operates over the industrial temperature range of –40 to 85 C. Application boards are available upon request.

Rev. PrB

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AD8368-SPECIFICATIONS

(V_S=5V, T=25°C, System Impedance Zo = 50Ω, MODE = 5V unless otherwise noted)

Parameter	Conditions	Min	Typ	Max	Units
POWER INTERFACE					
Supply Voltage		4.5		5.5	V
Total Supply Current	ENBL high		54		mA
Disable Current	ENBL low		1.0		mA
vs. Temperature	-40°C ≤ T_A ≤ 85°C	TBD		TBD	mA
SQUARE LAW DETECTOR					
Output Set-point	OUTP connected to DETI		-11		dBm
Input DC Level	DETI pin		$V_P/2$		V
Input Impedance	DETI pin		710		Ohm
			0.6		pF
Output Range	DETO pin	0		$V_P/2$	V
AGC Small-signal Response	C_{DETO}=5pF		1		us
MODE CONTROL INTERFACE (MODE)					
Mode LO Threshold	Device in negative slope mode of operation		TBD		V
Mode HI Threshold	Device in positive slope mode of operation		TBD		V
Input Current			TBD		uA
ENABLE INTERFACE (ENBL)					
Enable Threshold			2.5		V
Enable Response Time	Time delay following HI to LO transition until device meets full specifications.		1.5		µs
Enable Input Bias Current	ENBL = 5 V		TBD		µA
	ENBL = 0 V		TBD		nA

AD8368 SPECIFICATIONS

(V_S=5V, T=25°C, System Impedance Zo = 50Ω , MODE = 5V unless otherwise noted)

Parameter	Conditions	Min	Typ	Max	Units
OVERALL FUNCTION					
Frequency Range		LF		1000	MHz
Maximum Input	To Avoid Input Overload		3		V_P
Maximum Output	To Avoid Clipping		2		V_P
Input Resistance	From INPT to ICOM		50		Ω
Output Resistance	From OUTP to OCOM		50		Ω
GAIN CONTROL INTERFACE (GAIN)					
GAIN Span			34		dB
GAIN Scaling	MODE = 5 V, 50 mV ≤ V_{GAIN} ≤ 950 mV		37.16		dB/V
	MODE = 0 V, 50 mV ≤ V_{GAIN} ≤ 950 mV		-37.5		dB/V
Gain Accuracy	100 mV ≤ V_{GAIN} ≤ 900 mV		±0.4		dB
Maximum Gain	V_{GAIN} = 1 V		22		dB
Minimum Gain	V_{GAIN} = 0 V		-12		dB
V_{GAIN} Voltage Range		0		1	V
Gain Step Response	From 0 dB to 30 dB		TBD		ns
	From 30 dB to 0 dB		TBD		ns
Input Impedance	From GAIN To ICOM	10			kohm
f = 70 MHz					
Noise Figure	Maximum Gain		9		dB
Output IP3	f1 = 70 MHz, f2 = 71 MHz, V_{GAIN} = 1 V		33.7		dBm
Output 1dB Compression Point	V_{GAIN} = 1 V		17		dBm
f = 140 MHz					
Noise Figure	Maximum Gain		9		dB
Output IP3	f1 = 140 MHz, f2 = 141 MHz, V_{GAIN} = 1 V		31.6		dBm
Output 1dB Compression Point	V_{GAIN} = 1 V		13		dBm
f = 240 MHz					
Noise Figure	Maximum Gain		9		dB
Output IP3	f1 = 240MHz, f2 = 241 MHz, V_{GAIN} = 1 V		29		dBm
Output 1dB Compression Point	V_{GAIN} = 1 V		15		dBm

f = 380 MHz			
Noise Figure	Maximum Gain	9	dB
Output IP3	f1 = 380 MHz, f2 = 381 MHz, V_{GAIN} = 1 V	24.8	dBm
Output 1dB Compression Point	V_{GAIN} = 1 V	9	dBm

ABSOLUTE MAXIMUM RATINGS

Table 1.

Parameter	Rating
Supply Voltage, VPSO, VPSI	TBD V
ENBL and MODE Select Voltage	VPS+TBDmV
RF Input Level	20 dBm
Internal Power Dissipation	TBD mW
θ_{JA}	TBD °C/W
Maximum Junction Temperature	135°C
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature Range (Soldering 60 sec)	300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

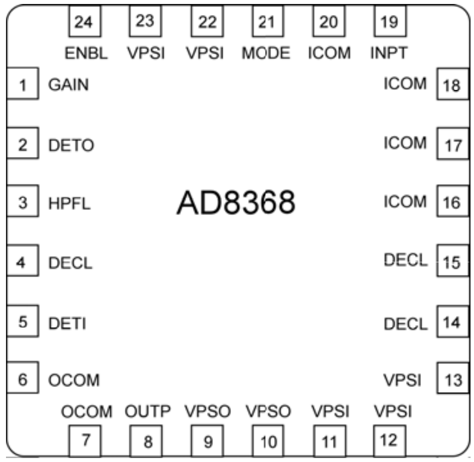

Figure 2. 24-Lead LFCSP

Table 2. Pin Function Descriptions

Pin	Name	Function
1	**GAIN**	Gain Control Voltage Input
2	**DETO**	Detector Output. Provides output current for RSSI function and AGC control.
3	**HPFL**	High Pass Filter Connection. A capacitor to ground sets the corner frequency of the output offset control loop.
4,14,15	**DECL**	Decoupling Pin. Can Be Used to Modify the Output Reference Level. ~V_{PS}/2
5	**DETI**	Detector Input
6,7,16, 17,18,20	**OCOM** **ICOM**	Common. Connect to low impedance ground. **ICOM** and **OCOM** are tied together internally with back to back PN junctions. They should be tied together externally and properly grounded.
8	**OUTP**	Signal Output. Must be AC coupled.
9,10,11, 12,13,22, 23	**VPSO** **VPSI**	Positive Supply Voltage. +4.5 V to +5.5 V. **VPSI** and **VPSO** are tied together internally with back to back PN junctions. They should be tied together externally and properly bypassed.
19	**INPT**	Signal Input. Must be AC coupled
21	**MODE**	Gain Direction Control. HI for Positive Slope. LO for Negative Slope.
24	**ENBL**	Apply a positive voltage (≤VS) to activate device.

TYPICAL PERFORMANCE CHARACTERISTICS

V_S=5V, T=25°C, System Impedance Zo = 50Ω , MODE = 5V unless otherwise noted

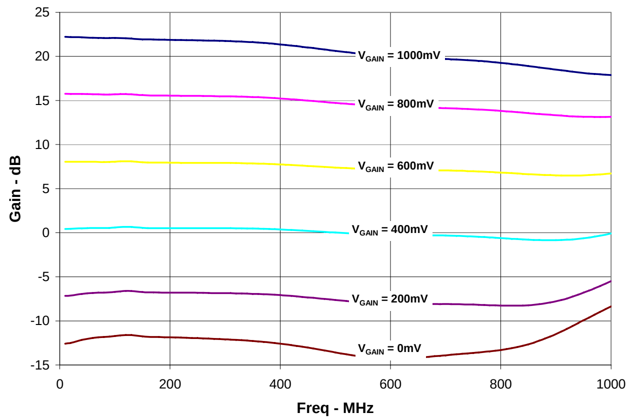

Figure 3. Gain vs. Frequency

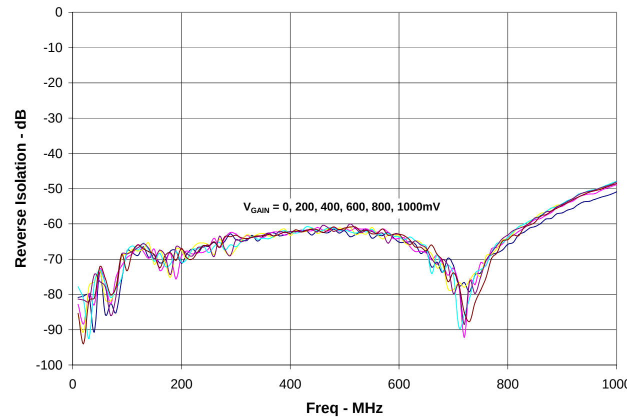

Figure 6. Reverse Isolation vs. Frequency

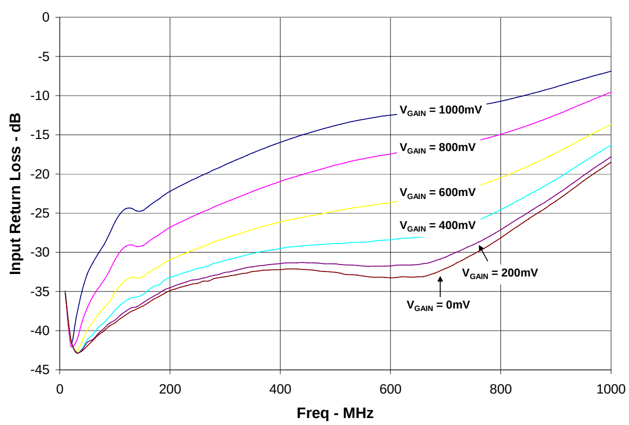

Figure 4. Input Return Loss vs. Frequency

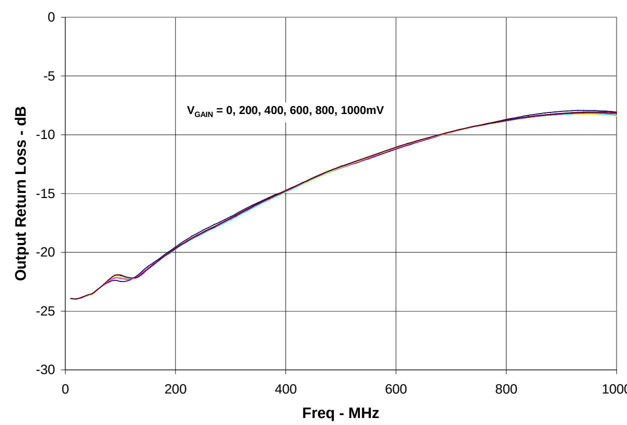

Figure 7. Output Return Loss vs. Frequency

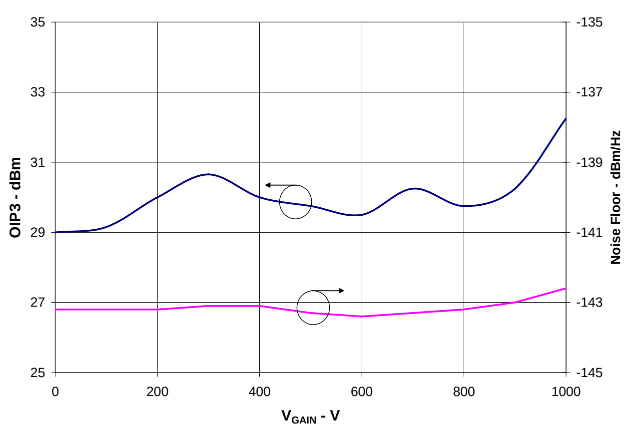

Figure 5. OIP3 and Output Noise Floor vs. V_{GAIN} at 140MHz

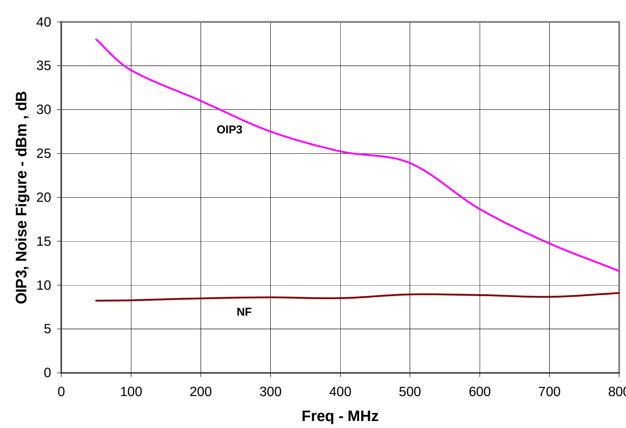

Figure 7.OIP3 and NF vs. Frequency

CIRCUIT DESCRIPTION

The AD8368 is a single-ended VGA with a bandwidth of 800MHz and a gain control range of 32dB from -10dB to +22dB. It also includes an onboard square-law detector that can be used as a standalone detector, or in an AGC loop with the VGA. Using Analog Devices' patented X-AMP architecture, the AD8368 achieves accurate linear-in-dB gain control. The part is designed with 50 Ω input and output impedances.

The main signal path consists of a variable input attenuator followed by an integrator and output buffer. Feedback around the integrator creates a fixed-gain amplifier. See Figure 8 for a block diagram of the part.

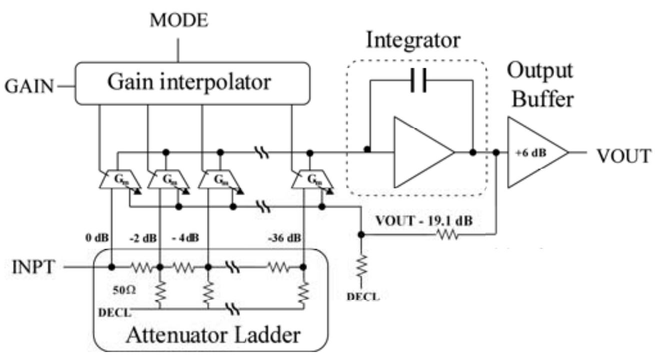

Figure 8. Simplified Block Diagram

Input Attenuator and Interpolator

The input attenuator is built from a resistor ladder with 18 -2dB tap points. Each of these tap points is fed into separate variable transconductance (g_m) stages, whose outputs are summed and fed into an integrator. Gain control is achieved by using the GAIN pin to control the interpolator. As GAIN is swept from 0V to 1V, the interpolator selects different tap points by varying the transconductance of the g_m stages. For gains between two tap points, the interpolator varies the transconductance such that the weighted sum of several adjacent tap points are chosen. In this way, an accurate continuous linear-in-dB gain control response is produced.

Integrator and Output Buffer

The current outputs of the g_m stages are summed and fed into an integrator. Resistive feedback from the output of the integrator to the g_m stages creates a low-noise, high-linearity fixed-gain amplifier. The output of this amplifier is fed into the output buffer which provides an active 50 Ω output and additional 6dB of fixed gain.

Output DC level and offset correction

Since the AD8368 is single-ended, the DC levels at the input and output are regulated to VPSI/2 by an internal regulator. The output of this regulator is connected to the DECL line and requires an external decoupling capacitor.

Since the fixed-gain amplifier and output stage have an extremely large overall gain, small DC offsets at the input of the fixed-gain amplifier could lead to large output offsets. To correct for this problem over Vgain, supply and temperature variations, a low-pass offset correction loop (see Figure 9) is used which senses and maintains the output DC level at the voltage on the DECL pin. The low-pass corner frequency of this loop is controlled by the size of the capacitor on the HPFL pin.

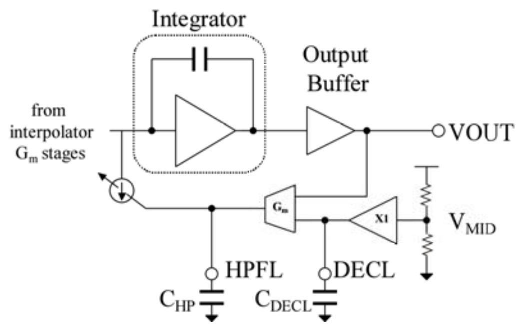

Figure 9. Output Centering Control Loop

Input and Output Impedances

The input to the AD8368 should be externally AC coupled to prevent disrupting the DC levels on the chip. Thus, a sufficiently large coupling capacitor should be used such that the series impedance of the capacitor is negligible at the frequencies of interest. On the chip, the input is connected directly to a resistor ladder network whose impedance is nominally 50 Ω.

The output of the part should also be AC coupled to prevent disrupting the output DC level. As with the input, a sufficiently large value of capacitance should be used so that the series impedance of the capacitor is negligible at the frequencies of interest.

The fixed gain of the rail to rail output buffer combined with the resistive feedback from output to input provides a nominally 50-Ω output impedance.

Gain Control Interface

The AD8368 has a linear-in-dB gain control interface that can be operated in either a gain-up or gain-down mode. In the gain-up mode with the MODE pin pulled high, the gain increases with increasing GAIN voltages. In gain-down mode, with the MODE pin pulled low, the gain decreases with increasing GAIN voltages.

Ideally, with MODE pulled high, the ideal gain function is given by the equation,

$$Gain(dB) = 37 \times V_{GAIN} - 14$$

With MODE pulled low, the ideal gain function is given by the equation,

$$Gain(dB) = -37.5 \times V_{GAIN} + 24.8$$

where V_{GAIN} is expressed in Volts in both above equations.

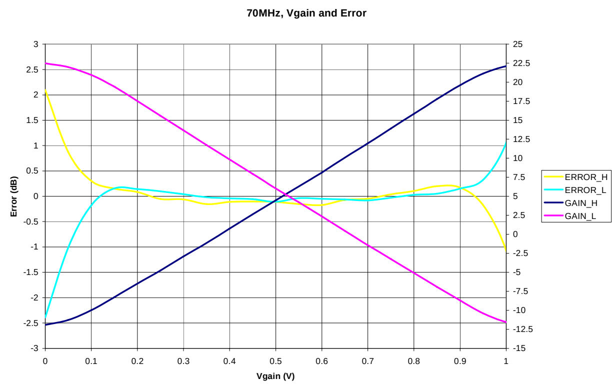

Figure 10 The gain function can be either an increasing or decreasing function of VGAIN, depending on the MODE pin.

It should be noted that gain-down mode is the gain mode required to use the onboard detector and VGA together as an AGC loop.

VGA Operation

The AD8368 is a general-purpose VGA suitable for use in a wide variety of applications where voltage-control of gain is needed. While having a 800 MHz bandwidth, its use is not limited to high frequency signal processing. Its accurate, temperature- and supply-stable linear-in-dB scaling will be valuable wherever it is important to have a more dependable response to the control voltage than is usually offered by VGAs of this sort.

The typical connections for using the AD8368 in VGA mode are illustrated in Figure 11. The input (INPT) and output (OUTP) of the AD8368 should be externally AC coupled to prevent disrupting the DC levels on the chip. Thus, a sufficiently large coupling capacitor should be used such that the series impedance of the capacitor is negligible at the frequencies of interest.

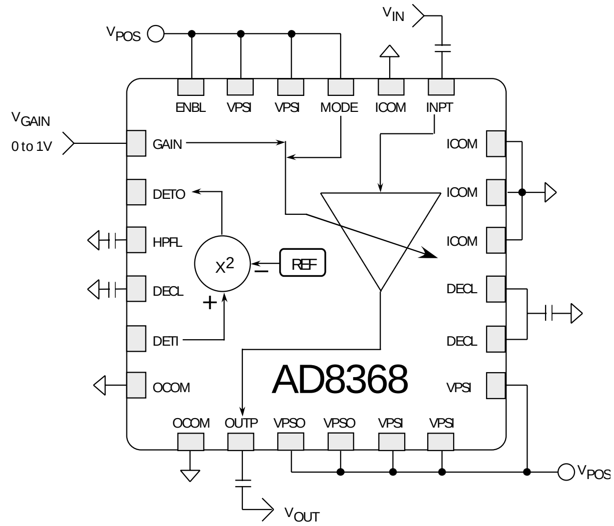

Figure 11. Typical Connections for VGA Mode

The MODE pin controls whether the gain of the part is an increasing or decreasing function of the GAIN voltage. When the MODE pin is high, the gain increases with increasing GAIN voltages. When the MODE pin is low, the gain decreases with increasing GAIN voltages. The ENBL pin is used to enable or disable the part. When ENBL is high, the part is enabled. With ENBL low, the part is disabled and draws a fraction of the normal supply current.

The DECL pin should be decoupled using a large capacitor so that DECL acts as an AC ground. The HPFL pin is used to control the low-pass corner frequency of the output offset correction loop. The high pass corner frequency is inversely proportional to the HPFL bypass capacitor.

AGC Operation

The AD8368 may be used as an AGC amplifier as shown in Figure 12. For this application, the accurate internal square-law detector is employed. The output of this detector is a current that varies in polarity depending on whether the rms value of the output is greater or less than its internally-determined“set-point” of 63mVrms. This is 178mV pk-pk for sine-wave signals, but the peak amplitude for other signals, such as Gaussian noise, or those carrying complex modulation, will be invariably be somewhat greater. However, for all waveforms having a reasonable crest factor (less than 13dB), the rms value will be correctly measured and delivered at VOUT. The output set-point may be adjusted using an external resistive divider network as depicted in Figure y. In this configuration the RMS output voltage will be equal to (1+n)63mVrms, where n=R2/R1. For the default set-point of 63mVrms simply short R1 (direct connection from OUTP to DETI) and remove R2.

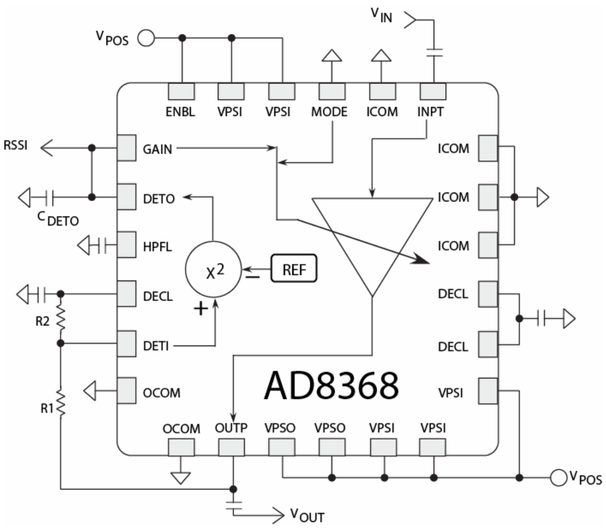

Figure 12. AGC Mode of Operation

The AGC mode of operation requires that the correct gain direction is chosen. Specifically, the gain must fall as V_{AGC} increases to restore the needed balance against the set-point. Therefore, the MODE pin must be pulled low. This very accurate leveling function is shown in Figure 13, where the rms output is held to within 0.2 dB of the set point for >30 dB range of input levels. This measurement was made using R1 = 100 ohms and R2 = 226 ohms to achieve 0 dBm output level.

A valuable feature of using a square law detector is that the RSSI voltage is a true reflection of signal power, and may be converted to an absolute *power measurement* for any given source impedance. The AD8368 may be employed as a true-power meter by monitoring the voltage present at the DETO/GAIN interface.

Figure 15 illustrates the measured error-vector-magnitude (EVM) performance for a 16-QAM modulation at 10MSymbols/sec using CDETO=1000pF. At lower symbol rates the AGC loop could start to track the peak to peak transitions due to the modulation. At lower symbol rates it may be necessary to slow down the response of the AGC loop by increasing the value of CDETO .

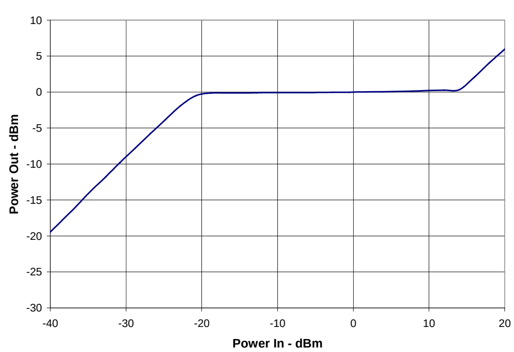

Figure 13 Output Power versus Input Power in AGC Mode at 140MHz.

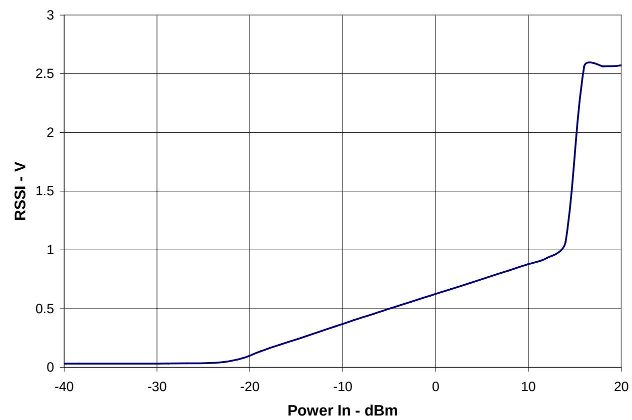

Figure 14. Monitoring the GAIN/DETO RSSI Voltage versus Input Power.

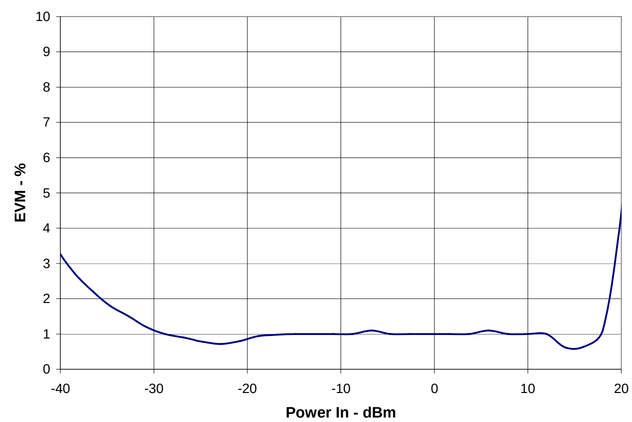

Figure 15. Error Vector Magnitude Performance for 16-QAM 10Msymbols/sec.

EVALUATION BOARD

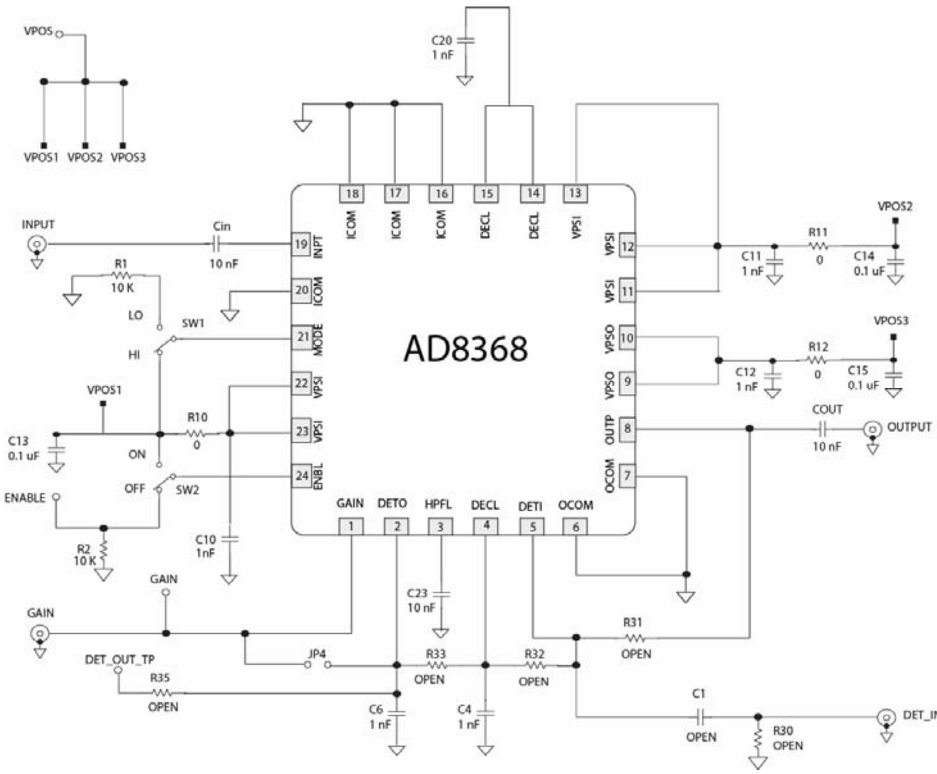

Table X. Evaluation Board Configuration Options

Component	Function	Default Conditions
R1, R2	Pull down resistors for mode and enable	R1 = R2 = 10 kΩ
R10	Jumper resistors	R10 = 0Ω
R11 , R12 , C10 , C11 , C12 , C13 , C14 , C15	Supply decoupling. Jumpers and power supply decoupling resistors and filter capacitors.	R11 = R12 = 0 Ω C11 = C12 = 1 nF C13 = C14 = C15 = 0.1 uF
CIN	RF input. Cin provides dc block for RF input.	CIN = 10 nF
COUT	RF output. Cin provides dc block for RF output.	COUT = 10 nF
R31, R32	Feedback path for AGC operation. For default set point of 63mVrms set R31 = 0 Ω and remove R32. For other AGC setpoints the RMS voltage output is determined from (1+n)63mVrms. Where n = R31/R32.	R31 = OPEN (VGA mode)

R35	**Detector out RSSI voltage**	**R35 = OPEN, poulate with 0 Ω to feed DET_OUT_TP**
R33		**R33 = OPEN**
C23	**Sets the corner frequency of output offset control loop high pass filter.**	**C23 = 10 nF**
C1, R30		**C1 =** **R30 =**
C20	**Decoupling Pin**	**C20 = 1 nF**
JP4	**Jumper for AGC mode of operation. Provides feedback from the detector output to the gain pin.**	
SW1	**Mode SW1. LO mode puts part in negative slope mode. HI puts part in positive slope mode. AGC operation requires negative slope mode.**	
SW2	**Power down. The part is disabled when the enable pin is tied to ground.**	

OUTLINE DIMENSIONS

24-Lead Frame Chip Scale Package [LFCSP]
4 mm x 4 mm Body
(CP-24)
Dimensions shown in millimeters

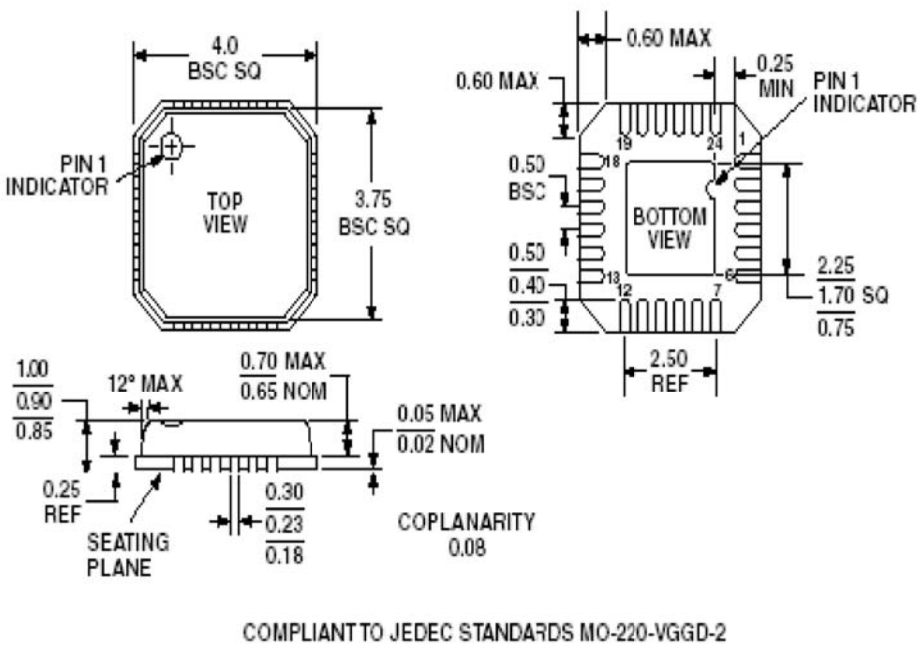

Figure 8. 8-Lead Lead Frame Chip Scale Package [LFCSP] 3 mm × 2 mm Body (CP-8-3) Dimensions in millimeters

ORDERING GUIDE

Model	Temperature Package	Package Description	Package Outline	Branding
AD8368ACPZ-REEL7[1]	−40°C to +85°C	24-Lead Lead Frame Chip Scale Package	CP-24-4	TBD
AD8368ACPZ-WP[1,2]	−40°C to +85°C	24-Lead Lead Frame Chip Scale Package	CP-24-4	TBD
AD8368-EVAL		Evaluation Board		

[1] Z = Pb-free part.
[2] WP = Waffle pack.

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