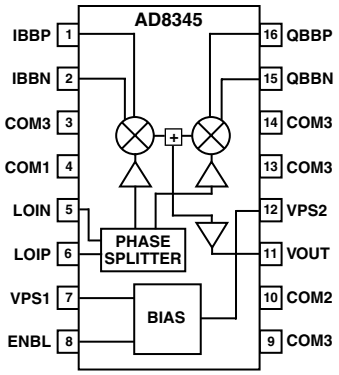
250 MHz–1000 MHz Quadrature Modulator

AD8345

FEATURES
250 MHz–1000 MHz Operating Frequency
+2.5 dBm P1 dB @ 800 MHz
–155 dBm/Hz Noise Floor
0.5 Degree RMS Phase Error (IS95)
0.2 dB Amplitude Balance
Single 2.7 V–5.5 V Supply
Pin-Compatible with AD8346
16-Lead Exposed Paddle TSSOP Package

APPLICATIONS
Cellular Communication Systems
W-CDMA/CDMA/GSM/PCS/ISM Transceivers
Fixed Broadband Access Systems LMDS/MMDS
Wireless LAN
Wireless Local Loop
Digital TV/CATV Modulators
Single Sideband Upconverter

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD8345 is a silicon RFIC quadrature modulator, designed for use from 250 MHz to 1000 MHz. Its excellent phase accuracy and amplitude balance enable the high performance direct modulation of an IF carrier.

The AD8345 accurately splits the external LO signal into two quadrature components through the polyphase phase-splitter network. The two I and Q LO components are mixed with the baseband I and Q differential input signals. Finally, the outputs of the two mixers are combined in the output stage to provide a single-ended 50 Ω drive at VOUT.

APPLICATIONS

The AD8345 Modulator can be used as the IF transmit modulator in digital communication systems such as GSM and PCS transceivers. It can also directly modulate an LO signal to produce QPSK and various QAM formats for 900 MHz communication systems as well as digital TV and CATV systems.

Additionally, this quadrature modulator can be used with direct digital synthesizers in hybrid phase-locked loops to generate signals over a wide frequency range with millihertz resolution.

The AD8345 Modulator is supplied in a 16-lead TSSOP package with exposed paddle. Its performance is specified over a –40°C to +85°C temperature range. This device is fabricated on Analog Devices' advanced silicon bipolar process.

REV. 0

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AD8345—SPECIFICATIONS (V_S = 5 V; LO= –2 dBm @ 800 MHz, 50 Ω source and load impedances, I and Q inputs 0.7 V ± 0.3 V on each side for a 1.2 V p-p differential input, I and Q inputs driven in quadrature @ 1 MHz Baseband Frequency. T_A = 25°C, unless otherwise noted.)

Parameters	Conditions	Min	Typ	Max	Unit
RF OUTPUT					
Operating Frequency[1]		250		1000	MHz
Output Power		–3	–1	+2	dBm
Output P1 dB			2.5		dBm
Noise Floor	20 MHz Offset from LO, All BB Inputs at 0.7 V		–155		dBm/Hz
Quadrature Error	(CDMA IS95 Setup, Refer to Figure 13)		0.5		Degree rms
I/Q Amplitude Balance	(CDMA IS95 Setup, Refer to Figure 13)		0.2		dB
LO Leakage			–42	–33	dBm
Sideband Rejection			–42	–34	dBc
Third Order Distortion			–52		dBc
Second Order Distortion			–60		dBc
Equivalent Output IP3			25		dBm
Equivalent Output IP2			59		dBm
Output Return Loss (S22)			–20		dB
RESPONSE TO CDMA IS95 BASEBAND SIGNALS	(Refer to Figure 13)				
ACPR			–72		dBc
EVM			1.3		%
Rho			0.9995		
LO INPUT					
LO Drive level		–10	–2	0	dBm
LOIP Input Return Loss (S11)[2]					
	No Termination on LOIP, LOIN at AC Ground		–5		dB
	50 Ω Terminating Resistor, Differential Drive via Balun		–9		dB
BASEBAND INPUTS					
Input Bias Current			10		µA
Input Capacitance			2		pF
DC Common Level		0.6	0.7	0.8	V
Bandwidth (3 dB)	Full Power (0.7 V ± 0.3 V on Each Input, Refer to TPC 2)		80		MHz
ENABLE					
Turn-On	Enable High to Output within 0.5 dB of Final Value		2.5		µs
Turn-Off	Enable Low to Supply Current Dropping below 2 mA		1.5		µs
ENBL High Threshold (Logic 1)			$+V_S/2$		V
ENBL Low Threshold (Logic 0)			$+V_S/2$		V
POWER SUPPLIES					
Voltage		2.7		5.5	V
Current Active		50	65	78	mA
Current Standby			70		µA

NOTES

[1]For information on operation below 250 MHz, see Figure 4.

[2]See LO Drive section for more details on input matching.

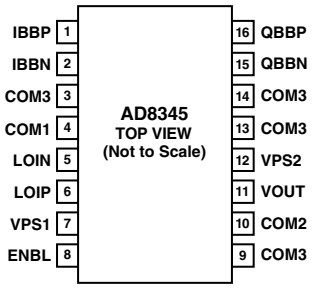
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

Supply Voltage VPS1, VPS2 . . . . . 5.5 V
Input Power LOIP, LOIN (re 50 Ω) . . . . . 10 dBm
IBBP, IBBN, QBBP, QBBN . . . . . 0 V, 2.5 V
Internal Power Dissipation . . . . . 500 mW
θ_{JA} (Exposed Paddle Soldered Down) . . . . . 30°C/W
θ_{JA} (Exposed Paddle not Soldered Down) . . . . . 95°C/W
Maximum Junction Temperature . . . . . 150°C
Operating Temperature Range . . . . . –40°C to +85°C
Storage Temperature Range . . . . . –65°C to +150°C
Lead Temperature Range (Soldering 60 sec) . . . . . 300°C

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PIN CONFIGURATION



CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD8345 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

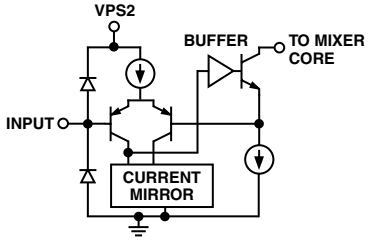
ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD8345ARE	–40°C to +85°C	Tube (16-Lead TSSOP with Exposed Pad)	RE-16
AD8345ARE-REEL		13" Tape and Reel	
AD8345ARE-REEL7		7" Tape and Reel	
AD8345-EVAL		Evaluation Board	

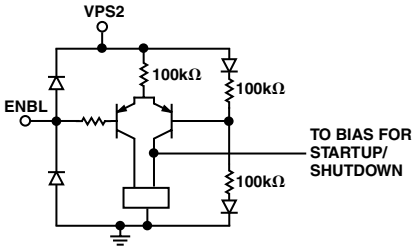
PIN FUNCTION DESCRIPTIONS

Pin No.	Mnemonic	Function	Equivalent Circuit
1, 2	IBBP, IBBN	I Channel Baseband Differential Input Pins. These high impedance inputs should be dc biased to approximately 0.7 V. Nominal characterized ac swing is 0.6 V p-p on each pin (0.4 V to 1 V). This gives a differential drive of 1.2 V p-p. Inputs are not self-biasing so external biasing circuitry must be used in ac-coupled applications.	Circuit A
3, 9, 13, 14	COM3	Ground Pin for Input V-to-I Converters and Mixer Core.	
4	COM1	Ground Pin for the LO Phase-Splitter and LO Buffers.	
5, 6	LOIN, LOIP	Differential LO Drive Pins. Internal dc bias (approximately 1.8 V @ V_S = 5 V) is supplied. Pins must be ac-coupled. Single-ended or differential drive is permissible.	Circuit B
7	VPS1	Power Supply Pin for the Bias Cell and LO Buffers. This pin should be decoupled using local 1000 pF and 0.01 μF capacitors.	
8	ENBL	Enable Pin. A high level enables the device; a low level puts the device in sleep mode.	Circuit C
10	COM2	Ground Pin for the Output Stage of Output Amplifier.	
11	VOUT	50 Ω DC-Coupled RF Output. Pin should be ac-coupled.	Circuit D
12	VPS2	Power supply pin for baseband input voltage to current converters and mixer core. This pin should be decoupled using local 1000 pF and 0.01 μF capacitors.	
15, 16	QBBN, QBBP	Q Channel Baseband Differential Input Pins. Inputs should be dc biased to approximately 0.7 V. Nominal characterized ac swing is 0.6 V p-p on each pin (0.4 V to 1 V). This gives a differential drive level of 1.2 V p-p. Inputs are not self-biasing so external biasing circuitry must be used in ac-coupled applications.	Circuit A

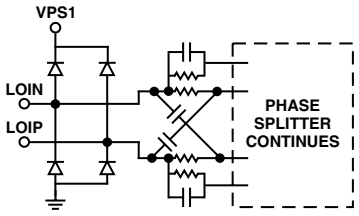
EQUIVALENT CIRCUITS



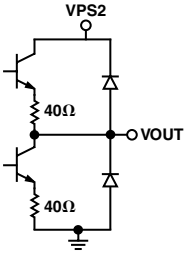
Circuit A



Circuit C

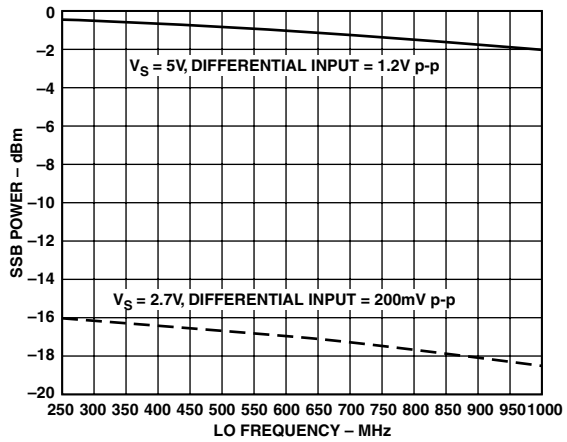


Circuit B

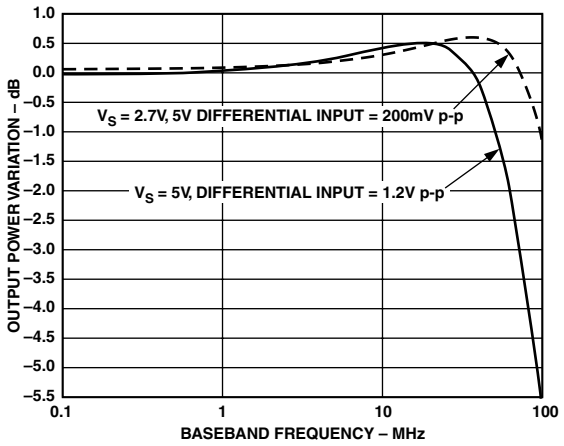


Circuit D

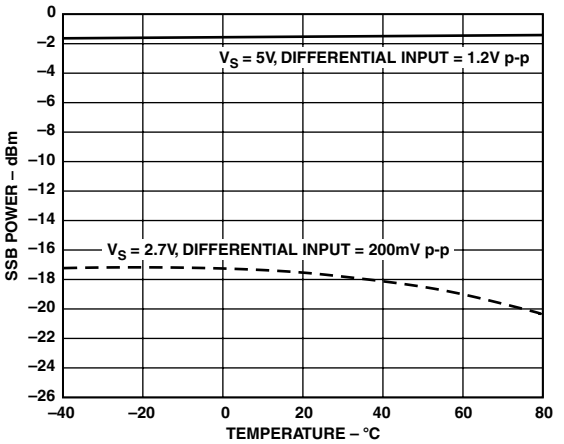
Figure 1. Equivalent Circuits



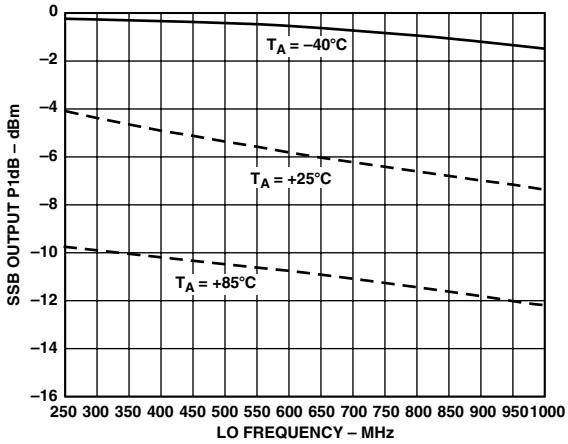
TPC 1. Single Sideband (SSB) Output Power (P_{OUT}) vs. LO Frequency (F_{LO}). (I and Q Inputs Driven in Quadrature at Baseband Frequency (F_{BB}) = 1 MHz; T_A = 25°C)



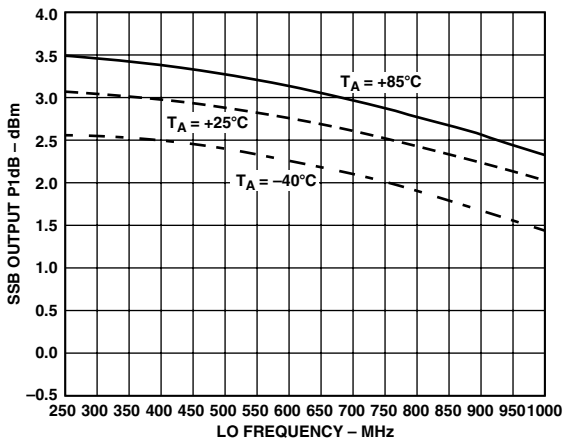
TPC 2. I and Q Input Bandwidth. (T_A = 25°C, F_{LO} = 800 MHz, LO Level = –2 dBm, I and Q Inputs Driven in Quadrature)



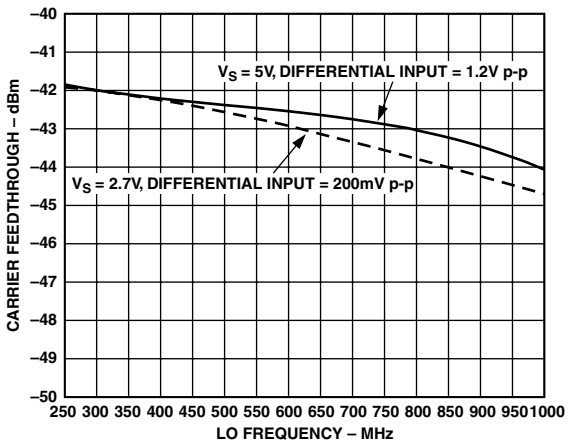
TPC 3. SSB P_{OUT} vs. Temperature. (F_{LO} = 800 MHz, LO Level = –2 dBm, F_{BB} = 1 MHz, I and Q Inputs Driven in Quadrature)



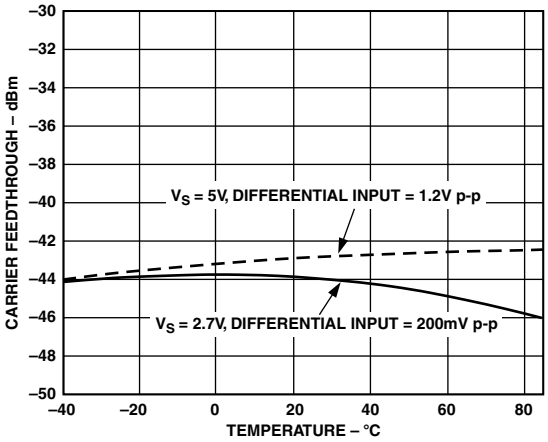
TPC 4. SSB Output 1 dB Compression Point (OP 1 dB) vs. F_{LO}. (V_S = 2.7 V, LO Level = –2 dBm, I and Q Inputs Driven in Quadrature, F_{BB} = 1 MHz)



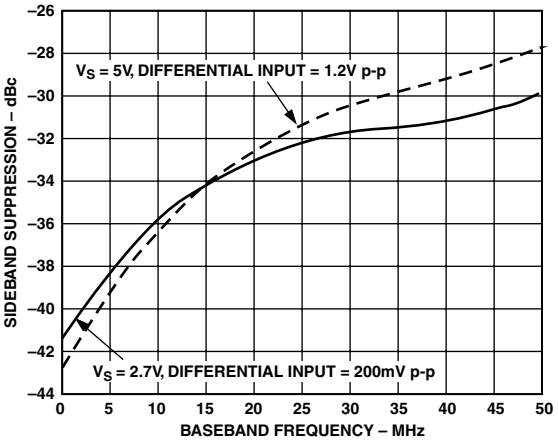
TPC 5. SSB Output 1 dB Compression Point (OP 1 dB) vs. F_{LO}. (V_S = 5 V, LO Level = –2 dBm, I and Q Inputs Driven in Quadrature, F_{BB} = 1 MHz)



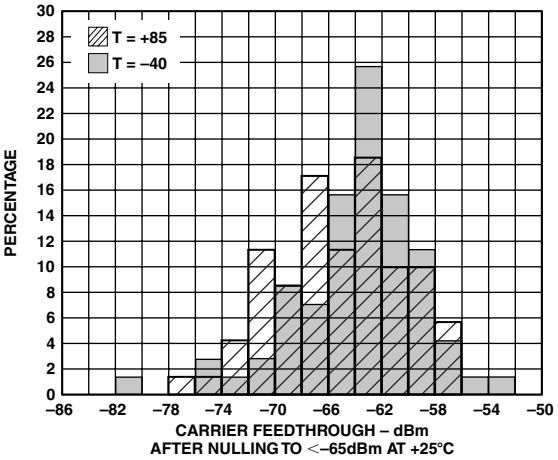
TPC 6. Carrier Feedthrough vs. F_{LO}. (LO Level = –2 dBm, T_A = 25°C)



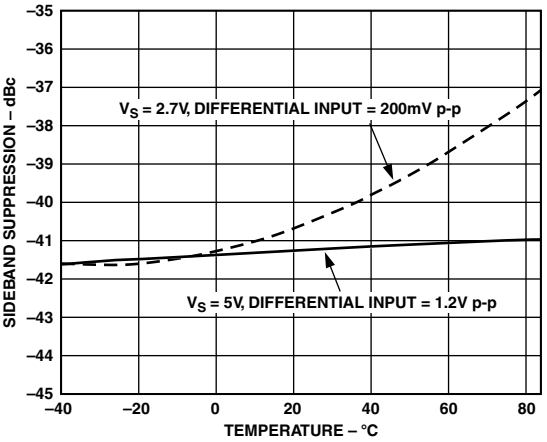
TPC 7. Carrier Feedthrough vs. Temperature. (F_{LO} = 800 MHz, LO Level = –2 dBm)



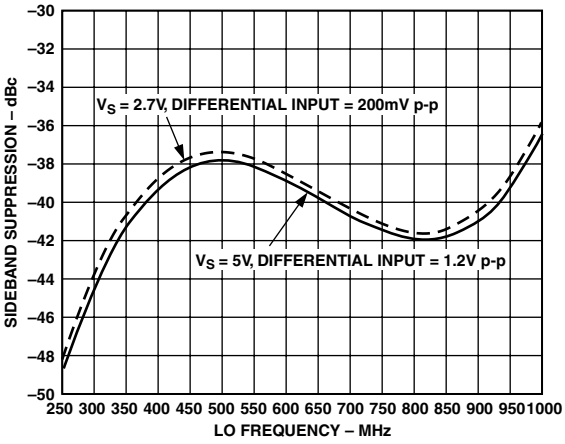
TPC 10. Sideband Suppression vs. F_{BB}. (T_A = 25°C, F_{LO} = 800 MHz, LO Level = –2 dBm, I and Q Inputs Driven in Quadrature)



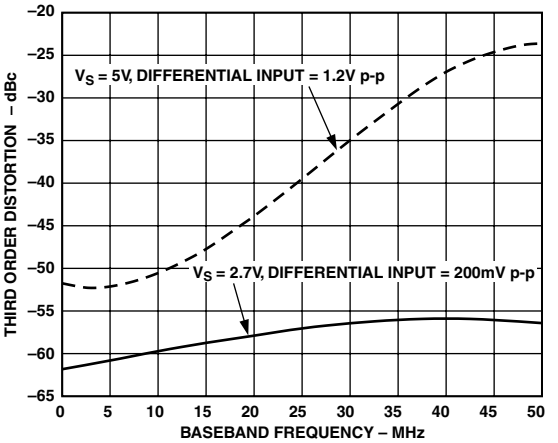
TPC 8. Carrier Feedthrough Distribution at Temperature Extremes. After Feedthrough Nulled to <–65 dBm at T_A = 25°C. (F_{LO} = 800 MHz, LO Level = –2 dBm)



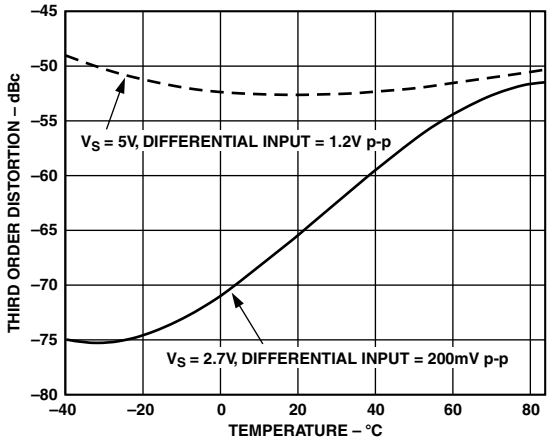
TPC 11. Sideband Suppression vs. Temperature. (F_{LO} = 800 MHz, LO Level = –2 dBm, F_{BB} =1 MHz, I and Q Inputs Driven in Quadrature)



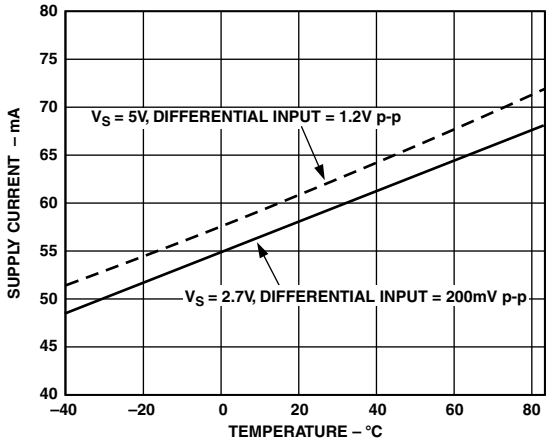
TPC 9. Sideband Suppression vs. F_{LO}. (T_A = 25°C, LO Level = –2 dBm, F_{BB} = 1 MHz, I and Q Inputs Driven in Quadrature)



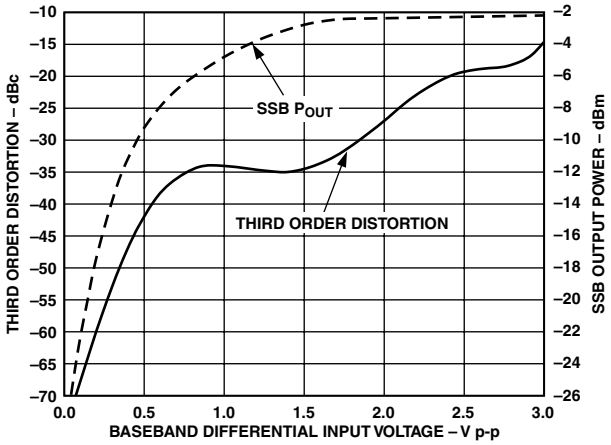
TPC 12. Third Order Distortion vs. F_{BB}. (T_A = 25°C, F_{LO} = 800 MHz, LO Level = –2 dBm, I and Q Inputs Driven in Quadrature)



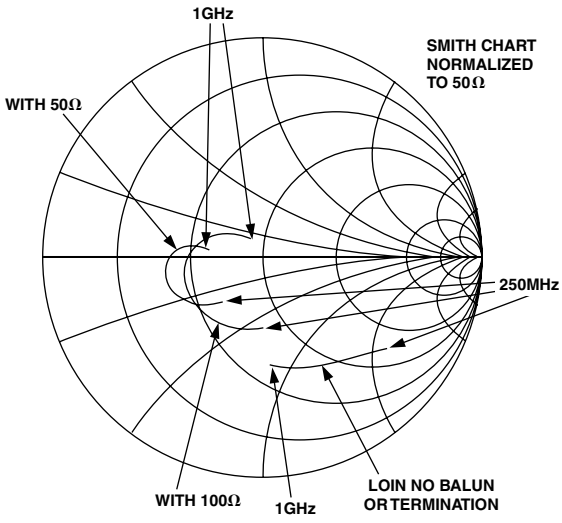
TPC 13. Third Order Distortion vs. Temperature. (F_{LO} = 800 MHz, LO Level = –2 dBm, F_{BB} =1 MHz, I and Q Inputs Driven in Quadrature)



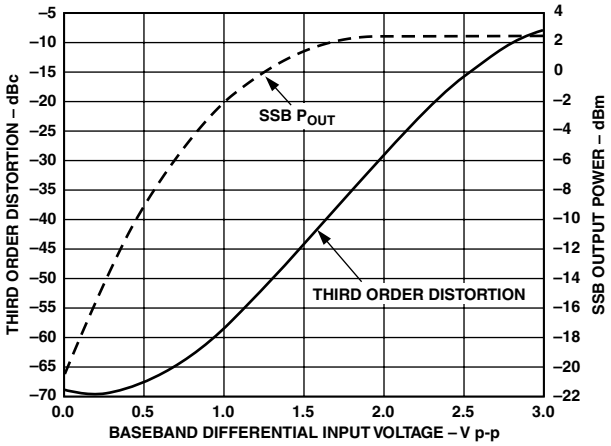
TPC 16. Power Supply Current vs. Temperature



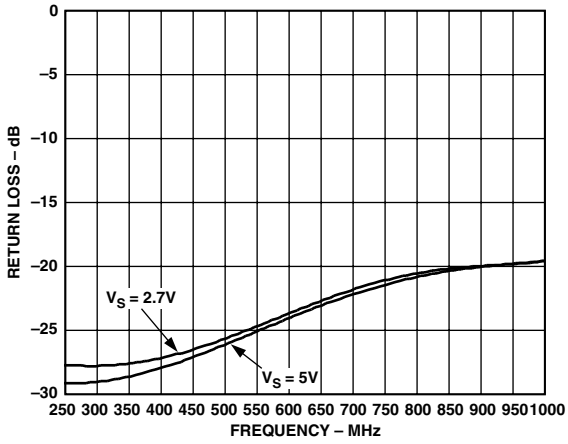
TPC 14. Third Order Distortion and SSB P_{OUT} vs. Baseband Differential Input Level. (T_A = 25°C, F_{LO} = 800 MHz, LO Level = –2 dBm, F_{BB} = 1 MHz, V_S = 2.7 V)



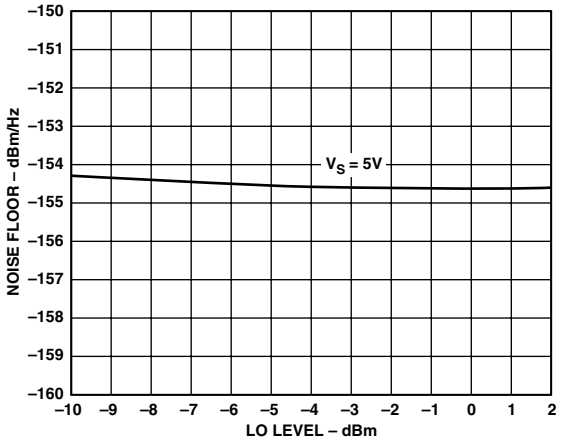
TPC 17. Smith Chart of LOIN Port S11 (LOIP Pin AC-Coupled to Ground). Curves with Balun and External Termination Resistors Also Shown. (V_S = 5 V, T_A = 25°C)



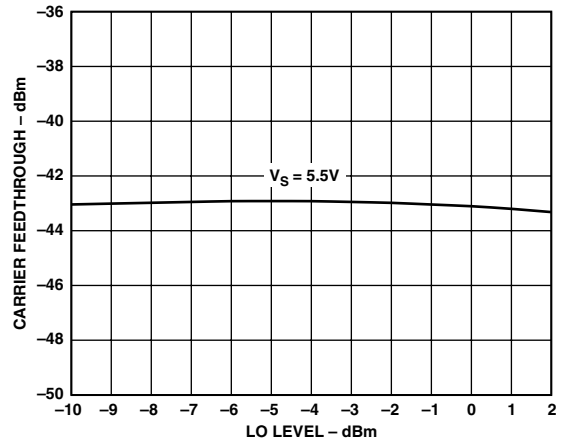
TPC 15. Third Order Distortion and SSB P_{OUT} vs. Baseband Differential Input Level. (T_A = 25°C, F_{LO} = 800 MHz, LO level = –2 dBm, F_{BB} = 1 MHz, V_S = 5 V)



TPC 18. Return Loss (S22) of VOUT Output (T_A = 25°C)



TPC 19. Noise Floor vs. LO Input Power. (T_A = 25°C, F_{LO} = 800 MHz, V_S = 5 V, All I and Q Inputs are DC-Biased to 0.7 V) Noise Measured at 20 MHz Offset from Carrier



TPC 20. LO Feedthrough vs. LO Input Power. (T_A = 25°C, LO = 800 MHz, V_S = 5.5 V)

CIRCUIT DESCRIPTION

Overview

The AD8345 can be divided into the following sections: Local Oscillator (LO) Interface, Mixer, Differential Voltage-to-Current (V-to-I) Converter, Differential-to-Single-Ended (D-to-S) Converter, and Bias. A block diagram of the part is shown in Figure 2.

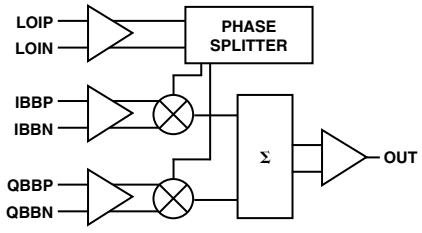


Figure 2. AD8345 Block Diagram

The LO Interface generates two LO signals at 90 degrees of phase difference with each other, to drive two mixers in quadrature. Baseband signals are converted into current form in the Differential V-to-I Converters, feeding into the two mixers. The outputs of the mixers are combined to feed the Differential-to-Single-Ended Converter, which provides a 50 Ω output interface. Bias currents to each section are controlled by the Enable (ENBL) signal. Detailed description of each section follows.

LO Interface

The LO Interface consists of interleaved stages of polyphase phase-splitters and buffer amplifiers. The polyphase phase-splitter contains resistors and capacitors connected in a circular manner to split the LO signal into I and Q paths in precise quadrature with each other. The signal on each path goes through a buffer amplifier to make up for the loss and high frequency roll-off. The two signals then go through another polyphase network to enhance the quadrature accuracy. The broad operating frequency range (250 MHz to 1000 MHz) is achieved by staggering the RC time constants of each stage of the phase-splitters. The outputs of the second phase-splitter are fed into the driver amplifiers for the mixers' LO inputs.

Differential V-to-I Converter

In this circuit, each baseband input pin is connected to an op amp driving a transistor connected as an emitter follower. A resistor between the two emitters maintains a varying current proportional to the differential input voltage through the transistor. These currents are fed to the two mixers in differential form.

Mixers

There are two double-balanced mixers, one for the In-phase Channel (I-Channel) and one for the Quadrature Channel (Q-Channel). Each mixer uses the Gilbert-cell design with four cross-connected transistors. The bases of the transistors are driven by the LO signal of the corresponding channel. The output currents from the two mixers are summed together in two load resistors. The signal developed across the load resistors is sent to the D-to-S stage.

Differential to Single-Ended Converter

The differential-to-single-ended converter consists of two emitter followers driving a totem-pole output stage whose output impedance is established by the emitter resistors in the output transistors. The output of this stage is connected to the output (VOUT) pin.

Bias

A bandgap reference circuit based on the Δ-VBE principle generates the Proportional-To-Absolute-Temperature (PTAT) as well as temperature-stable currents used by the different sections as references. When the bandgap reference is disabled by pulling down the voltage at the ENBL pin, all other sections are shut off accordingly.

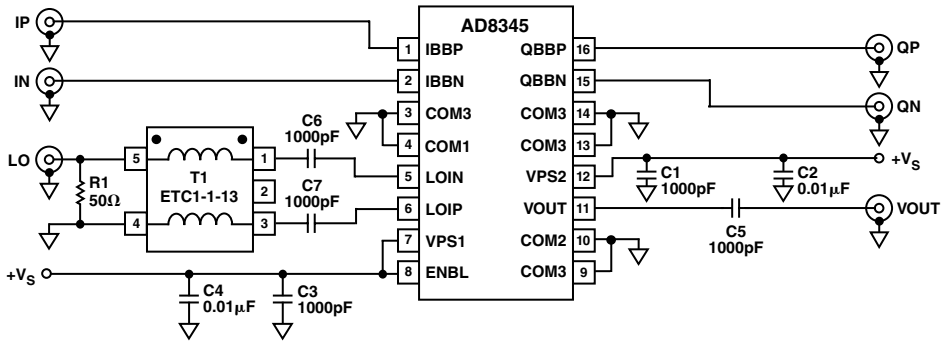


Figure 3. Basic Connections

BASIC CONNECTIONS

The basic connections for operating the AD8345 are shown in Figure 3. A single power supply of between 2.7 V and 5.5 V is applied to pins VPS1 and VPS2. A pair of ESD protection diodes are connected internally between VPS1 and VPS2 so these must be tied to the same potential. Both pins should be individually decoupled using 1000 pF and 0.01 µF capacitors, located as close as possible to the device. For normal operation, the enable pin, ENBL, must be pulled high. The turn-on threshold for ENBL is $V_S/2$. Pins COM1 to COM3 should all be tied to the same low impedance ground plane.

LO Drive

In Figure 3, a 50 Ω resistor to ground combines with the device's high input impedance to provide an overall input impedance of approximately 50 Ω (see TPC 17 for a plot of LO port input impedance). For maximum LO suppression at the output, a differential LO drive is recommended. In Figure 3, this is achieved using a balun (M/A-COM Part Number ETC1-1-13).

The output of the balun is ac coupled to the LO inputs which have a bias level about 1.8 V dc. An LO drive level of –2 dBm is recommended for lowest output noise. Higher levels will degrade linearity while lower levels will tend to increase the noise floor slightly. For example, reducing the LO power from –2 dBm to –10 dBm will increase the noise floor by approximately 0.3 dB (see TPC 19).

The LO terminal can be driven single-ended at the expense of slightly higher LO leakage. LOIN is ac coupled to ground using a capacitor and LOIP is driven through a coupling capacitor from a (single-ended) 50 Ω source (this scheme could also be reversed with the drive signal being applied to LOIN).

LO Frequency Range

The frequency range on the LO input is limited by the internal quadrature phase splitter. The phase splitter generates drive signals for the internal mixers which are 90° out of phase relative to one another. Outside of the specified LO frequency range of 250 MHz to 1 GHz, this quadrature accuracy degrades, resulting in decreased sideband suppression. See TPC 9 for a plot of sideband suppression vs. LO frequency from 250 MHz to 1 GHz. Figure 4 shows the sideband suppression of a typical device from 50 MHz to 300 MHz. The level of sideband suppression degradation below 250 MHz will be subject to manufacturing process variations.

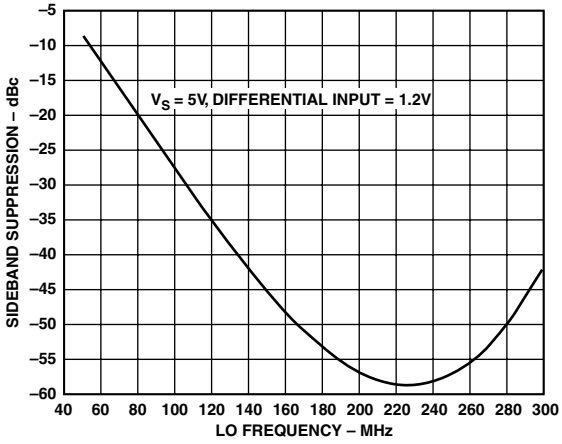


Figure 4. Typical Lower Frequency Sideband Suppression Performance

Baseband I and Q Channel Drive

The I and Q channel baseband inputs should be driven differentially. This is convenient as most modern high-speed DACs have differential outputs. For optimal performance at V_S = 5 V, the drive signal should be a 1.2 V p-p differential signal with a bias level of 0.7 V; that is, each input should swing from 0.4 V to 1 V. If the AD8345 is being run on a lower supply voltage, the peak-to-peak voltage on the I and Q channel inputs must be reduced to avoid input clipping. For example, at a supply voltage of 2.7 V, a 200 mV p-p differential drive is recommended. This will result in a corresponding reduction in output power (see TPC 1). The I and Q inputs have a large input bandwidth of approximately 80 MHz. At lower baseband input levels, the input bandwidth increases (see TPC 2).

If the baseband signal has a high peak-to-average ratio (e.g., CDMA or WCDMA), the rms signal strength will have to be backed off from this peak level in order to prevent clipping of the signal peaks. Clipping of signal peaks will tend to increase signal leakage into adjacent channels. Backing off the I and Q signal strength in the manner recommended will reduce the output power by a corresponding amount. This also applies to multicarrier applications where the per-carrier output power will be lower by 3 dB for each doubling of the number of output carriers.

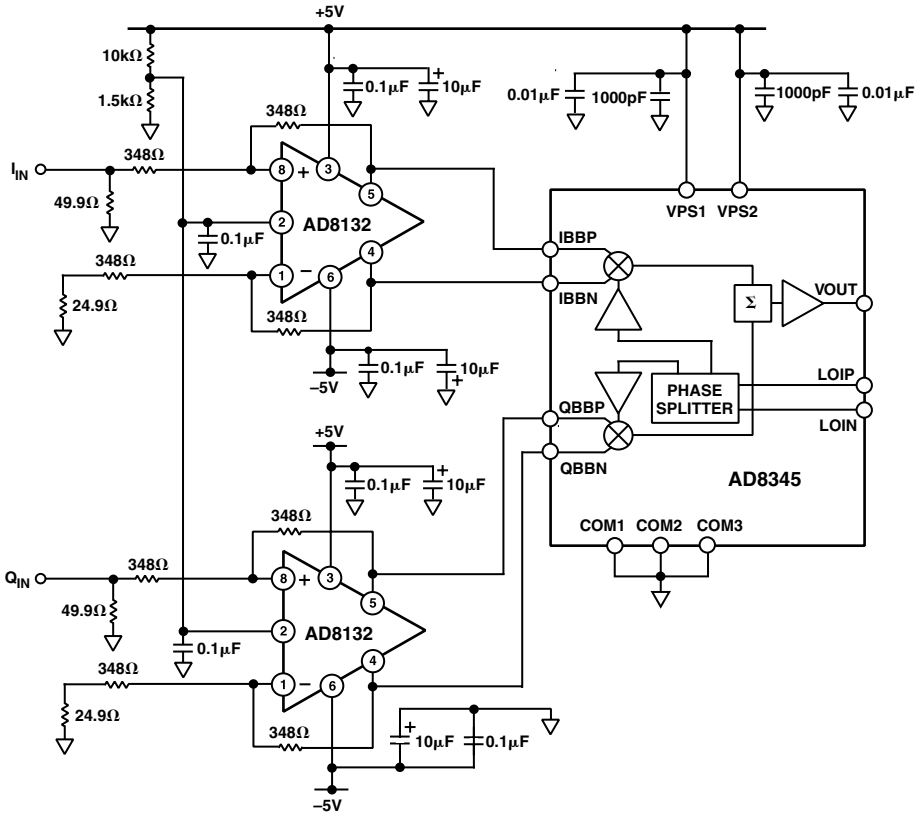


Figure 5. Single-Ended IQ Drive Circuit

The I and Q inputs have high input impedances because they connect directly to the bases of pnp transistors. If a (dc-coupled) filter is being used between a DAC and the modulator inputs, this filter will need to be terminated with the appropriate resistance. If the filter is differential, the termination resistor should be connected across the I and Q differential inputs.

Reduction of LO Leakage

Because the I and Q signals are being effectively multiplied with the LO, any internal offset voltages on these inputs will result in leakage of the LO. The nominal LO leakage of –42 dBm which results from these internal offset voltages, can be reduced further by applying offset compensation voltages on the I and Q inputs. (Note that LO feedthrough is reduced by varying the differential offset voltages on the I and Q inputs, not by varying the nominal bias level of 0.7 V.) This is easily accomplished by programming (and then storing) the appropriate DAC offset code to reduce the LO leakage. This does, however, require the path from the DAC to the I and Q inputs to be dc-coupled. (DC-coupling is also advantageous from the perspective of I and Q input biasing if the DAC is capable of delivering a bias level of 0.7 V).

The procedure for reducing the LO feedthrough is simple. In order to isolate the LO in the output spectrum, a single sideband configuration is recommended (set I and Q signals to sine and cosine waves at, say, 100 kHz, set LO to F_{RF} – 100 kHz). An offset voltage is applied from the I DAC until the LO leakage reaches a trough. With this offset level held, an offset voltage is applied to the Q DAC until a (lower) trough is reached.

LO leakage compensation holds up well over temperature. TPC 8 shows the effect of temperature on LO leakage after compensation at ambient.

Compensated LO leakage will degrade somewhat as the frequency is moved away from the frequency at which the compensation was performed. This is due to the effects of LO to RF output leakage which are not a result of offsets on the I and Q inputs.

Single-Ended I and Q Drive

Where only single-ended I and Q signals are available, a differential amplifier such as the AD8132 or AD8138 can be used to generate the required differential drive signal for the AD8345.

Even though most DACs have differential outputs, using a single-ended low-pass filter between the dual DAC and the I and Q inputs, may be more desirable from the perspective of component count and cost. As a result, the output signal from the filter must be converted back to differential mode and possibly be rebiased to 0.7 V common mode.

Figure 5 shows a circuit which converts a ground-referenced, single-ended signal to a differential signal and adds the required 0.7 V bias voltage. Two AD8132 differential op amps, configured for a gain of unity, are used. With a 50 Ω input impedance, this circuit is configured to accept a signal from a 50 Ω source (e.g., a low-pass filter). The input impedance can be easily changed by replacing the 49.9 Ω shunt resistor (and the corresponding 24.9 Ω resistor on the inverting input) with the appropriate value. The required dc-bias level is conveniently added to the signal by applying 0.7 V to the V_{OCM} pins of the differential amplifiers.

Differential amplifiers such as the AD8132 and AD8138 can also be used to implement active filters. For more information on this topic, consult the data sheets of these devices.

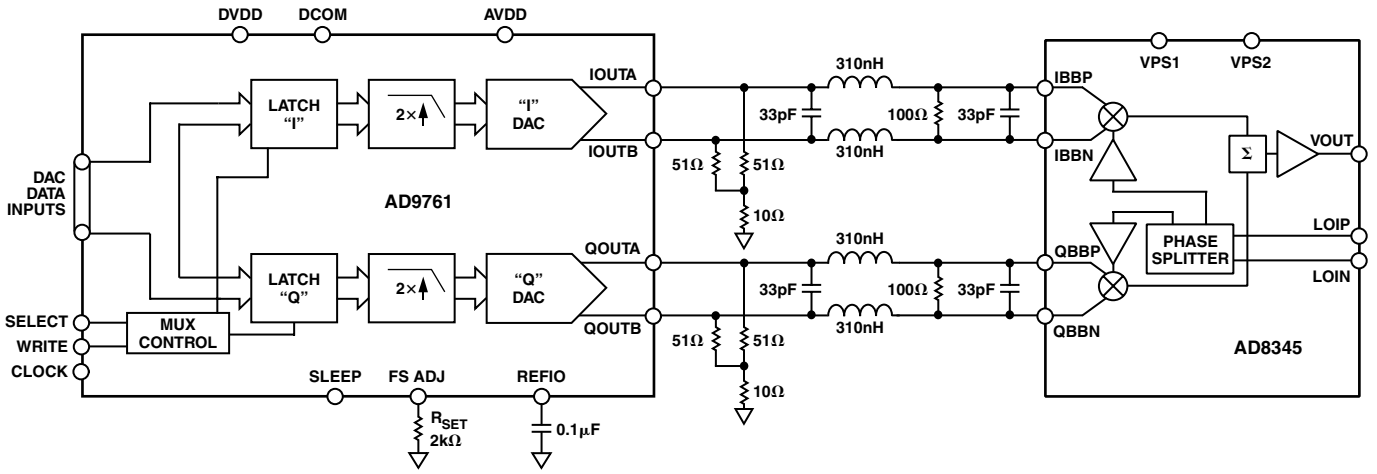


Figure 6. AD8345/TxDAC Interface

Note that this circuit assumes that the single-ended I and Q signals are ground referenced. Any differential dc-offsets will result in increased LO Leakage at the output of the AD8345.

It is possible to drive the baseband inputs with a single-ended signal biased to 0.7 V, with the unused inputs being biased to a dc level of 0.7 V. However, this mode of operation is not recommended because any dc level difference between the bias level of the drive signal and the dc level on the unused input (including the effect of temperature drift) will result in increased LO leakage. In addition, the maximum output power will be reduced by 6 dB.

RF Output

The RF output is designed to drive a 50 Ω load but should be ac coupled as shown in Figure 3. If the I and Q inputs are driven in quadrature by 1.2 V p-p signals, the resulting output power will be approximately –1 dBm (see TPC 1).

The RF output impedance is very close to 50 Ω. As a result, no additional matching circuitry is required if the output is driving a 50 Ω load.

Application with TxDAC

Figure 6 shows the AD8345 driven by the AD9761 TxDAC (any of the devices in ADI's TxDAC family can also be used in this application). The signal from the DAC is being filtered by a differential 51 MHz low-pass filter.

The I and Q DACs generate differential output currents of 0 mA to 20 mA and 20 mA to 0 mA, respectively. When loaded with 50 Ω ground-referenced resistors, this would produce a 2 V p-p differential signal (i.e., 1 V p-p on each output) with a common-mode level of 0.5 V. In the configuration shown, each DAC output sees a composite load of 48 Ω (10 Ω + 51 Ω‖(100 Ω + 51 Ω)) in the passband. So, for example, when IOUTA is driven to its positive full scale, IBBP will be equal to 0.96 V. With IOUTB at 0 mA, the voltage at IBBN will be equal to 0.456 V. This results in a full-scale differential signal of approximately 1 V p-p which will have a common-mode level of 0.7 V.

Soldering Information

The AD8345 is packaged in a 16-lead TSSOP package with exposed pad. For optimum thermal conductivity, the exposed pad can be soldered to the exposed metal of a ground plane. This results in a junction-to-air thermal impedance (θ_{JA}) of 30°C/W. However, soldering is not necessary for safe operation. If exposed pad is not soldered down, the θ_{JA} is equal to 95°C/W.

Evaluation Board

Figure 7. Shows the schematic of the AD8345 evaluation board. Note that uninstalled components are marked as open. This is a 4-layer board, with the two center layers used as ground plane and top and bottom layers used as signal and power planes.

The board is powered by a single supply (V_S) in the range, 2.7 V to 5.5 V. The power supply is decoupled by a 0.01 μF and 1000 pF capacitors. The circuit closely follows the basic connection schematic with SW1 in B Position. If SW1 is in Position A, the Enable pin will be pulled to ground by a 10 kΩ resistor and the device will be in its power-down mode.

All connectors are SMA-type. The I and Q inputs are dc-coupled to allow a direct connection to a dual DAC with differential outputs. Resistor pads are provided in case termination at the I and Q inputs is required. The local oscillator input (LO) is terminated to approximately 50 Ω with an external 50 Ω resistor to ground. A 1:1 wide-band transformer (ETC1-1-13) provides a differential drive to the AD8345's differential LO input. The device can also be driven single-ended by shorting out T1.

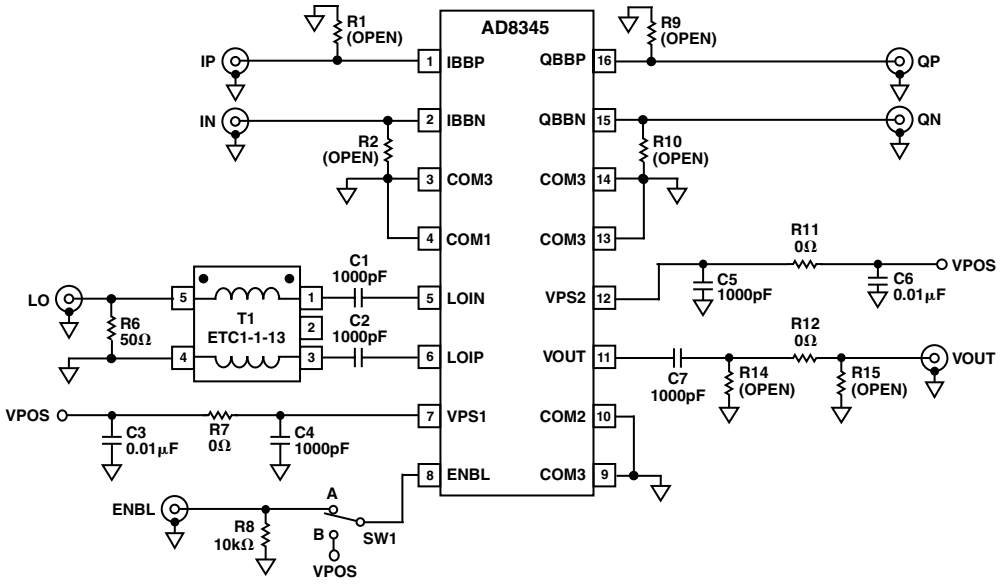


Figure 7. Evaluation Board Schematic

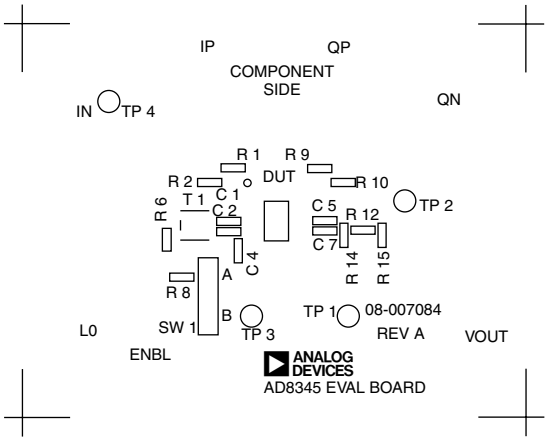


Figure 8. Evaluation Board Silkscreen

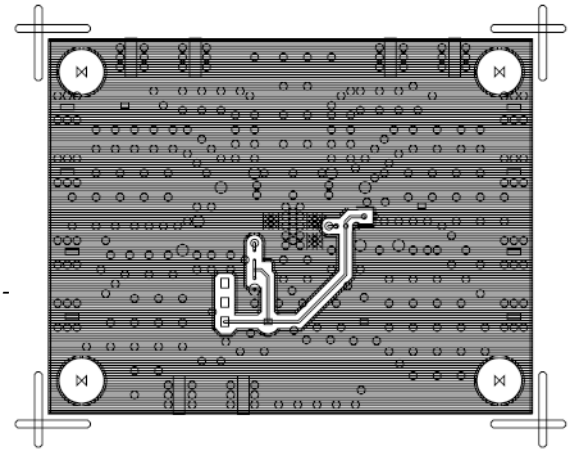


Figure 10. Layout of Evaluation Board, Bottom Layer

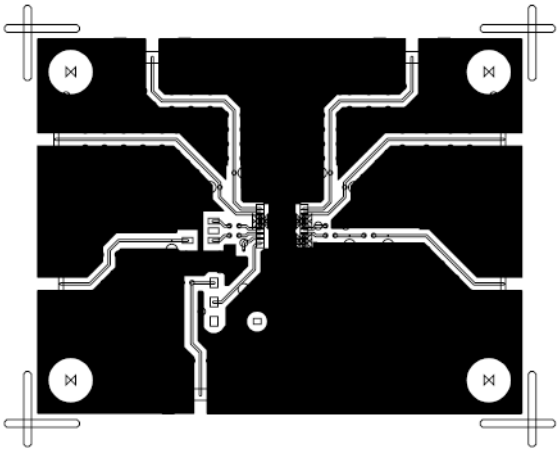


Figure 9. Layout of Evaluation Board, Top Layer

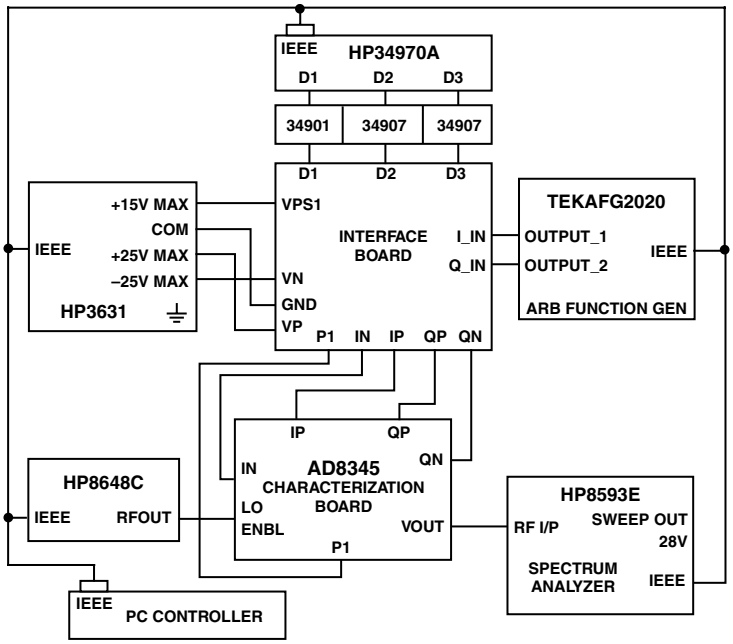


Figure 11. Characterization Board SSB Test Setup

CHARACTERIZATION SETUPS

SSB Setup

Essentially, two primary setups were used to characterize the AD8345. These setups are shown in Figures 11 and 13. Figure 11 shows the setup used to evaluate the product as a Single Sideband modulator. The interface board converts the single-ended I and Q inputs from the arbitrary function generator to differential inputs with a dc bias of approximately 0.7 V. The interface board also provides connections for power supply routing. The HP34970A and its associated plug-in 34901 were used to monitor power supply currents and voltages being supplied to the AD8345 characterization board. Two HP34907 plug-ins were used to provide additional miscellaneous dc and control signals to the interface board. The LO input was driven directly by an RF signal generator and the output was measured directly with a spectrum analyzer. With the I Channel driven with a sine wave and the Q Channel driven with a cosine wave, the lower sideband is the single sideband output. The typical SSB output spectrum is shown in Figure 12.

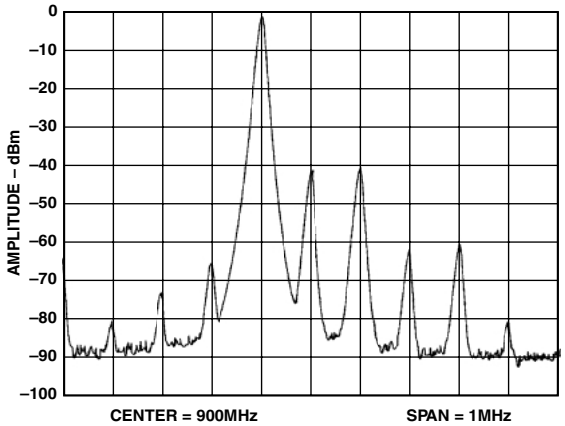


Figure 12. Typical SSB Output Spectrum

Modulated Waveform Setup

For evaluating the AD8345 with modulated waveforms, the setup shown in Figure 13 was used. A Rohde & Schwarz AMIQ signal generator with differential outputs was used to generate the baseband signals. For all measurements the input level on each baseband input pin was 0.7 V ± 0.3 V peak. The output was measured with a Rohde & Schwarz FSIQ spectrum/vector analyzer.

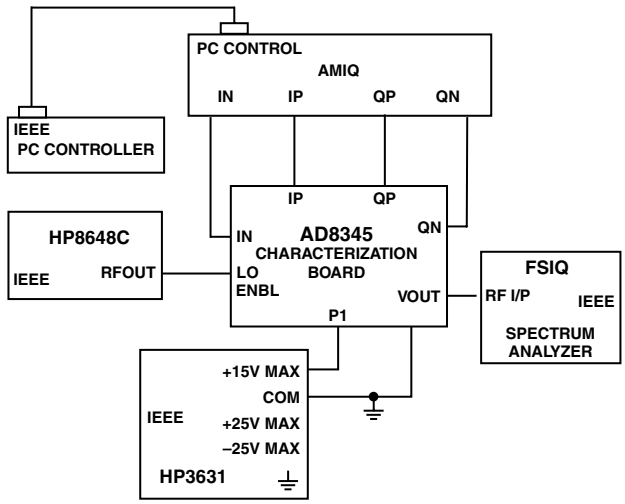


Figure 13. Test Setup for Evaluating AD8345 with Modulated Waveforms

CDMA IS95

For measuring ACPR, the I and Q input signals used were generated with Pilot (Walsh Code 00), Sync (WC 32), Paging (WC 01), and 6 Traffic (WC 08, 09, 10, 11, 12, 13) channels active. Figure 14 shows the typical output spectrum for this configuration.

For performing EVM, Rho, phase, and amplitude balance measurements, the I and Q input signals used were generated with only the Pilot Channel (Walsh Code 00) active.

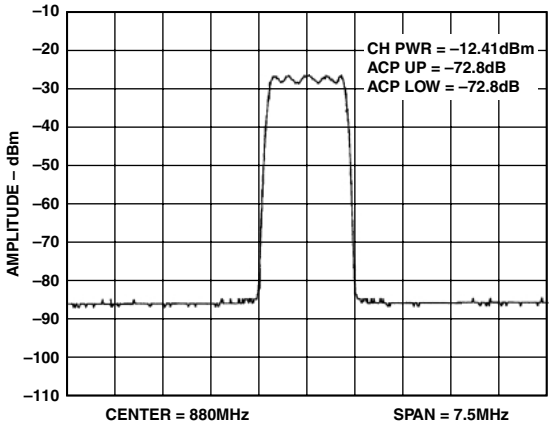


Figure 14. Typical IS95 Output Spectrum

WCDMA 3GPP

For evaluating the AD8345 for WCDMA, the 3GPP standard was used with a Chip Rate of 3.84 MHz. The plot in Figure 15 is an ACPR plot of the AD8345 using "Test Model 1" from the 3GPP specification with 64 channels active.

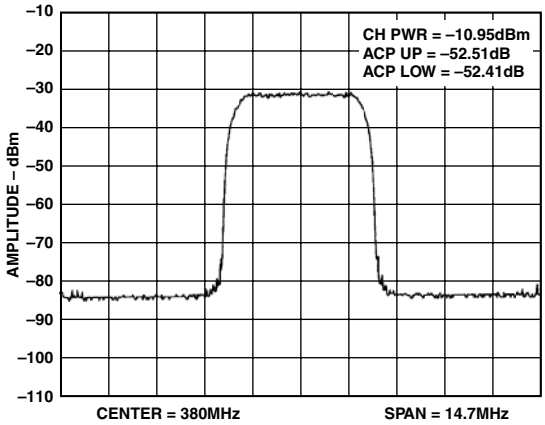


Figure 15. Typical AD8345 WCDMA 3GPP Output Spectrum

GSM

For comparing the AD8345 output to the GSM transmit mask I and Q signals were generated using MSK modulation, GSM differential coding, a Gaussian filter and a symbol rate of 270.833 kHz. The transmit mask was manually generated on the FSIQ using the GSM BTS specification for reference. The plot in Figure 16 shows that the AD8345 meets the GSM transmit mask requirements.

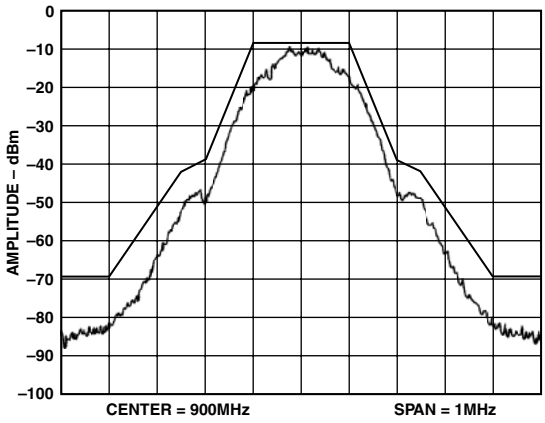
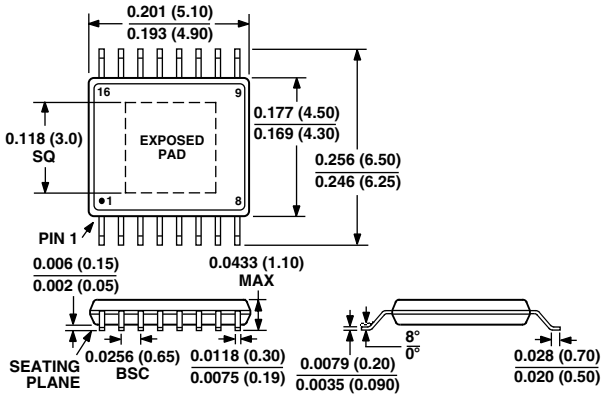


Figure 16. Typical AD8345 GSM Output Spectrum

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

16-Lead HTSSOP with Exposed Pad
(RE-16)



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