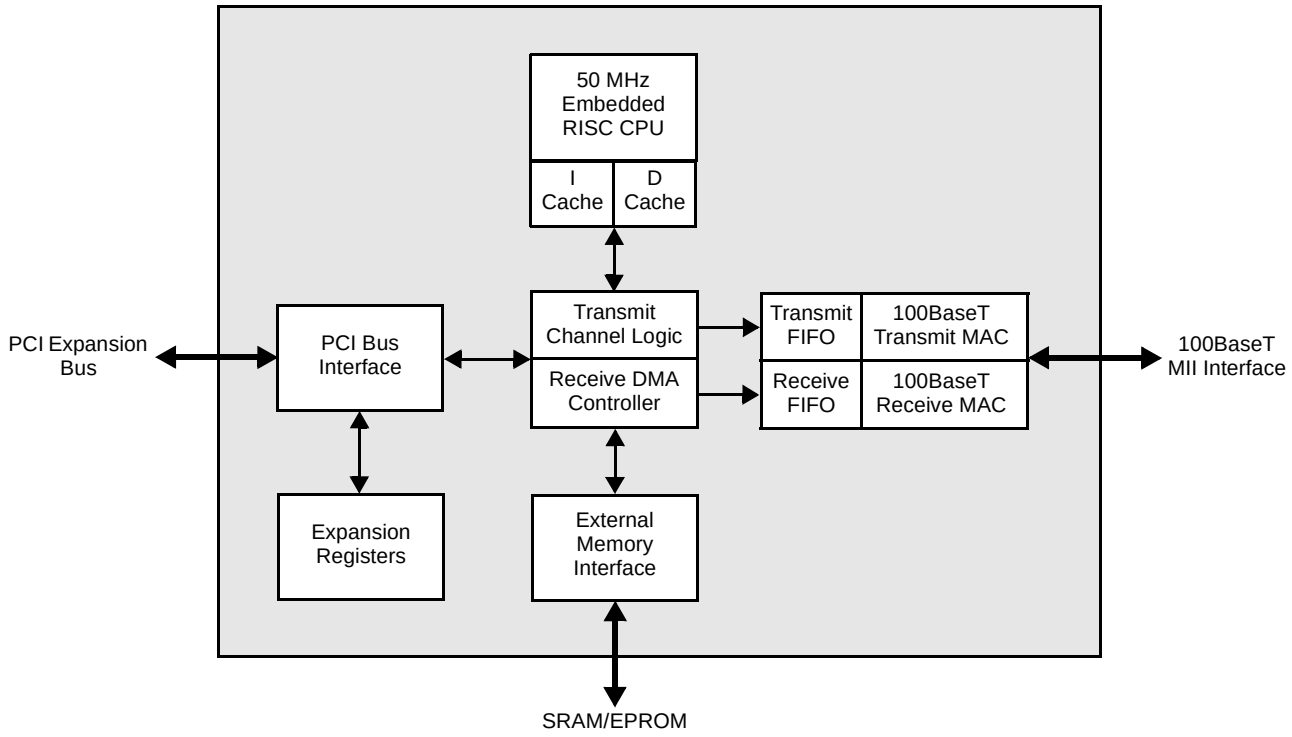
# Single-Port 10/100 Mbit/s Ethernet Switch

## FEATURES

- Single-chip, 1-port, full-duplex or half-duplex, 10/100BaseT switching device for low-cost unmanaged and managed networks.
- On-chip SmartPath™ 50 MHz RISC CPU core, multi-channel DMA controller, MAC-layer interface logic, FIFOs, PCI-based expansion port, and a flexible memory controller.
- CPU supports background applications running on local OS (e.g., SNMP), and real-time data-oriented applications (e.g., packet forwarding and filtering decisions).
- Performs packet switching at a rate of 200 Mbit/s (full-duplex) or 100 Mbit/s (half-duplex).
- Fully compatible with the PM3350 8-port 10 Mbit/s switch device; may be used to create a compact and inexpensive mixed 10/100 Mbit/s switching hub.
- Filtering and switching at wire rates (up to 148,8000 packets per second), supporting a mix of Ethernet and IEEE 802.3 protocols.
- Expansion port supports a peak system bandwidth of 1 Gbit/s, and is compatible with industry-standard PCI bus (version 2.1).
- Performs all address learning, address table management, and aging functions for up to 32,768 MAC addresses (limited by external memory). Address learning rate of up to 10,000 addresses per second.
- Maximum broadcast/multicast at wire rates with configurable broadcast storm rate limiting.
- Low-latency operation in both unicast and broadcast modes.
- Configuration, management, MIB statistics, and diagnostics available in-band.
- Store-and-forward operation with full error checking and filtering.
- Flow control supported for both full-duplex and half-duplex operation; supports IEEE 802.3x PAUSE frame flow control in full-duplex mode, and supports user-enabled backpressure flow control in half-duplex mode.
- Maintains and collects per-port and per-host statistics at wire rates.
- Interfaces directly to industry-standard 100 Mbit/s transceivers with no glue logic via the built-in Medium Independent Interface (MII) port with full support for the autonegotiation function implemented by the PHY devices.
- Fully static CMOS operation at 50 MHz clock rates.
- Implemented with a 3.3 V core and a 5 V-compatible I/O.
- Available in a 208-pin PQFP package.

## BLOCK DIAGRAM



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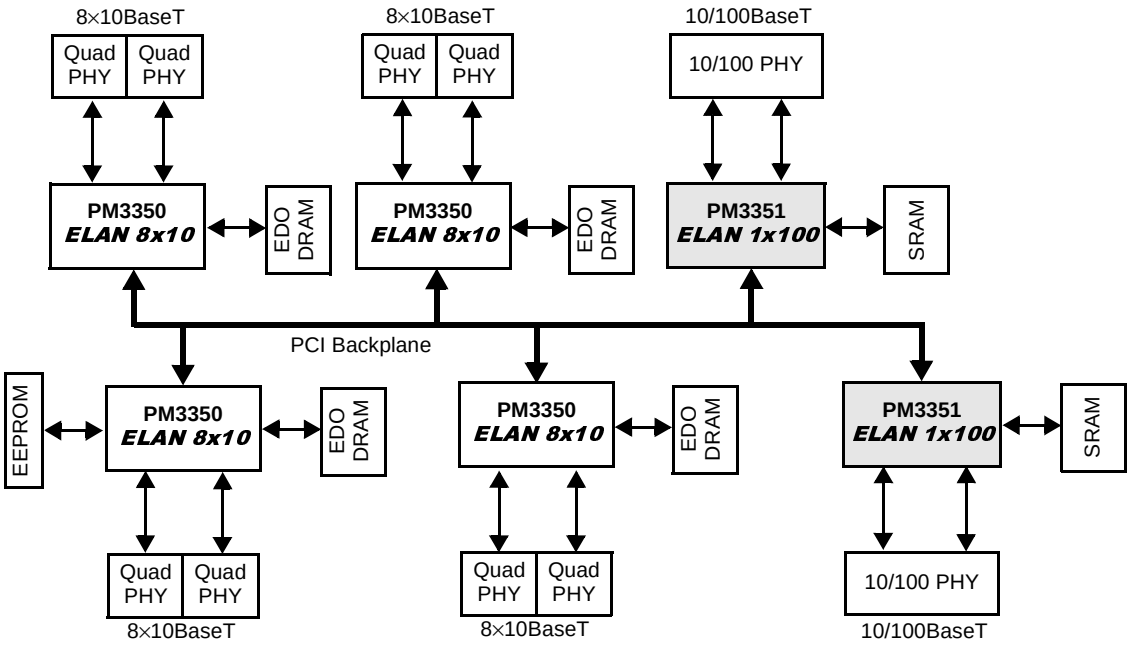
## TYPICAL APPLICATION

### *LOW-COST 10/100 Mbit/s ETHERNET SWITCH*

The ELAN 1×100 chip is used to build low-cost 10/100 Mbit/s switches for server/backbone applications. A switch can be created from the following:

- PM3351s (one for every 100 Mbit/s port required),
- one to seven PM3350s (one for every eight 10 Mbit/s ports required),
- a bank of memory per device (60 ns EDO DRAM for each PM3350,
- 15 ns SRAM for each PM3351) for holding frame buffers and switching tables,
- a single 256k × 8-bit EPROM or EEPROM (initialization, configuration, and SNMP support firmware),
- quad 10BaseT interface adapters (LXT944) for the PM3350s,
- one 100 Mbit/s PHY device per PM3351, and
- appropriate passive components.

A block diagram of a typical 32-port 10BaseT stackable switch with two 10/100 Mbit/s ports is shown. The PCI expansion bus is used to seamlessly connect the ELAN 8×10s and ELAN 1×100s.

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