DATA SHEET

NEC

# MOS FIELD EFFECT POWER TRANSISTORS

# μPA1712

## SWITCHING
## P-CHANNEL POWER MOS FET
## INDUSTRIAL USE

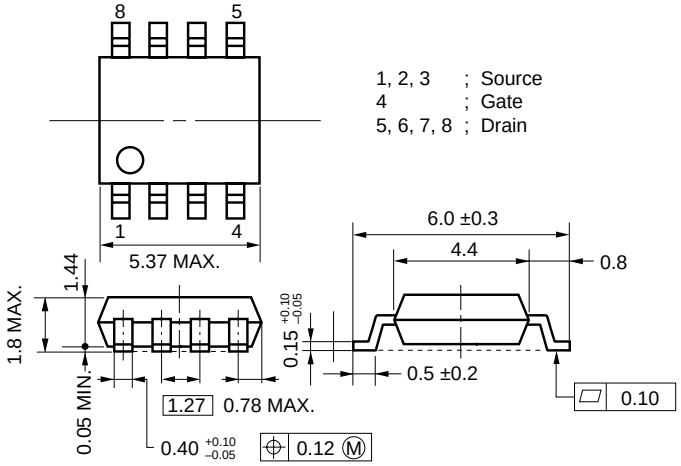
### DESCRIPTION

This product is P-Channel MOS Field Effect Transistor designed for power management applications of notebook computers and Li-ion battery protection circuit.

### FEATURES

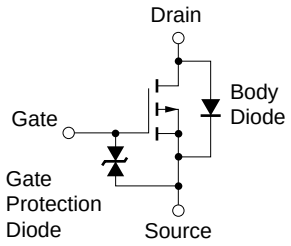
- Low On-Resistance
  $R_{DS(on)1}$ = 20 mΩ MAX. ($V_{GS}$ = –10 V, $I_D$ = –4.0 A)
  $R_{DS(on)2}$ = 48 mΩ MAX. ($V_{GS}$ = –4 V, $I_D$ = –4.0 A)
- Low $C_{iss}$ $C_{iss}$ = 2700 pF TYP.
- Built-in G-S Protection Diode
- Small and Surface Mount Package
  (Power SOP8)

### PACKAGE DIMENSIONS
**(in millimeter)**




### ABSOLUTE MAXIMUM RATINGS ($T_A$ = 25 °C, all terminals are connected)

| | | | |
|---|---|---|---|
| Drain to Source Voltage | $V_{DSS}$ | –30 | V |
| Gate to Source Voltage | $V_{GSS}$ | ∓20 | V |
| Drain Current (DC) | $I_{D(DC)}$ | ∓8.0 | A |
| Drain Current (pulse)[Notes1] | $I_{D(pulse)}$ | ∓32 | A |
| Total Power Dissipation ($T_A$ = 25 °C)[Notes2] | $P_T$ | 2.0 | W |
| Channel Temperature | $T_{ch}$ | 150 | °C |
| Storage Temperature | $T_{stg}$ | –55 to +150 | °C |




**Notes 1.** PW ≤ 10 μs, Duty Cycle ≤ 1 %

**2.** Mounted on ceramic substrate of 1200 mm² × 0.7 mm

The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device acutally used, an addtional protection circuit is externally required if voltage exceeding the rated voltage may be applied to this device.

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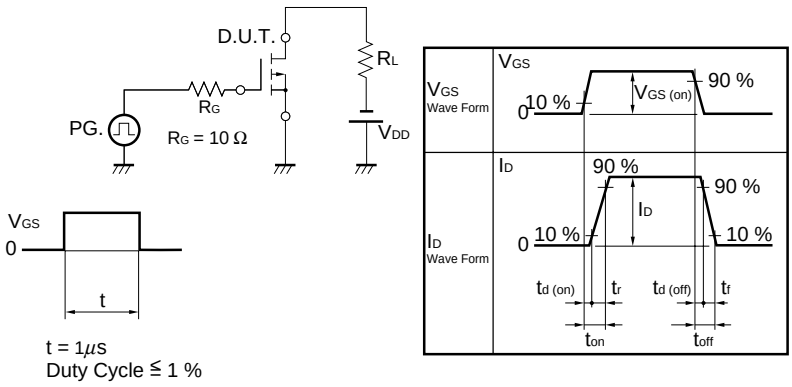
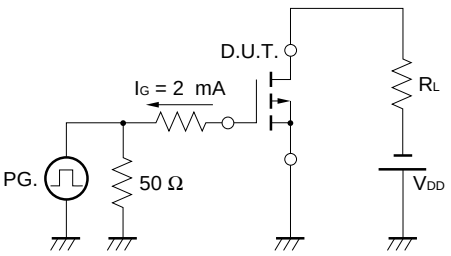
## ELECTRICAL CHARACTERISTICS ($T_A$ = 25 °C, all terminals are connected)

| CHARACTERISTICS | SYMBOL | TEST CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| Drain to Source On-state Resistance | $R_{DS(on)1}$ | $V_{GS}$ = –10 V, $I_D$ = –4.0 A | | 15 | 20 | mΩ |
| | $R_{DS(on)2}$ | $V_{GS}$ = –4 V, $I_D$ = –4.0 A | | 27 | 48 | mΩ |
| Gate to Source Cutoff Voltage | $V_{GS(off)}$ | $V_{DS}$ = –10 V, $I_D$ = –1 mA | –1.0 | –1.7 | –2.5 | V |
| Forward Transfer Admittance | $\|y_{fs}\|$ | $V_{DS}$ = –10 V, $I_D$ = –4.0 A | 6 | 13 | | S |
| Drain Leakage Current | $I_{DSS}$ | $V_{DS}$ = –30 V, $V_{GS}$ = 0 | | | –10 | μA |
| Gate to Source Leakage Current | $I_{GSS}$ | $V_{GS}$ = ∓20 V, $V_{DS}$ = 0 | | | ∓10 | μA |
| Input Capacitance | $C_{iss}$ | $V_{DS}$ = –10 V | | 2700 | | pF |
| Output Capacitance | $C_{oss}$ | $V_{GS}$ = 0 | | 1000 | | pF |
| Reverse Transfer Capacitance | $C_{rss}$ | f = 1 MHz | | 380 | | pF |
| Turn-On Delay Time | $t_{d(on)}$ | $I_D$ = –4.0 A | | 30 | | ns |
| Rise Time | $t_r$ | $V_{GS(on)}$ = –10 V | | 150 | | ns |
| Turn-Off Delay Time | $t_{d(off)}$ | $V_{DD}$ = –15 V | | 250 | | ns |
| Fall Time | $t_f$ | $R_G$ = 10 Ω | | 200 | | ns |
| Total Gate Charge | $Q_G$ | $I_D$ = –8.0 A | | 55 | | nC |
| Gate to Source Charge | $Q_{GS}$ | $V_{DD}$ = –24 V | | 7.5 | | nC |
| Gate to Drain Charge | $Q_{GD}$ | $V_{GS}$ = –10 V | | 14.5 | | nC |
| Body Diode Forward Voltage | $V_{F(S-D)}$ | $I_F$ = 8.0 A, $V_{GS}$ = 0 | | 0.80 | | V |
| Reverse Recovery Time | $t_{rr}$ | $I_F$ = 8.0 A, $V_{GS}$ = 0 | | 60 | | ns |
| Reverse Recovery Charge | $Q_{rr}$ | di/dt = 50 A/μs | | 40 | | nC |

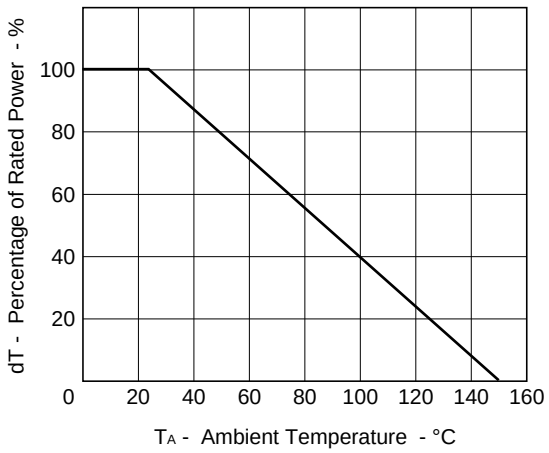
**Test Circuit 1 Switching Time**



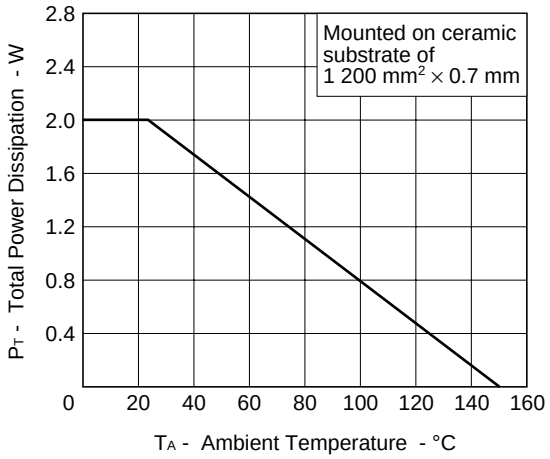

**Test Circuit 2 Gate Charge**



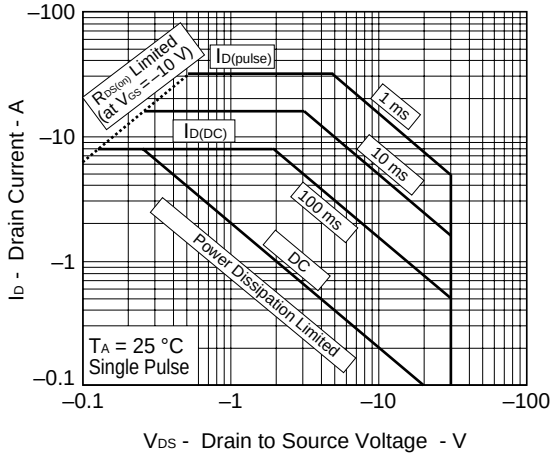
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA




TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE

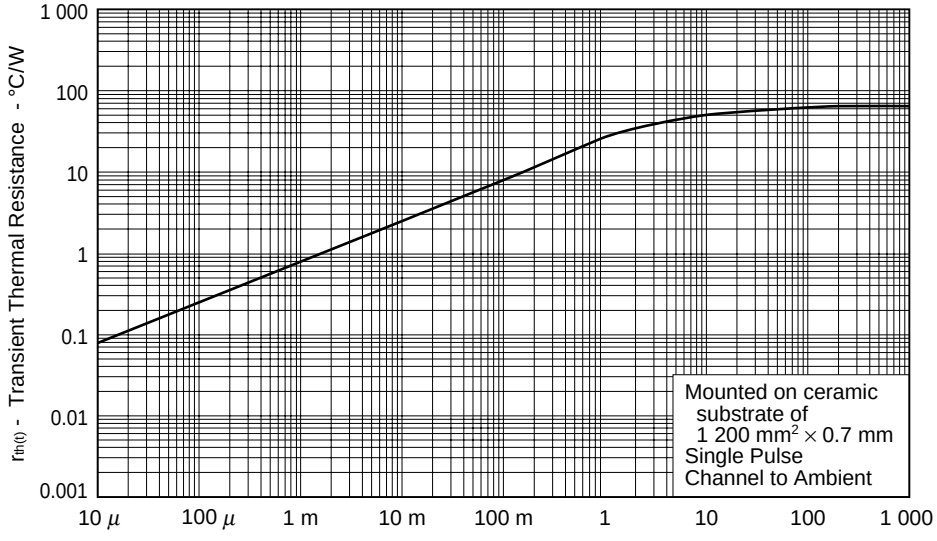



FORWARD BIAS SAFE OPERATING AREA

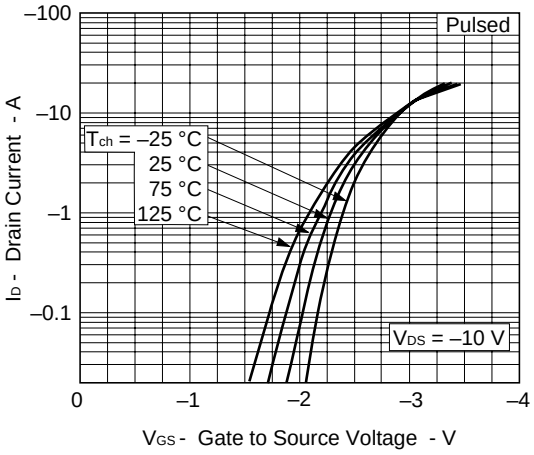



Note:
Mounted on ceramic substrate of 1 200 mm² × 0.7 mm

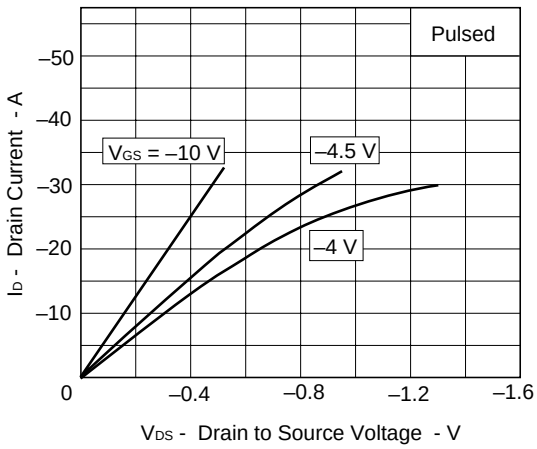
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



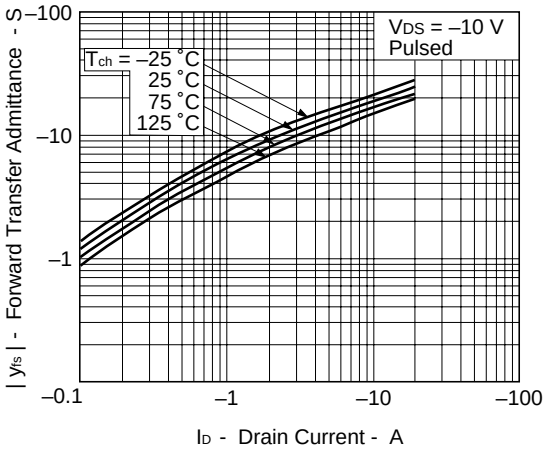
FORWARD TRANSFER CHARACTERISTICS



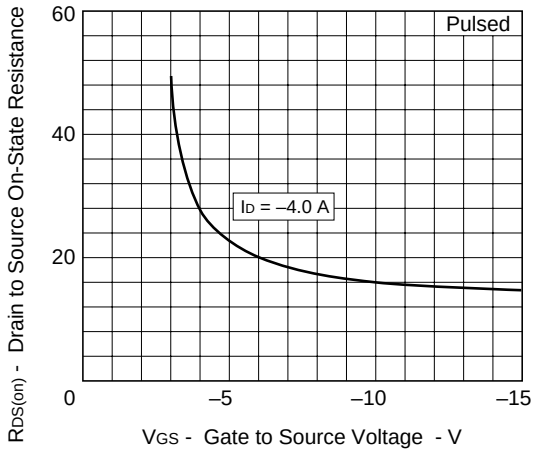

DRAIN CURRENT vs.
DRAIN TO SOURCE VOLTAGE



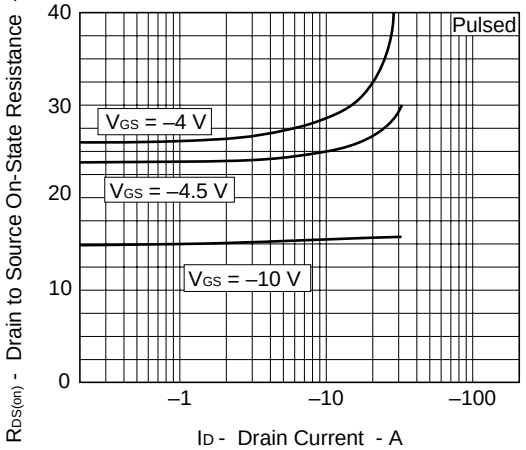

FORWARD TRANSFER ADMITTANCE vs.
DRAIN CURRENT



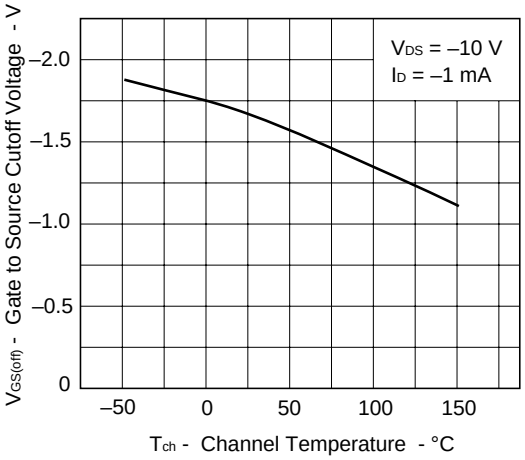

DRAIN TO SOURCE ON-STATE RESISTANCE vs.
GATE TO SOURCE VOLTAGE



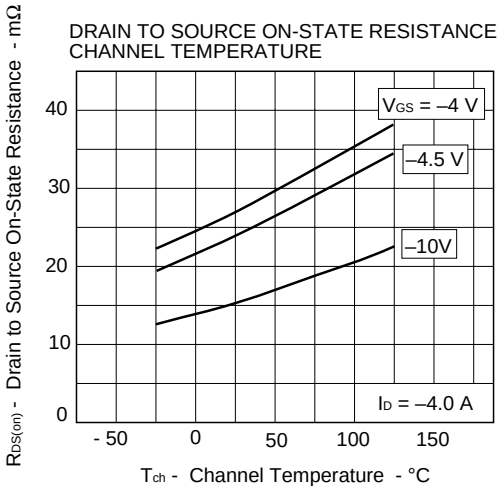

DRAIN TO SOURCE ON-STATE
RESISTANCE vs. DRAIN CURRENT



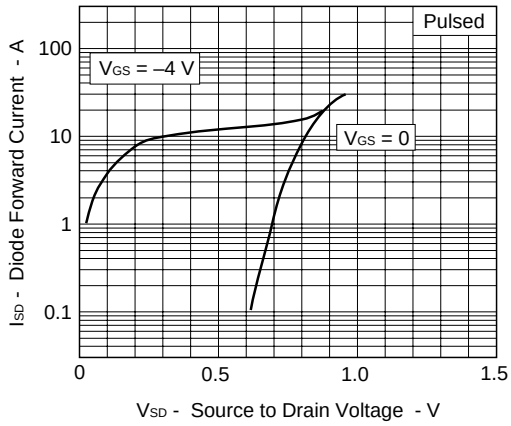

GATE TO SOURCE CUTOFF VOLTAGE vs.
CHANNEL TEMPERATURE



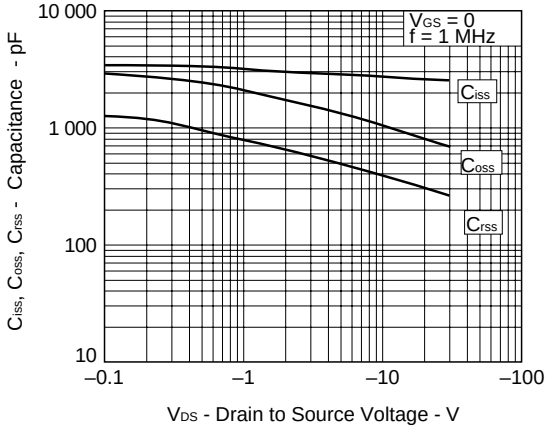
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



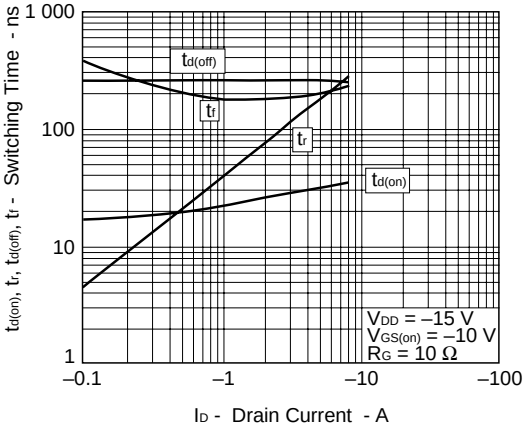

SOURCE TO DRAIN DIODE FORWARD VOLTAGE



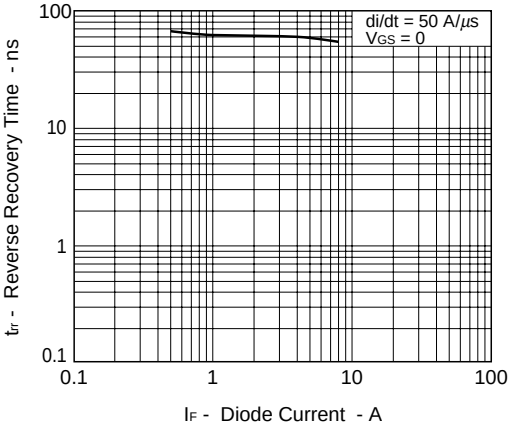

CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



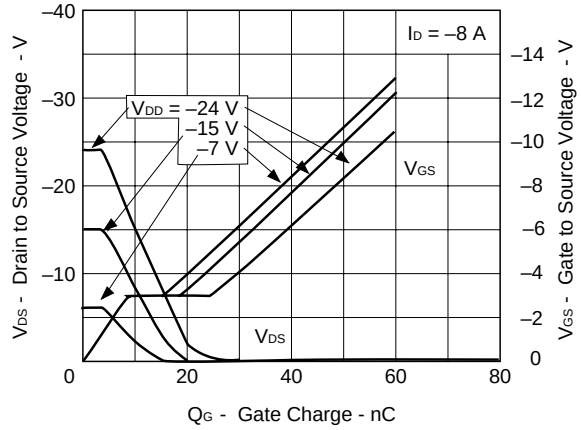

SWITCHING CHARACTERISTICS




REVERSE RECOVERY TIME vs. DRAIN CURRENT




DYNAMIC INPUT/OUTPUT CHARACTERISTICS



## REFERENCE

| Document Name | Document No. |
|---|---|
| NEC semiconductor device reliability/quality control system | TEI-1202 |
| Quality grade on NEC semiconductor devices | C11531E |
| Semiconductor device mounting technology manual | C10535E |
| Semiconductor device package manual | M10943X |
| Guide to quality assurance for semiconductor devices | MEI-1202 |
| Application circuits using Power MOS FET | TEA-1035 |
| Safe operating area of Power MOS FET | TEA-1037 |

**[MEMO]**

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