

SWITCHING P-CHANNEL POWER MOS FET INDUSTRIAL USE

DESCRIPTION

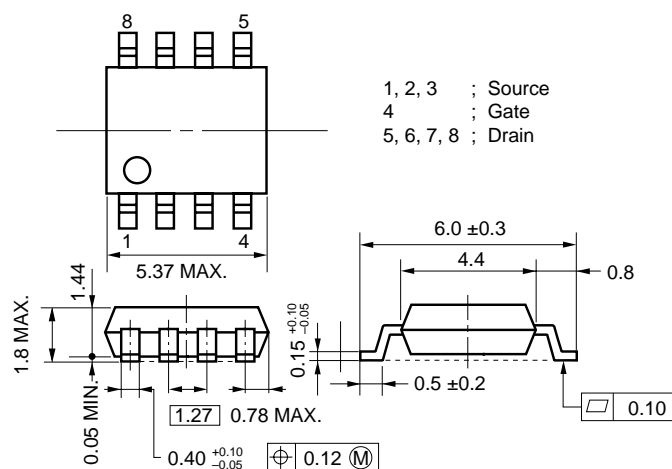
This product is P-Channel MOS Field Effect Transistor designed for power management applications of notebook computers and Li-ion battery protection circuit.

FEATURES

- Low On-Resistance
 $R_{DS(on)1} = 20 \text{ m}\Omega \text{ MAX. (} V_{GS} = -10 \text{ V, } I_D = -4.0 \text{ A)}$
 $R_{DS(on)2} = 48 \text{ m}\Omega \text{ MAX. (} V_{GS} = -4 \text{ V, } I_D = -4.0 \text{ A)}$
- Low C_{iss} $C_{iss} = 2700 \text{ pF TYP.}$
- Built-in G-S Protection Diode
- Small and Surface Mount Package (Power SOP8)

PACKAGE DIMENSIONS

(in millimeter)

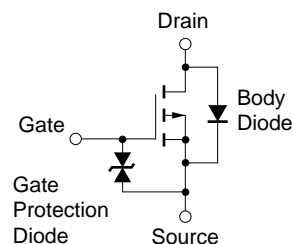


ABSOLUTE MAXIMUM RATINGS ($T_A = 25 \text{ }^\circ\text{C}$, all terminals are connected)

Drain to Source Voltage	V_{DSS}	-30	V
Gate to Source Voltage	V_{GSS}	±20	V
Drain Current (DC)	$I_D(\text{DC})$	±8.0	A
Drain Current (pulse) ^{Notes1}	$I_D(\text{pulse})$	±32	A
Total Power Dissipation ($T_A = 25 \text{ }^\circ\text{C}$) ^{Notes2}	P_T	2.0	W
Channel Temperature	T_{ch}	150	°C
Storage Temperature	T_{stg}	-55 to +150	°C

Notes 1. $PW \leq 10 \text{ } \mu\text{s}$, Duty Cycle $\leq 1 \%$

2. Mounted on ceramic substrate of $1200 \text{ mm}^2 \times 0.7 \text{ mm}$

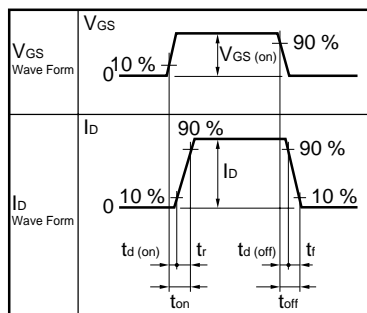
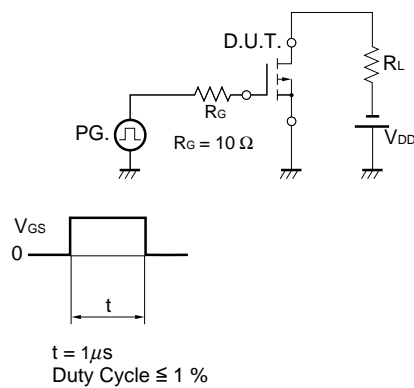


The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device acutally used, an additional protection circuit is externally required if voltage exceeding the rated voltage may be applied to this device.

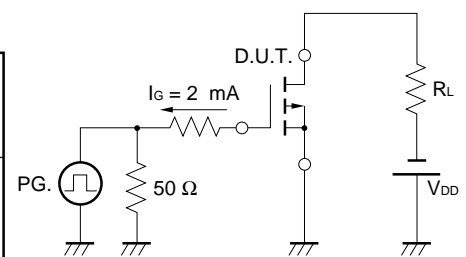
ELECTRICAL CHARACTERISTICS (T_A = 25 °C, all terminals are connected)

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Drain to Source On-state Resistance	R _{DS(on)1}	V _{GS} = -10 V, I _D = -4.0 A		15	20	mΩ
	R _{DS(on)2}	V _{GS} = -4 V, I _D = -4.0 A		27	48	mΩ
Gate to Source Cutoff Voltage	V _{GS(off)}	V _{DS} = -10 V, I _D = -1 mA	-1.0	-1.7	-2.5	V
Forward Transfer Admittance	y _{fs}	V _{DS} = -10 V, I _D = -4.0 A	6	13		S
Drain Leakage Current	I _{DSS}	V _{DS} = -30 V, V _{GS} = 0			-10	μA
Gate to Source Leakage Current	I _{GSS}	V _{GS} = ±20 V, V _{DS} = 0			±10	μA
Input Capacitance	C _{iss}	V _{DS} = -10 V		2700		pF
Output Capacitance	C _{oss}	V _{GS} = 0		1000		pF
Reverse Transfer Capacitance	C _{rss}	f = 1 MHz		380		pF
Turn-On Delay Time	t _{d(on)}	I _D = -4.0 A		30		ns
Rise Time	t _r	V _{GS(on)} = -10 V		150		ns
Turn-Off Delay Time	t _{d(off)}	V _{DD} = -15 V		250		ns
Fall Time	t _f	R _G = 10 Ω		200		ns
Total Gate Charge	Q _G	I _D = -8.0 A		55		nC
Gate to Source Charge	Q _{GS}	V _{DD} = -24 V		7.5		nC
Gate to Drain Charge	Q _{GD}	V _{GS} = -10 V		14.5		nC
Body Diode Forward Voltage	V _{F(S-D)}	I _F = 8.0 A, V _{GS} = 0		0.80		V
Reverse Recovery Time	t _{rr}	I _F = 8.0 A, V _{GS} = 0		60		ns
Reverse Recovery Charge	Q _{rr}	di/dt = 50 A/μs		40		nC

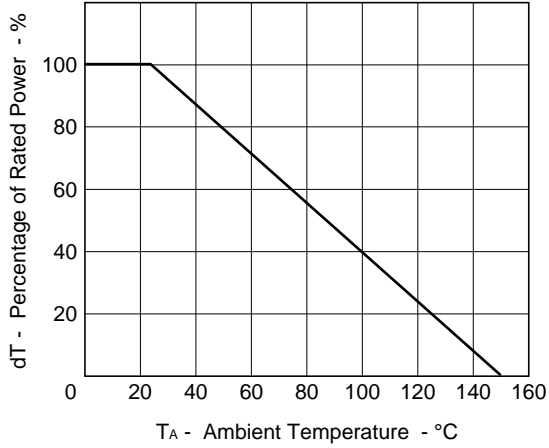
Test Circuit 1 Switching Time



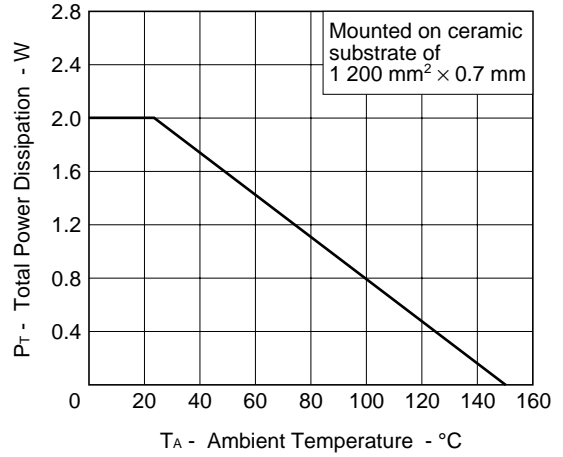
Test Circuit 2 Gate Charge



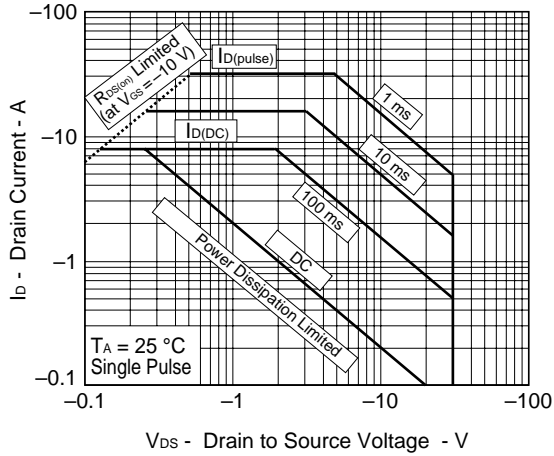
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE

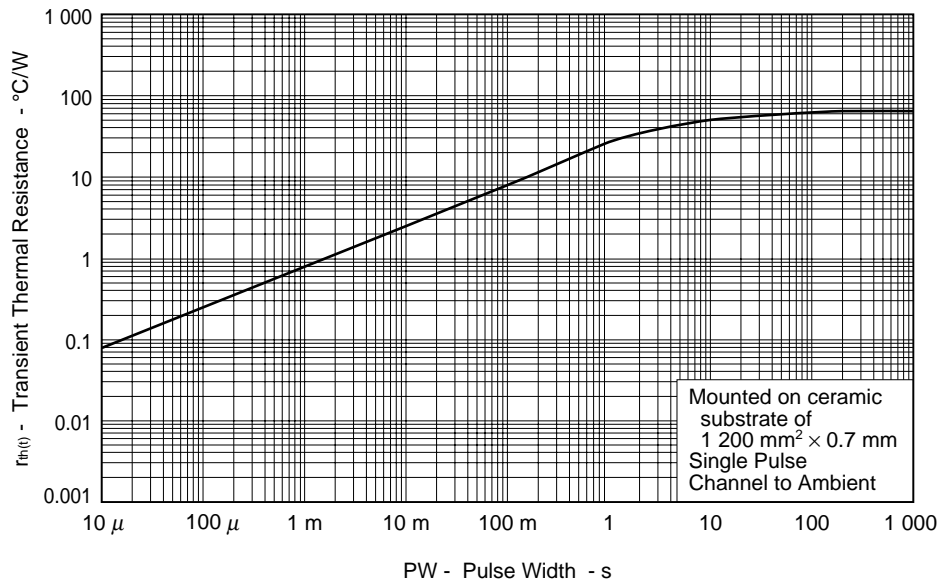


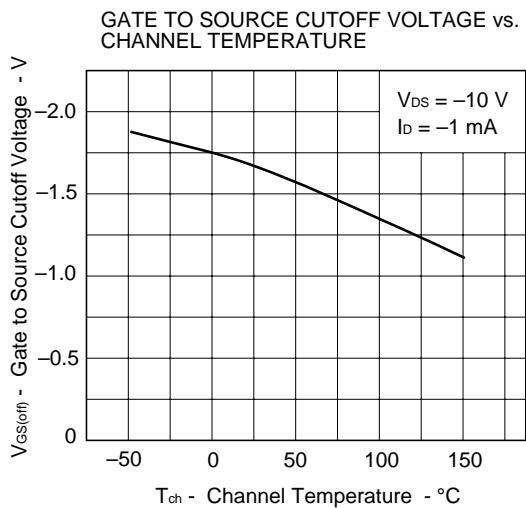
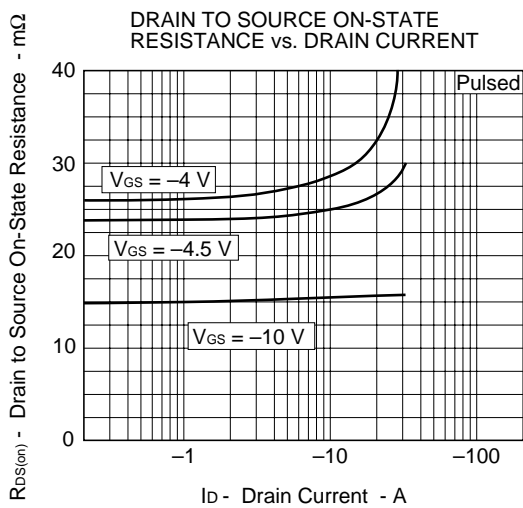
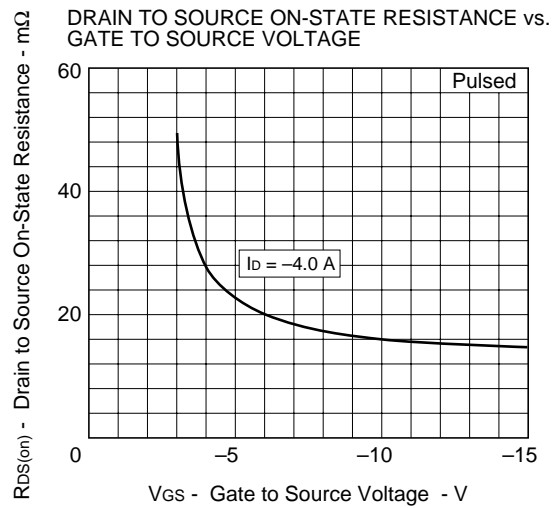
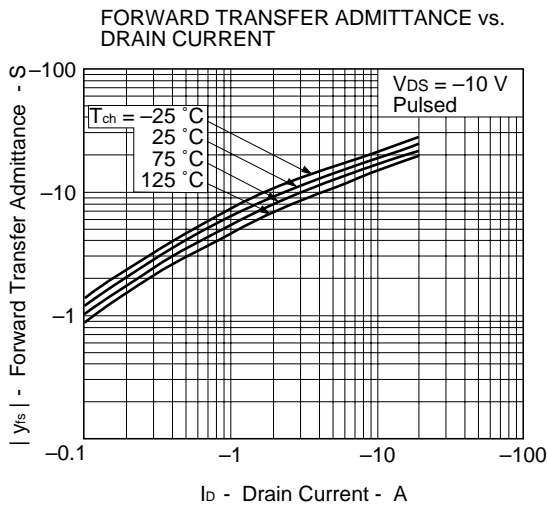
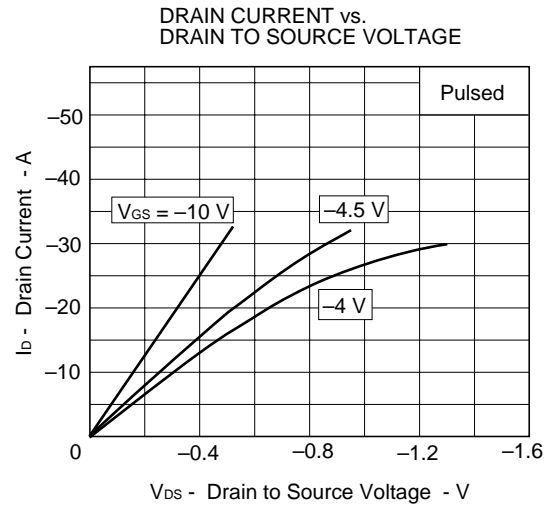
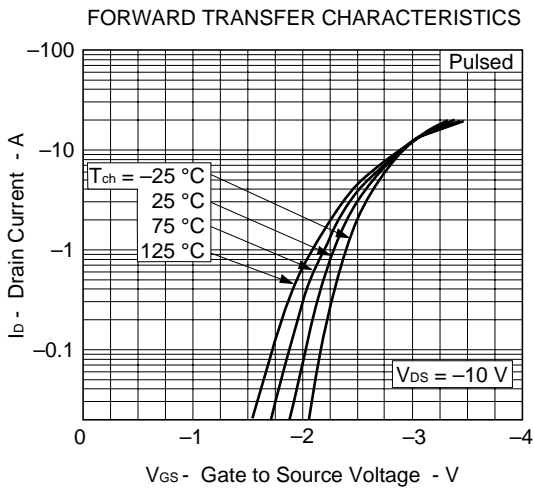
FORWARD BIAS SAFE OPERATING AREA

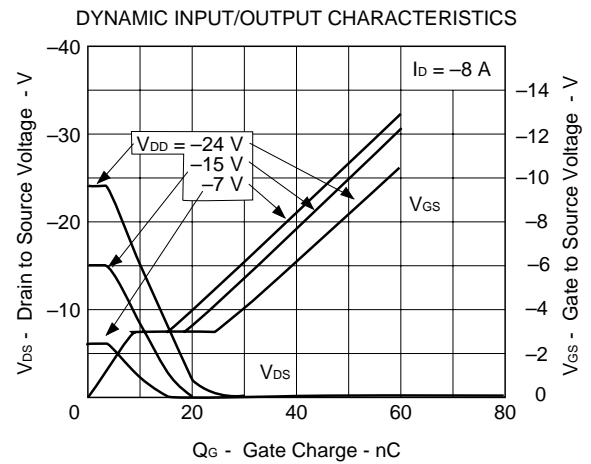
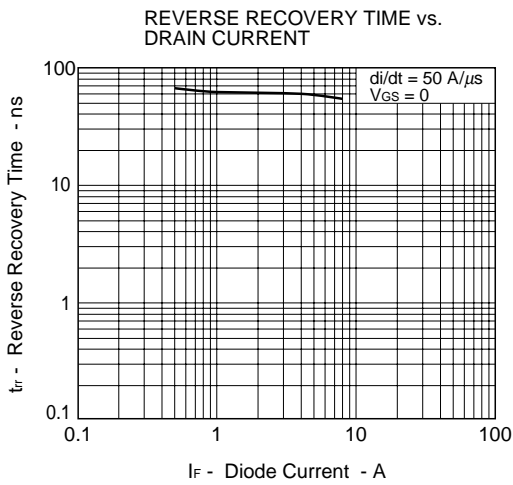
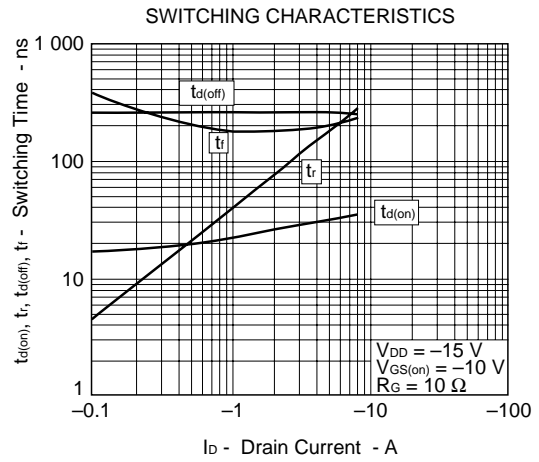
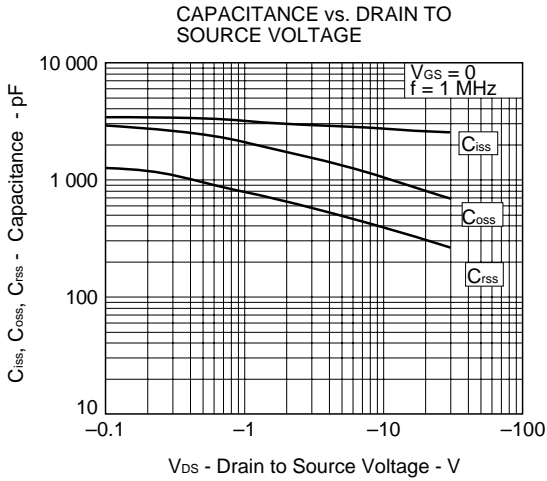
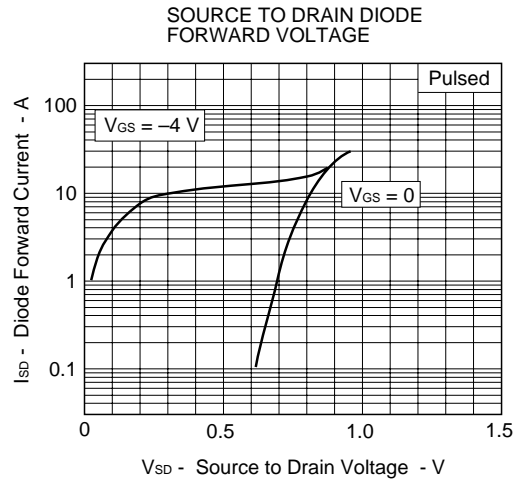
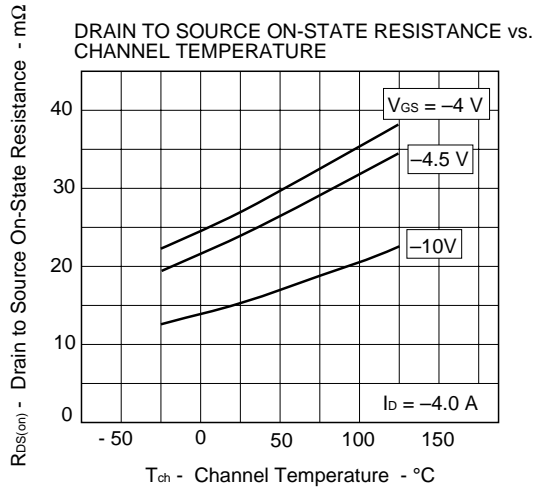


Note:
Mounted on ceramic
substrate of 1 200 mm² × 0.7 mm

TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH







REFERENCE

Document Name	Document No.
NEC semiconductor device reliability/quality control system	TEI-1202
Quality grade on NEC semiconductor devices	C11531E
Semiconductor device mounting technology manual	C10535E
Semiconductor device package manual	M10943X
Guide to quality assurance for semiconductor devices	MEI-1202
Application circuits using Power MOS FET	TEA-1035
Safe operating area of Power MOS FET	TEA-1037

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Anti-radioactive design is not implemented in this product.