OKI

Oki's MCU Solutions Powered by ARM

Audio Controllers

ML675200/ML67Q5200 Digital Audio Controller

Application Specific

Description

The Oki ML675200 and ML67Q5200 Application Specific Standard Products (ASSP) devices are targeted at the growing market for applications using the MP3 audio processing compression protocol. Available in two versions, ROM-less or Flash ROM, the ML675200 and ML67Q5200 devices incorporate an advanced dual processor core architecture featuring an ARM7TDMI™ 32-bit RISC CPU core and a Teak™ 16-bit DSP core.

The CPU-DSP architecture offers system developers both performance and flexibility. The ARM7TDMI RISC core provides 32-bit performance for application level software with access to general purpose I/O. The DSP core offers the numerical processing power dedicated to repetitive tasks such as MP3 encoding/decoding.

In addition to the two processor cores, the ML675200 and ML67Q5200 devices offer a wide variety of integrated peripherals, allowing system designers to implement a complete MP3 system requiring minimum external devices. Among these useful features are a USB 1.1 device controller, 32 Kbytes of SRAM, serial UART ports, GPIO, timers, and analog channels. Other powerful features include a 4-channel DMA controller for efficient data movement, a PLL circuit, a built-in controller for external memory, and a built-in voice Codec.

Features

- ARM7TDMI 32-bit RISC CPU
- 30 MHz CPU frequency, 60 MHz DSP frequency
- 256 Kbyte internal Flash ROM (ML67Q5200)
- 32 Kbyte internal RAM
- Audio Codec: MP3 encoder/decoder
- Voice Codec: 4-bit ADPCM2
- 4-channel DMA controller
- 4-channel A/D converter
- USB controller (version 1.1)

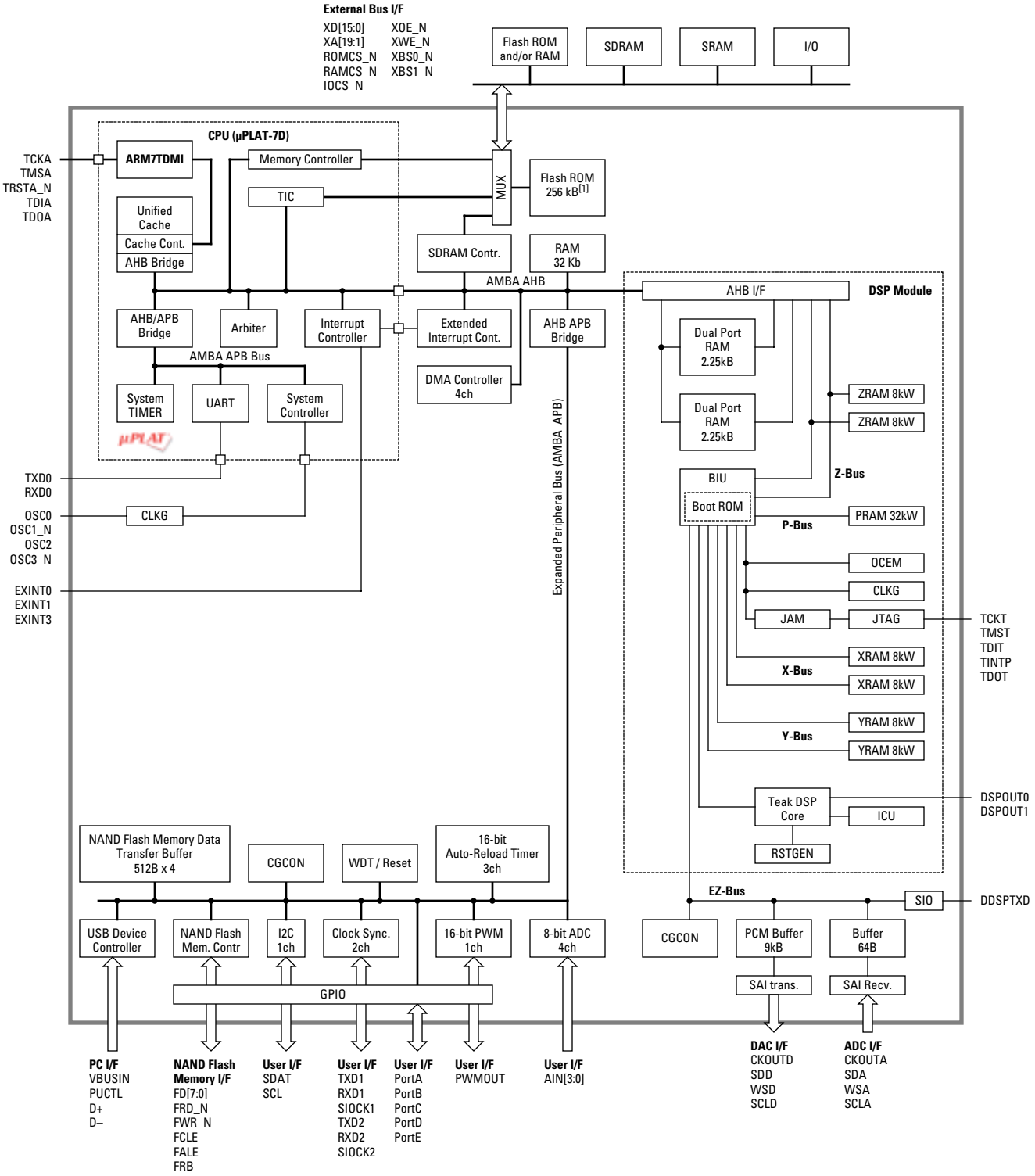
Applications

- Digital audio players (Portable MP3/WMA player, etc.)
- Educational toys
- Personal Digital Assistants (PDA)
- Home audio systems

ML675200/Q5200 Digital Audio Controllers

Part Number	Clock Frequency	Built-in Flash Size	Packages
ML675200-LA	30 MHz CPU, 60 MHz DSP	None (External Max 1 Mbyte)	144-pin plastic LFBGA (P-LFBGA144-1111-0.80)
ML67Q5200-NLA	30 MHz CPU, 60 MHz DSP	256 KB	144-pin plastic LFBGA (P-LFBGA144-1111-0.80)

Block Diagram



1. ML67Q5200 only. The ML675200 does not contain a built-in Flash ROM.

Functional Description

High-Performance ARM-based CPU

- Instructions: ARM (32-bit length) and Thumb (16-bit length) can be mixed.
- General register bank: 31 x 32 bits
- Built-in barrel shifter: ALU and barrel shift operations can be executed by one instruction.
- Multiplier: 32 bits x 8 bits (Modified Booth Algorithm)
- Cache: 8 Kbyte, 4-way copy back unified cache
- Built-in debug function: JTAG interface

DSP Module

The Teak DSP decodes MP3/WMA digital audio data. Also encodes/decodes voice data as Oki ADPCM.

- X-RAM: 16 Kwords (32 Kbytes)
- Y-RAM: 16Kwords (32 Kbytes)
- Z-RAM: 16 Kwords (32 Kbytes)
- P-program RAM: 32 Kwords (64 Kbytes)
- Built-in debug function: JTAG interface
- MP3 decoder:
  - MPEG-1 layer3, MPEG-2 layer3, MPEG-2.5
- WMA decoder:
  - Bit rate: 64 kbps, 96 kbps, 128 kbps, 160 kbps, 192 kbps
  - Sampling rate: 32 kHz, 44.1 kHz, 48 kHz
- MP3 encoder:
  - 64 kbps/96 kbps/128 kbps @ 44.1kHz

USB Control

The USB controller is compliant with the USB specification (version 1.1) and can transfer data at 12 Mbps.

The controller has 6 types of endpoints for control/bulk/isochronous/interrupt transfers.

NAND Flash Memory Control

The NAND Flash memory circuit automatically reads data from and writes data to an external 528-byte NAND Flash Memory.

Also includes an ECC circuit that detects and corrects multiple-bit data errors.

DMA Control

The 4-channel DMA controller transfers data between:

- Memory and memory
- I/O and memory
- I/O and I/O

External Memory Control

The external memory controller provides access to externally-connected devices such as ROM (FLASH), SRAM, SDRAM and I/O.

Connect 16-bit data bus length device and byte unit access device which have byte select function.

Power Management

The HALT, STOP, and SLEEP functions are supported as power-save functions.

Switching the CPU clock to the 1/2, 1/4, or 1/8 of the main clock enables operation in a low power consumption mode.

- HALT mode: Stops the ARM7TDMI and AHB/APB bus.
- STOP mode: Stops the DSP module clock first, then the clock for the entire device.
- SLEEP mode: Stops the power supply to the DSP module first, then stops the clock for the entire device.

Pin Configuration

NC	AIN3	PIOD9/ EXINT2	GND	PIOD5/ TXD0	PIOD2/ SDA	WSD	GND	VDD_IO	GND	VDD_IO	VDD_ CORE	NC	N
AIN2	AGND	VDD_IO	PIOD4/ SCLA	PIOD1/ CKOUTA	PIOD0/ PWMOUT	DSPOUT 1	VDD_ CORE	GND	OSC3_N	OSC1_N	TEST0	TEST1	M
AIN0	TCKT	AIN1	PIOD7/ EXINT0	PIOD6/ RXD0	SCLD	SDD	DSPOUT 0	OSC2	OSC0	GND	GND	TEST2	L
TMST	TINTP	AVDD	PIOD8/ EXINT1	PIOD3/ WSA	VDD_ CORE	CKOUTD	DSPTXD	VDD_ CORE	RES_N	PIOD14/ RXD2	PIOD11/ RXD1	PIOD15/ SIOCK2	K
TDOT	GND	TDIT	SDRAM MOD						PIOC10/ TXD1	PIOC13/ TXD2	PIOC8/ XBS0_N	PIOC12/ SIOCK1	J
VDD_ CORE	PIOE0/ FD0	VDD_IO	PIOE1/ FD1						GND	VDD_IO	VDD_ CORE	PIOC9/ XBS1_N	H
PIOE4/ FD4	GND	PIOE3/ FD3	PIOE2/ FD2			**144-Pin LFBGA (TOP VIEW)**			PIOC5/ IOCS_N	PIOC6/ XOE_N	PIOC4/ RAMCS_ N	PIOC7/ XWE_N	G
PIOE9/ FWR_N	PIOE7/ FD7	PIOE5/ FD5	PIOE6/ FD6						PIOC2/ XA19	PIOC3/ ROMCS _N	PIOC1/ XA18	PIOC0/ XA17	F
PIOE12/ FRB	PIOE8/ FRD_N	VDD_IO	PIOE10/ FCLE						PIOB15/ XA16	PIOB12/ XA13	GND	PIOB14/ XA15	E
PIOE14/ SCL	PIOE11/ FALE	PIOE13/ SDAT	VBUS	GND	PIOA5/ XD5	PIOA8/ XD8	GND	PIOA14/ XD14	PIOB2/ XA3	PIOB9/ XA10	PIOB13/ XA14	PIOB11/ XA12	D
PUCTL	PIOE15/ VBUSIN	TCKA	TRSTA_ N	PIOA0/ XD0	PIOA6/ XD6	PIOA9/ XD9	VDD_IO	GND	VDD_ CORE	PIOB7/ XA8	PIOB10/ XA11	PIOB8/ XA9	C
D+	D-	TDIA	PIOA1/ XD1	PIOA2/ XD2	PIOA4/ XD4	PIOA7/ XD7	PIOA11/ XD11	PIOA12/ XD12	PIOA15/ XD15	PIOB1/ XA2	PIOB4/ XA5	PIOB6/ XA7	B
NC	GND	TMSA	TDOA	VDD_IO	PIOA3/ XD3	PIOA10/ XD10	PIOA13/ XD13	VDD_IO	PIOB0/ XA1	PIOB3/ XA4	PIOB5/ XA6	NC	A
13	12	11	10	9	8	7	6	5	4	3	2	1	

Figure 1. 144-Pin LFBGA

Notes:

1. For pins that have multiple functions, the signals are noted by their primary / secondary functions.
2. Leave NC pins unconnected.

Pin Descriptions

In the Type column, an "I" indicates the signal is an input, an "O" indicates the signal is an output, and an "I/O" indicates the signal is bi-directional.

Signals with a "_N" suffix are active low.

Pin Descriptions

Classification	Primary Function			Secondary Function		
	Symbol	Type	Description	Symbol	Type	Description
Port	PIOA0	I/O	16-bit I/O port A.	XD0	I/O	External access data I/O port.
	PIOA1	I/O		XD1	I/O	
	PIOA2	I/O		XD2	I/O	
	PIOA3	I/O		XD3	I/O	
	PIOA4	I/O		XD4	I/O	
	PIOA5	I/O		XD5	I/O	
	PIOA6	I/O		XD6	I/O	
	PIOA7	I/O		XD7	I/O	
	PIOA8	I/O		XD8	I/O	
	PIOA9	I/O		XD9	I/O	
	PIOA10	I/O		XD10	I/O	
	PIOA11	I/O		XD11	I/O	
	PIOA12	I/O		XD12	I/O	
	PIOA13	I/O		XD13	I/O	
	PIOA14	I/O		XD14	I/O	
	PIOA15	I/O		XD15	I/O	
Port	PIOB0	I/O	16-bit I/O port B.	XA1	O	External access address output port.
	PIOB1	I/O		XA2	O	
	PIOB2	I/O		XA3	O	
	PIOB3	I/O		XA4	O	
	PIOB4	I/O		XA5	O	
	PIOB5	I/O		XA6	O	
	PIOB6	I/O		XA7	O	
	PIOB7	I/O		XA8	O	
	PIOB8	I/O		XA9	O	
	PIOB9	I/O		XA10	O	
	PIOB10	I/O		XA11	O	
	PIOB11	I/O		XA12	O	
	PIOB12	I/O		XA13	O	
	PIOB13	I/O		XA14	O	
	PIOB14	I/O		XA15	O	
	PIOB15	I/O		XA16	O	

Pin Descriptions

Classification	Primary Function			Secondary Function		
	Symbol	Type	Description	Symbol	Type	Description
Port	PIOC0	I/O	16-bit I/O port C.	XA17	O	External access address output port.
	PIOC1	I/O		XA18	O	
	PIOC2	I/O		XA19	O	
	PIOC3	I/O		ROMCS_N	O	External ROM chip select output pin.
	PIOC4	I/O		RAMCS_N	O	External RAM chip select output pin.
	PIOC5	I/O		IOCS_N	O	External I/O chip select output pin.
	PIOC6	I/O		XOE_N	O	External access read strobe output pin.
	PIOC7	I/O		XWE_N	O	External access write strobe output pin.
	PIOC8	I/O		XBS0_N	O	External access byte select (LSB) output pin.
	PIOC9	I/O		XBS1_N	O	External access byte select (MSB) output pin.
	PIOC10	I/O		TXD1	O	SIO1 transmit data output pin.
	PIOC11	I/O		RXD1	I	SIO1 receive data input pin.
	PIOC12	I/O		SIOCK1	I/O	SIO1 clock I/O pin.
	PIOC13	I/O		TXD2	O	SIO2 transmit data output pin.
	PIOC14	I/O		RXD2	I	SIO2 receive data input pin.
	PIOC15	I/O		SIOCK2	I/O	SIO2 clock I/O pin.
Port	PIOD0	I/O	10-bit I/O port D.	PWMOUT	O	PWM output pin.
	PIOD1	I/O		CKOUTA	O	External ADC interface system clock output pin.
	PIOD2	I/O		SDA	I	External ADC interface serial data input pin.
	PIOD3	I/O		WSA	O	External ADC interface channel select signal output pin.
	PIOD4	I/O		SCLA	O	External ADC interface serial clock output pin.
	PIOD5	I/O		TXD0	O	SIO0 transmit data output pin.
	PIOD6	I/O		RXD0	I	SIO0 receive data input pin.
	PIOD7	I/O		EXINT0	I	External interrupt 0 input pin.
	PIOD8	I/O		EXINT1	I	External interrupt 1 input pin.
	PIOD9	I/O		EXINT2	I	External interrupt 2 input pin.

Pin Descriptions

Classification	Primary Function			Secondary Function			
	Symbol	Type	Description	Symbol	Type	Description	
Port	PIOE0	I/O	16-bit I/O port E.	FD0/CAS_N	I/O or O	(SDRAMMOD = "H" level) NAND flash memory access data I/O port.	(SDRAMMOD = "H" level) SDRAM control signal output port.
	PIOE1	I/O		FD1/RAS_N	I/O or O		
	PIOE2	I/O		FD2/SDCLK	I/O or O		
	PIOE3	I/O		FD3/SDCS_N	I/O or O		
	PIOE4	I/O		FD4/SDCKE	I/O or O		
	PIOE5	I/O		FD5/DQM0	I/O or O		
	PIOE6	I/O		FD6/DQM1	I/O or O		
	PIOE7	I/O		FD7/PIOE7	I/O		Prohibit setting.
	PIOE8	I/O		FRD_N	O	NAND flash memory access read strobe output pin.	Prohibit setting
	PIOE9	I/O		FWR_N	O	NAND flash memory access write strobe output pin.	Prohibit setting.
	PIOE10	I/O		FCLE	O	NAND flash memory access command latch enable output pin.	Prohibit setting.
	PIOE11	I/O		FALE	O	NAND flash memory access address latch enable output pin.	Prohibit setting.
	PIOE12	I/O		FRB	I	NAND flash memory access Ready/Busy Input pin.	Prohibit setting
	PIOE13	I/O		SDAT	I/O	I2C data I/O pin.	
	PIOE14	I/O		SCL	O	I2C clock output pin.	
	PIOE15	I/O		VBUSIN	I	Vbus detect external interrupt input pin.	
DAC I/F	CKOUTD	O	External DAC interface system clock output pin.				
	SDD	O	External DAC interface serial data input pin.				
	WSD	O	External DAC interface channel select signal output pin.				
	SCLD	O	External DAC interface serial clock output pin.				
DSP port	DSPOUT0	O	DSP external control output pin.				
	DSPOUT1	O	DSP external control output pin.				
	DSPTXD	O	DSP debug serial data output pin.				
A/D port	AVDD	VDD	Analog reference voltage input pin (Connect to the VDD pin when the A/D converter is not used).				
	AIN0 to AIN3	I	A/D converter analog input port (Connect to the AVDD or AGND pin when the A/D converter is not used).				
	AGND	GND	Analog GND pin (Connect to the GND pin when the A/D converter is not used).				
USB I/F	D+	I/O	USB D+ pin.				
	D-	I/O	USB D- pin.				
	PUCTL	O	External control output pin.				
Reset	RES_N	I	Reset input pin.				

Pin Descriptions

Classification	Primary Function			Secondary Function		
	Symbol	Type	Description	Symbol	Type	Description
Oscillation	OSC0	I	Main clock oscillator input pin. Connect to a crystal or ceramic oscillator of f = 8 MHz. When an external clock is used, this pin is configured as the clock input.			
	OSC1_N	O	Main clock oscillator output pin. Connect to a crystal or ceramic oscillator of f = 8 MHz. The clock output is opposite in phase to OSC0. Leave this pin unconnected when an external clock is used.			
	OSC2	I	Audio clock oscillator input pin. Connect to a crystal or ceramic oscillator of f = 16.9344/ 11.2896 MHz. When an external clock is used, this pin is configured as the clock input.			
	OSC3_N	O	Audio clock oscillator output pin. Connect to a crystal or ceramic oscillator of f = 16.9344/ 11.2896 MHz. The clock output is opposite in phase to OSC2. Leave this pin unconnected when an external clock is used.			
CPU JTAG	TCKA	I	ARM JTAG clock input pin. Leave this pin unconnected for normal operation.			
	TMSA	I	ARM JTAG mode select input pin. Leave this pin unconnected for normal operation.			
	TRSTA_N	I	ARM JTAG reset input pin. Leave this pin unconnected for normal operation.			
	TDIA	I	ARM JTAG data input pin. Leave this pin unconnected for normal operation.			
	TDOA	O	ARM JTAG data output pin. Leave this pin unconnected for normal operation.			
DSP JTAG	TCKT	I	Teak-DSP JTAG clock input pin. Leave this pin unconnected for normal operation.			
	TMST	I	Teak-DSP JTAG mode select input pin. Leave this pin unconnected for normal operation.			
	TDIT	I	Teak-DSP JTAG data input pin. Leave this pin unconnected for normal operation.			
	TINTP	O	Teak-DSP JAM interrupt output pin. Leave this pin unconnected for normal operation.			
	TDOT	O	Teak-DSP JTAG data output pin. Leave this pin unconnected for normal operation.			
Power supply [1]	VDD_CORE	VDD	Core power supply pin. Connect all the VDD_CORE pins.			
	VDD_IO	VDD	IO power supply pin. Connect all the VDD_IO pins.			
	VBUS	VDD	USB power supply pin (Vbus input pin).			
	GND	GND	CORE and I/O GND pin.			
Others	TEST0	I	Test pin. Connect to GND pin for normal operation.			
	TEST1	I	Test pin. Connect to VDD_IO pin for normal operation.			
	TEST2	I	Test pin. Leave this pin unconnected for normal operation.			
	SDRAM-MOD	I	When this pin is "L" level, the NAND Flash memory interface is enabled. When this pin is "H" level, the SDRAM interface is enabled. This pin must not change state when power is supplied.			

1. Connect all VDD_IO pins, all VDD_CORE pins, and all GND pins. If a device has one or more unconnected VDD_IO, VDD_CORE, or GND pins, proper device operation is not guaranteed.

Electrical Characteristics

Absolute Maximum Ratings [1]

Parameter		Symbol	Conditions	Rating	Unit
Power supply voltage	Power supply for internal cell	V_{DD_CORE}	Tj = 25°C Reference GND = 0 V	-0.3 to +2.5	V
	Power supply for I/O circuit	V_{DD_IO}		-0.3 to +4.5	
	Analog power supply for A/D converter	A_{VDD}		-0.3 to +4.5	
	Power supply for USB bus	V_{BUS}		-0.3 to +4.5	
Input voltage		V_I		-0.3 to V_{DD_IO}+0.3	V
Output Current		I_O	4 mA buffer	16	mA
Power dissipation		P_D	Ta = 70°C per package	595	mW
Storage temperature		T_{STG}	—	-55 to +150	°C

1. These are maximum ratings not for general operation. Exceeding these maximum ratings could cause damage or lead to permanent deterioration of the device.

Recommended Operating Conditions

(GND = 0 V)

Item	Symbol	Conditions	Minimum	Typical	Maximum	Unit
Digital power supply voltage (core)	V_{DD_CORE}		1.65	1.80	1.95	V
Digital power supply voltage (I/O)	V_{DD_IO}		2.70	3.00	3.60	
Analog power supply voltage (A/D)	A_{VDD}		2.70	3.00	3.60	
Analog power supply voltage (USB)	V_{BUS}		3.00	3.30	3.60	
Analog input voltage	V_{AI}		0	–	A_{VDD}	V
Operating frequency	f_{OSC0}		–	8.00	–	MHz
	f_{OSC2}	256 x fs	–	11.2896	–	
		384 x fs	–	16.9344	–	
Ambient temperature	Ta	—	-30	+25	+70	°C
		During writing to flash ROM	0	+25	+70	

DC Characteristics

(V_{DD_CORE} = 2.25 to 2.75V, V_{DD_IO} = 3.0 to 3.6V, Ta = -40 to +85°C)

Item	Symbol	Conditions	Minimum	Typical	Maximum	Unit	Notes
High level input voltage	V_{IH}	TTL Input	2.2	—	V_{DD_IO}+0.3	V	[1]
Low level input voltage	V_{IL}		-0.3	—	0.8		
Schmitt input buffer threshold voltage	V_{T+}	TTL Input	—	1.5	2.2	V	[2]
	V_{T-}		0.6	1.0	—		
	V_{HYS}	V_{T+} - V_{T-}	—	0.4	—		
High level output voltage	V_{OH}	I_{OH} = -100 µA	V_{DD}–0.2	—	—	V	[3]
		I_{OH} = -4 mA	2.2	—	—		
Low level output voltage	V_{OL}	I_{OL} = 100 µA	—	—	0.2	V	
		I_{OL} = 4 mA	—	—	0.4		
High level input current	I_{IH}	V_{IH} = V_{DD_IO}	—	—	10	µA	[4]
		V_{IH} = V_{DD_IO} (50 kΩ pull-down)	10	66	200		[5]
Low level input current	I_{IL}	V_{IL} = GND	-10	—	—	µA	[4]
		V_{IL} = GND (50 kΩ pull-up)	-200	66	-10		[6]
3-State output leakage current	I_{OZH}	V_{OH} = V_{DD_IO}	—	—	20	µA	[7]
	I_{OZL}	V_{OL} = GND	-20	—	—		

1. Applicable to the TEST0 to TEST2 pins, SDRAMMOD pin and the JTAG input pins.
2. Applicable to the RES_N pin when inputting to the PIOA to PIOE ports.
3. Applicable when outputting from the PIOA to PIOE ports. Applicable to the CKOUTD/SDD/WSD/SCLD pins, DSPOUT1/DSPOUT0 pins and DSPTXD pin. Applicable to the JTAG output pins (TDOA, TDOT, and TINTP).
4. Applicable to the TEST0/TEST1 pins and SDRAMMOD pin.
5. Applicable to the pull-down pins (TEST2 pin and TCKA/NTRSTA/TCKT pins of JTAG).
6. Applicable to the pull-up pins (RES_N pin and TMSA/TDIA/TMST/TDIT pins of JTAG).
7. Applicable when inputting to the input-output pins (PIOA to PIOE ports).

AC Characteristics

External RAM/RAM Read Cycle [1]

(V_{DD_CORE} = 1.65 V to 1.95 V, V_{DD_IO} = 2.7 V to 3.6 V, T_A = –30°C to +70°C)

Parameter	Symbol	Condition	Min	Typ	Max	Units
ROMCS_N setup time	t_{XROMCS}	CL = 50 pF	$(n_0+n_1)Tc$ - 10	—	—	ns
RAMCS_N setup time	t_{XRAMCS}		$(n_0+n_1)Tc$ - 10	—	—	ns
ROMCS_N output hold time 1	$t_{XROMCSH1}$		Tc	—	—	ns
RAMCS_N output hold time 1	$t_{XRAMCSH1}$		Tc	—	—	ns
XA[19:1] setup time	t_{XAS}		$(n_0+n_1)Tc$ - 10	—	—	ns
XA[19:1] hold time 1	t_{XAH1}		-5	—	—	ns
XBS_N[1:0] setup time	t_{XBS}		$(n_0+n_1)Tc$ - 10	—	—	ns
XBS_N[1:0] hold time 1	t_{XBH1}		-5	—	—	ns
XOE_N pulse width	t_{XOEW}		n_1Tc - 10	—	—	ns
XD[15:0] input setup time	t_{XDIS}		40	—	—	ns
XD[15:0] input hold time	t_{XDIH}		0	—	—	ns

1. n_0 = address setup time, n_1 = XOE_N/XWE_N pulse width, Tc = HCLK cycle.
Address setup time and XOE_N/XWE_N pulse width are parameters that can be set by the ROMAC/RAMAC registers.

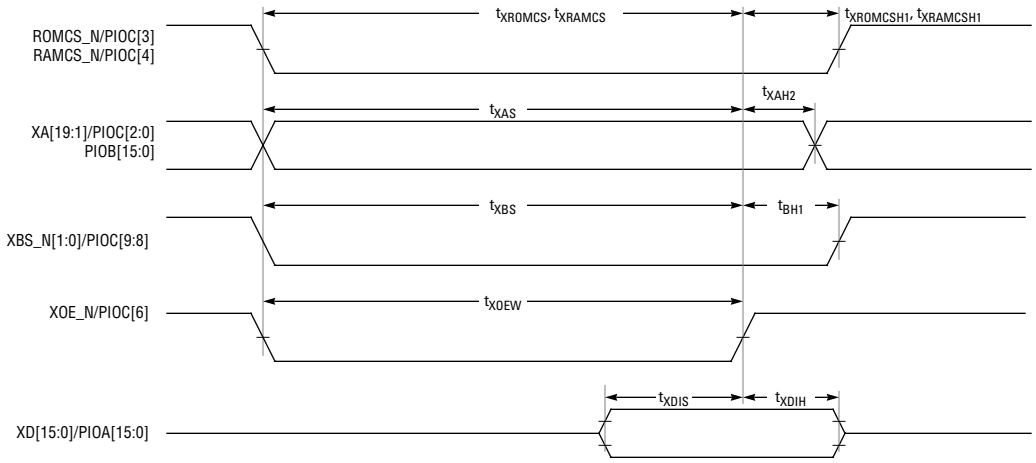


Figure 2. External ROM/RAM Read Cycle Timing

External RAM/RAM Write Cycle [1]

(V_{DD_CORE} = 1.65 V to 1.95 V, V_{DD_IO} = 2.7 V to 3.6 V, T_A = –30°C to +70°C)

Parameter	Symbol	Condition	Min	Typ	Max	Units
ROMCS_N pulse width	$t_{XROMCSW}$	CL = 50 pF	$(n_0+n_1+1)Tc$ - 10	—	—	ns
RAMCS_N pulse width	$t_{XRAMCSW}$		$(n_0+n_1+1)Tc$ - 10	—	—	ns
ROMCS_N output hold time 2	$t_{XROMCSH2}$		Tc	—	—	ns
RAMCS_N output hold time 2	$t_{XRAMCSH2}$		Tc	—	—	ns
XA[19:1] hold time 2	t_{XAH2}		-5	—	—	ns
XBS_N[1:0] hold time 2	t_{XBH2}		-5	—	—	ns
XWE_N output delay time	t_{XWED} [2]		n_0Tc - 10	—	—	ns
XWE_N output delay time pulse width	t_{XWEW}		n_1Tc - 10	—	—	ns
XD[15:0] output delay time	t_{XDOD} [2]		—	—	n_0Tc + 10	ns
XD[15:0] output hold time	t_{XDOH}		Tc - 5	—	—	ns

1. n_0 = address setup time, n_1 = XOE_N/XWE_N pulse width, Tc = HCLK cycle.
   Address setup time and XOE_N/XWE_N pulse width are parameters that can be set by the ROMAC/RAMAC registers.
2. t_{XDOD} and t_{XWED} are defined as a time period that starts from the point of change in ROMCS_N/RAMCS_N, XA[19:0], or XBS_N[1:0], whichever signal changes last.

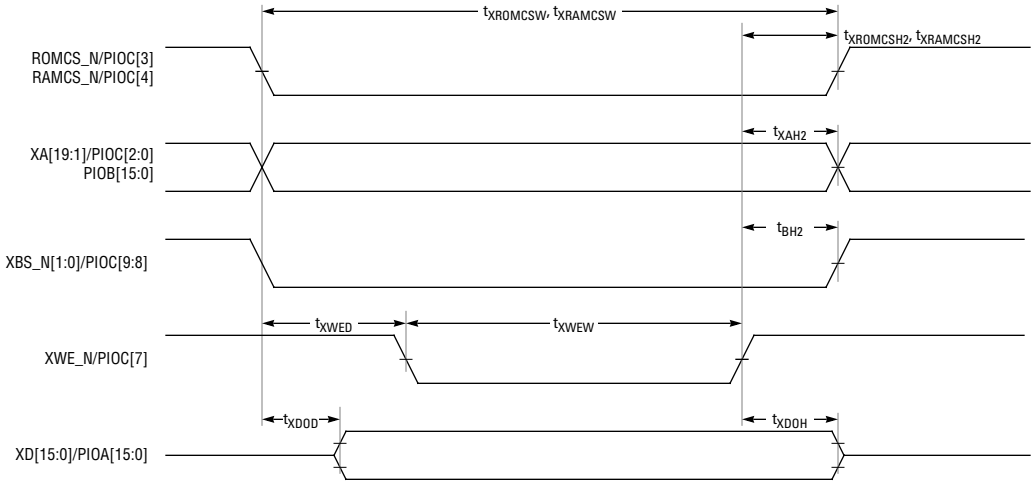


Figure 3. External ROM/RAM Write Cycle Timing

External SDRAM Bus Timing [1]

(V_{DD_CORE} = 1.65 V to 1.95 V, V_{DD_IO} = 2.7 V to 3.6 V, T_A = –30°C to +70°C)

Parameter	Symbol	Condition	Min	Typ	Max	Units
SDCKE output delay time	t_{SDCKED}	CL = 50 pF	0	—	10	ns
XA[19:1] output delay time	t_{SDXAD}		-5	—	10	ns
SDCS_N "L" output delay time	t_{SDCSLD}		-10	—	10	ns
RAS_N "L" output delay time	$t_{SDRASLD}$		-10	—	10	ns
RAS_N "H" output delay time	$t_{SDRALHD}$		-10	—	10	ns
CAS_N "L" output delay time	$t_{SDCASLD}$		-10	—	10	ns
CAS_N "H" output delay time	$t_{SDCALHD}$		-10	—	10	ns
RAS/CAS minimum delay time	t_{SDRCD}		nSD1Tc	—	—	ns
RAS active time	t_{SDRAS}		nSD2Tc	—	—	ns
RAS precharge time	t_{SDRP}		nSD3Tc	—	—	ns
XWE_N "L" output delay time	t_{SDWELD}		-10	—	10	ns
XWE_N "H" output delay time	t_{SDWEHD}		-10	—	10	ns
DQM[1]/DQM[0] "L" output delay time	t_{DOMD}		-10	—	10	ns
DQM[1]/DQM[0] "H" output delay time	t_{DOMD}		-10	—	10	ns
XD[15:0] input setup time	t_{SDXDIS}		15	—	—	ns
XD[15:0] input hold time	t_{SDXDIH}		0	—	—	ns
XD[15:0] output delay time	t_{SDXDOD}		-10	—	10	ns
XD[15:0] output hold time	t_{SDXDOH}		-10	—	—	ns

1. nSD1 = t_{RCD}, nSD2 = t_{RAS}, nSD3 = t_{RP}.
   t_{RCD}, t_{RAS}, and t_{RP} are parameters that can be set by the DRPC register. Refer to the User's Manual for more information on these timings.

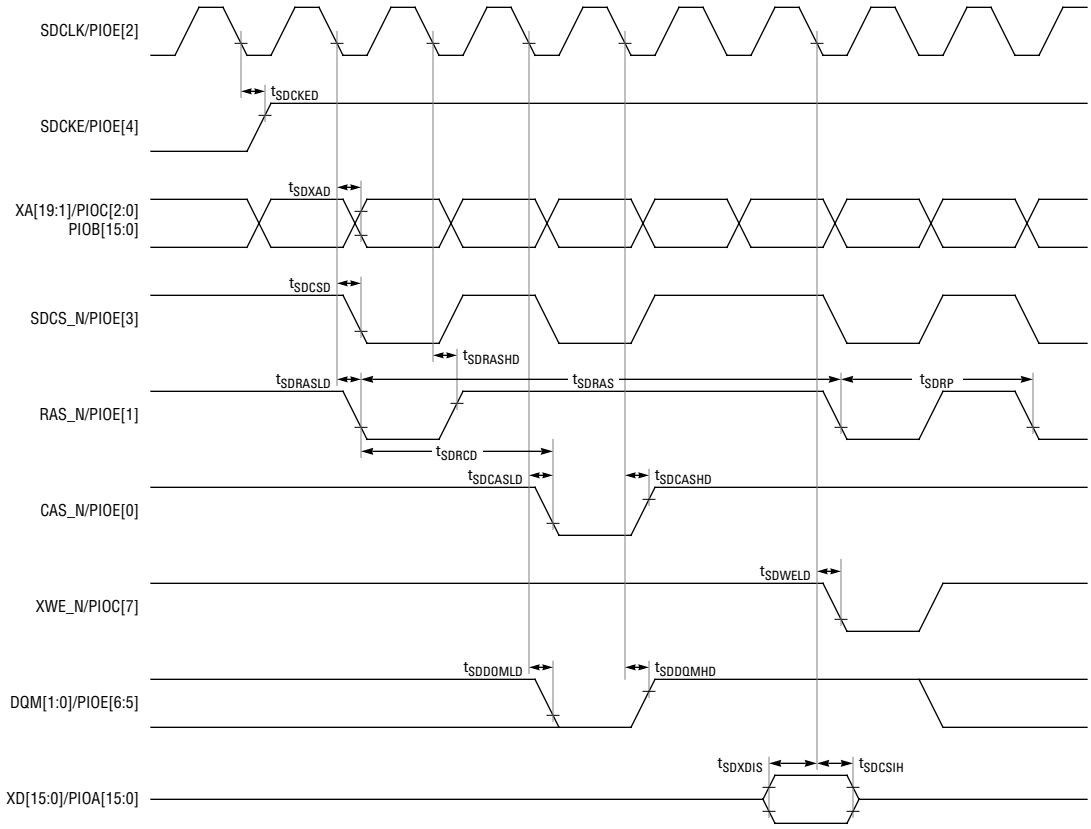


Figure 4. SDRAM Read Cycle Timing

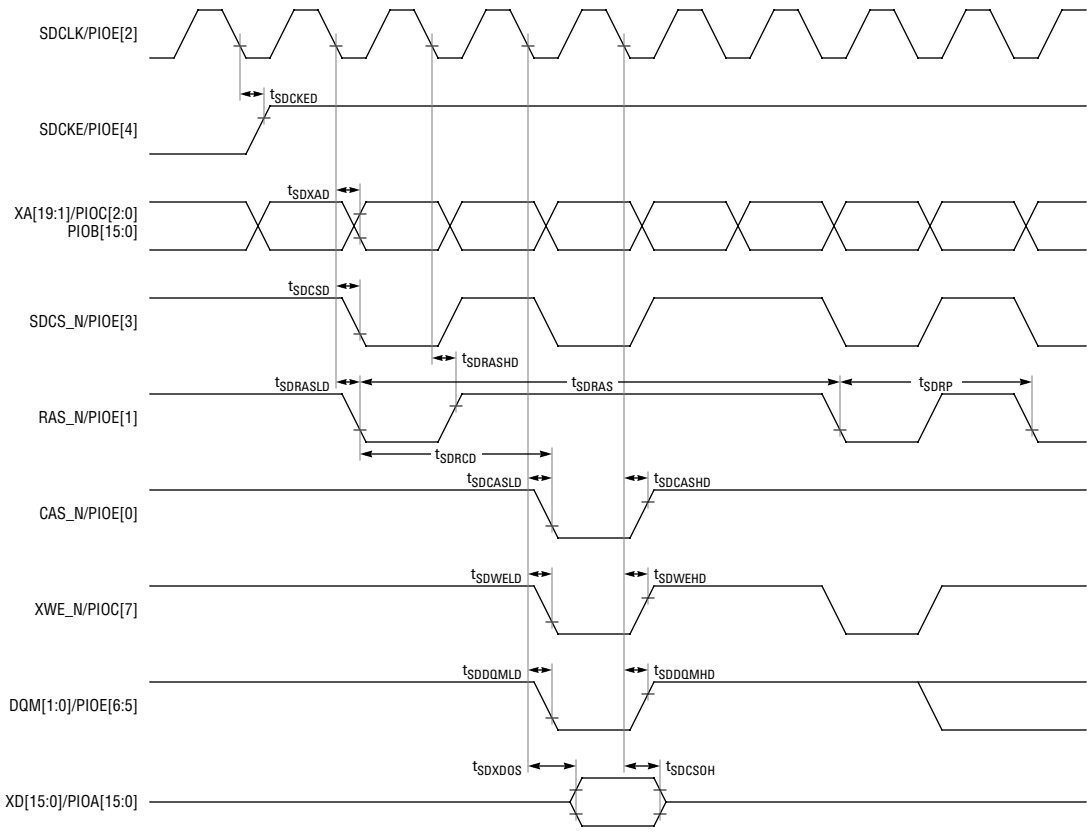


Figure 5. SDRAM Write Cycle Timing

External I/O Bus Read Cycle [1]

(V_{DD_CORE} = 1.65 V to 1.95 V, V_{DD_IO} = 2.7 V to 3.6 V, T_A = –30°C to +70°C)

Parameter	Symbol	Condition	Min	Typ	Max	Units
IOCS_N setup time	t_{XIOCS}	CL = 50 pF	(n_0+n_1)Tc - 10	—	—	ns
IOCS_N output hold time 1	$t_{XIOCSH1}$		Tc	—	—	ns
XA[19:1] setup time	t_{XIOAS}		(n_0+n_1)Tc - 10	—	—	ns
XA[19:1] hold time 1	t_{XIOAH1}		-5	—	—	ns
XBS_N[1:0] setup time	t_{XIOBS}		(n_0+n_1)Tc - 10	—	—	ns
XBS_N[1:0] hold time 1	t_{XIOBH1}		-5	—	—	ns
XOE_N output delay time	t_{XIOOED}		n_0Tc - 10	—	—	ns
XOE_N pulse width	t_{XIOOEW}		n_1Tc - 10	—	—	ns
XD[15:0] input setup time	t_{XIODIS}		40	—	—	ns
XD[15:0] input hold time	t_{XIODIH}		0	—	—	ns

1. n_0 = address setup time, n_1 = XOE_N/XWE_N pulse width, Tc = HCLK cycle
Address setup time and XOE_N/XWE_N pulse width are parameters that can be set by the IOAC register.

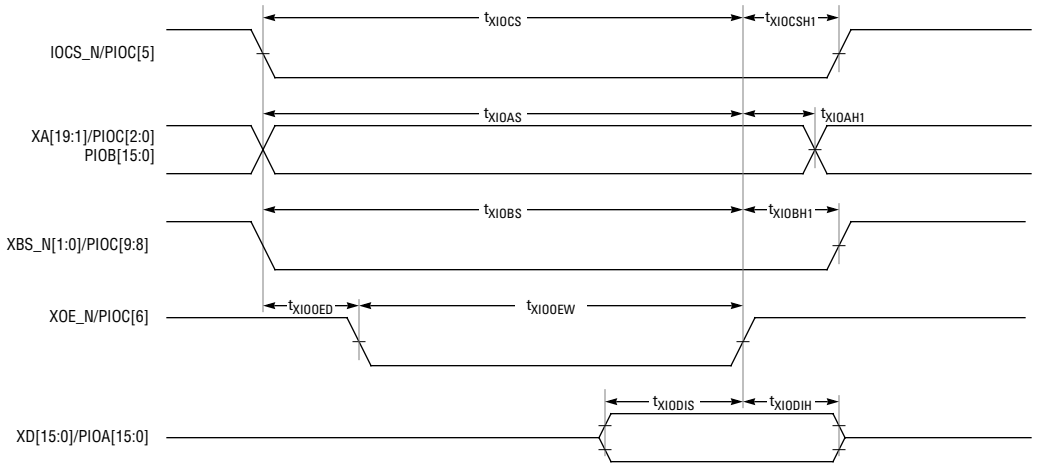


Figure 6. External I/O Bus Read Cycle Timing

External I/O Bus Write Cycle [1]

(V_{DD_CORE} = 1.65 V to 1.95 V, V_{DD_IO} = 2.7 V to 3.6 V, T_A = –30°C to +70°C)

Parameter	Symbol	Condition	Min	Typ	Max	Units
IOCS_N pulse width	t_{XIOCSW}	C_L = 50 pF	$(n_0+n_1+1)Tc - 3$	—	—	ns
IOCS_N output hold time 2	$t_{XIOCSH2}$		Tc	—	—	ns
XA[19:1] hold time 2	t_{XIOAH2}		-3	—	—	ns
XBS_N[1:0] hold time 2	t_{XIOBH2}		-3	—	—	ns
XWE_N output delay time	t_{XIOWED} [2]		$n_0Tc - 5$	—	—	ns
XWE_N output delay time pulse width	t_{XIOWEW}		$n_1Tc - 3$	—	—	ns
XD[15:0] output delay time	t_{XIODOD} [2]		—	—	$n_0Tc + 5$	ns
XD[15:0] output hold time	t_{XIODOH}		Tc - 3	—	—	ns

1. n_0 = address setup time, n_1 = XOE_N/XWE_N pulse width, Tc = HCLK cycle
   Address setup time and XOE_N/XWE_N pulse width are parameters that can be set by the IOAC register.
2. t_{XIODOD} and t_{XIOWED} are defined as a time period that starts from the point of change in IOCS_N, XA[19:0], or XBS_N[1:0], whichever signal changes last.

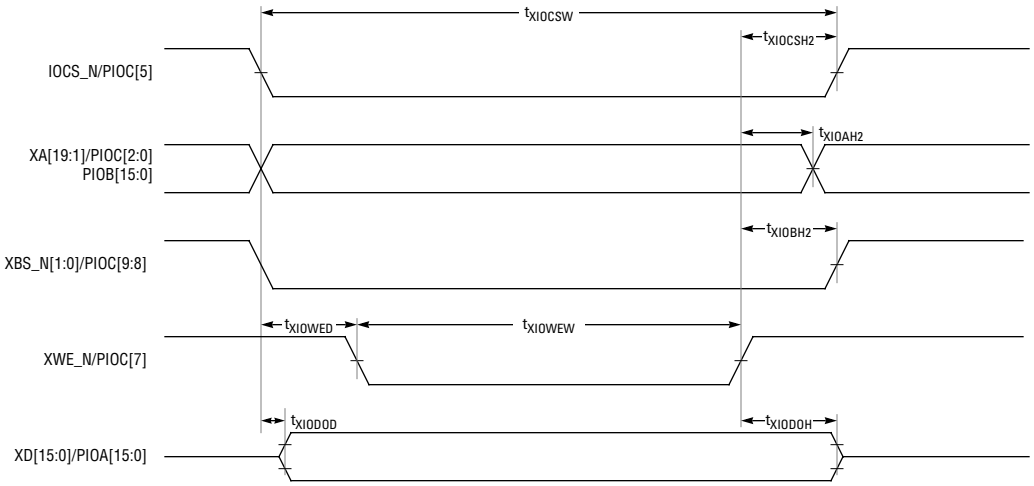


Figure 7. External I/O Bus Write Cycle Timing

Synchronous Serial Interface Timing

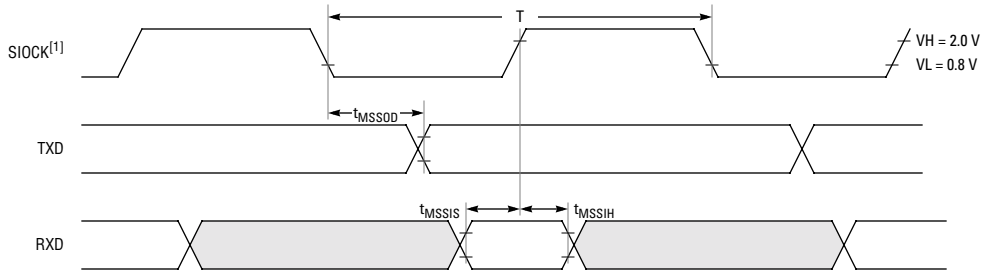
The synchronous serial interface operate in master mode or slave mode. It also allows the user to set the polarity of the serial clock.

When the polarity of the serial clock is set to positive, as shown in the figure below, transmit data (TXD) is driven on the falling edge of SIOCK. Receive data is sampled on the rising edge of SIOCK. Once the transmission/reception of the 8-bit data is completed, the clock stops at a high level, and the data output holds the last data.

When the polarity of the serial clock is set to negative, transmit data is driven on the rising edge of SIOCK, and receive data is sampled on the falling edge of SIOCK. Once the transmission/reception of 8-bit data is completed, the clock stops at a low level, and the data output holds the last data.

Master Mode

Parameter	Symbol	Condition	Min	Max	Units
Serial clock cycle	T	C_L = 50 pF	66.67	—	ns
Output data delay time	t_{MSSOD}		—	20	ns
Input data setup time	t_{MSSIS}		40	—	ns
Input data hold time	t_{MSSIH}		0	—	ns

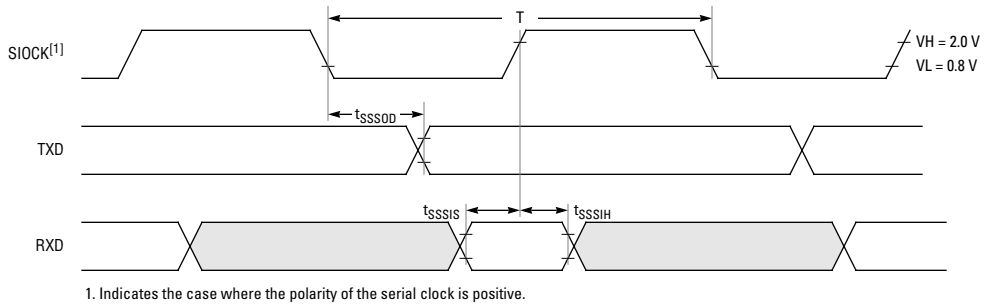


1. Indicates the case where the polarity of the serial clock is positive.

Figure 8. Synchronous Serial Interface – Master Mode Timing

Slave Mode

Parameter	Symbol	Condition	Min	Max	Units
Serial clock cycle	T	C_L = 50 pF	66.67	—	ns
Output data delay time	t_{SSSOD}		—	40	ns
Input data setup time	t_{SSSIS}		20	—	ns
Input data hold time	t_{SSSIH}		20	—	ns



1. Indicates the case where the polarity of the serial clock is positive.

Figure 9. Synchronous Serial Interface – Slave Mode Timing

I2C Bus Timing

Parameter	Symbol	Standard Mode		Fast Mode		Units
		Min	Max	Min	Max	
SCL clock frequency	f_{SCL}	—	100	—	400	kHz
SCL clock "L" period	t_{LOW}	4.7	—	1.3	—	µs
SCL clock "H" period	t_{HIGH}	4.0	—	0.6	—	µs
Hold time (repetitive) "START" condition (After this period, the first clock pulse is generated.)	$t_{HD:STA}$	4.0	—	0.6	—	µs
Setup time for repetitive "START" condition	$t_{SU:STA}$	4.7	—	0.6	—	µs
Data hold time	$t_{HD:DAT}$	5.0	—	—	—	µs
Data setup time	$t_{SU:DAT}$	250	—	100 [1]	—	µs
Setup time for "STOP" condition	$t_{SU:STO}$	4.0	—	0.6	—	µs

1. Although I2C bus devices in Fast mode can be used in a standard I2C bus system, it is necessary to satisfy the required condition $t_{SU:DAT} \geq 250$ ns. This means that such devices do not automatically extend the "L" period of the SCL signal.
   If a device does not extend the "L" period of the SCL signal, the next data must be output to the SDA pin at least "trmax + $t_{SU:DAT}$ = 1000 + 250 = 1250 ns" (output the data bits that are in effect in the Standard mode according to the I2C Bus Specification) earlier than the time the SCL pin is opened

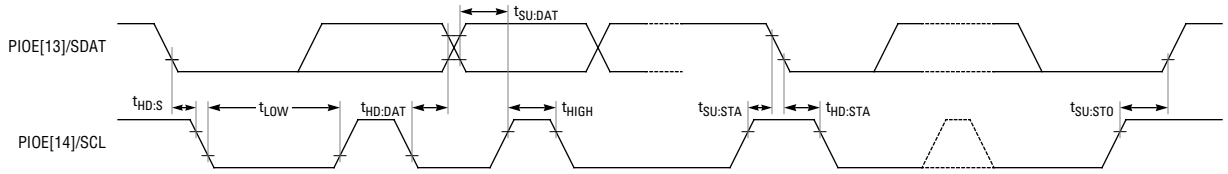


Figure 10. I2C Bus Timing

SAI Transceiver/Receiver Timing

Transceiver (for master only)

(V_{DD_CORE} = 1.65 V to 1.95 V, V_{DD_IO} = 2.7 V to 3.6 V, TA = –30°C to +70°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Remarks
Master clock frequency (256*fs) [1]		CL = 50 pF	2.0480	11.2896	12.2880	MHz	Division ratio = 1/1, 1/2, 1/4 fs = 44.1, 32, 48 kHz
Master clock frequency (384*fs) [1]			3.0720	16.9344	18.4320	MHz	
Serial clock frequency			—	32*fs	—	kHz	
Sampling frequency	fs		32	44.1	48	kHz	
CKOUTD period (256*fs)	t_{T_MCLK}		488	88.6	81.4	ns	
CKOUTD period (384*fs)			325	59	54.3	ns	
CKOUTD "L" period (256*fs)	t_{T_MCKL}		244	44.3	40.7	ns	
CKOUTD "L" period (384*fs)			162.5	29.5	27.15	ns	
CKOUTD "H" period (256*fs)	t_{T_MCKH}		244	44.3	40.7	ns	
CKOUTD "H" period (384*fs)			162.5	29.5	27.15	ns	
Serial clock period (fs = 44.1 KHz)	t_{T_SCK}		—	708	—	ns	
SCLD "L" period (fs = 44.1 KHz)	t_{T_SCL}		—	354	—	ns	
SCLD "H" period (fs = 44.1 KHz)	t_{T_SCH}		—	354	—	ns	
WS output delay time	t_{T_WSD}		—	—	50	ns	
Serial data (SDD) output delay time	t_{T_SDD}		—	—	50	ns	

1. Typ.: fs = 1/1 division of 44.1 kHz, Min.: fs = 1/4 division of 32 kHz, Max.: fs = 1/1 division of 48 kHz

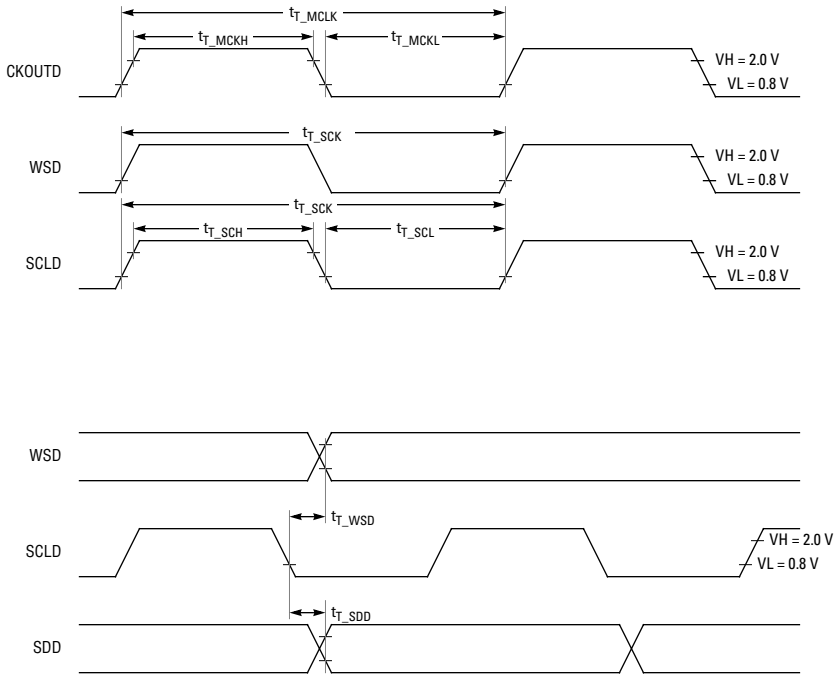


Figure 11. SAI Transceiver Timing

Receiver (for master only)

(V_{DD_CORE} = 1.65 V to 1.95 V, V_{DD_IO} = 2.7 V to 3.6 V, TA = –30°C to +70°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Remarks
Master clock frequency (256*fs) [1]		CL = 50 pF	2.0480	11.2896	12.2880	MHz	Division ratio = 1/1, 1/2, 1/4 fs = 44.1, 32, 48 kHz
Master clock frequency (384*fs) [1]			3.0720	16.9344	18.4320	MHz	
Serial clock frequency			—	32·fs	—	kHz	
Sampling frequency	fs		32	44.1	48	kHz	
CKOUTA period (256*fs)	t_{R_MCLK}		488	88.6	81.4	ns	
CKOUTA period (384*fs)			325	59	54.3	ns	
CKOUTA "L" period (256*fs)	t_{R_MCKL}		244	44.3	40.7	ns	
CKOUTA "L" period (384*fs)			162.5	29.5	27.15	ns	
CKOUTA "H" period (256*fs)	t_{R_MCKH}		244	44.3	40.7	ns	
CKOUTA "H" period (384*fs)			162.5	29.5	27.15	ns	
Serial clock period (fs = 44.1 KHz)	t_{R_SCK}		—	708	—	ns	
SCLA "L" period (fs = 44.1 KHz)	t_{R_SCL}		—	354	—	ns	
SCLA "H" period (fs = 44.1 KHz)	t_{R_SCH}		—	354	—	ns	
WS output delay time	t_{R_WSD}			—	50	ns	
Serial data (SDA) setup time	t_{R_SDIS}		50	—		ns	
Serial data (SDA) hold time	t_{R_SDIH}		0	—		ns	

1. Typ.: fs = 1/1 division of 44.1 kHz, Min.: fs = 1/4 division of 32 kHz, Max.: fs = 1/1 division of 48 kHz

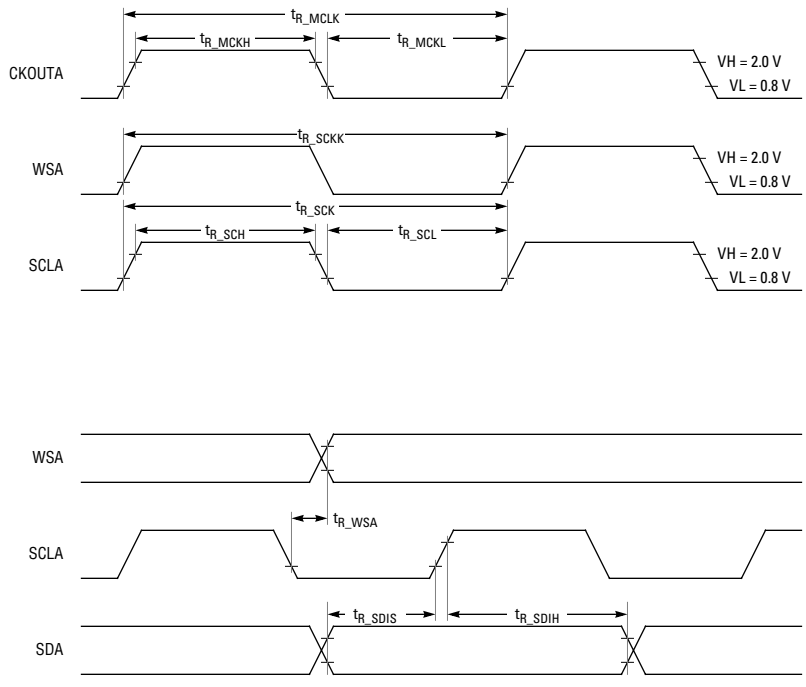


Figure 12. SAI Receiver Timing

NAND Flash Interface [1]

(V_{DD_CORE} = 1.65 V to 1.95 V, V_{DD_IO} = 2.7 V to 3.6 V, TA = –30°C to +70°C)

Parameter	Symbol	Condition	Min.	Max.	Unit
FWR_N pulse width	t_{FWP}	CL = 50 pF	(0.5·w1 + 1)Tc – 10	—	ns
FWR_N "H" output hold time	t_{FWH}		(0.5·w1 + 1)Tc – 10	(0.5·w1 + 1)Tc +10	ns
Data (FD[7:0]) setup time	t_{FDS}		w2·Tc – 20	—	ns
Data (FD[7:0]) hold time	t_{FDH}		w3·Tc – 10	—	ns
FRD_N pulse width	t_{FRP}		r1·Tc – 10	—	ns
FRD_N "H" output hold time	t_{FREH}		r2·Tc – 10	—	ns
FRD_N access time	t_{FREA}		r1·Tc – 20	—	ns
Data output hold time (FRD_N)	t_{FRHZ}		0	—	ns

1. Tc = HCLK cycle
   To calculate, use the following w1, w2, and w3 values during sequencer write and the following r1 and r2 values during sequencer read:

   w1: 0 for "no write wait" mode; 1 for "1 write wait" mode; 2 for "2 write wait" mode
   w2: 1.5 for "no write wait" mode; 2 for "1 write wait" mode; 3 for "2 write wait" mode
   w3: 0.5 for "no write wait" mode; 1 for "1 write wait" mode; 1 for "2 write wait" mode
   r1: 1.5 for "no read wait" mode; 2 for "1 read wait" mode; 3 for "2 read wait" mode
   r2: 0.5 for "no read wait" mode; 1 for "1 read wait" mode; 1 for "2 read wait" mode

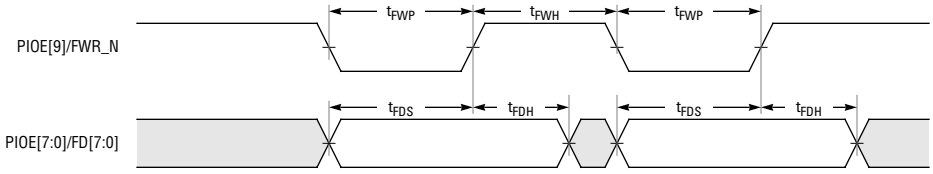


Figure 13. Write Transfer

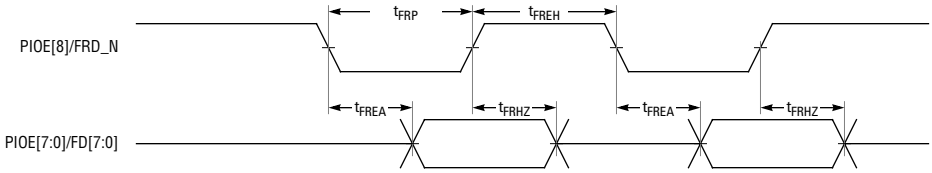


Figure 14. Read Transfer

USB Pins

USB – DC characteristics

(V_{BUS} = 3.0 V to 3.6 V, V_{DD_CORE} = 1.65 V to 1.95 V, TA = –30°C to +70°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Applied pin
Differential input sensitivity	V_{DI}	|(D+) – (D-)|	0.2	—	—	V	D+, D-
Differential common mode range	V_{CM}	VDI included	0.8	—	2.5		
Single-ended receiver threshold voltage	V_{SE}	—	0.8	—	2		
"H" output voltage	V_{OH}	15 kΩ to GND	2.8	—	—	V	D+, D-
		I_{OH} = –100 µA	V_{BUS} – 0.2	—	—		PUCTL
		I_{OH} = –4 mA	2.4	—	—		
"L" output voltage	V_{OL}	1.5 kΩ to 3.6 V	—	—	0.3	V	D+, D-
		I_{OL} = 100 µA	—	—	0.2	V	PUCTL
		I_{OL}= 4 mA	—	—	0.4		
Output leakage current	I_{OZH}	V_{OH} = VBUS	—	—	±10	µA	D+, D-
	I_{OZL}	V_{OL} = 0 V	—	—	±10		

USB - AC characteristics

(V_{BUS} = 3.0 V to 3.6 V, V_{DD_CORE} = 1.65 V to 1.95 V, TA = –30°C to +70°C)

Parameter	Symbol	Condition	Min.	Typ	Max.	Unit	Applied pin
Rise time	Tr	CL = 50 pF	4	—	20	ns	D+, D-
Fall time	Tf	CL = 50 pF	4	—	20	ns	
Rise/fall time ratio	TRFM	(TR/TF)	90	—	111.11	%	
Output signal crossover voltage	VCRS	—	1.3	—	2	V	
Driver output resistance	ZDRV	During steady-state driving	28	—	44	Ω	

USB - ADC Characteristics

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Remarks
Resolution	n	Analog input source impedance Ri < 5 kΩ	—	—	8	bit	
Linearity error	INL		—	±0.5	—	LSB	
Differential linearity error	DNL		—	±0.5	—	LSB	
Zero scale error	Efs		—	+2	—	LSB	
Full scale error	Ezs		—	-2	—	LSB	
Conversion time	Tconv		6.7	—	26.7	µs	per 1 channel

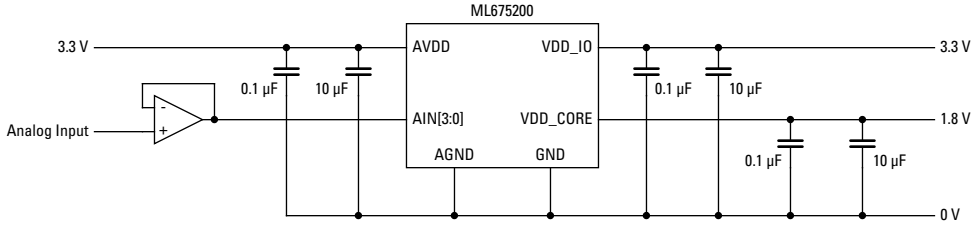
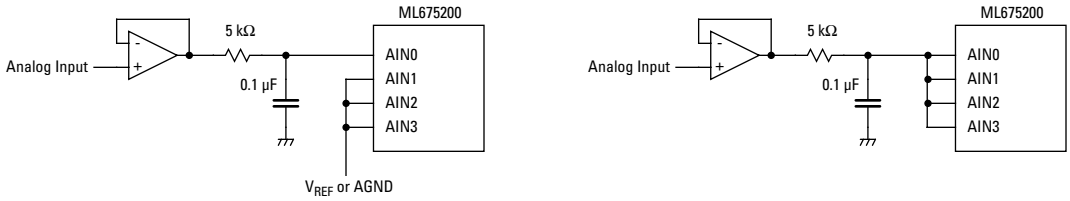


Figure 15. A/D External Filter Circuit



Crosstalk is the difference between the A/D conversion results when the same analog input is applied to AIN0 through AIN3 (right side of figure) and the A/D conversion results of the circuit on the left.

Figure 16. Crosstalk Measurements

JTAG Pins (ARM Side, Teak DSP Side)

AC characteristics

(V_{BUS} = 3.0 V to 3.6 V, V_{DD_CORE} = 1.65 V to 1.95 V, TA = –30°C to +70°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Applied pin
nTRST input pulse width	f_{W_NTRST}	CL = 50 pF	—	—	1	µs	NTRSTA
TCK maximum frequency	t_{TCK}		—	—	5	MHz	TCKA, TCKT
TDI input setup time	t_{S_TDI}		25	—	—	ns	TDIA, TDIT
TDI input hold time	t_{H_TDI}		25	—	—	ns	
TMS input setup time	t_{S_TMS}		25	—	—	ns	TMSA, TMST
TMS input hold time	t_{H_TMS}		25	—	—	ns	
TDO output delay time	t_{D_TDO}		—	—	100	ns	TDOA, TDOT
TINTP output delay time	t_{D_TINT}		—	—	100	ns	TINTP

Development Environment

- SDT2.51

  ARM Software Development Toolkit (C Compiler, C Linker, Assembler)

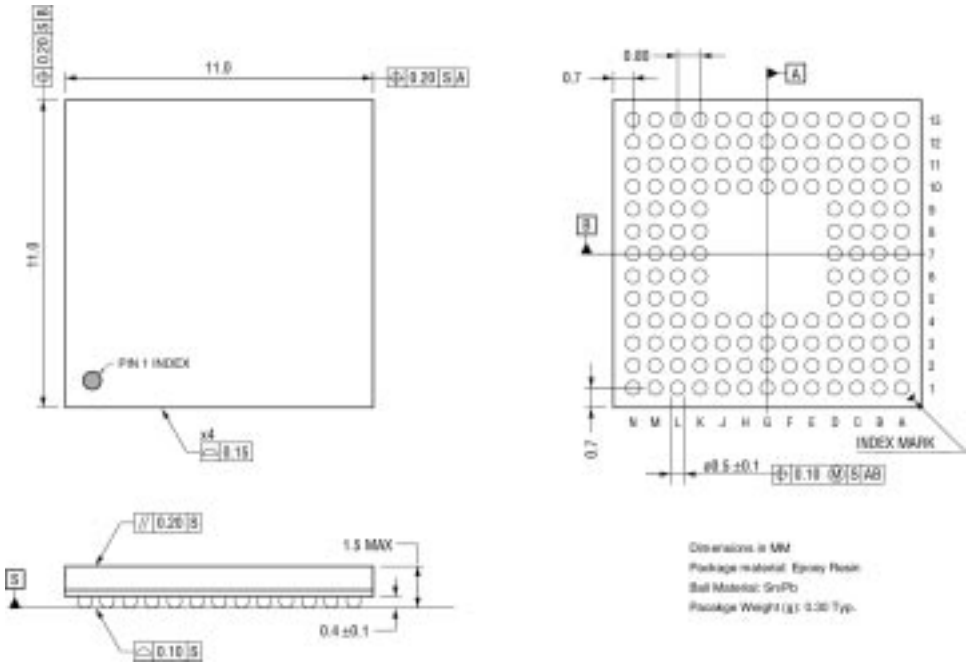
- Oki ADI board

  Interface board for device having the same interface as ARM Multi-ICE. Oki is selling it under license from ARM.

- ML675200 SDK (Under Development)

  Digital audio player software development kit (Sample software and board etc.)

Package Dimensions



Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage.

Therefore, before performing reflow mounting, contact the responsible Oki sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

Figure 17. P-LFBGA144-1111-0.80

Related Oki Documents for the ML675200/Q5200 [1]

Document	Date
ML675200 User's Manual	April, 2003

1. Available on the Oki Semiconductor web site www.okisemi.com/us.

Notice

The information contained herein can change without notice owing to product and/or technical improvements.

Please make sure before using the product that the information you are referring to is up-to-date.

The outline of action and examples of application circuits described herein have been chosen as an explanation of the standard action and performance of the product. When you actually plan to use the product, please ensure that the outside conditions are reflected in the actual circuit and assembly designs.

Oki assumes no responsibility or liability whatsoever for any failure or unusual or unexpected operation resulting from misuse, neglect, improper installation, repair, alteration or accident, improper handling, or unusual physical or electrical stress including, but not limited to, exposure to parameters outside the specified maximum ratings or operation outside the specified operating range.

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April 2003

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