LZ1440 BiCMOS High Voltage Driver IC

Description

The LZ1440 is a 40-bit serial input/parallel output high voltage driver IC fabricated using BiCMOS process technology. This driver consists of two 20-bit shift registers, latch circuit, and high voltage push-pull type driver unit.

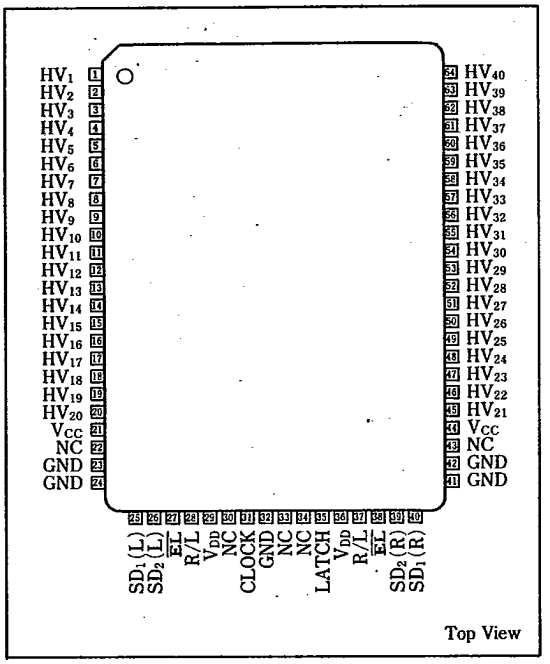
As for the data shift system, it features a double speed transfer system in which shift register 1 and shift register 2 are shifted at clock rise and fall respectively.

It is best suited to use in EL display panels and plasma display panels.

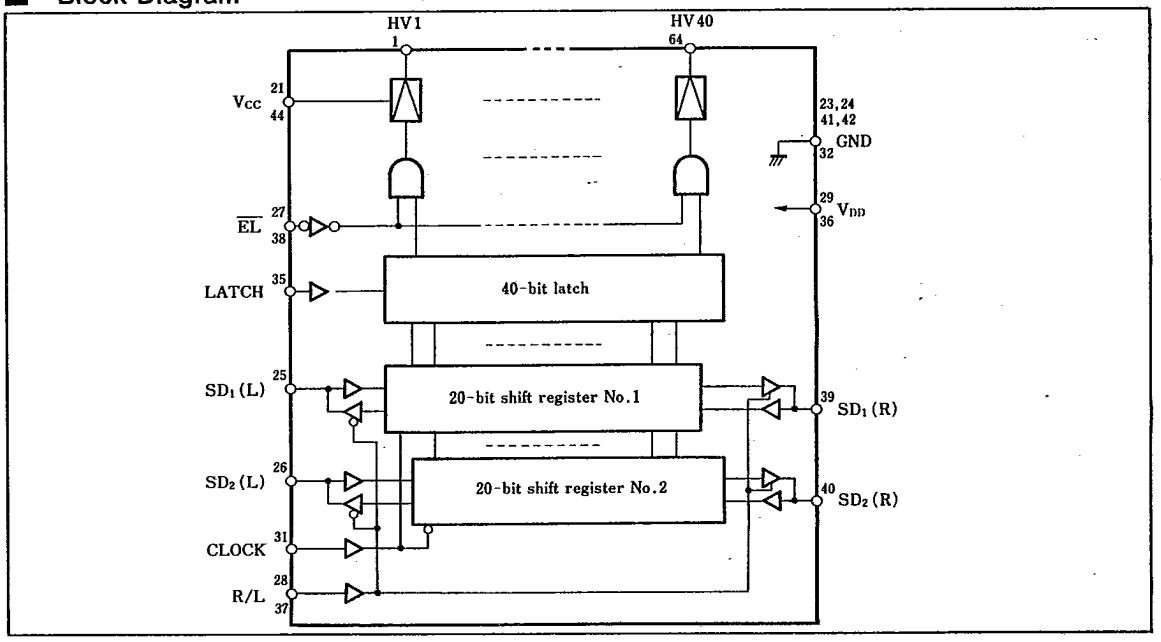
Features

1. High voltage output : 70V
2. Large current drive output : ±15mA (MAX.)
3. Push-pull output : 40 outputs
4. High-speed data transfer : 8MHz
5. Bidirectional data shift function
6. 64-pin flat package (ternary directions)

Pin Connections



Block Diagram



Pin Functions

Pin No.	I/O	Symbol	Pin name	Pin No.	I/O	Symbol	Pin name
1	O	HV_1	Driver output 1	33		NC	Non-connection
2	O	HV_2	Driver output 2	34		NC	Non-connection
3	O	HV_3	Driver output 3	35	I	LATCH	Latch
4	O	HV_4	Driver output 4	36		V_{DD}	Power supply
5	O	HV_5	Driver output 5	37	I	R/L	Shift direction selector
6	O	HV_6	Driver output 6	38	I	$\overline{EL}$	Output all "Low"
7	O	HV_7	Driver output 7	39	I/O	$SD_2(R)$	Data input and output 2
8	O	HV_8	Driver output 8	40	I/O	$SD_1(R)$	Data input and output 1
9	O	HV_9	Driver output 9	41		GND	Ground (driver)
10	O	HV_{10}	Driver output 10	42		GND	Ground (driver)
11	O	HV_{11}	Driver output 11	43		NC	Non-connection
12	O	HV_{12}	Driver output 12	44		V_{CC}	Power supply
13	O	HV_{13}	Driver output 13	45	O	HV_{21}	Driver output 21
14	O	HV_{14}	Driver output 14	46	O	HV_{22}	Driver output 22
15	O	HV_{15}	Driver output 15	47	O	HV_{23}	Driver output 23
16	O	HV_{16}	Driver output 16	48	O	HV_{24}	Driver output 24
17	O	HV_{17}	Driver output 17	49	O	HV_{25}	Driver output 25
18	O	HV_{18}	Driver output 18	50	O	HV_{26}	Driver output 26
19	O	HV_{19}	Driver output 19	51	O	HV_{27}	Driver output 27
20	O	HV_{20}	Driver output 20	52	O	HV_{28}	Driver output 28
21		V_{CC}	Power supply	53	O	HV_{29}	Driver output 29
22		NC	Non-connection	54	O	HV_{30}	Driver output 30
23		GND	Ground (driver)	55	O	HV_{31}	Driver output 31
24		GND	Ground (driver)	56	O	HV_{32}	Driver output 32
25	I/O	$SD_1(L)$	Data input and output 1	57	O	HV_{33}	Driver output 33
26	I/O	$SD_2(L)$	Data input and output 2	58	O	HV_{34}	Driver output 34
27	I	$\overline{EL}$	Output all "Low"	59	O	HV_{35}	Driver output 35
28	I	R/L	Shift direction selector	60	O	HV_{36}	Driver output 36
29		V_{DD}	Power supply	61	O	HV_{37}	Driver output 37
30		NC	Non-connection	62	O	HV_{38}	Driver output 38
31	I	CLOCK	Clock	63	O	HV_{39}	Driver output 39
32		GND	Ground (logic)	64	O	HV_{40}	Driver output 40

■ Absolute Maximum Ratings

(Ta=25℃)

Parameter		Symbol	Conditions	Rating	Unit
Supply voltage	Logic	V_{DD}	Reference to GND	−0.3 to+7.0	V
	Driver	V_{CC}	Reference to GND	−0.3 to+70	V
Input voltage		V_{IN}	Reference to GND	−0.3 to (V_{DD}+0.3)	V
Power dissipation		P_D		900	mW
P_D derating ratio		ΔP_D/℃	Ta≧25℃	8	mW/℃
Operating temperature		T_{opr}		−40 to+85	℃
Storage temperature		T_{stg}		−55 to+150	℃

■ Recommended Operating Conditions

(Ta=−40 to +85℃)

Parameter		Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Supply voltage	Logic	V_{DD}		4.5	5.0	5.5	V
	Driver	V_{CC}			60		V
Output "High" current		I_{OH}	SD pin			−2	mA
			HVn pins			−15	mA
Output "Low" current		I_{OL}	SD pin			2	mA
			HVn pins			15	mA
Input voltage		V_{IN}		0		V_{DD}	V
Clock frequency		f_{CLK}				8	MHz
Clock pulse width		$t_{W(CLK)}$		60			ns

■ DC Characteristics

(V_{DD}=4.5 to 5.5V, V_{CC}=60V, Ta=−40 to+85℃)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input "High" voltage	V_{IH}			V_{DD}−1.0		V_{DD}	V
Input "Low" voltage	V_{IL}			0		1.0	V
Input current	I_{IN}	V_{IN}=GND or V_{DD}				±10	μA
Output "High" voltage	V_{OH}	SD pin	I_{OH}=−0.5mA	V_{DD}−1.0			V
		HVn pins	I_{OH}=−10μA	V_{CC}−4.0			V
			I_{OH}=−12mA	V_{CC}−8.0			V
Output "Low" voltage	V_{OL}	SD pin	I_{OL}=0.5mA			1.0	V
		HVn pins	I_{OL}=10μA			1.0	V
			I_{OL}=12mA			5	V
Output diode voltage	V_F	I_F=−12mA				−2.5	V
Current consumption (V_{DD}=5V, V_{CC}=60V)	I_{DD1}	All input pins : GND potential All output pins : Open				500	μA
	I_{DD2}	f_{CLK}=6MHz, f_{SD}=3MHz, C_L=20pF LATCH, $\overline{EL}$, R/L pins : V_{DD} potential				12	mA
	I_{CCH}	All HV output pins : "High"				12	mA
	I_{CCL}	All HV output pins : "Low"				10	μA

■ AC Characteristics

(V_{DD}=4.5 to 5.5V, V_{CC}=60V, Ta=−40 to+85℃, V_{IN}=V_{DD} or GND)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Maximum operating frequency	f(max)		8			MHz
Propagation "High" time	t_{PLH}	CLOCK-SD C_L=20pF			100	ns
		CLOCK-HVn C_L=2200pF			10	μs
		LATCH-HVn C_L=2200pF			10	μs
		$\overline{EL}$-HVn C_L=2200pF			10	μs
Propagation "Low" time	t_{PHL}	CLOCK-SD C_L=20pF			100	ns
		CLOCK-HVn C_L=2200pF			8	μs
		LATCH-HVn C_L=2200pF			8	μs
		$\overline{EL}$-HVn C_L=2200pF			8	μs
Pulse width	t_W	CLOCK	60			ns
		LATCH	60			ns
Data setup time	t_{setup}		25			ns
Latch setup time	t_{Lsetup}		60			ns
Data hold time	t_{hold}		10			ns
Clock rise time	t_r				500	ns
Clock fall time	t_f				500	ns
Maximum output rise time	t_{or}	HVn pins C_L=2200pF			10	μs
Maximum output fall time	t_{of}	HVn pins C_L=2200pF			10	μs

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■ Pin Descriptions

(1) CLOCK (Pin 31)

The CLOCK input for an internal shift register : the shift register 1 (HV_1, HV_3, HV_5,⋯HV_{39} outputs) shifts at the input rising edge, while the shift register 2 (HV_2, HV_4, HV_6, ⋯HV_{40} outputs) shifts at the falling edge.

(2) LATCH (Pin 35)

The LATCH input pin is used to latch the shift register output. If it is in High level, the shift register output is transferred to the output buffer as it is. If it is in Low level, the data just before going Low is latched.

(3) $\overline{EL}$ (Pins 27 and 38)

The $\overline{EL}$ pin is used to control the output buffer. If it is in High level, the latch circuit output is transferred to the output buffer, while it is in Low level, all driver outputs go Low.

(4) R/L (Pins 28 and 37)

The R/L pin is used to switch the shifting direction of shift registers. If it is in High level the shift register shifts in forward direction, while it shifts in reverse direction in Low level.

(5) SD_1 (L), SD_2 (L), SD_1 (R), and SD_2 (R) (Pins 25, 26, 40 and 39)

The SD_1 (L), SD_2 (L), SD_1 (R) and SD_2 (R) are data I/O pins for shift registers 1 and 2. When High level is given, the driver output becomes High, and when Low level is given, the driver output becomes Low. (In case LATCH=High, EL=High)

(6) HVn (n=1-40) (Pins 1-20, 45-64)

The HVn are high voltage driver output pins which consist of push-pull outputs with N-channel DMOS for the source and N-channel DMOS for the sink.

(7) V_{CC} (Pins 21 and 44)

Both V_{CC} pins are the power supply inputs for the output buffer.

(8) V_{DD} (Pins 29 and 36)

Both V_{DD} pins are the power supply inputs for the logic unit.

(9) GND (Pins 23, 24, 32 41 and 42)

GND pins are the reference power supply inputs.

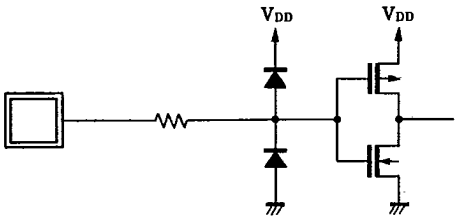
■ Precautions

As for the power supply pins (V_{DD}, V_{CC} and GND), pins with the same signal name should be externally connected to use on the same potential.

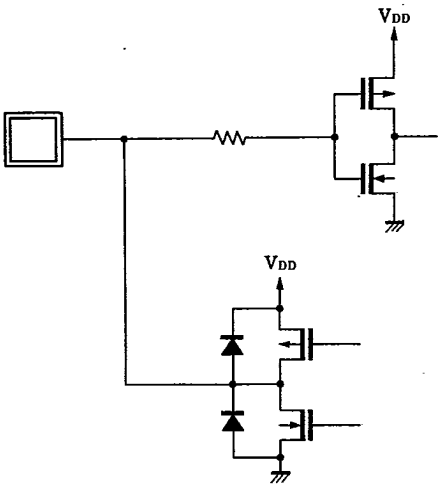
As the $\overline{EL}$ pins 27 and 38, and the R/L pins 28 and 37 are inter-connected respectively, the signal may be input only to one of the two. These interconnected signals can be connected in daisy chain fashion. In this case, note that the number of devices to be connected is not limitless, and care must be taken for the signal delay. Be sure not to put the signal line out from the middle of the daisy chain to connect the other device input.

■ Input/Output Circuit Configuration

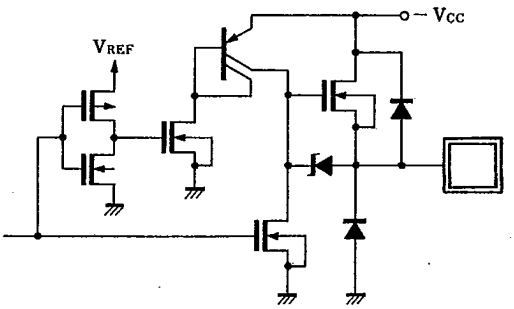
(1) CLOCK, LATCH, $\overline{EL}$, R/L pins (Input)



(2) SD_1 (L), SD_2 (L), SD_1 (R), SD_2 (R) pins (I/O)



(3) HVn (n=1-40) pins (High voltage output)



■ Truth Table

Input				Input and output				Driver output						
CLOCK	LATCH	$\overline{EL}$	R/L	SD_1(L)	SD_2(L)	SD_1(R)	SD_2(R)	HV_1	HV_2	HV_3	HV_4	···	HV_{39}	HV_{40}
↑	H	H	H	Dn	Dń	Dn-19	Dń-20	Dn	Dń-1	Dn-1	Dń-2	···	Dn-19	Dń-20
↓	H	H	H	Dn	Dń	Dn-20	Dń-19	Dn-1	Dń	Dn-2	Dń-1	···	Dn-20	Dń-19
↑	L	H	H	Dn	Dń	Dn-19	Dń-20	Dn-1	Dń-1	Dn-2	Dń-2	···	Dn-20	Dń-20
↓	L	H	H	Dn	Dń	Dn-20	Dń-19	Dn-1	Dń-1	Dn-2	Dń-2	···	Dn-20	Dń-20
↑	H	L	H	Dn	Dń	Dn-19	Dń-20	L	L	L	L	···	L	L
↓	H	L	H	Dn	Dń	Dn-20	Dń-19	L	L	L	L	···	L	L
↑	L	L	H	Dn	Dń	Dn-19	Dń-20	L	L	L	L	···	L	L
↓	L	L	H	Dn	Dń	Dn-20	Dń-19	L	L	L	L	···	L	L
↑	H	H	L	Dn-19	Dń-20	Dn	Dń	Dn-19	Dń-20	Dn-18	Dń-19	···	Dn	Dń-1
↓	H	H	L	Dn-20	Dń-19	Dn	Dń	Dn-20	Dń-19	Dn-18	Dń-18	···	Dn-1	Dń
↑	L	H	L	Dn-19	Dń-20	Dn	Dń	Dn-20	Dń-20	Dn-19	Dń-19	···	Dn-1	Dń-1
↓	L	H	L	Dn-20	Dń-19	Dn	Dń	Dn-20	Dń-20	Dn-19	Dń-19	···	Dn-1	Dń-1
↑	H	L	L	Dn-19	Dń-20	Dn	Dń	L	L	L	L	···	L	L
↓	H	L	L	Dn-20	Dń-19	Dn	Dń	L	L	L	L	···	L	L
↑	L	L	L	Dn-19	Dń-20	Dn	Dń	L	L	L	L	···	L	L
↓	L	L	L	Dn-20	Dń-19	Dn	Dń	L	L	L	L	···	L	L

LATCH and $\overline{EL}$ are asynchronous for CLOCK.
I/O data inside ▭ represent the input data.

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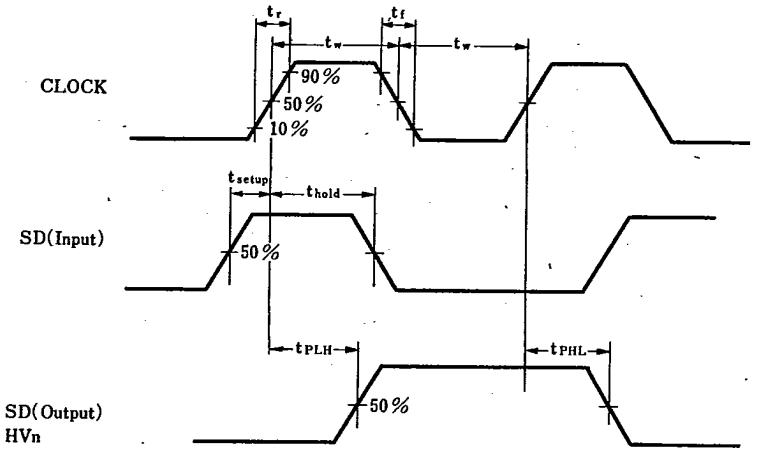
■ Shift Direction

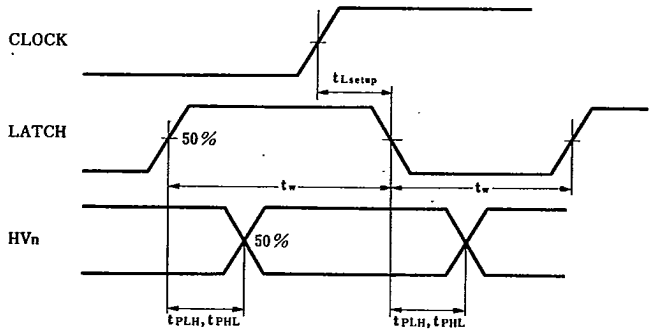
R/L pin	Data input	Shift sequence	Data output	Remarks
H	SD_1 (L)	$HV_1 \rightarrow HV_3 \rightarrow HV_5 \rightarrow$ ···· $\rightarrow HV_{39}$	SD_1 (R)	Forward
	SD_2 (L)	$HV_2 \rightarrow HV_4 \rightarrow HV_6 \rightarrow$ ···· $\rightarrow HV_{40}$	SD_2 (R)	directiron
L	SD_1 (R)	$HV_{39} \rightarrow HV_{37} \rightarrow HV_{35} \rightarrow$ ···· $\rightarrow HV_1$	SD_1 (L)	Reverse
	SD_2 (R)	$HV_{40} \rightarrow HV_{38} \rightarrow HV_{36} \rightarrow$ ···· $\rightarrow HV_2$	SD_2 (L)	directiron

■ Timing Diagrams

(1) CLOCK-SD, HVn



(2) CLOCK-LATCH-HVn



(3) $\overline{EL}$-HVn