Integrated Device Technology, Inc.

CMOS DUAL-PORT RAM 8K (1K x 8-BIT)

IDT7130SA/LA
IDT7140SA/LA

FEATURES

- High-speed access
  - —Military: 25/35/55/100ns (max.)
  - —Commercial: 25/35/55/100ns (max.)
  - —Commercial: 20ns in PLCC only for 7130
- Low-power operation
  - —IDT7130/IDT7140SA
    - Active: 325mW (typ.)
    - Standby: 5mW (typ.)
  - —IDT7130/IDT7140LA
    - Active: 325mW (typ.)
    - Standby: 1mW (typ.)
- MASTER IDT7130 easily expands data bus width to 16-or-more-bits using SLAVE IDT7140
- On-chip port arbitration logic (IDT7130 Only)
- $\overline{BUSY}$ output flag on IDT7130; $\overline{BUSY}$ input on IDT7140
- $\overline{INT}$ flag for port-to-port communication
- Fully asynchronous operation from either port
- Battery backup operation–2V data retention
- TTL-compatible, single 5V ±10% power supply
- Military product compliant to MIL-STD-883, Class B
- Standard Military Drawing #5962-86875
- Industrial temperature range (–40°C to +85°C) is available, tested to military electrical specifications

DESCRIPTION

The IDT7130/IDT7140 are high-speed 1K x 8 Dual-Port Static RAMs. The IDT7130 is designed to be used as a stand-alone 8-bit Dual-Port RAM or as a "MASTER" Dual-Port RAM together with the IDT7140 "SLAVE" Dual-Port in 16-bit-or-more word width systems. Using the IDT MASTER/SLAVE Dual-Port RAM approach in 16-or-more-bit memory system applications results in full-speed, error-free operation without the need for additional discrete logic.

Both devices provide two independent ports with separate control, address, and I/O pins that permit independent asynchronous access for reads or writes to any location in memory. An automatic power down feature, controlled by $\overline{CE}$, permits the on chip circuitry of each port to enter a very low standby power mode.

Fabricated using IDT's CMOS high-performance technology, these devices typically operate on only 325mW of power. Low-power (LA) versions offer battery backup data retention capability, with each Dual-Port typically consuming 200µW from a 2V battery.

The IDT7130/IDT7140 devices are packaged in 48-pin sidebraze or plastic DIPs, LCCs, or flatpacks, 52-pin PLCCs and 64-pin TQFPs. Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

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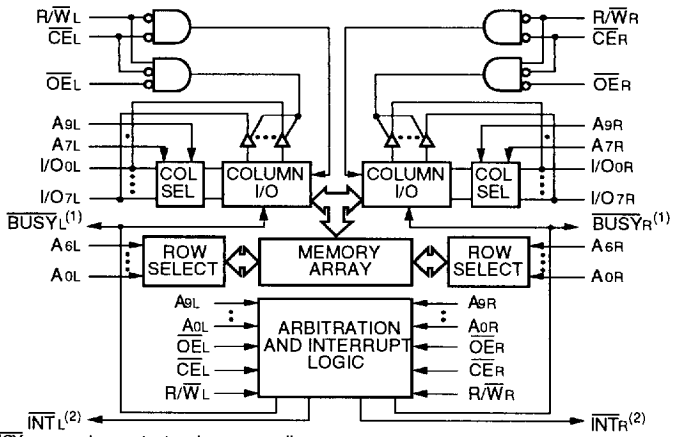
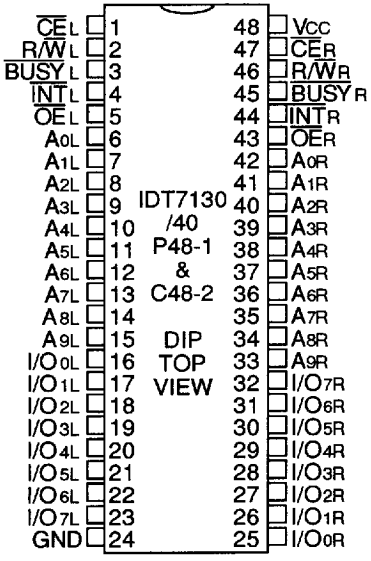
FUNCTIONAL BLOCK DIAGRAM

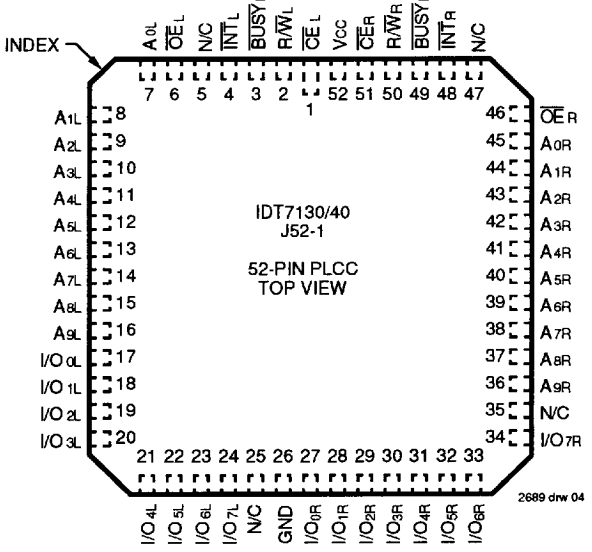


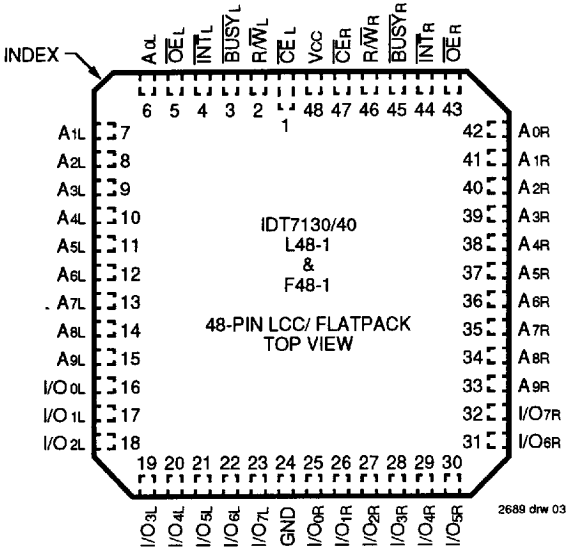
NOTES:
1 IDT7130 (MASTER): $\overline{BUSY}$ is open drain output and requires pullup resistor
IDT7140 (SLAVE) $\overline{BUSY}$ is input
2 Open drain output: requires pullup resistor

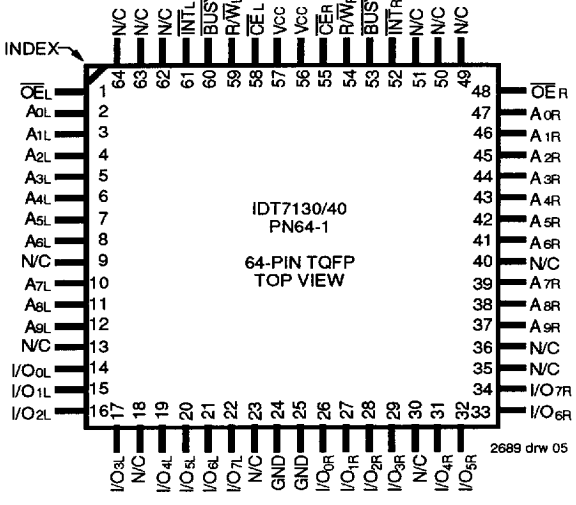
PIN CONFIGURATIONS



2689 drw 02







* Index Indicator is PIN 1 ID in package outline.

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
I_{OUT}	DC Output Current	50	50	mA

2689 tbl 01

NOTE:
1 Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2 V_{TERM} must not exceed V_{CC} + 0.5V.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6.0(2)	V
V_{IL}	Input Low Voltage	–0.5(1)	—	0.8	V

2689 tbl 02

NOTE:
1 V_{IL} (min) = -3.0V for pulse width less than 20ns
2 V_{TERM} must not exceed Vcc + 0.5V.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Military	–55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

2689 tbl 03

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE (V_{CC} = 5.0V ± 10%)

Symbol	Parameter	Test Conditions	7130SA 7140SA Min.	7130SA 7140SA Max.	7130LA 7140LA Max.	7130LA 7140LA Max.	Unit
$\|I_{LI}\|$	Input Leakage Current(1)	2.0 ≤ V_{CC} ≤ 5.5V, V_{IN} = 0V to V_{CC}	—	10	—	5	µA
$\|I_{LO}\|$	Output Leakage Current(1)	2.0 ≤ V_{CC} ≤ 5.5V, $\overline{CE}$ = V_{IH}, V_{OUT} = 0V to V_{CC}	—	10	—	5	µA
V_{OL}	Output Low Voltage (I/O0-I/O7)	I_{OL} = 4mA	—	0.4	—	0.4	V
V_{OL}	Open Drain Output Low Voltage ($\overline{BUSY}$, $\overline{INT}$)	I_{OL} = 16mA	—	0.5	—	0.5	V
V_{OH}	Output High Voltage	I_{OH} = -4mA	2.4	—	2.4	—	V

2689 tbl 04

NOTES:
1 At Vcc<2.0V leakages are undefined

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DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[1,6] (V_{CC} = 5.0V ± 10%)

Symbol	Parameter	Test Conditions	Version		7130x20[2] Typ.	7130x20[2] Max.	7130x25[3] 7140x25[3] Typ.	7130x25[3] 7140x25[3] Max.	7130x35 7140x35 Typ.	7130x35 7140x35 Max.	7130x55 7140x55 Typ.	7130x55 7140x55 Max.	7130x100 7140x100 Typ.	7130x100 7140x100 Max.	Unit
I_{CC}	Dynamic Operating Current (Both Ports Active)	$\overline{CE}$ = V_{IL}, Outputs open, f = f_{MAX}[4]	MIL	SA	—	—	125	300	125	290	65	230	65	190	mA
				LA	—	—	125	240	125	230	65	185	65	155	
			COM'L.	SA	125	265	125	260	75	195	65	180	65	180	
				LA	125	215	125	210	75	155	65	140	65	130	
I_{SB1}	Standby Current (Both Ports - TTL Level Inputs)	$\overline{CE}_L$ and $\overline{CE}_R \geq V_{IH}$, f = f_{MAX}[4]	MIL	SA	—	—	30	80	30	80	25	65	25	65	mA
				LA	—	—	30	60	30	60	25	55	25	45	
			COM'L.	SA	30	65	30	65	25	65	25	65	25	55	
				LA	30	45	30	45	25	45	25	45	25	35	
I_{SB2}	Standby Current (One Port - TTL Level Inputs)	$\overline{CE}_L$ or $\overline{CE}_R \geq V_{IH}$ Active Port Outputs Open, f = f_{MAX}[4]	MIL.	SA	—	—	80	195	80	185	40	135	40	125	mA
				LA	—	—	80	160	80	150	40	110	40	100	
			COM'L.	SA	80	180	80	175	40	130	40	115	40	110	
				LA	80	145	80	140	40	95	40	85	40	75	
I_{SB3}	Full Standby Current (Both Ports - All CMOS Level Inputs	$\overline{CE}_L$ and $\overline{CE}_R \geq V_{CC}$ -0 2V, $V_{IN} \geq V_{CC}$ -0.2V or $V_{IN} \leq$ 0.2V, f = 0[5]	MIL.	SA	—	—	1 0	30	1.0	30	1.0	30	1 0	30	mA
				LA	—	—	0.2	10	0.2	10	0.2	10	0.2	10	
			COM'L	SA	1 0	15	1 0	15	1.0	15	1 0	15	1 0	15	
				LA	0 2	5	0.2	5	0.2	4	0.2	4	0.2	4	
I_{SB4}	Full Standby Current (One Port - All CMOS Level Inputs)	$\overline{CE}_L$ or $\overline{CE}_R \geq V_{CC}$ -0.2V, $V_{IN} \geq V_{CC}$ -0.2V or $V_{IN} \leq$ 0 2V, Active Port Outputs Open, f = f_{MAX}[4]	MIL	SA	—	—	70	185	70	175	40	120	40	110	mA
				LA	—	—	70	150	70	140	35	90	35	80	
			COM'L.	SA	70	175	70	170	40	115	40	100	40	95	
				LA	70	140	70	135	35	90	35	75	35	70	

NOTES:

2689 tbl 05

1. x in part numbers indicates power rating (SA or LA)
2. 0°C to +70°C temperature range only, PLCC package only.
3. Not available in DIP packages..
4. At f = f_{Max}, address and control lines (except Output Enable) are cycling at the maximum frequency read cycle of 1/t_{RC}, and using "AC TEST CONDITIONS" of input levels of GND to 3V
5. f = 0 means no address or control lines change. Applies only to inputs at CMOS level standby
6. V_{CC}=5V, T_A=+25°C for Typ.

DATA RETENTION CHARACTERISTICS (LA Version Only)

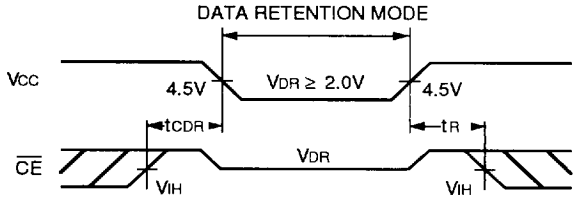
Symbol	Parameter	Test Conditions		IDT7130LA/IDT7140LA Min.	Typ.[1]	Max.	Unit
V_{DR}	V_{CC} for Data Retention	V_{CC} = 2 0V, $\overline{CE} \geq V_{CC}$ -0.2V $V_{IN} \geq V_{CC}$ -0.2V or $V_{IN} \leq$ 0 2V		2.0	—	—	V
I_{CCDR}	Data Retention Current		Mil.	—	100	4000	µA
			Com'l.	—	100	1500	µA
t_{CDR}[3]	Chip Deselect to Data Retention Time			0	—	—	ns
t_R[3]	Operation Recovery Time			t_{RC}[2]	—	—	ns

NOTES:

2689 tbl 06

1. V_{CC} = 2V, T_A = +25°C
2. t_{RC} = Read Cycle Time
3. This parameter is guaranteed but not tested

DATA RETENTION WAVEFORM



2689 drw 06

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1, 2, and 3

2689 tbl 07

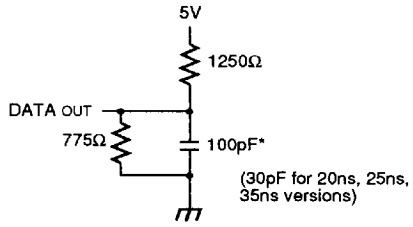


Figure 1. Output Load

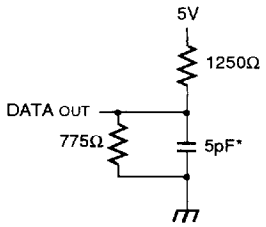


Figure 2. Output Load
(for tHZ, tLZ, tWZ, and tOW)

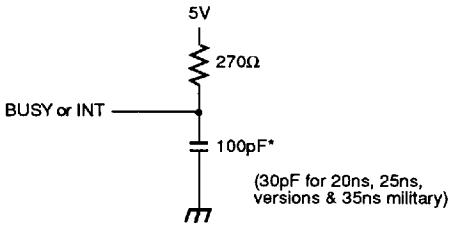


Figure 3. $\overline{BUSY}$ and $\overline{INT}$ Output Load

2689 drw 07

* Including scope and jig

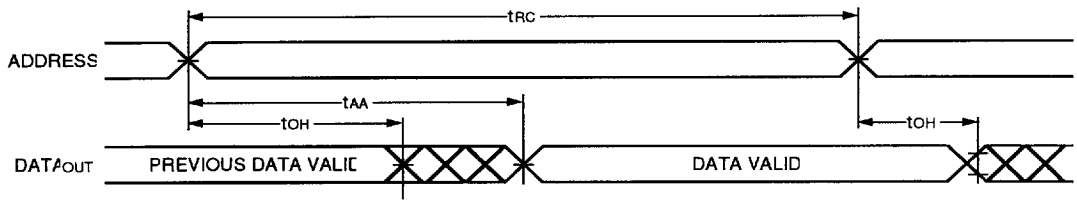
AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[3]

Symbol	Parameter	7130x20[2] Min.	7130x20[2] Max.	7130x25[5] 7140x25[5] Min.	7130x25[5] 7140x25[5] Max.	7130x35 7140x35 Min.	7130x35 7140x35 Max.	7130x55 7140x55 Min.	7130x55 7140x55 Max.	7130x100 7140x100 Min.	7130x100 7140x100 Max.	Unit
Read Cycle												
tRC	Read Cycle Time	20	—	25	—	35	—	55	—	100	—	ns
tAA	Address Access Time	—	20	—	25	—	35	—	55	—	100	ns
tACE	Chip Enable Access Time	—	20	—	25	—	35	—	55	—	100	ns
tAOE	Output Enable Access Time		11	—	12	—	25	—	35	—	40	ns
tOH	Output Hold From Address Change	0	—	0	—	0	—	0	—	10	—	ns
tLZ	Output Low-Z Time[1,4]	0	—	0	—	0	—	5	—	5	—	ns
tHZ	Output High-Z Time[1,4]	—	10	—	10	—	15	—	25	—	40	ns
tPU	Chip Enable to Power Up Time[4]	0	—	0	—	0	—	0	—	0	—	ns
tPD	Chip Disable to Power Down Time[4]	—	50	—	50	—	50	—	50	—	50	ns

NOTES:
2689 tbl 08

1. Transition is measured ±500mV from low or high impedance voltage load (Figure 2).
2. 0°C to +70°C temperature range only, PLCC package only.
3. "x" in part numbers indicates power rating (SA or LA).
4. This parameter is guaranteed but not tested
5 Not available in DIP packages.

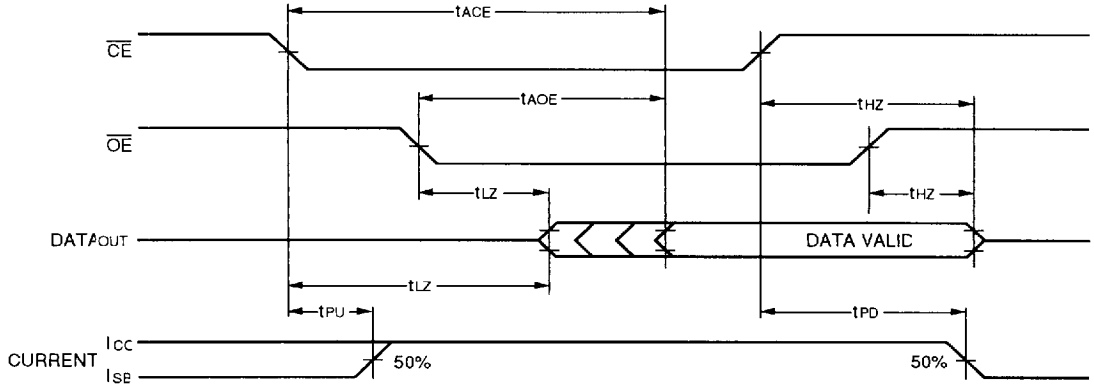
TIMING WAVEFORM OF READ CYCLE NO. 1, EITHER SIDE[1,2,4]



NOTES:
2689 drw 08

1. R/$\overline{W}$ is high for Read Cycles.
2. Device is continuously enabled, $\overline{CE}$ = VIL.
3. Addresses valid prior to or coincident with $\overline{CE}$ transition low.
4. $\overline{OE}$ = VIL.

TIMING WAVEFORM OF READ CYCLE NO. 2, EITHER SIDE(1,3)



NOTES:
1 R/W is high for Read Cycles.
2 Device is continuously enabled, CE = VIL
3 Addresses valid prior to or coincident with CE transition low
4 OE = VIL

2689 drw 09

AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE(5)

Symbol	Parameter	7130x20(2) Min.	7130x20(2) Max.	7130x25(6) 7140x25(6) Min.	7130x25(6) 7140x25(6) Max.	7130x35 7140x35 Min.	7130x35 7140x35 Max.	7130x55 7140x55 Min.	7130x55 7140x55 Max.	7130x100 7140x100 Min.	7130x100 7140x100 Max.	Unit
Write Cycle												
tWC	Write Cycle Time(3)	20	—	25	—	35	—	55	—	100	—	ns
tEW	Chip Enable to End-of-Write	15	—	20	—	30	—	40	—	90	—	ns
tAW	Address Valid to End-of-Write	15	—	20	—	30	—	40	—	90	—	ns
tAS	Address Set-up Time	0	—	0	—	0	—	0	—	0	—	ns
tWP	Write Pulse Width(4)	15	—	15	—	25	—	30	—	55	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	0	—	0	—	ns
tDW	Data Valid to End-of-Write	10	—	12	—	15	—	20	—	40	—	ns
tHZ	Output High-Z Time(1)	—	10	—	10	—	15	—	25	—	40	ns
tDH	Data Hold Time	0	—	0	—	0	—	0	—	0	—	ns
tWZ	Write Enabled to Output in High-Z(1)	—	10	—	10	—	15	—	30	—	40	ns
tOW	Output Active From End-of-Write(1)	0	—	0	—	0	—	0	—	0	—	ns

NOTES:
1 Transition is measured ±500mV from low or high impedance voltage with load(Figure 2) This parameter guaranteed but not tested
2. 0°C to +70°C temperature range only, PLCC package only
3 For MASTER/SLAVE combination, tWC = tBAA + tWP
4. Specified for OE at high (Refer to "Timing Waveform of Write Cycle", Note 6)
5 "x" in part numbers indicates power rating (SA or LA)
6 Not available in DIP packages

2689 tbl 09

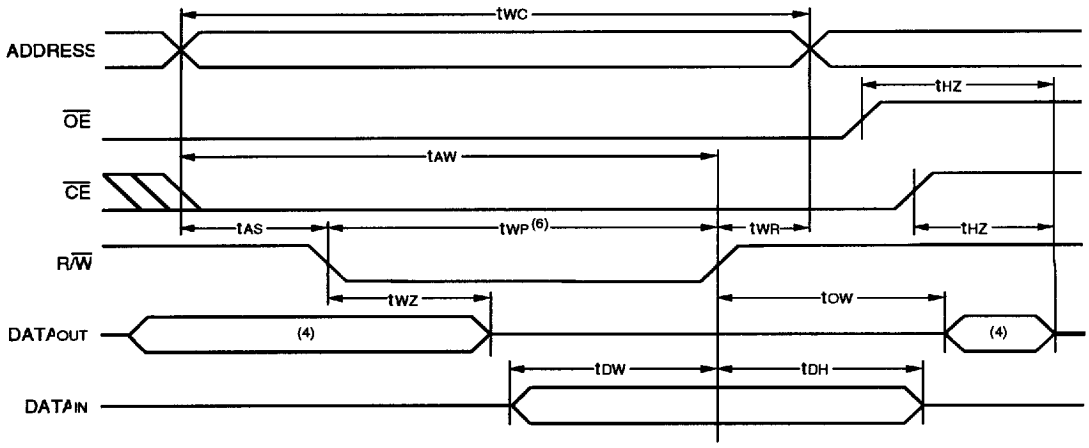
CAPACITANCE (TA = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Max.	Unit
CIN	Input Capacitance	VIN = 0V	11	pF
COUT	Output Capacitance	VIN = 0V	11	pF

NOTE:
1 This parameter is determined by device characterization but is not production tested

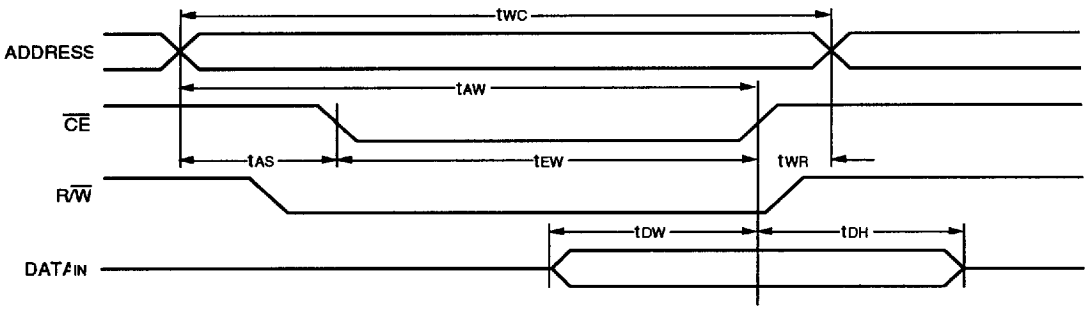
2689 tbl 10

TIMING WAVEFORM OF WRITE CYCLE NO. 1, (R/$\overline{W}$ CONTROLLED TIMING)(1,2,3,6)



2689 drw 10

TIMING WAVEFORM OF WRITE CYCLE NO. 2, ($\overline{CE}$ CONTROLLED TIMING)(1,2,3,5)



2689 drw 11

NOTES:
1. Either R/$\overline{W}$ or $\overline{CE}$ must be high during all address transitions.
2. A write occurs during the overlap (tEW or tWP) of a low $\overline{CE}$ and a low R/$\overline{W}$.
3. tWR is measured from the earlier of $\overline{CE}$ or R/$\overline{W}$ going high to the end of the write cycle.
4. During this period, the I/O pins are in the output state and input signals must not be applied.
5. If the $\overline{CE}$ low transition occurs simultaneously with or after the R/$\overline{W}$ low transition, the outputs remain in the high impedance state.
6. If $\overline{OE}$ is low during a R/$\overline{W}$ controlled write cycle, the write pulse width must be larger of tWP or (tWZ + tDW) to allow the I/O drivers to turn off and data to be placed on the bus for the required tDW. If $\overline{OE}$ is high during an R/$\overline{W}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified tWP.

AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[7]

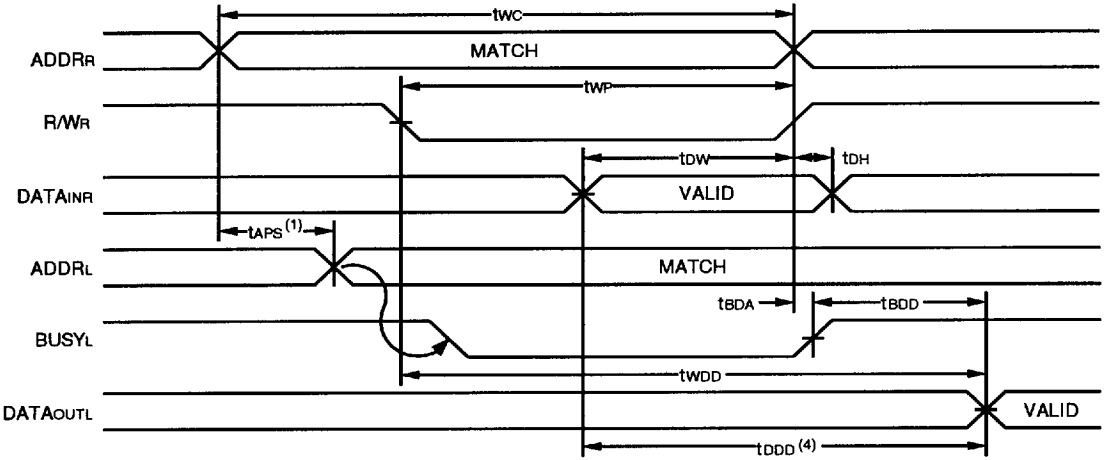
Symbol	Parameter	7130x20[1] Min.	7130x20[1] Max.	7130x25[9] 7140x25[9] Min.	7130x25[9] 7140x25[9] Max.	7130x35 7140x35 Min.	7130x35 7140x35 Max.	7130x55 7140x55 Min.	7130x55 7140x55 Max.	7130x100 7140x100 Min.	7130x100 7140x100 Max.	Unit
Busy Timing (For Master IDT7130 Only)												
t_{BAA}	$\overline{BUSY}$ Access Time from Address	—	25	—	25	—	35	—	45	—	50	ns
t_{BDA}	$\overline{BUSY}$ Disable Time from Address	—	20	—	20	—	30	—	40	—	50	ns
t_{BAC}	$\overline{BUSY}$ Access Time from Chip Enable	—	20	—	20	—	30	—	35	—	50	ns
t_{BDC}	$\overline{BUSY}$ Disable Time from Chip Enable	—	20	—	20	—	25	—	30	—	50	ns
t_{WDD}	Write Pulse to Data Delay[2]	—	50	—	50	—	60	—	80	—	120	ns
t_{DDD}	Write Data Valid to Read Data Delay[2]	—	35	—	35	—	35	—	55	—	100	ns
t_{APS}	Arbitration Priority Set-up Time[3]	5	—	5	—	5	—	5	—	5	—	ns
t_{BDD}	$\overline{BUSY}$ Disable to Valid Data[4]	—	Note 4	—	Note 4	—	Note 4	—	Note 4	—	Note 4	ns
Busy Timing (For Slave IDT7140 Only)												
t_{WB}	Write to $\overline{BUSY}$ Input[5]	—	—	0	—	0	—	0	—	0	—	ns
t_{WH}	Write Hold After $\overline{BUSY}$[6]	—	—	15	—	20	—	20	—	20	—	ns
t_{WDD}	Write Pulse to Data Delay[8]	—	—	—	50	—	60	—	80	—	120	ns
t_{DDD}	Write Data Valid to Read Data Delay[8]	—	—	—	35	—	35	—	55	—	100	ns

2689 tbl 11

NOTES:

1 0°C to +70°C temperature range only, PLCC package only
2 Port-to-port delay through RAM cells from writing port to reading port, refer to "Timing Waveform of Read With $\overline{BUSY}$ (For Master IDT7130 only)"
3 To ensure that the earlier of the two ports wins
4 t_{BDD} is a calculated parameter and is the greater of 0, t_{WDD}-t_{WP} (actual) or t_{DDD} - t_{DW} (actual)
5 To ensure that the write cycle is inhibited during contention
6 To ensure that a write cycle is completed after contention
7 "x" in part numbers indicates power rating (SA or LA)
8 Port-to-port delay through RAM cells from writing port to reading port, refer to "Timing Waveform of Read With Port-to-Port Delay (For Slave IDT7140 Only)".
9. Not available in DIP packages

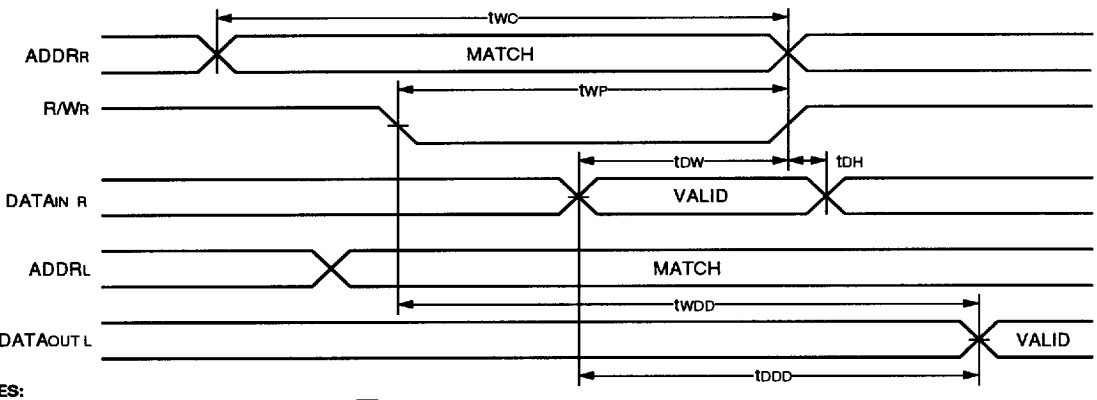
TIMING WAVEFORM OF READ WITH $\overline{BUSY}$ (1,2,3) (FOR MASTER IDT7130 ONLY)



NOTES:
1. To ensure that the earlier of the two ports wins.
2. Write Cycle parameters should be adhered to in order to ensure proper writing.
3. Device is continuously enabled for both ports.
4. $\overline{OE}$ at LO for the reading port.

2689 drw 12

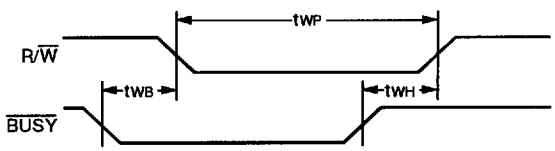
TIMING WAVEFORM OF READ WITH PORT-TO-PORT DELAY (1,2,3) (FOR SLAVE IDT7140 ONLY)



NOTES:
1. Assume $\overline{BUSY}$ input at HI for the writing port, and $\overline{OE}$ at LO for the reading port.
2. Write Cycle parameters should be adhered to in order to ensure proper writing.
3. Device is continuously enabled for both ports.

2689 drw 13

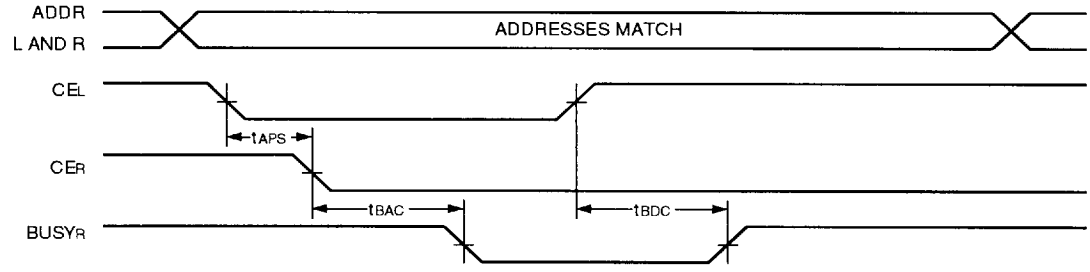
TIMING WAVEFORM OF WRITE WITH BUSY INPUT (FOR SLAVE IDT7140 ONLY)



2689 drw 14

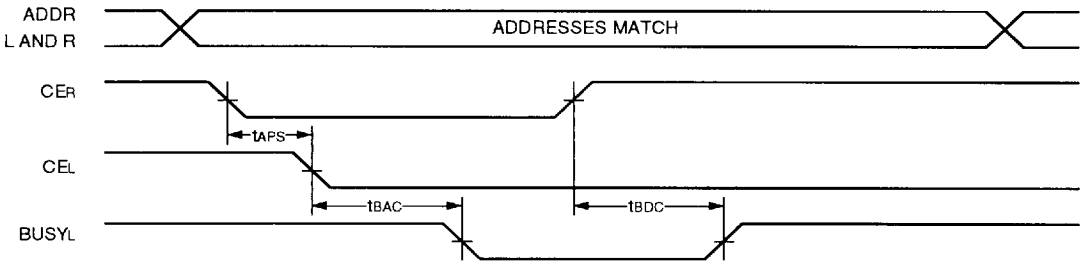
TIMING WAVEFORM OF CONTENTION CYCLE NO. 1, $\overline{CE}$ ARBITRATION (FOR MASTER IDT7130 ONLY)

$\overline{CE}_L$ VALID FIRST:



$\overline{CE}_R$ VALID FIRST:

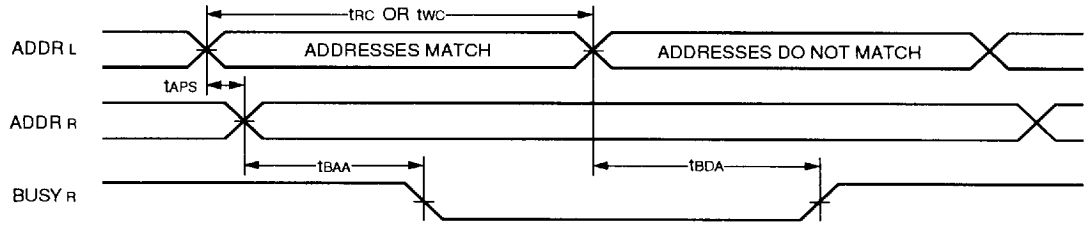
2689 drw 15



2689 drw 16

TIMING WAVEFORM OF CONTENTION CYCLE NO. 2, ADDRESS VALID ARBITRATION(1) (FOR MASTER IDT7130 ONLY)

LEFT ADDRESS VALID FIRST:



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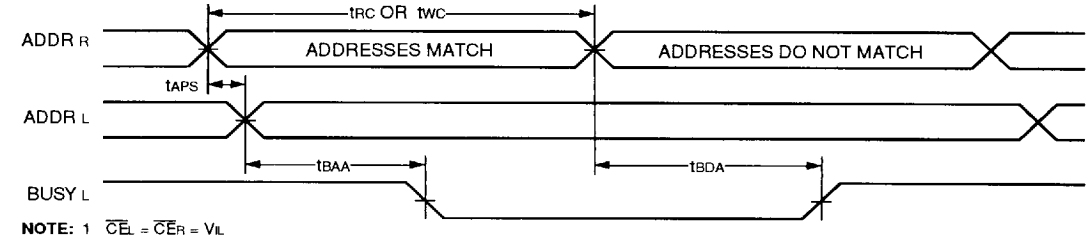
RIGHT ADDRESS VALID FIRST:



NOTE: 1 $\overline{CE}_L = \overline{CE}_R = V_{IL}$

2689 drw 18

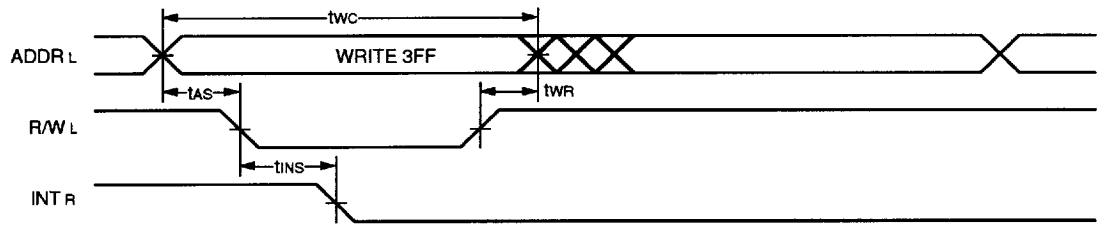
AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[2]

Symbol	Parameter	7130x20[1] Min.	7130x20[1] Max.	7130x25[3] 7140x25[3] Min.	7130x25[3] 7140x25[3] Max.	7130x35 7140x35 Min.	7130x35 7140x35 Max.	7130x55 7140x55 Min.	7130x55 7140x55 Max.	7130x100 7140x100 Min.	7130x100 7140x100 Max.	Unit
Interrupt Timing												
t_{AS}	Address Set-up Time	0	—	0	—	0	—	0	—	0	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	0	—	0	—	ns
t_{INS}	Interrupt Set Time	—	25	—	25	—	35	—	45	—	60	ns
t_{INR}	Interrupt Reset Time	—	25	—	25	—	35	—	45	—	60	ns

NOTES:
1. 0°C to +70°C temperature range only, PLCC package only.
2. "x" in part numbers indicates power rating (SA or LA).
3. Not available in DIP packages .

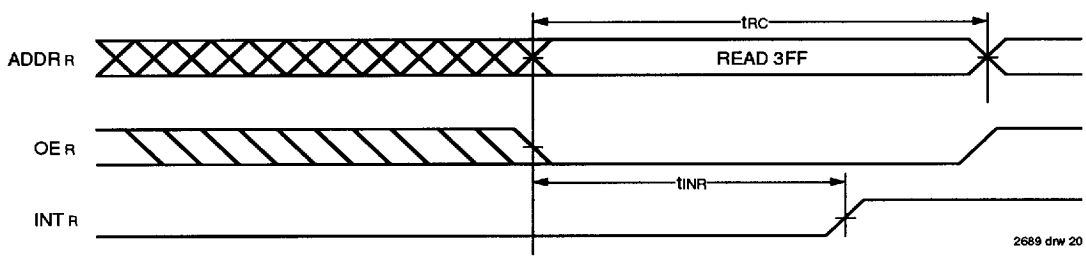
TIMING WAVEFORM OF INTERRUPT MODE

LEFT SIDE SETS $\overline{INT}_R$:[1]



2689 drw 19

RIGHT SIDE CLEAR $\overline{INT}_R$:[2]

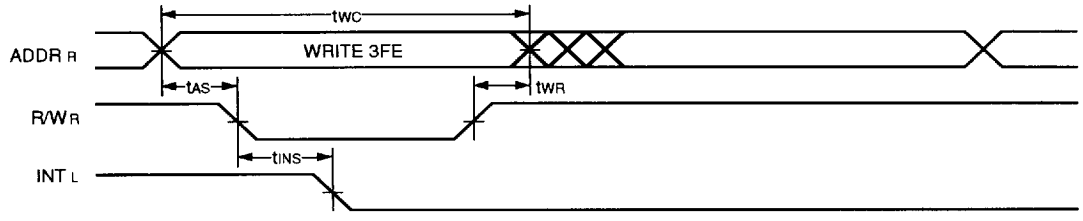


2689 drw 20

NOTES:
1. $\overline{CE}_L$ = Low, $\overline{BUSY}_L$ = High.
2. $\overline{CE}_R$ = Low, $\overline{BUSY}_R$ = High.

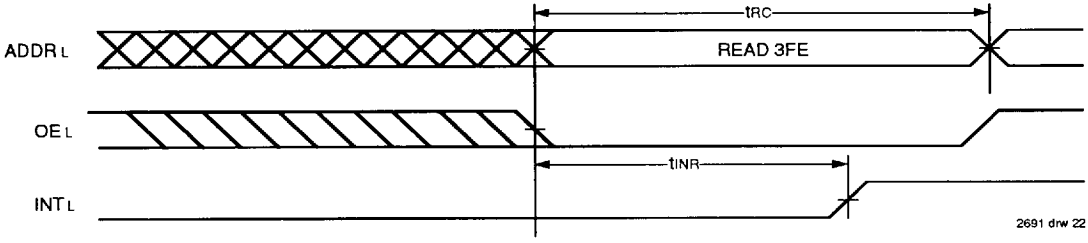
TIMING WAVEFORM OF INTERRUPT MODE

RIGHT SIDE SETS $\overline{INT}_L$:(1)



2689 drw 21

LEFT SIDE CLEAR $\overline{INT}_L$:(2)

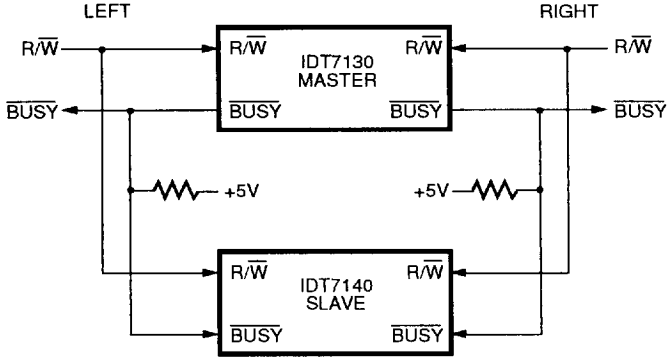


2691 drw 22

NOTES:
1. $\overline{CE}_R$ = Low, $\overline{BUSY}_R$ = High
2. $\overline{CE}_L$ = Low, $\overline{BUSY}_L$ = High

6

16-BIT MASTER/SLAVE DUAL-PORT MEMORY SYSTEMS



NOTE:
1. In IDT7140 (SLAVE), $\overline{BUSY}$-IN inhibits write - there is no arbitration

2689 drw 23

FUNCTIONAL DESCRIPTION:

The IDT7130/IDT7140 provides two ports with separate control, address, and I/O pins that permit independent access for reads or writes to any locations in memory. The IDT7130/IDT7140 has an automatic power down feature controlled by $\overline{CE}$. The $\overline{CE}$ controls on-chip power down circuitry that permits the respective port to go into a standby mode when not selected ($\overline{CE}$ high). When a port is enabled, access to the entire memory array is permitted. Each port has its own Output Enable control ($\overline{OE}$). In the read mode, the port's $\overline{OE}$ turns on the output drivers when set LOW. Non-contention READ/WRITE conditions are illustrated in Table 1.

The interrupt flag ($\overline{INT}$) permits communication between ports or systems. If the user chooses to use the interrupt function, a memory location (mail box or message center) is assigned to each port. The left port interrupt flag ($\overline{INT}_L$) is set when the right port writes to memory location 3FE (HEX). The left port clears the interrupt by reading address location 3FE. Likewise, the right port interrupt flag ($\overline{INT}_R$) is set when the left port writes to memory location 3FF (HEX) and to clear the interrupt flag ($\overline{INT}_R$), the right port must read the memory location 3FF. The message (8-bits) at 3FE or 3FF is user defined. If the interrupt function is not used, address locations 3FE or 3FF are not used as mailboxes, but as part of the random access memory. Refer to Table II for the interrupt operation.

ARBITRATION LOGIC FUNCTIONAL DESCRIPTION:

The arbitration logic will resolve an address match or a chip enable match down to 5ns minimum and determine which port has access. In all cases, an active $\overline{BUSY}$ flag will be set for the delayed port.

The $\overline{BUSY}$ flags are provided for the situation when both ports simultaneously access the same memory location. When this situation occurs, on-chip arbitration logic will determine which port has access and sets the delayed port's $\overline{BUSY}$ flag. $\overline{BUSY}$ is set at speeds that permit the processor to hold the operation and its respective address data. It is important to note that the write operation is invalid for the port that has $\overline{BUSY}$ set LOW. The delayed port will have access when $\overline{BUSY}$ goes inactive.

Contention occurs when both left and right ports are active and both addresses match. When this situation occurs, the on-chip arbitration logic determines access. Two modes of arbitration are provided: (1) if the addresses match and are valid before $\overline{CE}$, on-chip control logic arbitrates between $\overline{CE}_L$ and $\overline{CE}_R$ for access; or (2) if the $\overline{CE}$s are low before an address match, on-chip control logic arbitrates between the left and right addresses for access (refer to Table II). In either mode of arbitration, the delayed port's $\overline{BUSY}$ flag is set and will reset when the port granted access completes its operation and ADDR/$\overline{CE}$ conditions which produced the contention state are removed.

DATA BUS WIDTH EXPANSION MASTER/SLAVE DESCRIPTION:

Expanding the data bus width to sixteen-or-more-bits in a Dual-Port RAM system implies that several chips will be active at the same time. If each chip includes a hardware arbitrator, and the addresses for each chip arrive at the same time, it is possible that one will activate its $\overline{BUSY}_L$ while another activates its $\overline{BUSY}_R$ signal. Both sides are now busy and the CPUs will wait indefinitely for their port to become free.

To avoid the "Busy Lock-Out" problem, IDT has developed a MASTER/SLAVE approach where only one arbitrator, in the MASTER, is used. The SLAVE has BUSY inputs which allow an interface to the MASTER with no external components and with a speed advantage over other systems.

When expanding Dual-Port RAMs in width, the writing of the SLAVE RAMs must be delayed, until after the $\overline{BUSY}$ input has settled. Otherwise, the SLAVE chip may begin a write cycle during a contention situation. Conversely, the write pulse must extend a hold time past $\overline{BUSY}$ to ensure that a write cycle takes place after the contention is resolved. This timing is inherent in all Dual-Port memory systems where more than one chip is active at the same time.

The write pulse to the SLAVE should be delayed by the maximum arbitration time of the MASTER. If, then, a contention occurs, the write to the SLAVE will be inhibited due to $\overline{BUSY}$ from the MASTER.

TRUTH TABLES

TABLE I – NON-CONTENTION READ/WRITE CONTROL[4]

Left Or Right Port [1]				
R/$\overline{W}$	$\overline{CE}$	$\overline{OE}$	D0-7	Function
X	H	X	Z	Port Disabled and in Power Down Mode ISB2 or ISB4
X	H	X	Z	$\overline{CER}$ = $\overline{CEL}$ = H, Power Down Mode, ISB1 or ISB3
L	L	X	DATAIN	Data on Port Written into Memory[2]
H	L	L	DATAOUT	Data in Memory Output on Port[3]
H	L	H	Z	High Impedance Outputs

2689 tbl 13

NOTES:
1. A_{0L}-$A_{10L} \neq A_{0R}$-A_{10R}
2. If $\overline{BUSY}$ = L, data is not written
3. If $\overline{BUSY}$ = L, data may not be valid, see twDD and tBDD timing
4. H = HIGH, L = LOW, X = DON'T CARE, Z = HIGH IMPEDANCE

TABLE II – INTERRUPT FLAG[1,4]

Left Port					Right Port					Function
R/$\overline{W}_L$	$\overline{CE}_L$	$\overline{OE}_L$	A_{0L}-A_{10L}	$\overline{INT}_L$	R/$\overline{W}_R$	$\overline{CE}_R$	$\overline{OE}_R$	A_{0L}-A_{10R}	$\overline{INT}_R$	
L	L	X	3FF	X	X	X	X	X	L[2]	Set Right $\overline{INT}_R$ Flag
X	X	X	X	X	X	L	L	3FF	H[3]	Reset Right $\overline{INT}_R$ Flag
X	X	X	X	L[3]	L	L	X	3FE	X	Set Left $\overline{INT}_L$ Flag
X	L	L	3FE	H[2]	X	X	X	X	X	Reset Left $\overline{INT}_L$ Flag

2689 tbl 14

NOTES:
1. Assumes $\overline{BUSY}_L$ = $\overline{BUSY}_R$ = H
2. If $\overline{BUSY}_L$ = L, then NC.
3. If $\overline{BUSY}_R$ = L, then NC
4. H = HIGH, L = LOW, X = DON'T CARE, NC = NO CHANGE

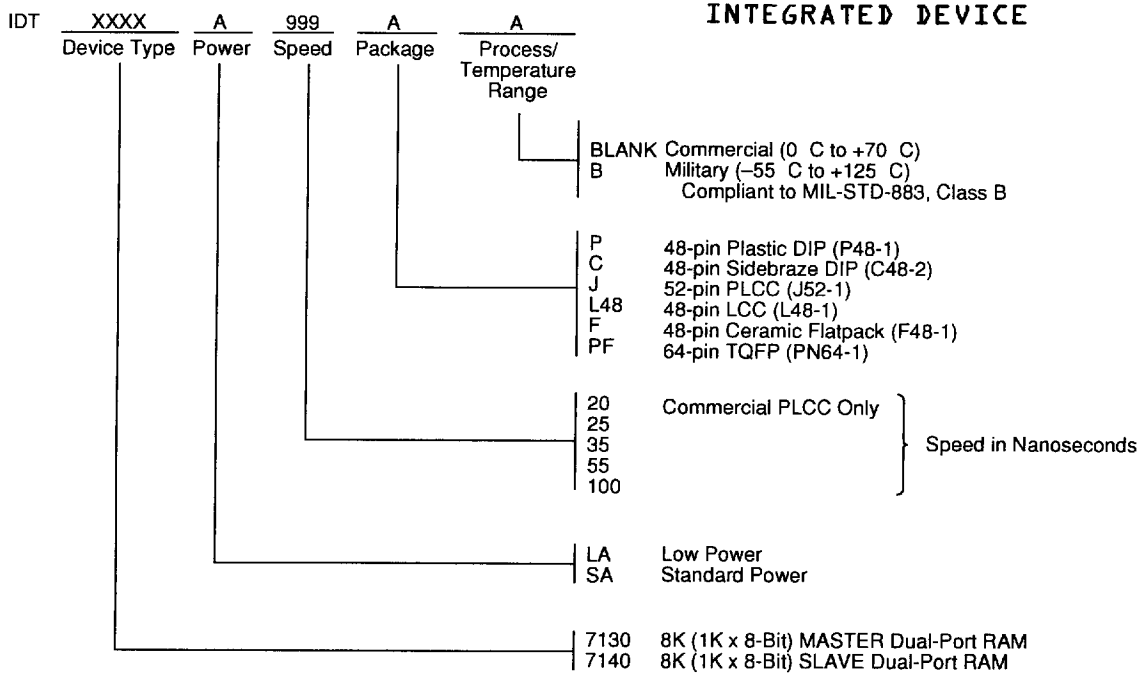
TABLE III – ARBITRATION[1,2]

Left Port		Right Port		Flags		Function[3]
$\overline{CE}_L$	A_{0L}-A_{9L}	$\overline{CE}_R$	A_{0R}-A_{9R}	$\overline{BUSY}_L$	$\overline{BUSY}_R$	
H	X	H	X	H	H	No Contention
L	X	H	X	H	H	No Contention
H	X	L	X	H	H	No Contention
L	≠ A_{0R}-A_{9R}	L	≠ A_{0L}-A_{9L}	H	H	No Contention
Address Arbitration With $\overline{CE}$ Low Before Address Match						
L	LV5R	L	LV5R	H	L	L-Port Wins
L	RV5L	L	RV5L	L	H	R-Port Wins
L	Same	L	Same	H	L	Arbitration Resolved
L	Same	L	Same	L	H	Arbitration Resolved
$\overline{CE}$ Arbitration With Address Match Before $\overline{CE}$						
LL5R	= A_{0R}-A_{9R}	LL5R	= A_{0L}-A_{9L}	H	L	L-Port Wins
RL5L	= A_{0R}-A_{9R}	RL5L	= A_{0L}-A_{9L}	L	H	R-Port Wins
LW5R	= A_{0R}-A_{9R}	LW5R	= A_{0L}-A_{9L}	H	L	Arbitration Resolved
LW5R	= A_{0R}-A_{9R}	LW5R	= A_{0L}-A_{9L}	L	H	Arbitration Resolved

2689 tbl 15

NOTES:
1. $\overline{INT}$ Flags Don't Care
2. X = DON'T CARE, L = LOW, H = HIGH
   LV5R = Left Address Valid ≥ 5ns before right address
   RV5L = Right Address Valid ≥ 5ns before left address.
   Same = Left and Right Addresses match within 5ns of each other.
   LL5R = Left $\overline{CE}$ = LOW ≥ 5ns before Right $\overline{CE}$.
   RL5L = Right $\overline{CE}$ = LOW ≥ 5ns before Left $\overline{CE}$
   LW5R = Left and Right $\overline{CE}$ = LOW within 5ns of each other
3. Arbitration Resolved = Contention resolved arbitrarily, if specified tAPS is not observed, then either $\overline{BUSY}_L$ Or $\overline{BUSY}_R$ will go Low (active), but which one goes Low cannot be predicted

ORDERING INFORMATION



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