

DESCRIPTION

The HY514260B is the new generation and fast dynamic RAM organized 262,144 × 16-bit configuration employing advance submicron CMOS process technology and advanced circuit design techniques to achieve fast access time. Independent read and write of upper and lower byte is controlled by 2 separate CAS inputs. Refresh control is provided through RAS-only, CAS-before-RAS, hidden refresh and self refresh modes. The HY514260B conforms to JEDEC pinpoint standards and is available in industry standard 400mil 40pin SOJ and 40/44pin TSOP-II and reverse TSOP-II packages.

FEATURES

- Low power dissipation
- Max. battery back-up 1.65mW (L-part)
Max. CMOS standby 1.1mW (L-part)
5.5mW
- Max. TTL standby 11mW
- Max. Self refresh 1.1mW (SL-part)
- Max. operating

Speed	Power
50	935.0mW
60	715.0mW
70	660.0mW

- Single power supply of 5V±10%
- TTL compatible inputs and outputs
- Fast access and cycle time

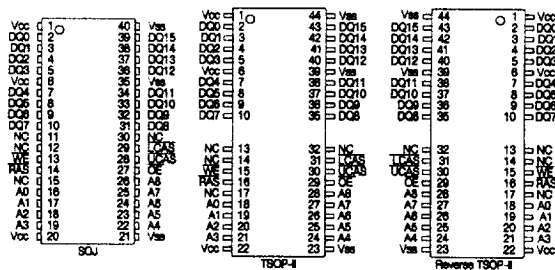
Speed	t _{TRAC}	t _{CAC}	t _{PC}
50	50ns	15ns	35ns
60	60ns	15ns	40ns
70	70ns	20ns	45ns

- Fast page mode operation
- 2CAS inputs for upper and lower byte control
- Read-Modify-Write capability
- CAS-before-RAS, RAS-only, Hidden refresh and Self refresh capability
- 512 refresh cycles / 128ms (L-part)
512 refresh cycles / 8ms

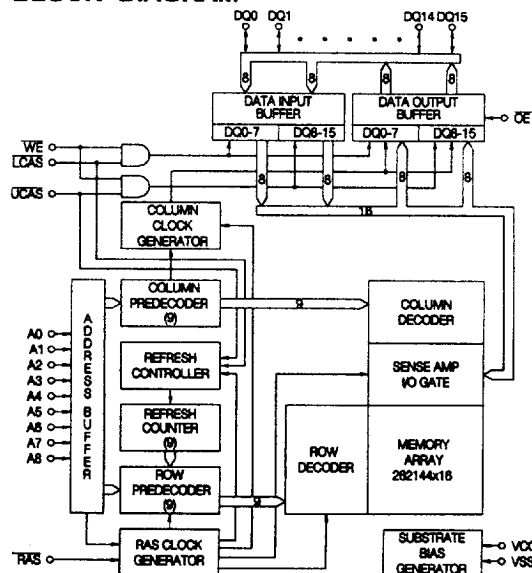
PIN DESCRIPTION

RAS	Row Address Strobe
LCAS, UCAS	Column Address Strobe
WE	Write Enable
OE	Output Enable
A0 - A8	Address Input
DQ0 - DQ15	Data Input/Output
Vcc	Power (+5V)
Vss	Ground

PIN CONNECTION



BLOCK DIAGRAM



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ABSOLUTE MAXIMUM RATING

SYMBOL	PARAMETER	RATING	UNIT
TA	Ambient Temperature	0 to 70	°C
TSTG	Storage Temperature	-55 to 150	°C
VIN, VOUT	Voltage on Any Pin Relative to Vss	-1.0 to 7.0	V
VCC	Voltage on VCC Relative to Vss	-1.0 to 7.0	V
Ios	Short Circuit Output Current	50	mA
PD	Power Dissipation	0.90	W
TSOLDER	Soldering Temperature • Time	260 • 10	°C • sec

NOTE: Operation at or above Absolute Maximum Ratings can adversely affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS

(TA = 0°C to 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
VCC	Supply Voltage	4.5	5.0	5.5	V
VIH	Input High Voltage	2.4	-	VCC+1.0	V
VIL	Input Low Voltage	-1.0	-	0.8	V

NOTE: All Voltage are referenced to Vss.

DC CHARACTERISTICS

(TA=0°C to 70°C, VCC=5V±10%, VSS=0V, unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS	SPEED/ POWER	MIN.	MAX.	UNIT	NOTE
IL1	Input Leakage Current (Any Input Pins)	VSS ≤ VIN ≤ 6.5V All other pins not under test=VSS		-10	10	μA	
ILO	Output Leakage Current (High impedance State)	VSS ≤ VOUT ≤ 5.5V RAS & CAS at VIH		-10	10	μA	
ICC1	VCC Supply Current, Operating	trc = trc (min.)	50 60 70	- - -	170 130 120	mA	1,2,3,7
ICC2	VCC Supply Current, TTL Standby	RAS & CAS at VIH, other inputs ≥ VSS		-	2	mA	
ICC3	VCC Supply Current, RAS-only refresh	trc = trc (min.)	50 60 70	- - -	170 130 120	mA	1,3,7
ICC4	VCC Supply Current, Fast Page mode	tpc = tpc (min.)	50 60 70	- - -	90 80 70	mA	1,2,3,7
ICC5	VCC Supply Current, CMOS Standby	RAS & CAS ≥ VCC-0.2V	L-part	-	1 200	mA μA	5
ICC6	VCC Supply Current, CAS-before- RAS refresh	trc = trc (min.)	50 60 70	- - -	170 130 120	mA	1,3,7
ICC7	VCC Supply Current, Battery Back up (L-part only)	trc = 250μs, trAS ≤ 1μs CAS = CBR cycling or 0.2V OE & WE = VCC-0.2V, A0-A8 = VCC-0.2V or 0.2V DQ0-DQ15 = 0.2V, VCC-0.2V or open		-	300	μA	1,4,5
ICC8	VCC Supply Current, Self Refresh (SL-part only)	RAS & CAS ≤ 0.2V other pins same as ICC7		-	200	μA	6
VOL	Output Low Voltage	IOL = 4.2mA		-	0.4	V	
VOH	Output High Voltage	IOH = -5mA		2.4	-	V	

NOTE :

1. ICC1, ICC3, ICC4 and ICC8 depend on cycle rate.
2. ICC1, ICC3, ICC4 and ICC6 are dependent on output loading. Specified values are obtained with the output open.
3. ICC is specified as average current. ICC1, ICC3, ICC6, Address can be changed maximum two times while RAS = VIL. ICC4, Address can be changed maximum once while CAS = VIH.
4. Only trAS(max.) = 1μs is applied to refresh of battery backup but trAS(max.) = 10μs is applied to normal functional operation.
5. ICC5(max.) = 0.15mA and ICC7 are applied to L-parts (HY514260BLJC, HY514260BLTC, HY514260BLRC, HY514260BSLJC, HY514260BSLTC, HY514260BSLRC.)
6. ICC8 is applied to SL-parts only (HY514260BSLJC, HY514260BSLTC and HY514260BSLRC.)
7. Operating Condition for 50ns Part is VCC=5V ± 5%, Cout=100pF.

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AC CHARACTERISTICS

(TA=0°C to 70°C, Vcc=5V ±10%, Vss=0V, unless otherwise noted.) NOTE1,2,3,13

#	SYMBOL	PARAMETER	HY514260BJC/TC/RC/LJC/LTC/LRC/ SLJC/SLTC/SLRC						UNIT	NOTE
			- 60		- 60		- 70			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
1	t _{RC}	Random Read or Write Cycle Time	90	-	110	-	130	-	ns	
2	t _{RWC}	Read-Modify-Write Cycle Time	130	-	155	-	185	-	ns	
3	t _{PC}	Fast Page Mode Cycle Time	35	-	40	-	45	-	ns	
4	t _{PRWC}	Fast Page Mode Read-Modify-Write Cycle Time	75	-	80	-	95	-	ns	
5	t _{RAC}	Access Time from $\overline{\text{RAS}}$	-	50	-	60	-	70	ns	4,9,10
6	t _{CAC}	Access Time from $\overline{\text{CAS}}$	-	15	-	15	-	20	ns	4,9
7	t _{AA}	Access Time from Column Address	-	25	-	30	-	35	ns	4,10
8	t _{CPA}	Access Time from $\overline{\text{CAS}}$ Precharge	-	30	-	35	-	40	ns	4,15
9	t _{CLZ}	$\overline{\text{CAS}}$ to Output Low Impedance	0	-	0	-	0	-	ns	4
10	t _{DOH}	Output Buffer Turn-off Delay	0	15	0	15	0	20	ns	5
11	t _T	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	3
12	t _{RP}	$\overline{\text{RAS}}$ Precharge Time	30	-	40	-	50	-	ns	
13	t _{RAS}	$\overline{\text{RAS}}$ Pulse Width	50	10K	60	10K	70	10K	ns	
14	t _{RASP}	$\overline{\text{RAS}}$ Pulse Width (Fast Page Mode)	50	100K	60	100K	70	100K	ns	
15	t _{RSH}	$\overline{\text{RAS}}$ Hold Time	15	-	15	-	20	-	ns	
16	t _{CSH}	$\overline{\text{CAS}}$ Hold Time	50	-	60	-	70	-	ns	
17	t _{CAS}	$\overline{\text{CAS}}$ Pulse width	15	10K	15	10K	20	10K	ns	
18	t _{RCD}	$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Delay	15	35	20	45	20	50	ns	9
19	t _{RAD}	$\overline{\text{RAS}}$ to Column Address Delay Time	10	25	15	30	15	35	ns	10
20	t _{CRP}	$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ Precharge Time	5	-	5	-	5	-	ns	15
21	t _{CP}	$\overline{\text{CAS}}$ Precharge Time	10	-	10	-	10	-	ns	17
22	t _{ASR}	Row Address Set-up Time	0	-	0	-	0	-	ns	
23	t _{RAH}	Row Address Hold time	8	-	10	-	10	-	ns	
24	t _{ASC}	Column Address Set-up Time	0	-	0	-	0	-	ns	14
25	t _{CAH}	Column Address Hold Time	15	-	15	-	15	-	ns	14
26	t _{AR}	Column Address Hold Time from $\overline{\text{RAS}}$	40	-	50	-	55	-	ns	
27	t _{RAL}	Column Address to $\overline{\text{RAS}}$ Lead Time	25	-	30	-	35	-	ns	
28	t _{RCS}	Read Command Set-up Time	0	-	0	-	0	-	ns	14
29	t _{RCH}	Read Command Hold Time Referenced to $\overline{\text{CAS}}$	0	-	0	-	0	-	ns	6,14
30	t _{RRH}	Read Command Hold Time Referenced to $\overline{\text{RAS}}$	0	-	0	-	0	-	ns	6
31	t _{WCH}	Write Command Hold Time	10	-	10	-	15	-	ns	14
32	t _{WCR}	Write Command Hold Time from $\overline{\text{RAS}}$	40	-	45	-	55	-	ns	
33	t _{WP}	Write Command Pulse Width	10	-	10	-	15	-	ns	
34	t _{RWL}	Write Command to $\overline{\text{RAS}}$ Lead Time	15	-	15	-	20	-	ns	
35	t _{CWL}	Write Command to $\overline{\text{CAS}}$ Lead Time	15	-	15	-	20	-	ns	16
36	t _{DS}	Data-In Set-up Time	0	-	0	-	0	-	ns	7
37	t _{DH}	Data-In Hold Time	15	-	15	-	15	-	ns	7
38	t _{DHR}	Data-In Hold Time Referenced to $\overline{\text{RAS}}$	40	-	50	-	55	-	ns	
39	t _{REF}	Refresh Period (512 cycles)	-	8	-	8	-	8	ms	12
		L-part	-	128	-	128	-	128		11
40	t _{WCS}	Write Command Set up Time	0	-	0	-	0	-	ns	8,14

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AC CHARACTERISTICS

(continued)

#	SYMBOL	PARAMETER	HY514260BJC/TC/LJC/LTC/LRC/ SLJC/SLTC/SLRC						UNIT	NOTE
			- 50		- 60		- 70			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
41	tCWD	CAS to $\overline{WE}$ Delay Time	35	-	40	-	50	-	ns	8
42	tRWD	RAS to $\overline{WE}$ Delay Time	70	-	85	-	100	-	ns	8
43	tAWD	Column Address to $\overline{WE}$ Delay Time	45	-	55	-	65	-	ns	8
44	tCSR	CAS Set-up Time (CBR Cycle)	5	-	5	-	5	-	ns	14
45	tCHR	CAS Hold Time (CBR Cycle)	10	-	10	-	10	-	ns	15
46	tRPC	RAS to CAS Precharge Time	5	-	5	-	5	-	ns	14
47	tCPT	CAS Precharge Time (CBR Counter Test)	20	-	20	-	25	-	ns	17
48	tROH	RAS Hold Time Referenced to $\overline{OE}$	0	-	0	-	0	-	ns	
49	tOEA	$\overline{OE}$ Access Time	-	15	-	15	-	20	ns	
50	tOED	$\overline{OE}$ to Data Delay	15	-	15	-	20	-	ns	
51	tOEZ	Output Buffer Turn Off Delay Time from $\overline{OE}$	0	15	0	15	0	20	ns	5
52	tOEH	$\overline{OE}$ Command Hold Time	15	-	15	-	20	-	ns	
53	tCPWD	$\overline{WE}$ Delay Time from CAS Precharge	50	-	55	-	65	-	ns	8
54	tRHCP	RAS Hold Time from CAS Precharge	35	-	35	-	40	-	ns	
55	tRASS	RAS Pulse Width (Self Refresh)	100	-	100	-	100	-	ns	
56	tRPS	RAS Precharge Time (Self Refresh)	120	-	130	-	150	-	μ s	
57	tCHS	CAS Hold Time from RAS (Self Refresh)	- 50	-	- 50	-	- 50	-	ns	

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NOTE:

1. An initial pause of 200 μ s is required after power-up followed by any 8 $\overline{\text{RAS}}$ cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ initialization cycles instead of 8 $\overline{\text{RAS}}$ -only refresh cycles are required.
2. If $\overline{\text{RAS}}=\text{Vss}$ during power-up, the HY51V4260B could begin an active cycle. This condition results in higher current than necessary current which is demanded from the power supply during power-up. It is recommended that $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ track with Vcc during power-up or be held at a valid Vih in order to minimize the power-up current.
3. $\text{Vih}(\text{min.})$ and $\text{Vil}(\text{max.})$ are reference levels for measuring timing of input signals. Transition times are measured between $\text{Vih}(\text{min.})$ and $\text{Vil}(\text{max.})$, and are assumed to be 5ns for all inputs.
4. Measured at $\text{Voh}=2.4\text{V}$ and $\text{Vol}=0.4\text{V}$ with a load equivalent to 2 TTL loads and 50pF.
5. $\text{toff}(\text{max.})$ and toez define the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
6. Either trch or trrh must be satisfied for a read cycle.
7. These parameters are referenced to $\overline{\text{LCAS}}$ or $\overline{\text{UCAS}}$ leading edge in early write cycles and $\overline{\text{WE}}$ leading edge in Read-Modify-Write cycles.
8. twcs , trwd , tcwd , tawd and tcpwd are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $\text{twcs} \geq \text{twcs}(\text{min.})$, the cycle is an early write cycle and data out pin will remain open circuit (high impedance) through the entire cycle. If $\text{trwd} \geq \text{trwd}(\text{min.})$, $\text{tcwd} \geq \text{tcwd}(\text{min.})$, $\text{tawd} \geq \text{tawd}(\text{min.})$, and $\text{tcpwd} \geq \text{tcpwd}(\text{min.})$, the cycle is a Read-Modify-Write cycle and data out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminated.
9. Operation within the $\text{trcd}(\text{max.})$ limit insures that $\text{trac}(\text{max.})$ can be met. $\text{trcd}(\text{max.})$ is specified as a reference point only. If trcd is greater than the specified $\text{trcd}(\text{max.})$ limit, then access time is controlled by tcac .
10. Operation within the $\text{trad}(\text{max.})$ limit insures that $\text{trac}(\text{max.})$ can be met. $\text{trad}(\text{max.})$ is specified as a reference point only. If trad is greater than the specified $\text{trad}(\text{max.})$ limit, then access time is controlled by taa .
11. $\text{tref}(\text{max.})=128\text{ms}$ is applied to L-Parts (HY514260BLJC, HY514260BLTC, HY514260BLRC, HY514260BSLJC, HY514260BSLTC, HY514260BSLRC).
12. A burst of 512 $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh cycles must be executed within 8ms (128ms for L-part) after exiting self refresh.
13. When both $\overline{\text{LCAS}}$ and $\overline{\text{UCAS}}$ go low at the same time, all 16-bits data are written into the device. $\overline{\text{LCAS}}$ and $\overline{\text{UCAS}}$ must be transitioned simultaneously within a same read or write cycle.
14. These parameters are determined by the earlier falling edge of $\overline{\text{LCAS}}$ or $\overline{\text{UCAS}}$.
15. These parameters are determined by the later rising edge of $\overline{\text{LCAS}}$ or $\overline{\text{UCAS}}$.
16. tcwl must be satisfied by both $\overline{\text{LCAS}}$ and $\overline{\text{UCAS}}$ for 16-bits access cycles.
17. tcp and cpt are measured when both $\overline{\text{LCAS}}$ and $\overline{\text{UCAS}}$ are high state.
18. Operating Condition for 50ns Part is $\text{Vcc}=5\text{V} \pm 5\%$, $\text{Cout}=100\text{pF}$.

CAPACITANCE

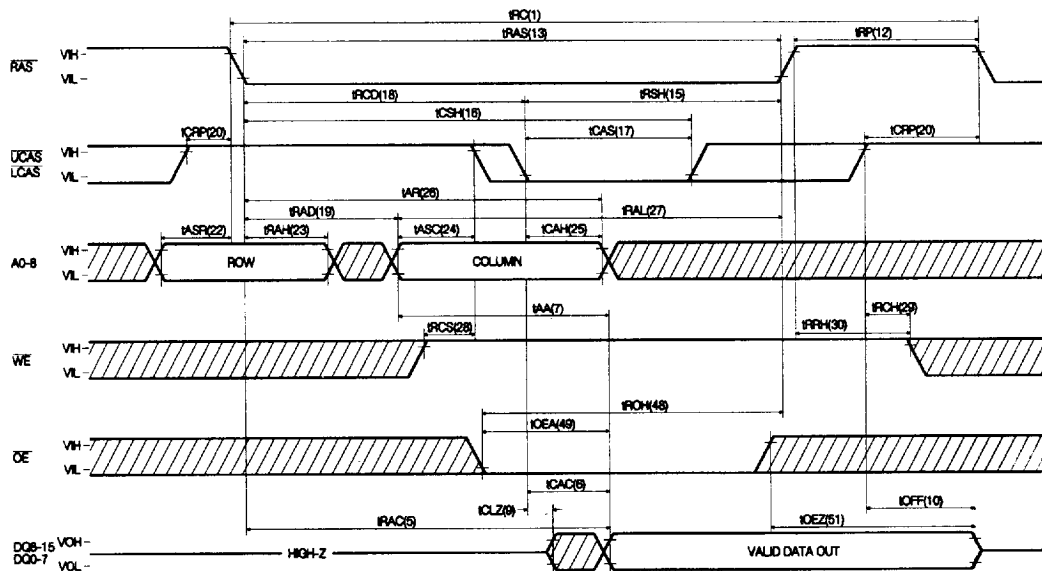
($\text{TA}=25^\circ\text{C}$, $\text{Vcc}=5\text{V} \pm 10\%$, $\text{Vss}=0\text{V}$, $f=1\text{MHz}$, unless otherwise noted.)

SYMBOL	PARAMETER	TYP.	MAX.	UNIT
CIN1	Input Capacitance (A0-A8)	-	5	pF
CIN2	Input Capacitance ($\overline{\text{RAS}}$, $\overline{\text{LCAS}}$, $\overline{\text{UCAS}}$, $\overline{\text{WE}}$, $\overline{\text{OE}}$)	-	7	pF
CDQ	Data Input/Output Capacitance (DQ0-DQ15)	-	7	pF

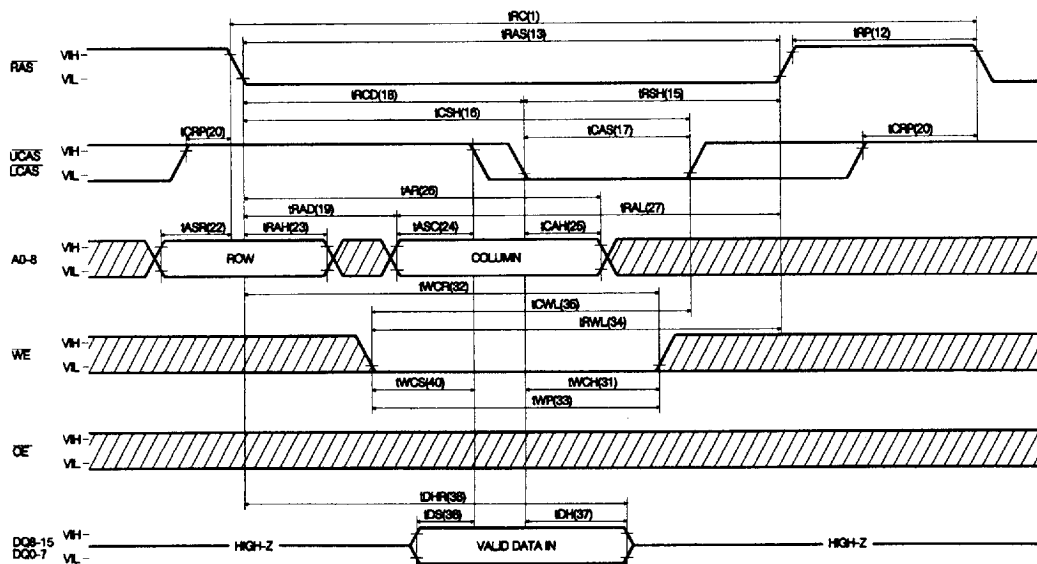
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TIMING DIAGRAM

READ CYCLE



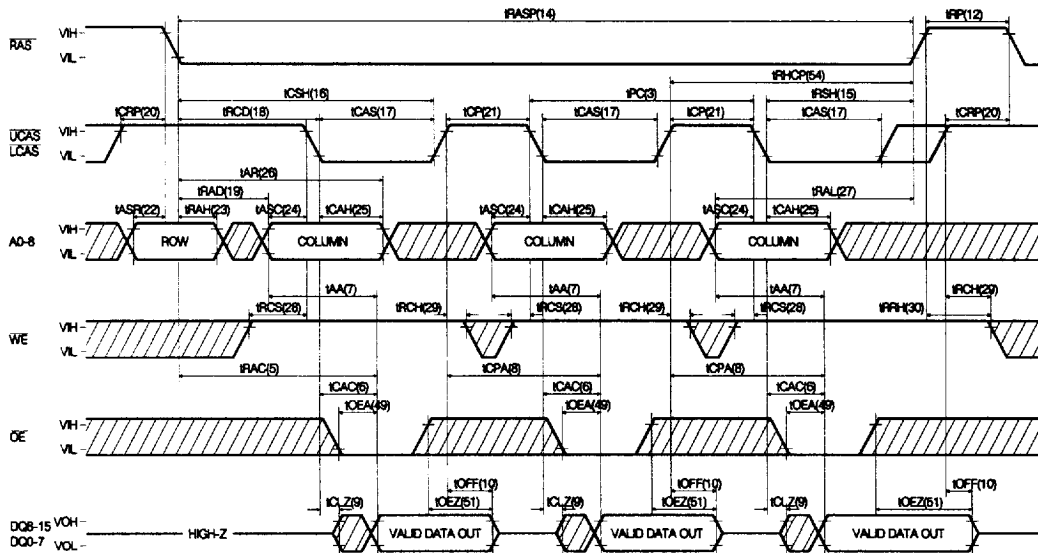
EARLY WRITE CYCLE



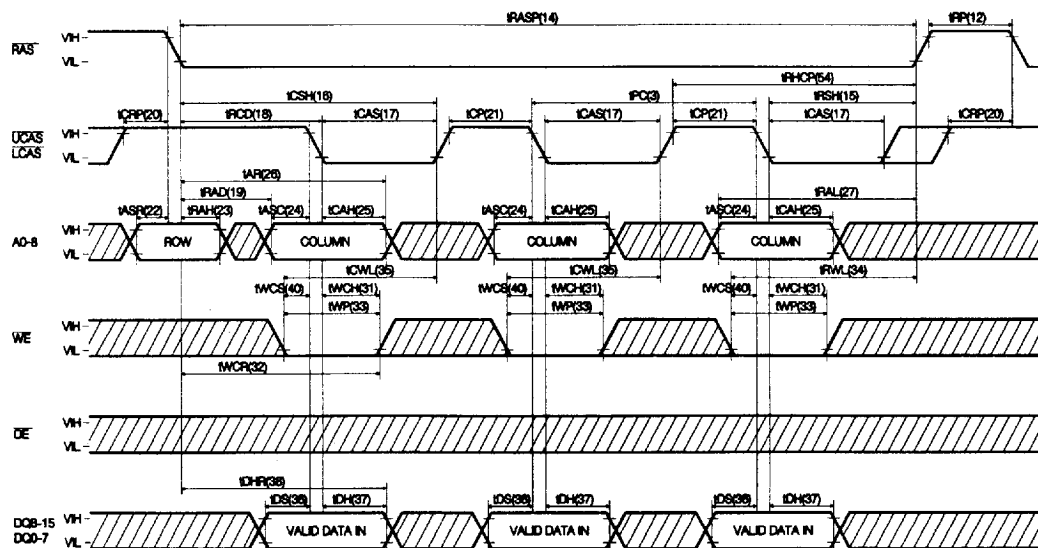
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FAST PAGE MODE READ CYCLE

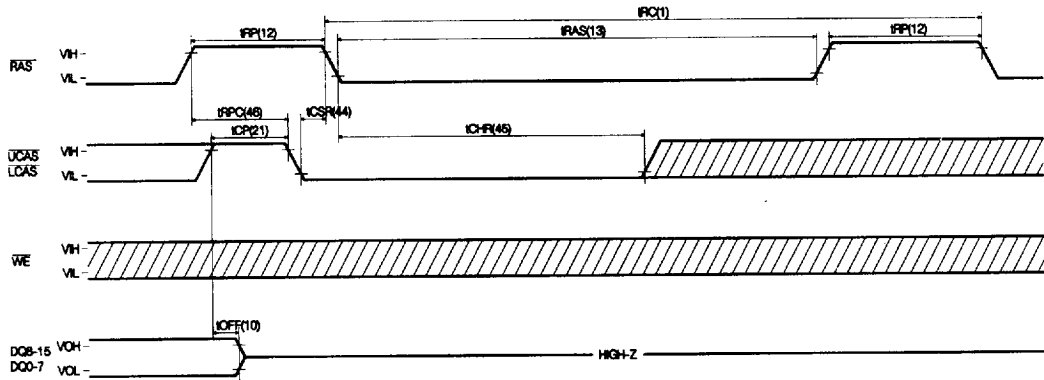


FAST PAGE MODE EARLY WRITE CYCLE



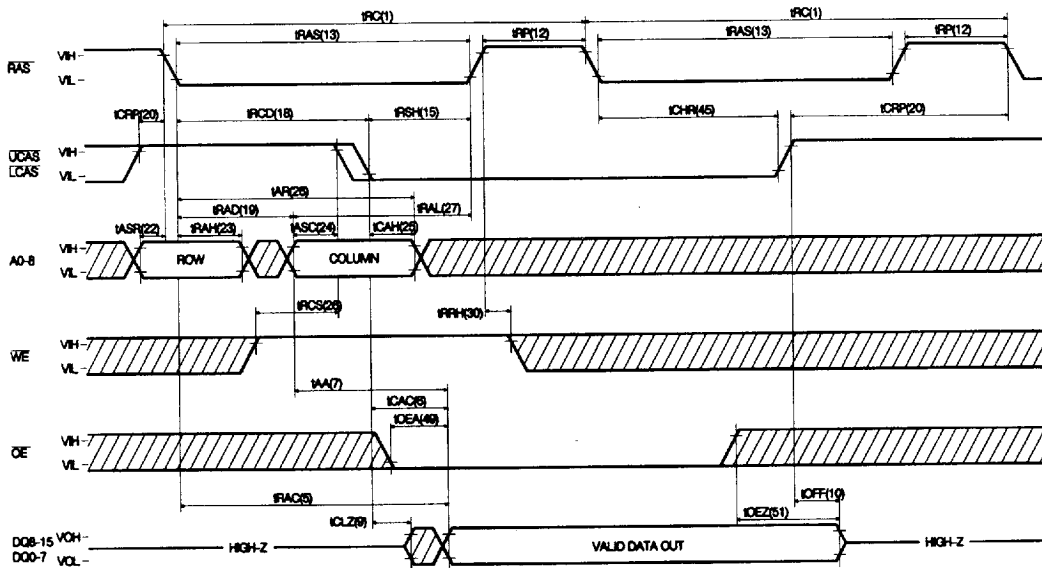
NOTE : OE and WE = "H" or "L"

CAS-BEFORE-RAŚ REFRESH CYCLE



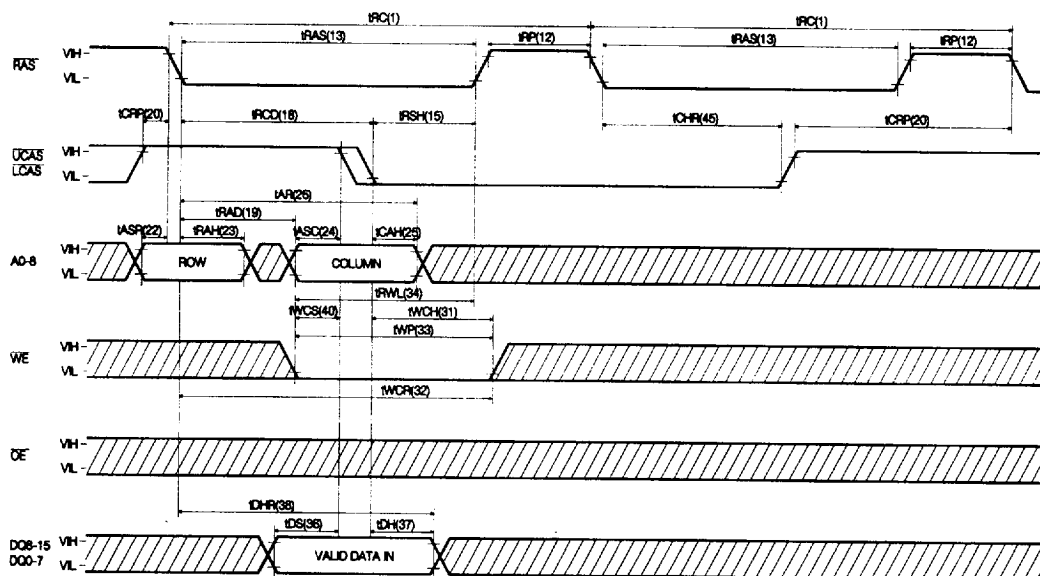
NOTE : A0-9 and OE = "H" or "L"

HIDDEN REFRESH CYCLE (READ)

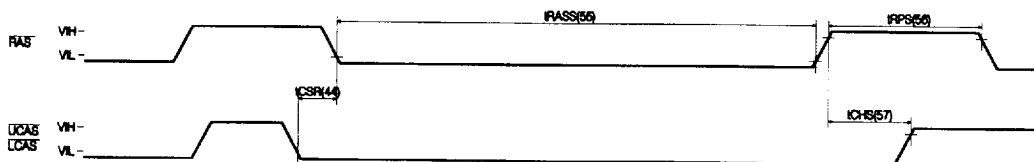


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HIDDEN REFRESH CYCLE (WRITE)

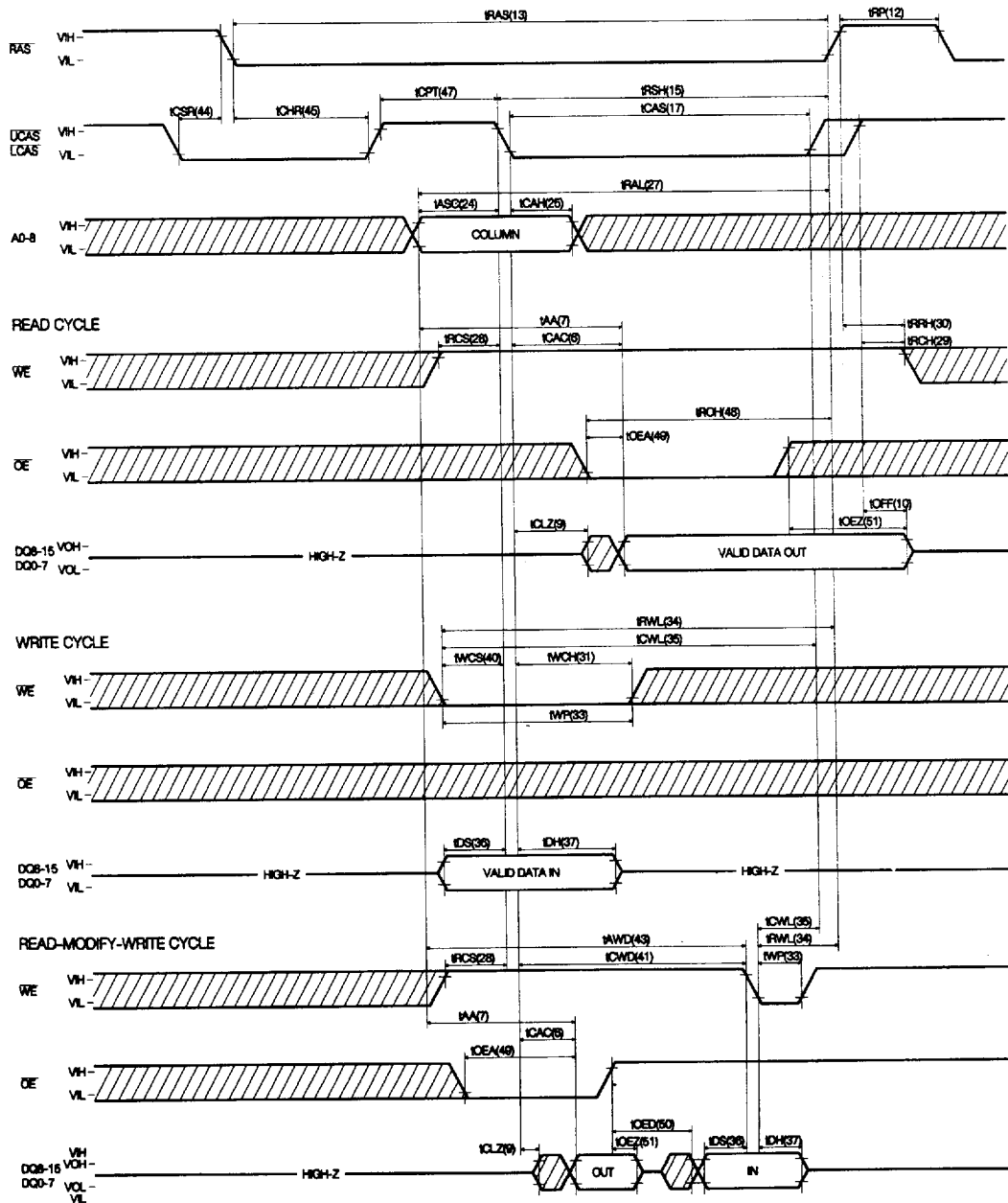


CAS-BEFORE-RAS SELF REFRESH CYCLE



NOTE: A0-8, WE and OE= "H" or "L"

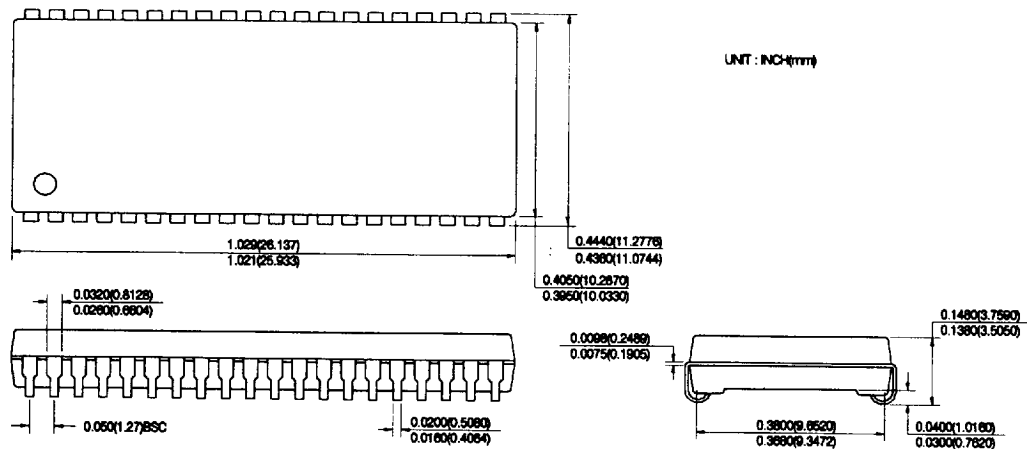
CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE



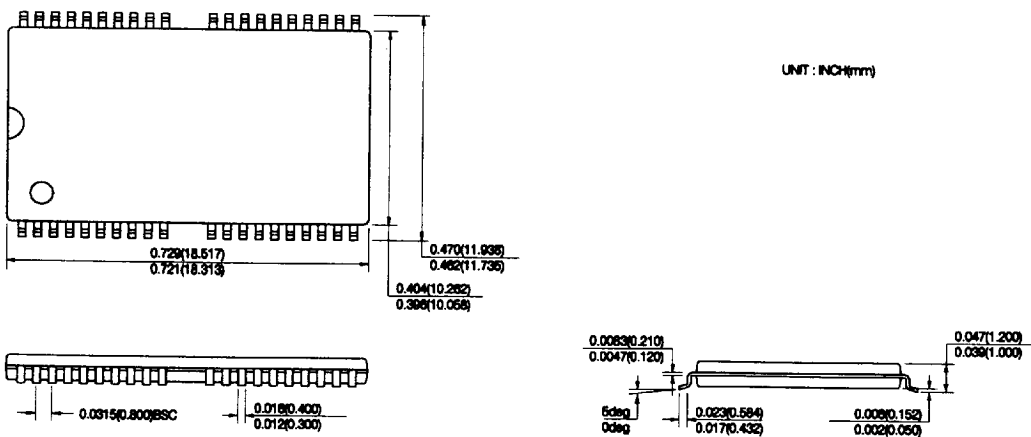
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PACKAGE INFORMATION

400 mil 40 pin Small Outline J-form Package (JC)



400 mil 40/44 pin Thin Small Outline Package (TC)(RC)



ORDERING INFORMATION

PART NUMBER	SPEED	POWER	PACKAGE
HY514260BJC	50/60/70		SOJ
HY514260BLJC	50/60/70	L-part	SOJ
HY514260BSLJC	50/60/70	SL-part	SOJ
HY514260BTC	50/60/70		TSOP-II
HY514260BLTC	50/60/70	L-part	TSOP-II
HY514260BSLTC	50/60/70	SL-part	TSOP-II
HY514260BRC	50/60/70		TSOP-II(R)
HY514260BLRC	50/60/70	L-part	TSOP-II(R)
HY514260BSLRC	50/60/70	SL-part	TSOP-II(R)

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