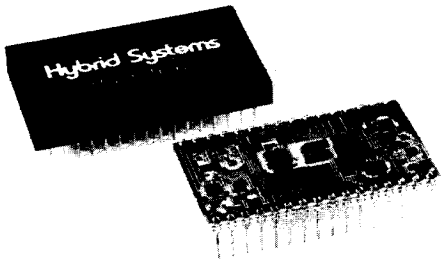
COMPLETE 0.0008% ACCURATE (16-BIT) ADC

FEATURES

- True 16-bit (±0.0008%) linearity error
- Full 16-bit resolution (1 part in 65,536)
- No missing codes (16-bits) 0°C to +70°C
- Six user selectable input ranges
- Completely self-contained
- Parallel data output
- Low full scale drift 10ppm/°C (max)

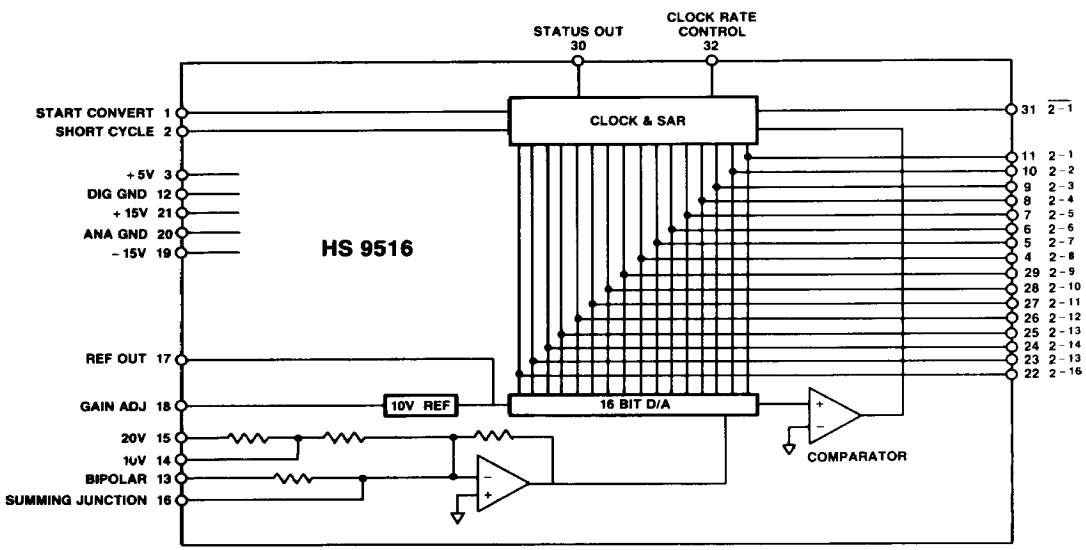
DESCRIPTION

The HS9516 is a 16-bit successive approximation analog to digital converter in a 32 pin triple DIP package. The 9516 is completely self-contained with clock, reference, comparator, successive approximation register and low power 16-bit DAC. It converts in 100 microseconds on 0 to +5V, 0 to +10V, 0 to +20V, ±2.5V, ±5V and ±10V input ranges. Output data is available in parallel binary and 2's complement formats. Short cycle and internal clock rate control may be externally adjusted to provide less conversion time at lower resolutions.



The HS9516 is available with 14-bit (±0.003% FSR), 15-bit (±0.0015% FSR) or 16-bit (±0.0008% FSR) nonlinearity. The B versions are fully screened and tested to MIL-STD-883C and are packaged in a hermetic 32-pin DIP.

FUNCTIONAL DIAGRAM



SPECIFICATIONS

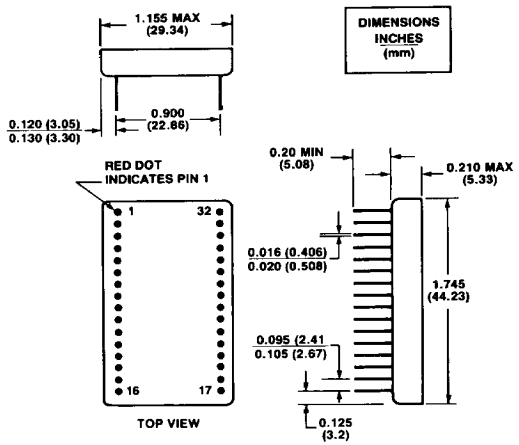
(Typical @ +25°C and nominal supply voltages)

MODEL	HS9516C-6	HS9516C-5	HS9516C-4	HS9516B-6	HS9516B-5	HS9516B-4
ANALOG INPUT						
Nominal Input Voltage Ranges	5V, 10V, 20V, ±2.5V, ±5V, ±10V	*	*	*	*	*
Absolute Max Input Voltage	±25V	*	*	*	*	*
Input Impedance	2.5KΩ on 5V ranges, 5KΩ on 10V ranges, 10KΩ on 20V ranges	*	*	*	*	*
Input Circuitry Settling Time	20μsec for full rated accuracy after FSR analog change	*	*	*	*	*
DIGITAL OUTPUTS						
Data Coding		*	*	*	*	*
Unipolar	16-bits binary	*	*	*	*	*
Bipolar	Offset binary, 2's complement	*	*	*	*	*
Status Output	'H' = conversion in process; goes low 50nsec before LSB is stable	*	*	*	*	*
Logic '1' Voltage	2.4V min to 5V	*	*	*	*	*
Logic '0' Voltage	0V min to 0.4V max	*	*	*	*	*
Max Loading	2 std TTL loads, each output					
DIGITAL INPUTS						
Start Convert	Positive pulse, 50nsec min width, initiates conversion on trailing edge. Must remain low during conversion.	*	*	*	*	*
Short Cycle	'H' enables conversion. Must be tied to logic supply for 16-bit conversion and to bit N + 1 for N bit conversion.	*	*	*	*	*
Logic '1' Voltage	2V min to 5.5V max	*	*	*	*	*
Logic '0' Voltage	−0.5V min to 0.8V max	*	*	*	*	*
Loading	1 LPTTL load max each input					
POWER REQUIREMENTS						
+15V Supply Range	+15V ±10%	*	*	*	*	*
+15V Supply Current	30mA max	*	*	*	*	*
−15V Supply Range	−15V ±10%	*	*	*	*	*
−15V Supply Current	30mA max	*	*	*	*	*
+5V Supply Range	+5V ±10%	*	*	*	*	*
+5V Supply Current	60mA max	*	*	*	*	*
Total Power Dissipation	1.2W max					
REFERENCE OUTPUT						
Voltage	+10V ±10%	*	*	*	*	*
Output Resistance	0.1Ω	*	*	*	*	*
Max Loading	±1mA					
ACCURACY						
Quantization	±½ LSB	*	*	*	*	*
Scale Factor Error	±0.1% max[1]	*	*	*	*	*
Zero Error (Unipolar or Bipolar)	±0.1% FSR max[1]					
Differential Linearity Error (% of FSR, max)	±0.0015	±0.003	±0.006	±0.0015	±0.003	±0.006
No Missing Codes[2]	16 bits	15 bits	14 bits	14 bits	**	**
Integral Linearity Error (% of FSR, max)	±0.0008 typ	±0.0015	±0.003	±0.0008 typ	±0.0015	±0.003
	±0.0015 max	±0.003	±0.006	±0.0015 max	±0.003	±0.006
Noise (2σ p-p, RTI)	⅓ LSB	*	*	*	*	*
CONVERSION TIME[2]	100μsec max	*	*	*	*	*
STABILITY						
Scale Factor Tempco	±10ppm/°C max	*	*	*	*	*
Zero Tempco						
Unipolar	±2ppm FSR/°C	*	*	*	*	*
Bipolar	±5ppm FSR/°C	*	*	*	*	*
Integral Linearity Tempco	±1ppm FSR/°C max	*	*	*	*	*
Differential Linearity	±0.5ppm FSR/°C max	*	*	*	*	*
Change in Absolute Accuracy with Change in Power Supply Voltages						
+15V	0.002%/% ΔV_S max	*	*	*	*	*
−15V	0.002%/% ΔV_S max	*	*	*	*	*
+5V	0.002%/% ΔV_S max	*	*	*	*	*
ENVIRONMENTAL LIMITS						
Operating Temp Range	0°C to +70°C	*	*	−55°C to +125°C	**	**
Storage Temp Range	−55°C to +85°C	*	*	−65°C to +150°C	**	**
PACKAGE	Case A	*	*	Case A	**	**

NOTES: 1. Adjustable to zero. 2. Over full operating temperature range.

*Specifications same as HS 9516C-6. **Specifications same as HS 9516B-6.

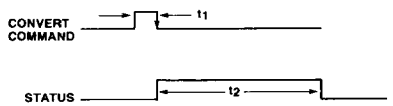
PACKAGE OUTLINE



PIN ASSIGNMENTS

PIN	FUNCTION	PIN	FUNCTION
1	START CONVERT	32	CLOCK RATE CONTROL
2	SHORT CYCLE	31	$\overline{2^{-1}}$
3	+5V	30	STATUS OUT
4	2^{-8}	29	2^{-9}
5	2^{-7}	28	2^{-10}
6	2^{-6}	27	2^{-11}
7	2^{-5}	26	2^{-12}
8	2^{-4}	25	2^{-13}
9	2^{-3}	24	2^{-14}
10	2^{-2}	23	2^{-15}
11	2^{-1} (MSB)	22	2^{-16} (LSB)
12	DIG GND	21	+15V
13	BIPOLAR	20	ANA GND
14	10V INPUT	19	−15V
15	20V INPUT	18	GAIN ADJ
16	SUMMING JUNCTION	17	REF OUT

TIMING



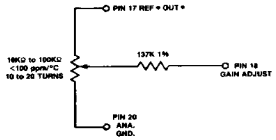
$t_1 \geq$ 50nsec CONVERT COMMAND MUST STAY LOW
$t_2 \leq 100\mu$sec

PIN 2 CONNECTS TO	16-BIT	15-BIT	14-BIT	13-BIT	12-BIT
	+5V	Pin 22	Pin 23	Pin 24	Pin 25

SHORT CYCLE CONNECTIONS

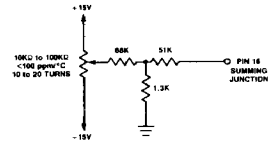
APPLICATIONS INFORMATION

OPTIONAL OFFSET AND GAIN ADJUSTMENTS



GAIN ADJUST CIRCUIT MIN ADJUST RANGE = ±0.2% FSR

Unipolar & Bipolar: Apply +F.S. −3/2 LSB analog input and set the potentiometer for a digital output that alternates between 111...1 and 111...0.



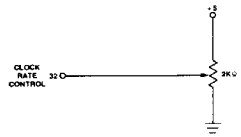
OFFSET ADJUST CIRCUIT MIN ADJUST RANGE = +0.2% FSR

Unipolar: Apply +½ LSB analog input and set potentiometer for a digital output that alternates between 000...0 and 000...1.
Bipolar: Apply +½ LSB and set potentiometer for a digital output that alternates between 1000...0 and 1000...1.

CONNECTIONS FOR VARIOUS INPUT RANGES

INPUT RANGE	ANALOG IN TO PIN	CONNECT PIN 13 TO	NOTES
−2.5V to +2.5V	14	17	Connect pins 15 + 16
−5V to +5V	14	17	
−10V to +10V	15	17	
0V to 5V	14	20	Connect pins 15 + 16
0V to 10V	14	20	
0V to 20V	15	20	

CLOCK RATE CONTROL



ADJUSTMENT RANGE IS 50μsec to 200μsec at 16-BIT RESOLUTION

The HS 9516 clock rate is set by the factory for a conversion time of 100μsec, i.e. Pin 32 left open. For higher or lower clock rates, connect Pin 32 to a multi-turn potentiometer as shown above.

GROUNDING AND POWER SUPPLY DECOUPLING

Connect Analog GND to Digital GND at package pins. If not possible, connect 1μf* tantalum capacitor in parallel with a 0.1μf ceramic capacitor between Analog GND and Digital GND pins. Decouple +15V and −15V supplies to Analog GND and +5V supply to Digital GND at package pins with 1μf tantalum and 0.1μf ceramic capacitors.

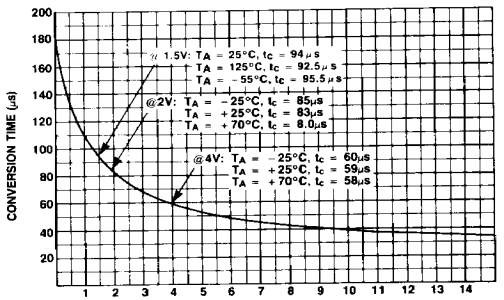
*Non-polarized

TRANSFER CHARACTERISTICS

MSB LSB	BIPOLAR INPUT VOLTAGE RANGE			UNIPOLAR INPUT VOLTAGE RANGE		
	±2.5	±5V	±10V	0 to 5V	0 to 10V	0 to 20V
1111111111111110	2.49989V	5.99977V	9.99954V	4.99989V	9.99977V	19.99954V
0000000000000000	−0.038mV	−0.076mV	−0.153mV	2.49996V	4.99992V	9.99985V
0000000000000000	−2.49992V	−4.99992V	−9.99985V	−0.038mV	−0.076mV	−0.153mA

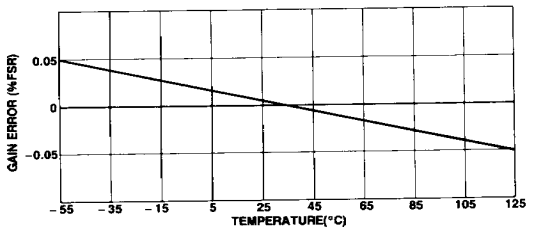
NOTES:
1. Codings shown are binary and offset binary. Use $\overline{MSB}$ for 2's complement coding. 2. One LSB = FSR/2^{16}. 3. The voltages given are the theoretical values for the transitions indicated. Ideally, with the converter continuously converting the output bits indicated as 0 will change from "1" to "0" or from "0" to "1" as the input voltage passes through the level indicated.

TYPICAL CHARACTERISTIC CURVES

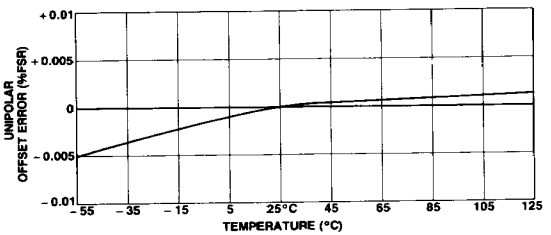


CONVERSION TIME VS. CONTROL VOLTAGE, T_A = +25°C

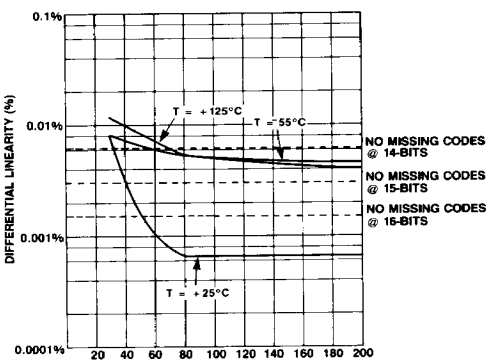
NOTE: CONVERSION TIME WILL BE 100µsec MAX IF VOLTAGE TO PIN 32 IS 'OPEN', AND TYPICALLY 200µsec IF PIN 32 IS AT 0V (GROUND).



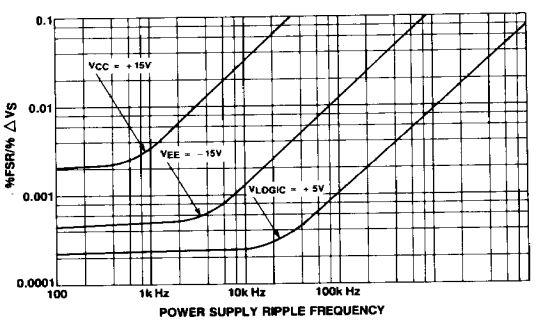
GAIN DRIFT VS. TEMPERATURE



OFFSET DRIFT VS. TEMPERATURE



HS 9516-6 DIFFERENTIAL LINEARITY VS. CONVERSION TIME



POWER SUPPLY REJECTION

ORDERING INFORMATION

MODEL	DESCRIPTION
HS 9516C-6	16-Bit ADC with ±0.001% Integral Linearity, 0°C to 70°C
HS 9516C-5	16-Bit ADC with ±0.0015% Integral Linearity, 0°C to 70°C
HS 9516C-4	16-Bit ADC with ±0.003% Integral Linearity, 0°C to 70°C
HS 9516B-6	16-Bit ADC with ±0.001% Integral Linearity, −55°C to +125°C
HS 9516B-5	16-Bit ADC with ±0.0015% Integral Linearity, −55°C to +125°C
HS 9516B-4	16-Bit ADC with ±0.003% Integral Linearity, −55°C to +125°C