HC2040 / HC2041

NSP FAMILY

HUGHES

SEMICONDUCTOR
PRODUCTS CENTER

NONVOLATILE SERIALLY PROGRAMMABLE
DUAL SOLID STATE TRIM CAPACITORS

PRELIMINARY

DESCRIPTION

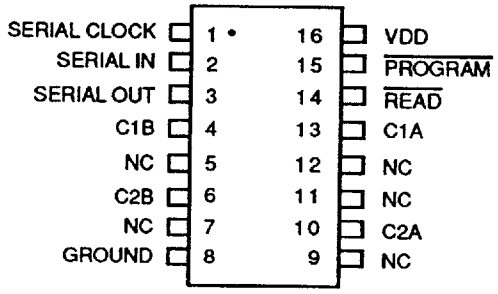
The Hughes HC2040 and HC2041 contain dual digitally controlled adjustable capacitors. Each device has two independent sets of eight binary weighted capacitors that can be connected in parallel. Series CMOS switches, controlled by nonvolatile latches, are used to connect and disconnect the capacitors. A maximum capacitance of typically 100pF(HC2040) or 250pF(HC2041) results when all the switches are closed. The minimum capacitance step size is typically 0.4pF(HC2040) or 1.0pF(HC2041).

Nonvolatile data latches retain the last programmed state when power is removed. The correct state is automatically restored when power is reapplied. A standard serial interface, common to all the NSP devices, is used to access the nonvolatile memory.

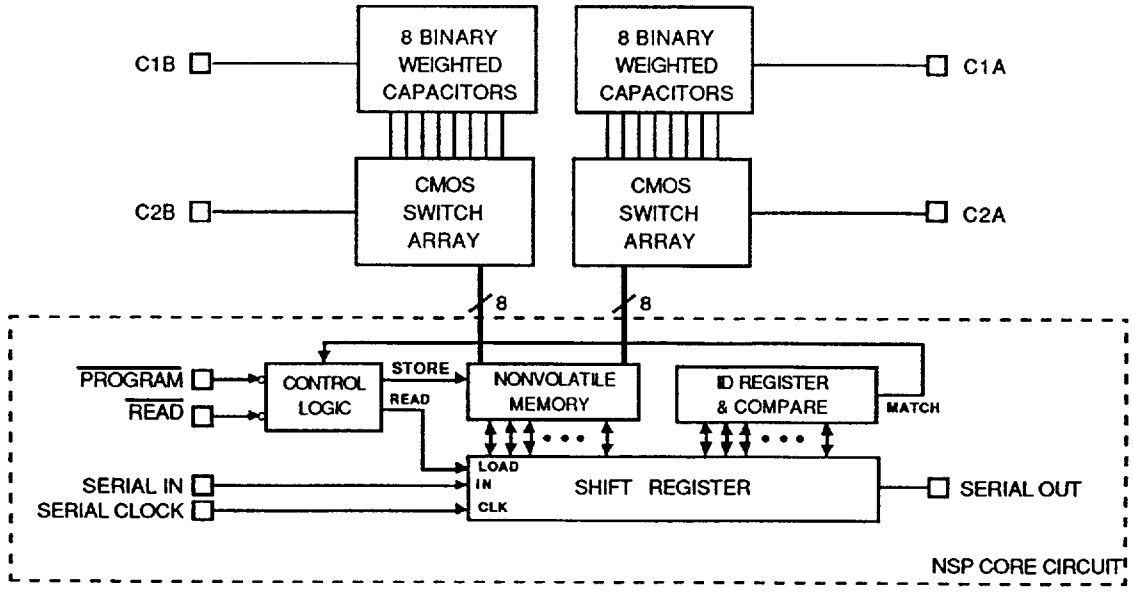
FEATURES

- CMOS
- Wide Supply Range (3 to 10 volts)
- 2 Independently Controlled Capacitors
- Standard "NSP" Serial Interface
- $C_{MAX} \approx$ 100pF(HC2040), 250pF(HC2041)
- 0.4 % Resolution
- Low Temperature Coefficient
- Nonvolatile Data Latches

PIN CONFIGURATION



BLOCK DIAGRAM



SERIAL INTERFACE BIT ALLOCATION

HC2040

SERIAL IN	DATA BITS																ID BITS								SERIAL OUT
	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	DØ	1	Ø	Ø	1	Ø	Ø	1	1	

MSB—— $DATA_B$ ——LSB MSB—— $DATA_A$ ——LSB 9 3

HC2041

SERIAL IN	DATA BITS																ID BITS								SERIAL OUT
	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	DØ	1	Ø	Ø	1	Ø	1	1	Ø	

MSB—— $DATA_B$ ——LSB MSB—— $DATA_A$ ——LSB 9 6

DETAIL DESCRIPTION

The HC2040/HC2041 provides dual variable capacitors by connecting one or more binary weighted capacitors in parallel. Each capacitor has a CMOS switch in series with it. The state of the switch is controlled by a nonvolatile data bit. A logic one closes the switch. Data bits D7-D0 and D15-D8 control the 8 binary weighted capacitors in trim capacitor A and B respectively. Data Bit D0 and D8 control the smallest capacitors, D15 and D7 control the largest capacitors. When all the data bits are zero (DATA=0), the capacitance between pins C1 and C2 is at its minimum value. As the value of DATA increases, the capacitance between pins C1 and C2 increases proportionately. The maximum capacitance occurs when DATA equals 255 (all ones).

$DATA_{A,B}$	CAPACITANCE (C_A, C_B)
Ø	C_{stray}
1	$1/256\ C_{max} + C_{stray}$
2	$2/256\ C_{max} + C_{stray}$
:	
255	$255/256\ C_{max} + C_{stray}$

$C_A = (DATA_A / 256) \cdot C_{max} + C_{stray}$

$C_B = (DATA_B / 256) \cdot C_{max} + C_{stray}$

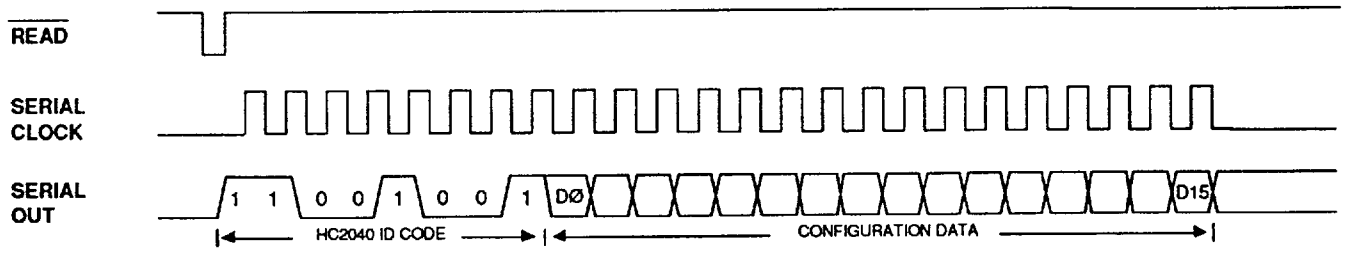
$C_{max} \approx$ 100pF (HC2040), 250pF (HC2041)

$C_{stray} <$ 5pF

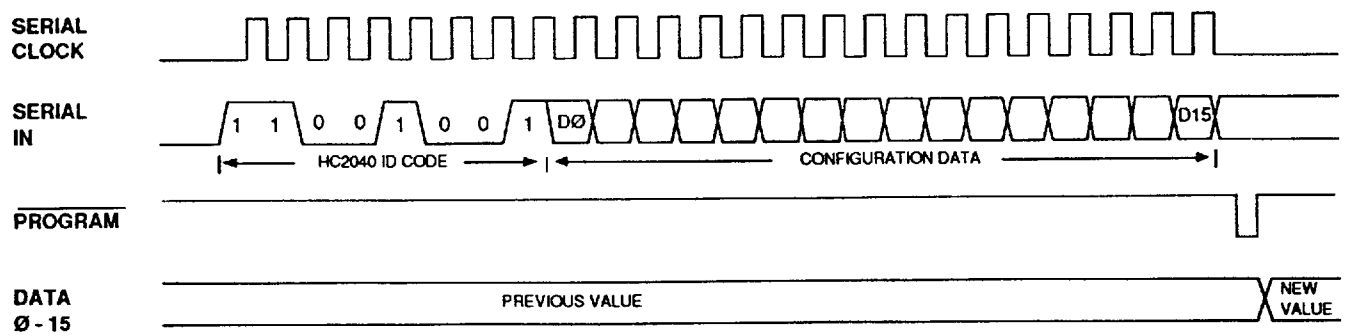
$DATA_A$ = D7 through D0 (D0 = LSB)

$DATA_B$ = D15 through D8 (D8 = LSB)

TYPICAL READ TIMING



TYPICAL WRITE TIMING



ABSOLUTE MAXIMUM RATINGS

VDD.....-.3 to +12V
Inputs (All).....+VSS -.3V to +VDD + .3V
Operating Temperature
Plastic Package.....-40 to + 85° C
Ceramic Package.....-55 to + 125° C
Storage Temperature.....-65 to + 150° C
Note: Specifications for the Military Temperature Range are available upon request.

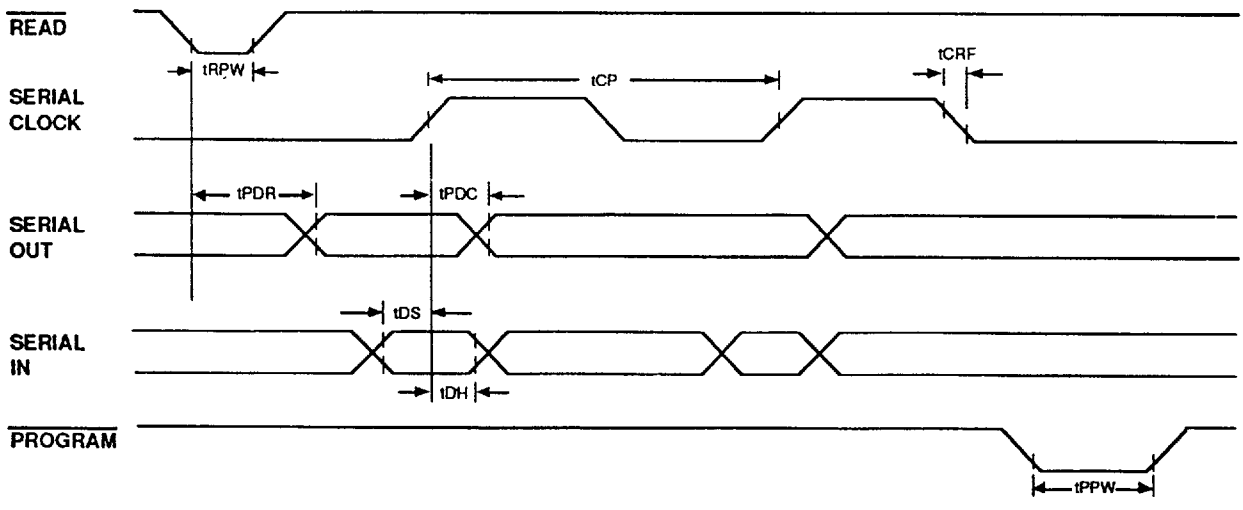
NOTE: Operating the device above the "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS at VDD = 5V

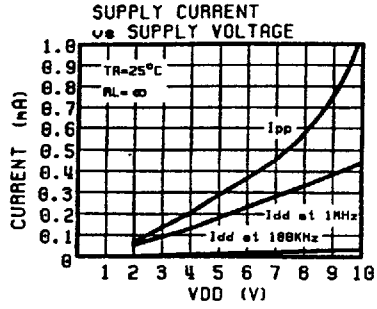
PARAMETER	SYMBOL	CONDITION	-40° C		25° C			85° C		UNITS
			MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.	
Operating Voltage	VDD		3	10	3	-	10	3	10	V
Quiescent Current	IQ	$\overline{Prog}$, $\overline{Read}$=VDD	-	10	-	< 0.1	10	-	10	µA
Dynamic Current (1)	Idd	CLOCK Freq = 1MHz	-	250	-	175	250	-	250	µA
Programming Current	Ipp	$\overline{Prog}$ = 0 V	-	1	-	0.3	0.5	-	0.25	mA
Pull Up Resistance (2)	Rint		10	50	15	35	75	20	100	KΩ
Input High Level	Vih		3.5	-	3.5	2.75	-	3.5	-	V
Input Low Level	Vil		-	1.5	-	2.25	1.5	-	1.5	V
Input Leakage Current	IL	Vin = 2.5V	-	1	-	< 0.001	1	-	1	µA
Input Capacitance	Ci		-	-	-	5	-	-	-	pF
Output High Level	Voh	Iin = 1 mA	4.80	-	4.70	4.85	-	4.60	-	V
Output Low Level	Vol	Iin = 1 mA		0.10		0.06	0.15	-	0.20	V
Clock Rate	tCP	50% Duty Cycle	DC		DC	5	2	DC	1	MHz
Clock Rise/Fall Times	tCRF		-	1	-	-	1	-	1	µs
Data Set-up Time	tDS		15	-	20	10	-	25	-	ns
Data Hold Time	tDH		10	-	10	- 10	-	10	-	ns
Read Pulse Width	tRPW		75	-	100	20	-	125	-	ns
Program Pulse Width	tPPW		1	100	1	-	100	1	100	ms
Data Out Prop. Delay	tPDC	Cload = 50pF	-	115	-	85	150	-	200	ns
Data Out Prop. Delay	tPDR	Cload = 50pF	-	115	-	85	150	-	200	ns
Nonvolatile Endurance	NVE	tPPW = 10 ms	-	10^5	-	10^6	10^5	-	10^5	Cycles
Nonvolatile Retention	NVR	Temp ≤ 125°C	10	-	10	-	-	10	-	Years
Capacitance (Max) 2040	C	Data = FF (Hex)	75	125	75	100	125	75	125	pF
Capacitance (Max) 2041	C	Data = FF (Hex)	200	300	200	250	300	200	300	pF
Dielectric Absorption	DA		-	-	-	0.6	1.0	-	-	%
NonLinearity	NLin		-	-	-	0.25	0.50	-	-	%FS
Max. Step Error 2040	MSE		-	-	-	0.25	0.50	-	-	LSB
Max. Step Error 2041	MSE		-	-	-	0.10	0.25	-	-	LSB
Temperature Coefficent	TC	Data = FF (Hex)	-	-	-	60	100	-	-	ppm/°C

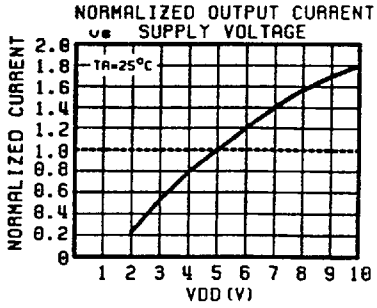
Note (1): $\overline{Read}$ and $\overline{Program}$ = VDD, Serial In = 0.5 MHz Square Wave, Serial Out Load = 10pF.
Note (2): $\overline{Read}$ and $\overline{Program}$ inputs

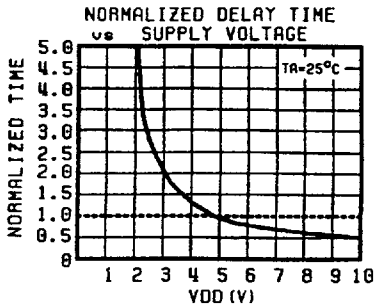
TIMING DIAGRAM

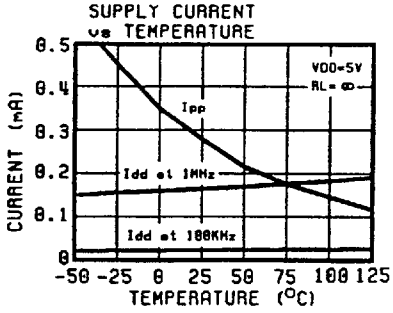


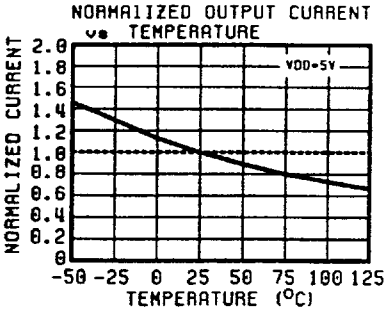
TYPICAL OPERATING CHARACTERISTICS

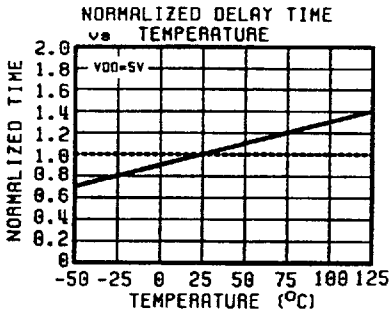


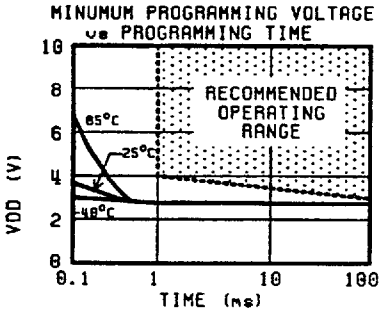


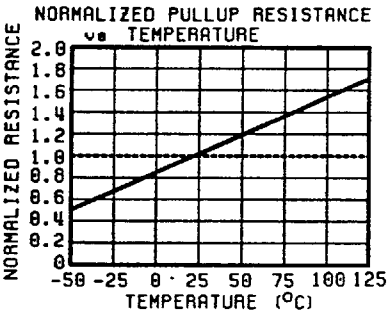


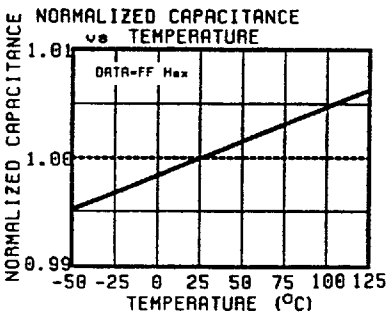






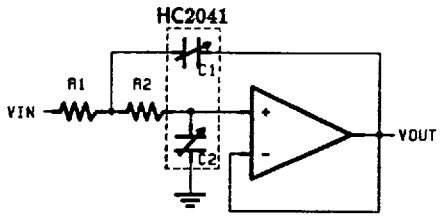




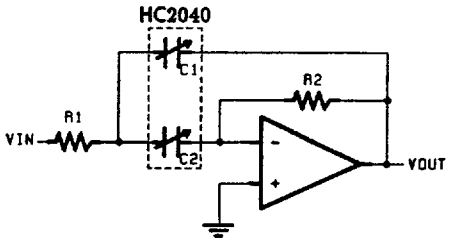


TYPICAL APPLICATIONS

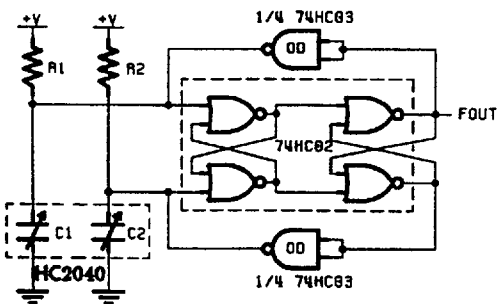
LOW PASS FILTER



BANDPASS FILTER



RELAXATION OSCILLATOR



SINE WAVE OSCILLATOR