CY7C43622
CY7C43632/CY7C43642
CY7C43662/CY7C43682

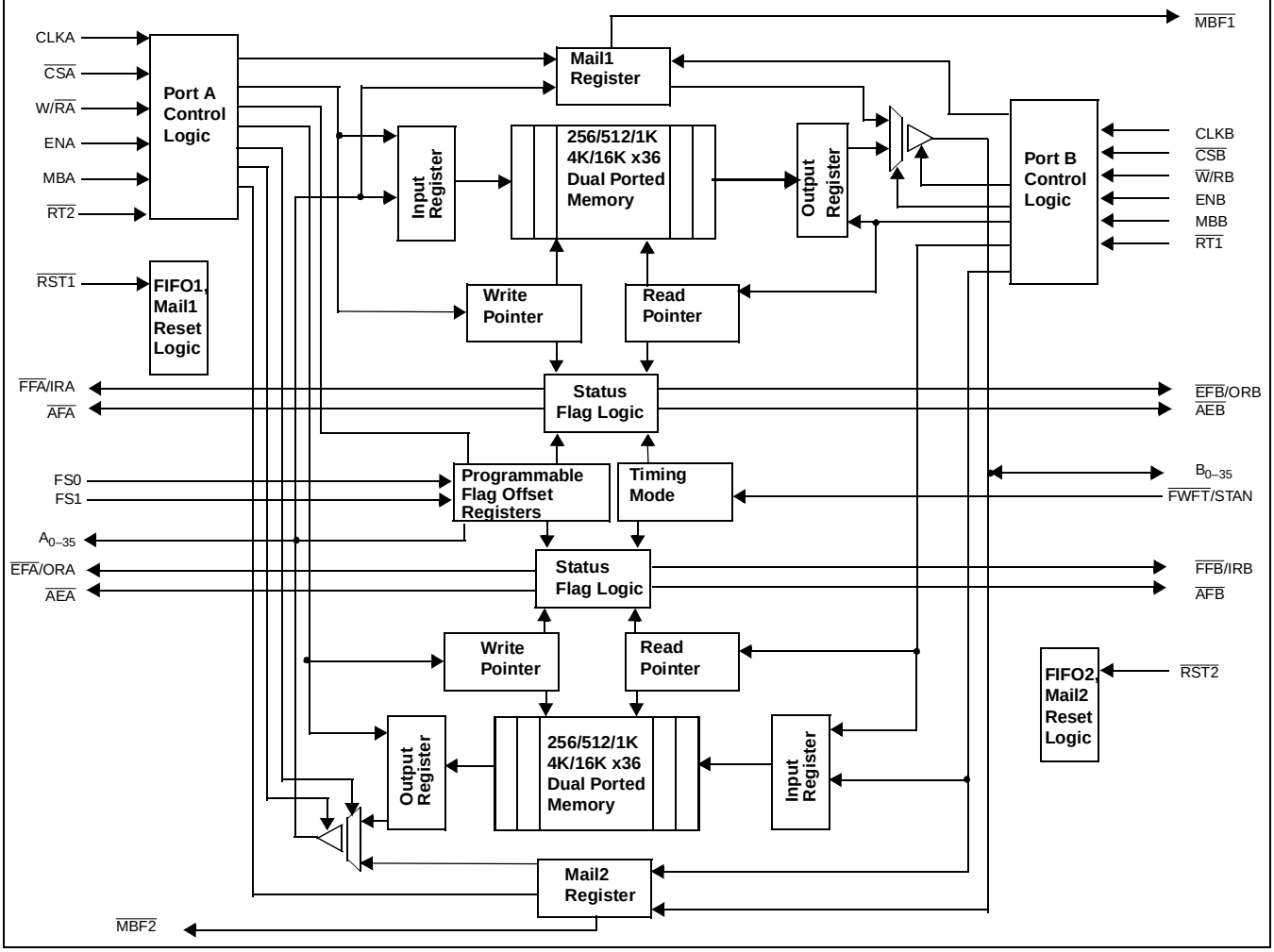
PRELIMINARY

256/512/1K/4K/16K x36 x2 Bidirectional Synchronous FIFO

Features

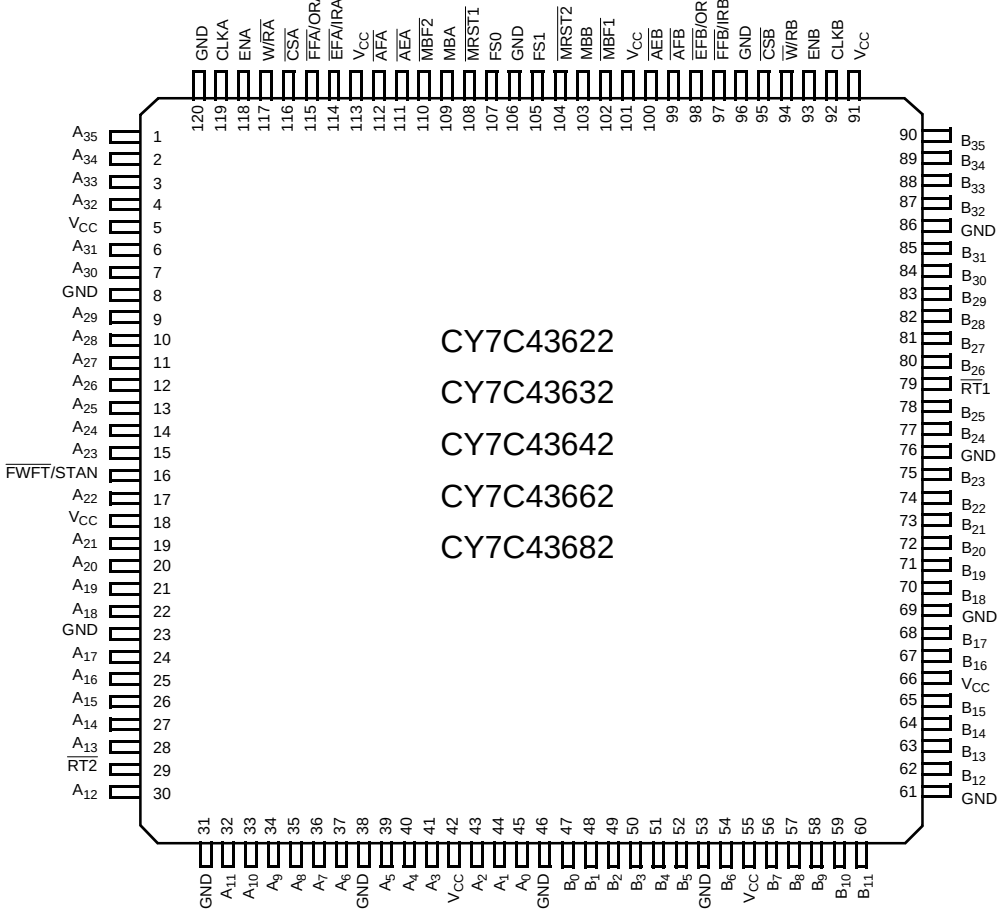
- High-speed, low-power, bidirectional, First-In First-Out (FIFO) memories
- 256x36x2 (CY7C43622)
- 512x36x2 (CY7C43632)
- 1Kx36x2 (CY7C43642)
- 4Kx36x2 (CY7C43662)
- 16Kx36x2 (CY7C43682)
- 0.35-micron CMOS for optimum speed/power
- High speed 133-MHz operation (7.5-ns read/write cycle times)
- Low power
  - I_{CC}= 100 mA
  - I_{SB}= 10 mA
- Fully asynchronous and simultaneous read and write operation permitted
- Mailbox bypass register for each FIFO
- Parallel Programmable Almost Full and Almost Empty flags
- Retransmit function
- Standard or FWFT mode user selectable
- 120-pin TQFP packaging
- Pin-compatible, feature enhanced, density upgrade to IDT723622/32/42 family
- Easily expandable in width and depth

Logic Block Diagram



Pin Configuration

TQFP
Top View



Functional Description

The CY7C436X2 is a monolithic, high-speed, low-power, CMOS Bidirectional Synchronous (clocked) FIFO memory which supports clock frequencies up to 133 MHz and has read access times as fast as 6 ns. Two independent 256/512/1K/4K/16K x 36 dual-port SRAM FIFOs on board each chip buffer data in opposite directions.

The CY7C436X2 is a synchronous (clocked) FIFO, meaning each port employs a synchronous interface. All data transfers through a port are gated to the LOW-to-HIGH transition of a port clock by enable signals. The clocks for each port are independent of one another and can be asynchronous or coincident. The enables for each port are arranged to provide a simple bidirectional interface between microprocessors and/or buses with synchronous control.

Communication between each port may bypass the FIFOs via two mailbox registers. The mailbox registers' width matches the selected Port B bus width. Each mailbox register has a flag ($\overline{MBF1}$ and $\overline{MBF2}$) to signal when new mail has been stored.

Master Reset initializes the read and write pointers to the first location of the memory array, and selects parallel flag programming, or one of the three possible default flag offset settings, 8, 16, or 64. Each FIFO has its own independent Master Reset pin, $\overline{RST1}$ and $\overline{RST2}$.

The CY7C436X2 have two modes of operation: In the CY Standard Mode, the first word written to an empty FIFO is deposited into the memory array. A read operation is required to access that word (along with all other words residing in memory). In the First-Word Fall-Through Mode (FWFT), the first word (36-bit wide) written to an empty FIFO appears automatically on the outputs, no read operation required (nevertheless, accessing subsequent words does necessitate a formal read request). The state of the $\overline{FWFT}$/STAN pin during FIFO operation determines the mode in use.

Each FIFO has a combined Empty/Output Ready Flag ($\overline{EFA}$/ORA and $\overline{EFB}$/ORB) and a combined Full/Input Ready Flag ($\overline{FFA}$/IRA and $\overline{FFB}$/IRB). The $\overline{EF}$ and $\overline{FF}$ functions are selected in the CY Standard Mode. $\overline{EF}$ indicates whether the memory is full or not. The IR and OR functions are selected in the First-Word Fall-Through Mode. IR indicates whether or not the FIFO has available memory locations. OR shows whether the FIFO has data available for reading or not. It marks the presence of valid data on the outputs.

Each FIFO has a programmable Almost Empty flag ($\overline{AEA}$ and $\overline{AEB}$) and a programmable Almost Full flag ($\overline{AFA}$ and $\overline{AFB}$). $\overline{AEA}$ and $\overline{AEB}$ indicate when a selected number of words written to FIFO memory achieve a predetermined "almost empty state." $\overline{AFA}$ and $\overline{AFB}$ indicate when a selected number of words written to the memory achieve a predetermined "almost full state."

IRA, IRB, $\overline{AFA}$, and $\overline{AFB}$ are synchronized to the port clock that writes data into its array. ORA, ORB, $\overline{AEA}$, and $\overline{AEB}$ are synchronized to the port clock that reads data from its array. Programmable offset for $\overline{AEA}$, $\overline{AEB}$, $\overline{AFA}$, and $\overline{AFB}$ are loaded in parallel using Port A. Three default offset settings are also provided. The $\overline{AEA}$ and $\overline{AEB}$ threshold can be set at 8, 16, or 64 locations from the empty boundary and $\overline{AFA}$ and $\overline{AFB}$ threshold can be set at 8, 16, or 64 locations from the full boundary. All these choices are made using the FS0 and FS1 inputs during Master Reset.

Two or more devices may be used in parallel to create wider data paths. If at any time the FIFO is not actively performing a function, the chip will automatically power down. During the power-down state, supply current consumption (I_{CC}) is at a minimum. Initiating any operation (by activating control inputs) will immediately take the device out of the power-down state.

The CY7C436X2 are characterized for operation from 0°C to 70°C. Input ESD protection is greater than 2001V, and latch-up is prevented by the use of guard rings.

Selection Guide

		CY7C43622/32/42/62/82 -7	CY7C43622/32/42/62/82 -10	CY7C43622/32/42/62/82 -15
Maximum Frequency (MHz)		133	100	66.7
Maximum Access Time (ns)		6	8	10
Minimum Cycle Time (ns)		7.5	10	15
Minimum Data or Enable Set-Up (ns)		3	4	5
Minimum Data or Enable Hold (ns)		0	0	0
Maximum Flag Delay (ns)		6	8	8
Active Power Supply Current (I_{CC1}) (mA)	Commercial	100	100	100
	Industrial			10

	CY7C43622	CY7C43632	CY7C43642	CY7C43662	CY7C43682
Density	256 x 36	512 x 36	1K x 36	4K x 36	16K x 36
Package	120 TQFP	120 TQFP	120 TQFP	120 TQFP	120 TQFP

Pin Definitions

Signal Name	Description	I/O	Function
A_{0-35}	Port A Data	I/O	36-bit bidirectional data port for side A.
$\overline{AEA}$	Port A Almost Empty Flag	O	Programmable Almost Empty flag synchronized to CLKA. It is LOW when the number of words in FIFO2 is less than or equal to the value in the Almost Empty A offset register, X2.
$\overline{AEB}$	Port B Almost Empty Flag	O	Programmable Almost Empty flag synchronized to CLKB. It is LOW when the number of words in FIFO1 is less than or equal to the value in the Almost Empty B offset register, X1.
$\overline{AFA}$	Port A Almost Full Flag	O	Programmable Almost Full flag synchronized to CLKA. It is LOW when the number of empty locations in FIFO1 is less than or equal to the value in the Almost Full A offset register, Y1.
$\overline{AFB}$	Port B Almost Full Flag	O	Programmable Almost Full flag synchronized to CLKB. It is LOW when the number of empty locations in FIFO2 is less than or equal to the value in the Almost Full B offset register, Y2.
B_{0-35}	Port B Data	I/O	36-bit bidirectional data port for side B.
$\overline{FWFT}$/STAN	Big Endian/ First-Word Fall-Through Select	I	During Master Reset. A HIGH on $\overline{FWFT}$ selects CY Standard mode, a LOW selects First-Word Fall-Through mode. Once the timing mode has been selected, the level on $\overline{FWFT}$/STAN must be static throughout device operation.
CLKA	Port A Clock	I	CLKA is a continuous clock that synchronizes all data transfers through Port A and can be asynchronous or coincident to CLKB. $\overline{FFA}$/IRA, $\overline{EFA}$/ORA, $\overline{AFA}$, and $\overline{AEA}$ are all synchronized to the LOW-to-HIGH transition of CLKA.
CLKB	Port B Clock	I	CLKB is a continuous clock that synchronizes all data transfers through Port B and can be asynchronous or coincident to CLKA. $\overline{FFB}$/IRB, $\overline{EFB}$/ORB, $\overline{AFB}$, and $\overline{AEB}$ are all synchronized to the LOW-to-HIGH transition of CLKB.
$\overline{CSA}$	Port A Chip Select	I	$\overline{CSA}$ must be LOW to enable a LOW-to HIGH transition of CLKA to read or write on Port A. The A_{0-35} outputs are in the high-impedance state when $\overline{CSA}$ is HIGH.
$\overline{CSB}$	Port B Chip Select	I	$\overline{CSB}$ must be LOW to enable a LOW-to HIGH transition of CLKB to read or write on Port B. The B_{0-35} outputs are in the high-impedance state when $\overline{CSB}$ is HIGH.
$\overline{EFA}$/ORA	Port A Empty/ Output Ready Flag	O	This is a dual-function pin. In the CY Standard Mode, the $\overline{EFA}$ function is selected. $\overline{EFA}$ indicates whether or not the FIFO2 memory is empty. In the FWFT mode, the ORA function is selected. ORA indicates the presence of valid data on A_{0-35} outputs, available for reading. $\overline{EFA}$/ORA is synchronized to the LOW-to-HIGH transition of CLKA.
$\overline{EFB}$/ORB	Port B Empty/ Output Ready Flag	O	This is a dual-function pin. In the CY Standard Mode, the $\overline{EFB}$ function is selected. $\overline{EFB}$ indicates whether or not the FIFO1 memory is empty. In the FWFT mode, the ORB function is selected. ORB indicates the presence of valid data on B_{0-35} outputs, available for reading. $\overline{EFB}$/ORB is synchronized to the LOW-to-HIGH transition of CLKB.
ENA	Port A Enable	I	ENA must be HIGH to enable a LOW-to-HIGH transition of CLKA to read or write data on Port A.
ENB	Port B Enable	I	ENB must be HIGH to enable a LOW-to-HIGH transition of CLKB to read or write data on Port B.
$\overline{FFA}$/IRA	Port A Full/Input Ready Flag	O	This is a dual-function pin. In the CY Standard Mode, the $\overline{FFA}$ function is selected. $\overline{FFA}$ indicates whether or not the FIFO1 memory is full. In the FWFT mode, the IRA function is selected. IRA indicates whether or not there is space available for writing to the FIFO1 memory. $\overline{FFA}$/IRA is synchronized to the LOW-to-HIGH transition of CLKA.
$\overline{FFB}$/IRB	Port B Full/Input Ready Flag	O	This is a dual-function pin. In the CY Standard Mode, the $\overline{FFB}$ function is selected. $\overline{FFB}$ indicates whether or not the FIFO2 memory is full. In the FWFT mode, the IRB function is selected. IRB indicates whether or not there is space available for writing to the FIFO2 memory. $\overline{FFB}$/IRB is synchronized to the LOW-to-HIGH transition of CLKB.

Pin Definitions (continued)

Signal Name	Description	I/O	Function
FS1	Flag Offset Select 1	I	The LOW-to-HIGH transition of a FIFO's reset input latches the values of FS0 and FS1. If either FS0 or FS1 is HIGH when a reset input goes HIGH, one of the three preset values (8, 16, or 64) is selected as the offset for the FIFO's Almost Full and Almost Empty flags. If both FIFOs are reset simultaneously and both FS0 and FS1 are LOW when RST1 and RST2 go HIGH, the first four writes to FIFO1 Almost Empty offsets for both FIFOs.
FS0	Flag Offset Select 0	I	
MBA	Port A Mailbox Select	I	A HIGH level on MBA chooses a mailbox register for a Port A read or write operation. When the A_{0-35} outputs are active, a HIGH level on MBA selects data from the Mail2 register for output and a LOW level selects FIFO2 output register data for output.
MBB	Port B Mailbox Select	I	A HIGH level on MBB chooses a mailbox register for a Port B read or write operation. When the B_{0-35} outputs are active, a HIGH level on MBB selects data from the Mail1 register for output and a LOW level selects FIFO1 output register data for output.
$\overline{MBF1}$	Mail1 Register Flag	O	$\overline{MBF1}$ is set LOW by a LOW-to-HIGH transition of CLKA that writes data to the Mail1 register. Writes to the Mail1 register are inhibited while $\overline{MBF1}$ is LOW. $\overline{MBF1}$ is set HIGH by a LOW-to-HIGH transition of CLKB when a Port B read is selected and MBB is HIGH. $\overline{MBF1}$ is set HIGH following either a Master or Partial Reset of FIFO1.
$\overline{MBF2}$	Mail2 Register Flag	O	$\overline{MBF2}$ is set LOW by a LOW-to-HIGH transition of CLKB that writes data to the Mail2 register. Writes to the Mail2 register are inhibited while $\overline{MBF2}$ is LOW. $\overline{MBF2}$ is set HIGH by a LOW-to-HIGH transition of CLKA when a Port A read is selected and MBA is HIGH. $\overline{MBF2}$ is set HIGH following either a Master or Partial Reset of FIFO2.
$\overline{RST1}$	FIFO1 Master Reset	I	A LOW on this pin initializes the FIFO1 read and write pointers to the first location of memory and sets the Port B output register to all zeroes. A LOW pulse on $\overline{RST1}$ selects the programming method (serial or parallel) and one of three programmable flag default offsets for FIFO1. Four LOW-to-HIGH transitions of CLKA and four LOW-to-HIGH transitions of CLKB must occur while $\overline{RST1}$ is LOW.
$\overline{RST2}$	FIFO2 Master Reset	I	A LOW on this pin initializes the FIFO2 read and write pointers to the first location of memory and sets the Port A output register to all zeroes. A LOW pulse on $\overline{RST2}$ selects one of three programmable flag default offsets for FIFO2. Four LOW-to-HIGH transitions of CLKA and four LOW-to-HIGH transitions of CLKB must occur while $\overline{RST2}$ is LOW.
W/$\overline{RA}$	Port A Write/ Read Select	I	A HIGH selects a write operation and a LOW selects a read operation on Port A for a LOW-to-HIGH transition of CLKA. The A_{0-35} outputs are in the HIGH impedance state when W/$\overline{RA}$ is HIGH.
$\overline{W}$/RB	Port B Write/ Read Select	I	A LOW selects a write operation and a HIGH selects a read operation on Port B for a LOW-to-HIGH transition of CLKB. The B_{0-35} outputs are in the HIGH impedance state when $\overline{W}$/RB is LOW.

Maximum Ratings[1]

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... –65°C to +150°C

Ambient Temperature with Power Applied..... –55°C to +125°C

Supply Voltage to Ground Potential.....–0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State[2] .....–0.5V to V_{CC}+0.5V

DC Input Voltage[2].....–0.5V to V_{CC}+0.5V

Output Current into Outputs (LOW) .....20 mA

Static Discharge Voltage .....>2001V (per MIL-STD-883, Method 3015)

Latch-Up Current.....>200mA

Operating Range

Range	Ambient Temperature	V_{CC}[3]
Commercial	0°C to +70°C	5.0V ± 0.5V
Industrial	–40°C to +85°C	5.0V ± 0.5V

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions		CY7C43622/32/42/62/82 Min.	CY7C43622/32/42/62/82 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = 4.5V, I_{OH} = –4.0 mA		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = 4.5V, I_{OL} = 8.0 mA			0.5	V
V_{IH}	Input HIGH Voltage			2.0	V_{CC}	V
V_{IL}	Input LOW Voltage			–0.5	0.8	V
I_{IX}	Input Leakage Current	V_{CC} = Max.		–10	+10	µA
I_{OZL} I_{OZH}	Output OFF, High Z Current	$\overline{OE} \geq V_{IH}$, $V_{SS} < V_O < V_{CC}$		–10	+10	µA
I_{CC1}[4]	Active Power Supply Current		Com'l		100	mA
			Ind		100	mA
I_{SB}[5]	Average Standby Current		Com'l		10	mA
			Ind		10	mA

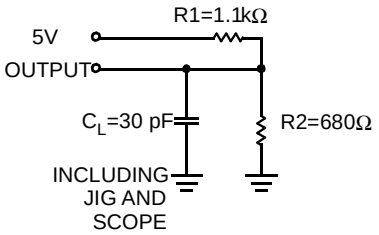
Capacitance[6]

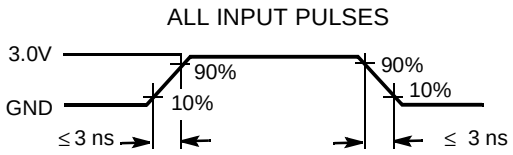
Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 3.3V	4	pF
C_{OUT}	Output Capacitance		8	pF

Notes:

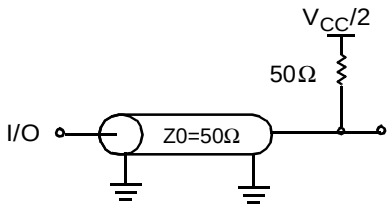
1. Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operationg conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded provided the input and output current ratings are observed.
3. Operating V_{CC} Range for -7 speed is 5.0V ± 0.25V.
4. Input signals switch from 0V to 3V with a rise/fall time of less than 3 ns, clocks and clock enables switch at 20 MHz, while data inputs switch at 10 MHz. Outputs are unloaded.
5. All inputs = V_{CC} – 0.2V, except RCLK and WCLK (which are at frequency = 0 MHz). All outputs are unloaded.
6. Tested initially and after any design or process changes that may affect these parameters.

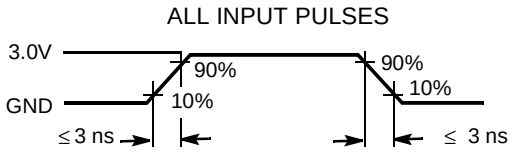
AC Test Loads and Waveforms (-10 & -15)





AC Test Loads and Waveforms (-7)





Switching Characteristics Over the Operating Range

Parameter	Description	CY7C43622/ 32/42/62/82 -7		CY7C43622/ 32/42/62/82 -10		CY7C43622/ 32/42/62/82 -15		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
f_S	Clock Frequency, CLKA or CLKB		133		100		67	MHz
t_{CLK}	Clock Cycle Time, CLKA or CLKB	7.5		10		15		ns
t_{CLKH}	Pulse Duration, CLKA or CLKB HIGH	3.5		4		6		ns
t_{CLKL}	Pulse Duration, CLKA or CLKB LOW	3.5		4		6		ns
t_{DS}	Set-Up Time, $A_{0–35}$ before CLKA↑ and $B_{0–35}$ before CLKB↑	3		4		5		ns
t_{ENS}	Set-Up Time, $\overline{CSA}$, W/$\overline{RA}$, ENA, and MBA before CLKA↑; $\overline{CSB}$, $\overline{W}$/RB, ENB, and MBB before CLKB↑	3		4		5		ns
t_{RSTS}	Set-Up Time, $\overline{RST1}$ or $\overline{RST2}$ LOW before CLKA↑ or CLKB↑[7]	2.5		4		5		ns
t_{FSS}	Set-Up Time, FS0 and FS1 before $\overline{RST1}$ and $\overline{RST2}$ HIGH	5		7		7.5		ns
t_{BES}	Set-Up Time, $\overline{FWFT}$/STAN before $\overline{RST1}$ and $\overline{RST2}$ HIGH	5		7		7.5		ns
t_{SDS}	Set-Up Time, FS0 before CLKA↑	3		4		5		ns
t_{SENS}	Set-Up Time, FS1 before CLKA↑	3		4		5		ns
t_{FWS}	Set-Up Time, FWFT before CLKA↑	0		0		0		ns
t_{DH}	Hold Time, $A_{0–35}$ after CLKA↑ and $B_{0–35}$ after CLKB↑	0		0		0		ns

Note:
7. Requirement to count the clock edge as one of at least four needed to reset a FIFO.

Switching Characteristics Over the Operating Range (continued)

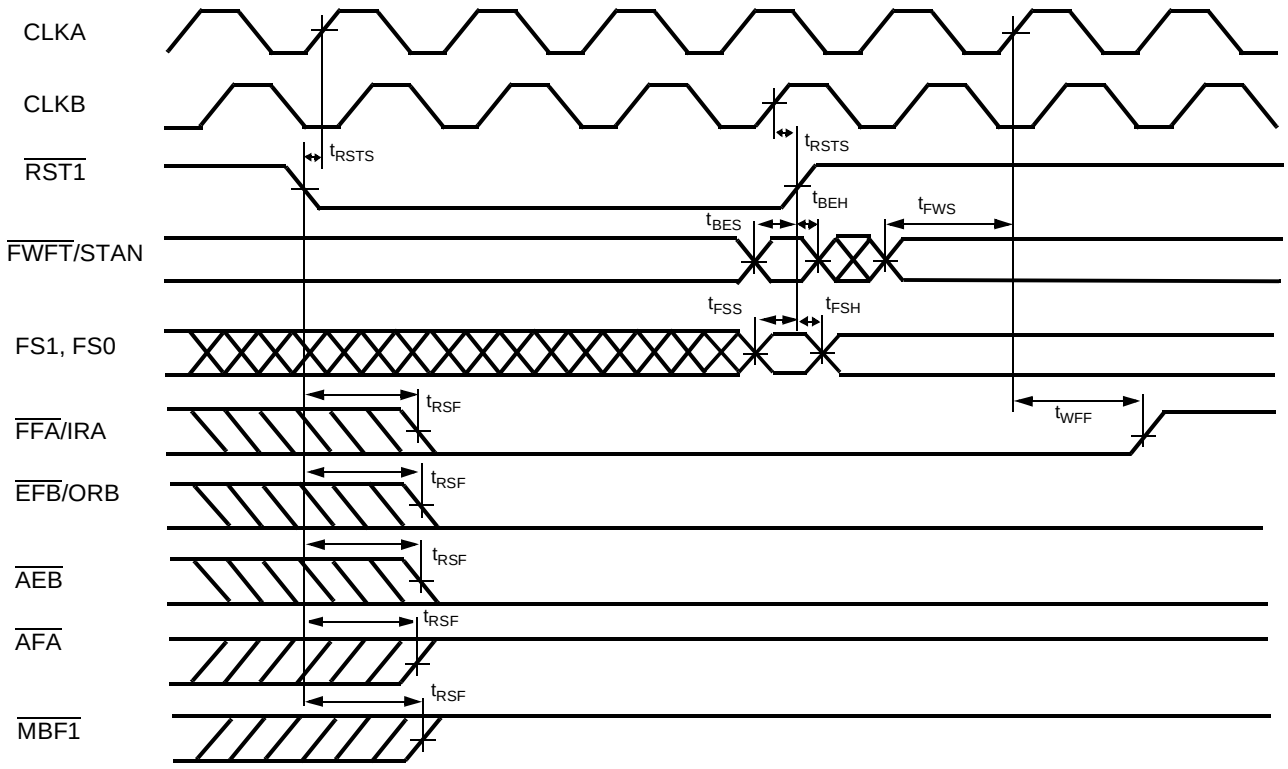
Parameter	Description	CY7C43622/32/42/62/82 -7		CY7C43622/32/42/62/82 -10		CY7C43622/32/42/62/82 -15		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{ENH}	Hold Time, $\overline{CSA}$, W/$\overline{RA}$, ENA, and MBA after CLKA↑; $\overline{CSB}$, $\overline{W}$/RB, ENB, and MBB after CLKB↑	0		0		0		ns
t_{RSTH}	Hold Time, $\overline{RST1}$ or $\overline{RST2}$, LOW after CLKA↑ or CLKB↑[7]	1		2		4		ns
t_{FSH}	Hold Time, FS0 and FS1 after $\overline{RST1}$ and $\overline{RST2}$ HIGH	1		1		2		ns
t_{BEH}	Hold Time, $\overline{FWFT}$/STAN after $\overline{RST1}$ and $\overline{RST2}$ HIGH	1		1		2		ns
t_{SDH}	Hold Time, FS0 after CLKA↑	0		0		0		ns
t_{SENH}	Hold Time, FS1 after CLKA↑	0		0		0		ns
t_{SPH}	Hold Time, FS1 HIGH after $\overline{RST1}$ and $\overline{RST2}$ HIGH	0		1		2		ns
t_{SKEW1}[8]	Skew Time between CLKA↑ and CLKB↑ for $\overline{EFA}$/ORA, $\overline{EFB}$/ORB, $\overline{FFA}$/IRA, and $\overline{FFB}$/IRB	5		5		7.5		ns
t_{SKEW2}[8]	Skew Time between CLKA↑ and CLKB↑ for $\overline{AEA}$, $\overline{AEB}$, $\overline{AFA}$, $\overline{AFB}$	7		8		12		ns
t_A	Access Time, CLKA↑ to $A_{0–35}$ and CLKB↑ to $B_{0–35}$	1	6	1	8	3	10	ns
t_{WFF}	Propagation Delay Time, CLKA↑ to $\overline{FFA}$/IRA and CLKB↑ to $\overline{FFB}$/IRB	1	6	1	8	2	8	ns
t_{REF}	Propagation Delay Time, CLKA↑ to $\overline{EFA}$/ORA and CLKB↑ to $\overline{EFB}$/ORB	1	6	1	8	1	8	ns
t_{PAE}	Propagation Delay Time, CLKA↑ to $\overline{AEA}$ and CLKB↑ to $\overline{AEB}$	1	6	1	8	1	8	ns
t_{PAF}	Propagation Delay Time, CLKA↑ to $\overline{AFA}$ and CLKB↑ to $\overline{AFB}$	1	6	1	8	1	8	ns
t_{PMF}	Propagation Delay Time, CLKA↑ to $\overline{MBF1}$ LOW or $\overline{MBF2}$ HIGH and CLKB↑ to $\overline{MBF2}$ LOW or $\overline{MBF1}$ HIGH	0	6	0	8	0	12	ns
t_{PMR}	Propagation Delay Time, CLKA↑ to $B_{0–35}$[9] and CLKB↑ to $A_{0–35}$[10]	1	7	2	11	3	12	ns
t_{MDV}	Propagation Delay Time, MBA to $A_{0–35}$ valid and MBB to $B_{0–35}$ valid	1	6	2	9	3	11	ns
t_{RSF}	Propagation Delay Time, $\overline{RST1}$ LOW to $\overline{AEB}$ LOW, $\overline{AFA}$ HIGH, $\overline{FFA}$/IRA Low, $\overline{EFB}$/ORB LOW, and $\overline{MBF1}$ HIGH and $\overline{RST2}$ LOW to $\overline{AEA}$ LOW, $\overline{AFB}$ HIGH, $\overline{FFB}$/IRB Low, $\overline{EFA}$/ORA LOW,and $\overline{MBF2}$ HIGH	1	6	1	10	1	15	ns
t_{EN}	Enable Time, $\overline{CSA}$ or W/$\overline{RA}$ LOW to $A_{0–35}$ Active and $\overline{CSB}$ LOW and $\overline{W}$/RB HIGH to $B_{0–35}$ Active	1	6	2	8	2	10	ns
t_{DIS}	Disable Time, $\overline{CSA}$ or W/$\overline{RA}$ HIGH to $A_{0–35}$ at High Impedance and $\overline{CSB}$ HIGH or $\overline{W}$/RB LOW to $B_{0–35}$ at High Impedance	1	5	1	6	1	8	ns
t_{PRT}	Retransmit Pulse Width	60		60		60		ns
t_{RTR}	Retransmit Recovery Time	90		90		90		ns

Notes:

8. Skew time is not a timing constraint for proper device operation and is only included to illustrate the timing relationship between the CLKA cycle and the CLKB cycle.
9. Writing data to the Mail1 register when the $B_{0–35}$ outputs are active and MBB is HIGH.
10. Writing data to the Mail2 register when the $A_{0–35}$ outputs are active and MBA is HIGH.

Switching Waveforms

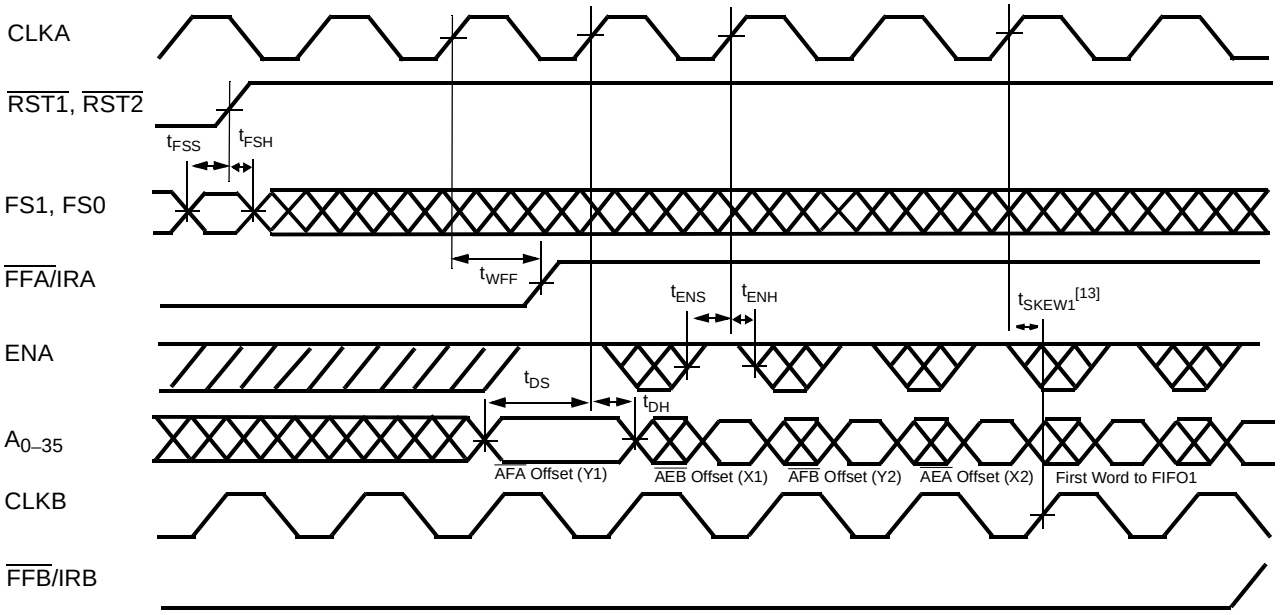
FIFO1 Reset Loading X1 and Y1 with a Preset Value of Eight [11]



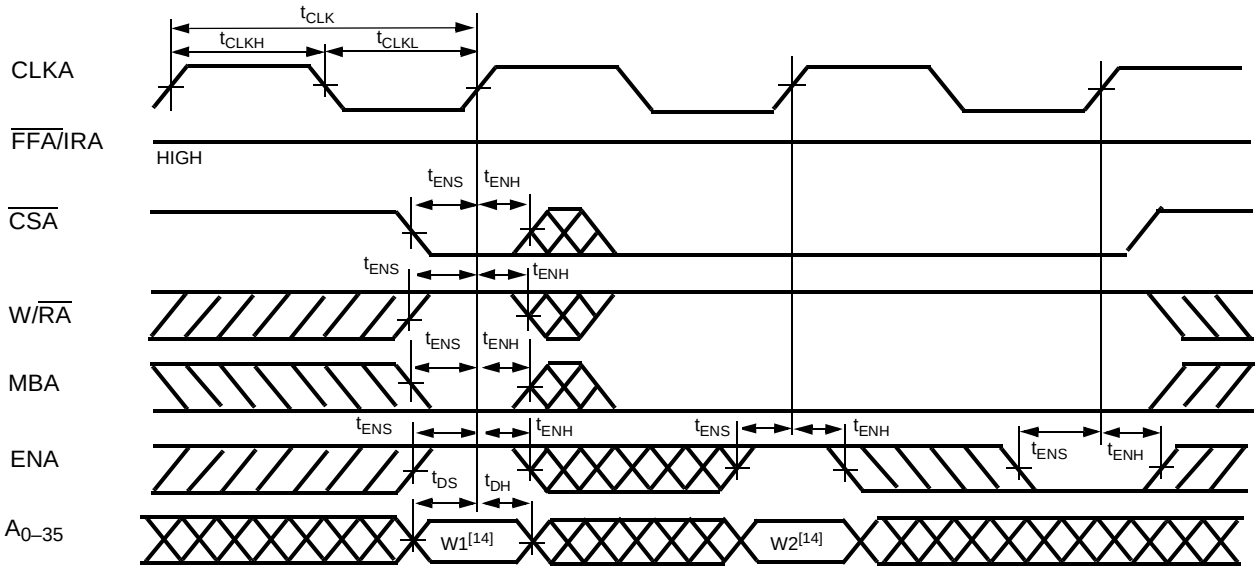
Note:
11. Reset is performed in the same manner for FIFO2 to load X2 and Y2 with a preset value.

Switching Waveforms (continued)

Programming of the Almost-Full Flag and Almost-Empty Flag Offset Values after Reset (CY Standard and FWFT Modes) [12]



Port A Write Cycle Timing for FIFO1 (CY Standard and FWFT Modes)

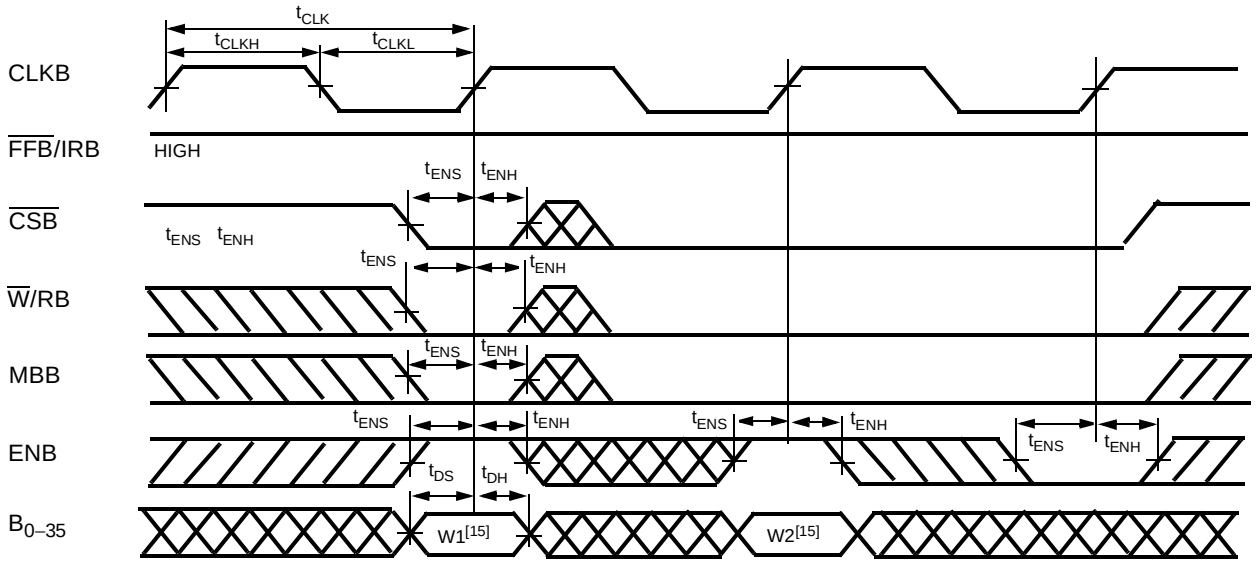


Notes:

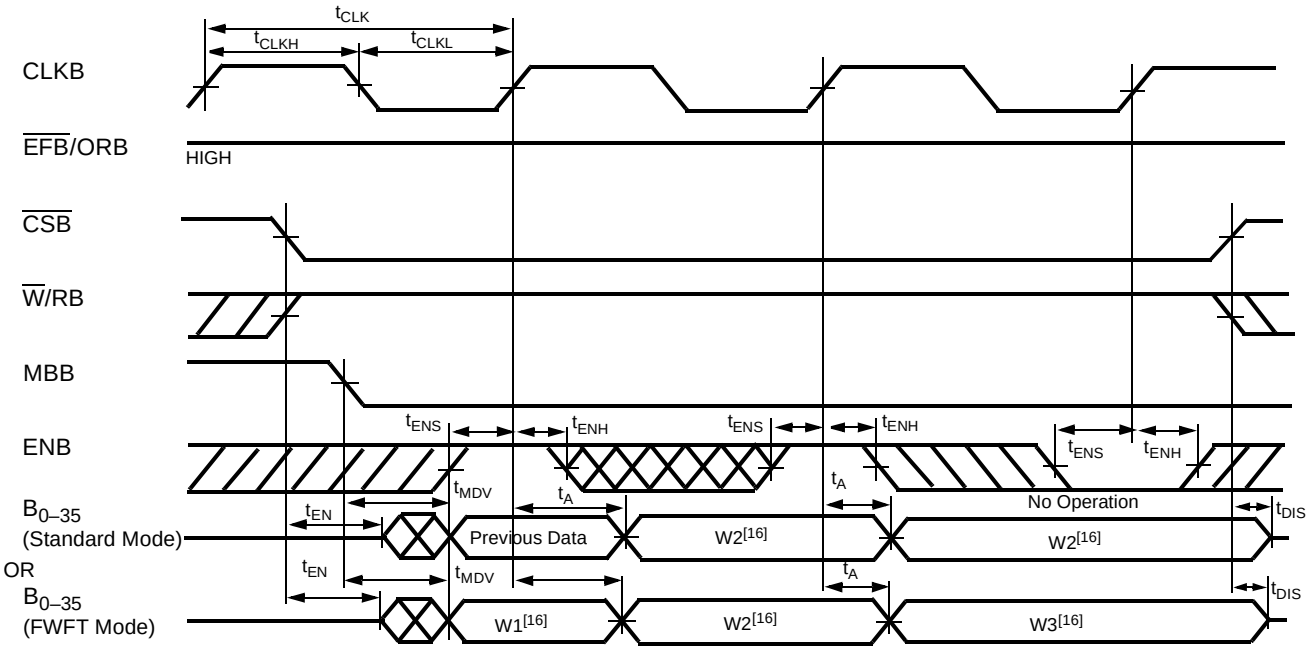
12. CSA=LOW, W/RA=HIGH, MBA=LOW. It is not necessary to program offset register on consecutive clock cycles.
13. t_{SKEW1} is the minimum time between the rising CLKA edge and a rising CLKB for FFB/IRB to transition HIGH in the next cycle. If the time between the rising edge of CLKA and rising edge of CLKB is less than t_{SKEW1}, then FFB/IRB may transition HIGH one cycle later than shown.
14. Written to FIFO1.

Switching Waveforms (continued)

Port B Write Cycle Timing for FIFO2 (CY Standard and FWFT Modes)



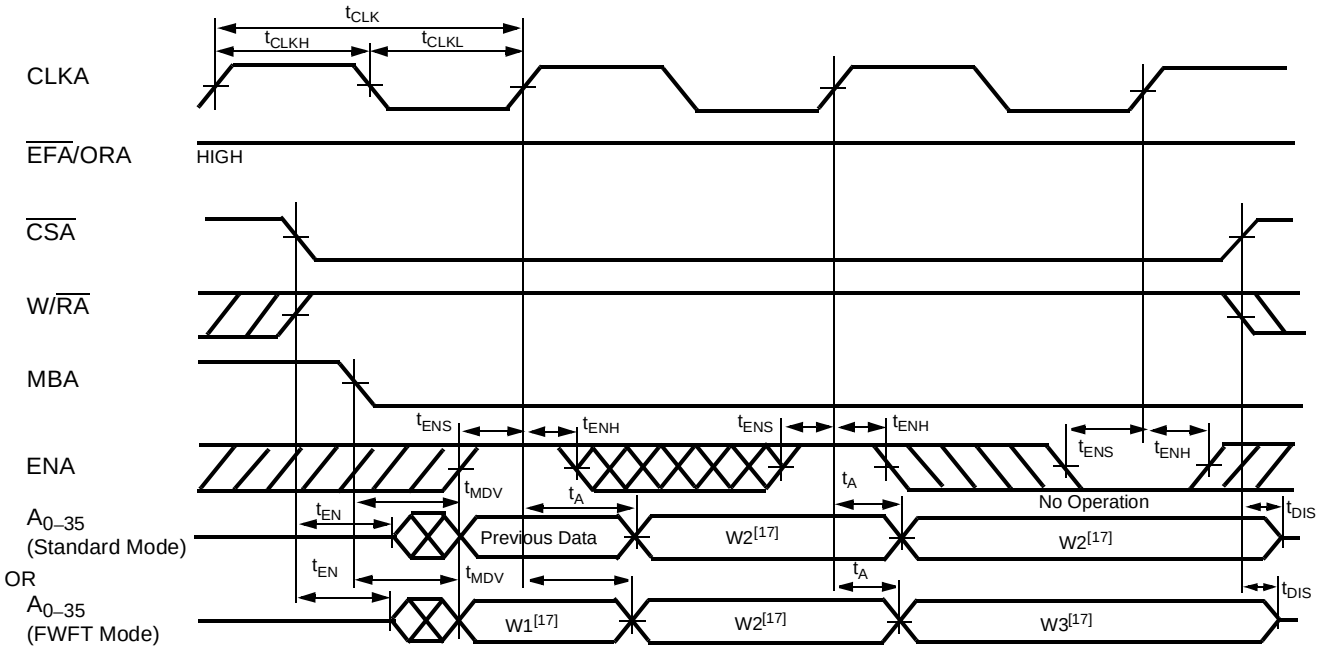
Port B Read Cycle Timing for FIFO1 (CY Standard and FWFT Modes)



Notes:
15. Written to FIFO2.
16. Read from FIFO1.

Switching Waveforms (continued)

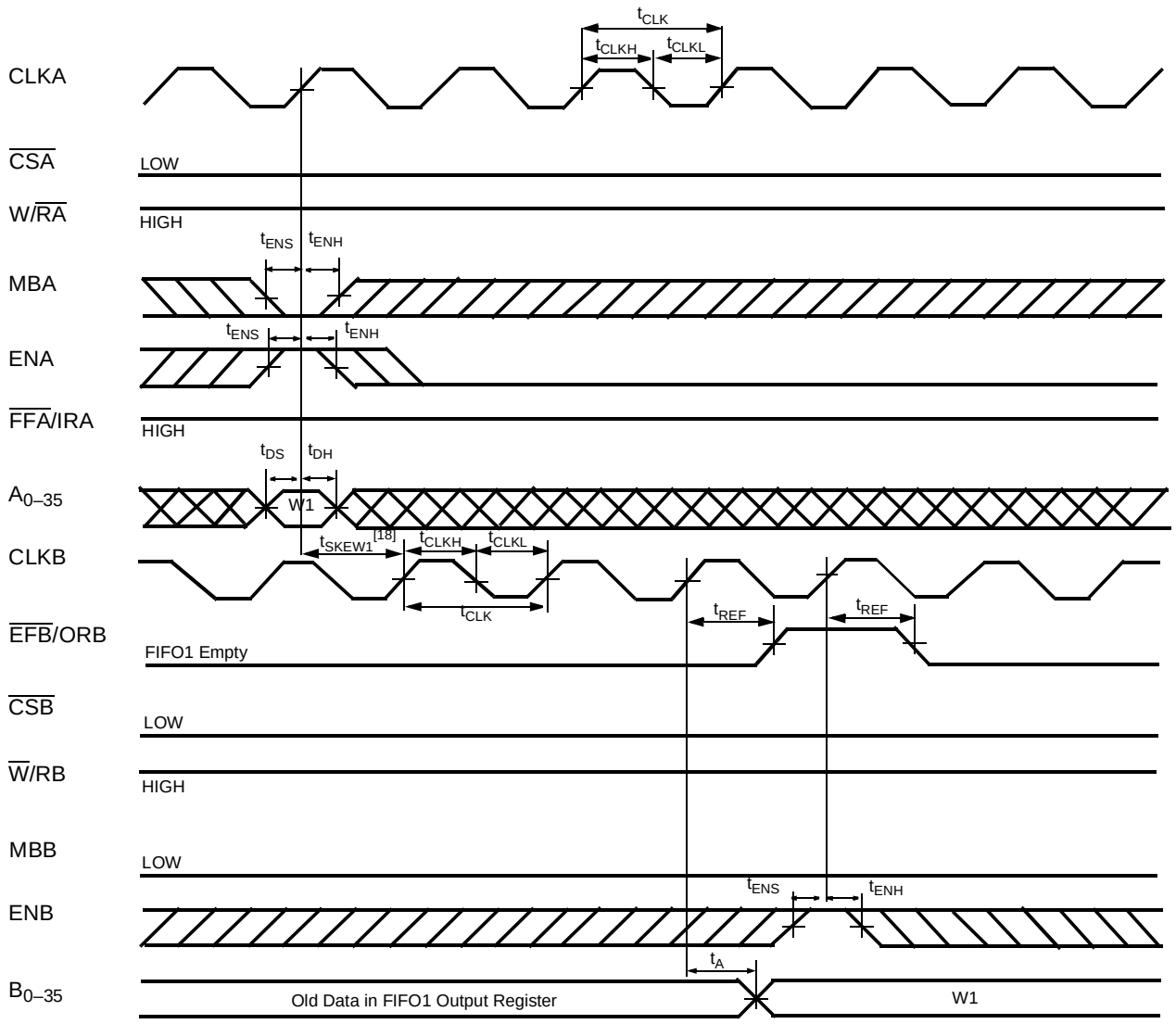
Port A Read Cycle Timing for FIFO2 (CY Standard and FWFT Modes)



Note:
17. Read From FIFO2.

Switching Waveforms (continued)

ORB Flag Timing and First Data Word Fall Through when FIFO1 is Empty (FWFT Mode)

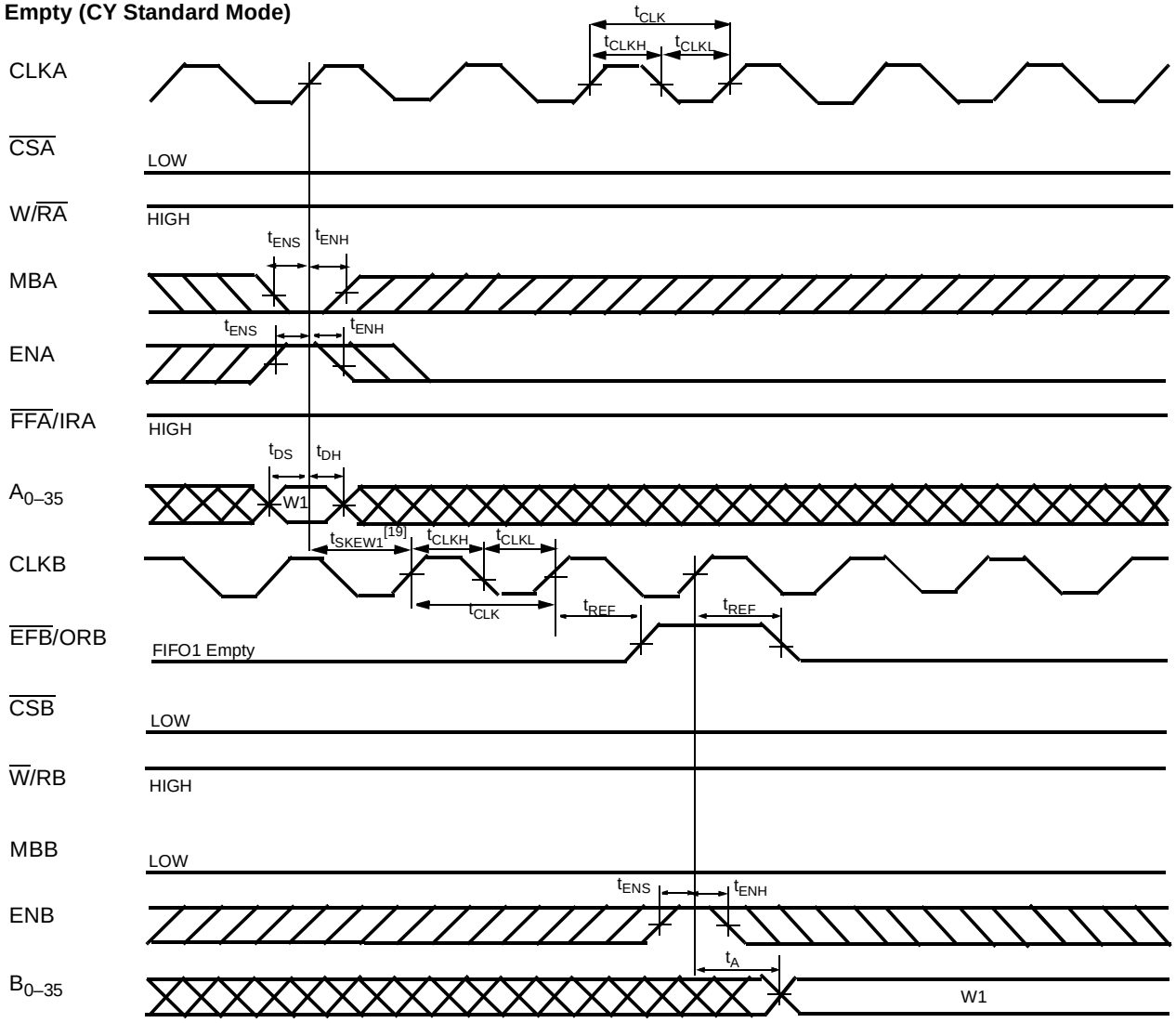


Note:

18. t_{SKEW1} is the minimum time between a rising CLKA edge and a rising CLKB edge for ORB to transition HIGH and to clock the next word to the FIFO1 output register in three CLKB cycles. If the time between the rising CLKA edge and rising CLKB edge is less than t_{SKEW1}, then the transition of ORB HIGH and load of the first word to the output register may occur one CLKB cycle later than shown.

Switching Waveforms (continued)

$\overline{EFB}$ Flag Timing and First Data Read Fall Through when FIFO1 is Empty (CY Standard Mode)

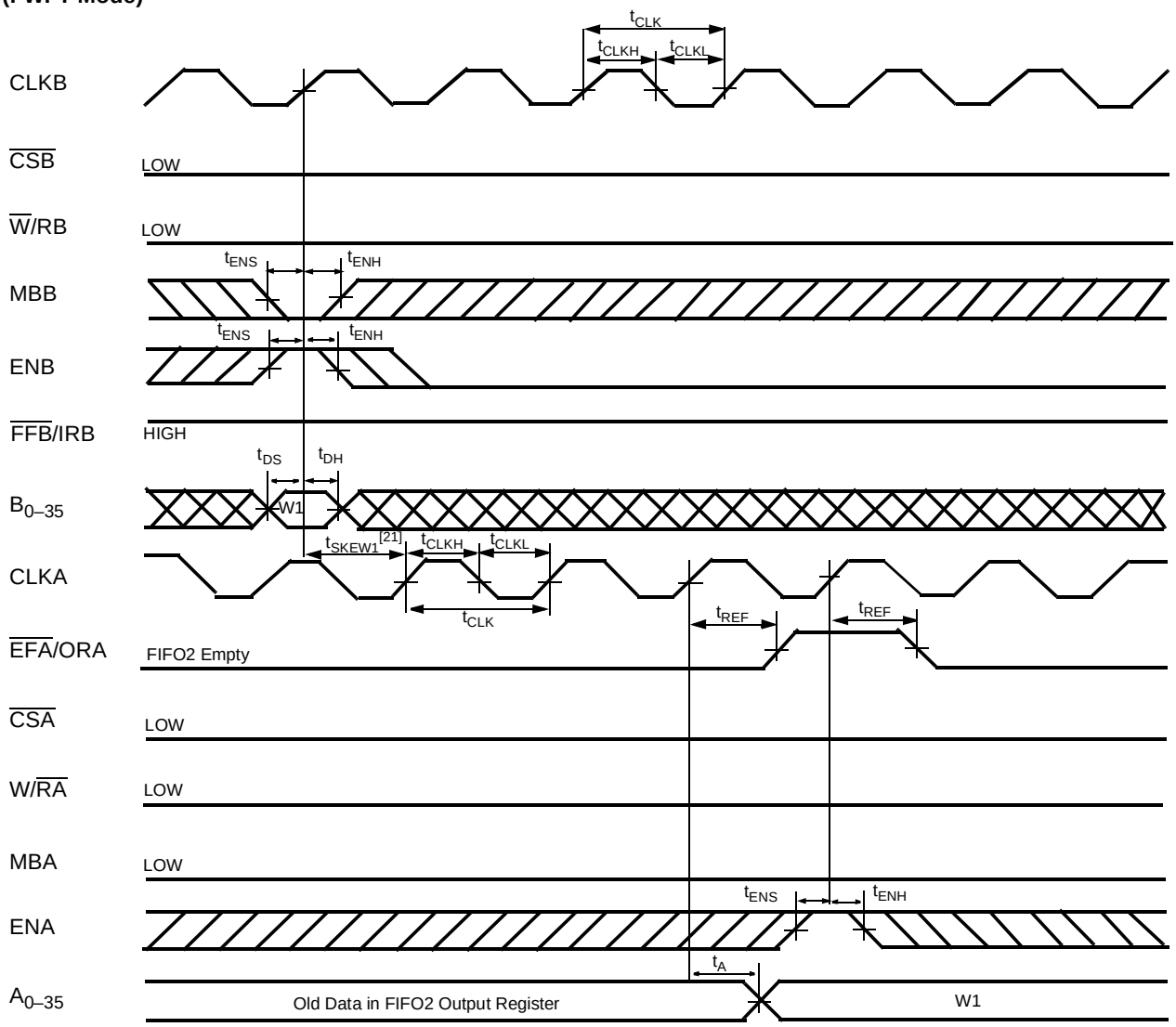


Note:

19. t_{SKEW1} is the minimum time between a rising CLKA edge and a rising CLKB edge for $\overline{EFB}$ to transition HIGH in the next CLKB cycle. If the time between the rising CLKA edge and rising CLKB edge is less than t_{SKEW1}, then the transition of $\overline{EFB}$ HIGH may occur one CLKB cycle later than shown.

Switching Waveforms (continued)

ORA Flag Timing and First Data Word Fall Through when FIFO2 is Empty (FWFT Mode) [20]

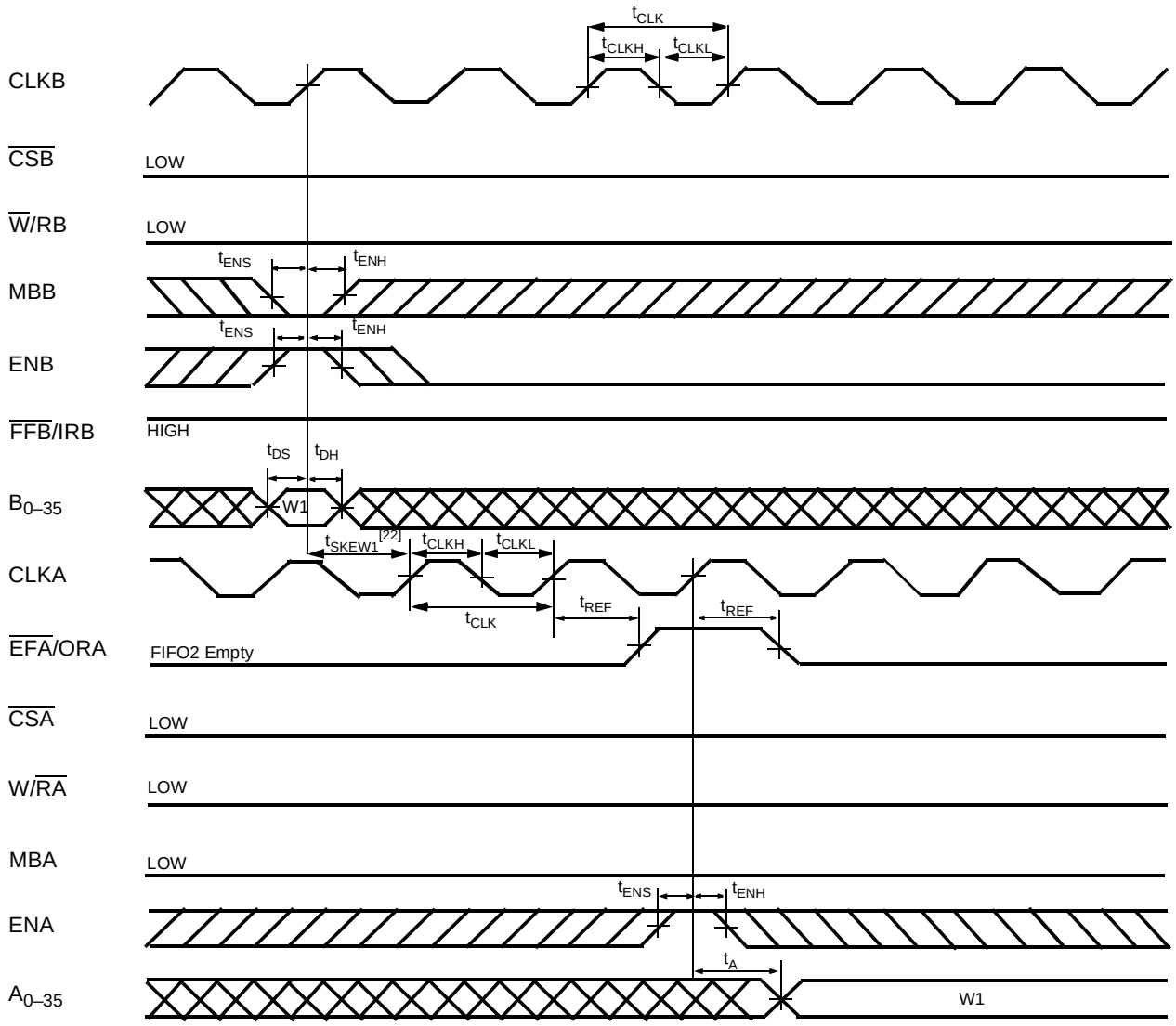


Notes:

20. t_{SKEW1} is referenced to the rising CLKB edge that writes the last word or byte of the long word, respectively.
21. t_{SKEW1} is the minimum time between a rising CLKB edge and a rising CLKA edge for ORA to transition HIGH and to clock the next word to the FIFO2 output register in three CLKA cycles. If the time between the rising CLKB edge and rising CLKA edge is less than t_{SKEW1}, then the transition of ORA HIGH and load of the first word to the output register may occur one CLKA cycle later than shown.

Switching Waveforms (continued)

$\overline{EFA}$ Flag Timing and First Data Read when FIFO2 is Empty (CY Standard Mode)

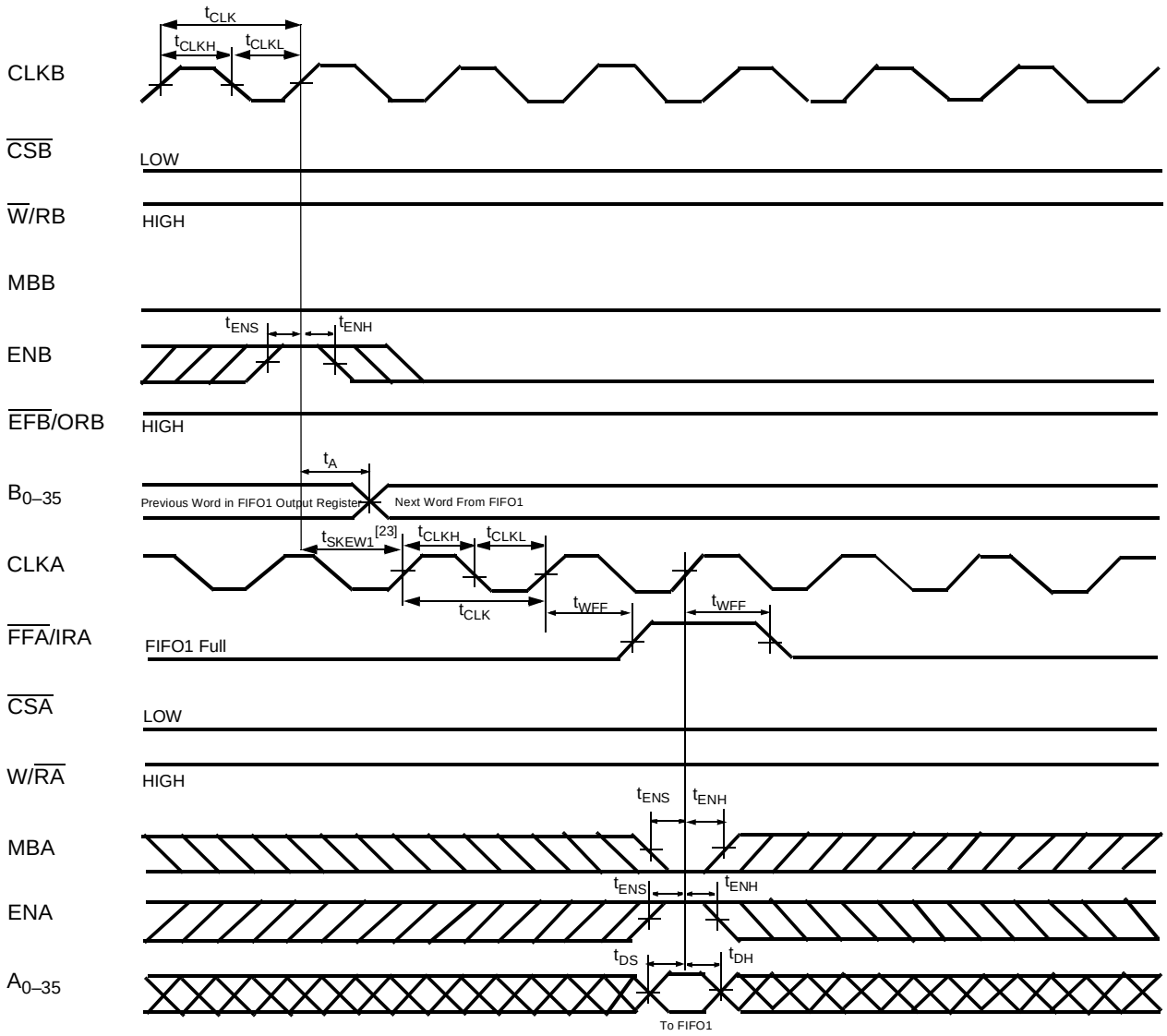


Note:

22. t_{SKEW1} is the minimum time between a rising CLKB edge and a rising CLKA edge for $\overline{EFA}$ to transition HIGH in the next CLKA cycle. If the time between the rising CLKB edge and rising CLKA edge is less than t_{SKEW1}, then the transition of $\overline{EFA}$ HIGH may occur one CLKA cycle later than shown.

Switching Waveforms (continued)

IRA Flag Timing and First Available Write when FIFO1 is Full (FWFT Mode)

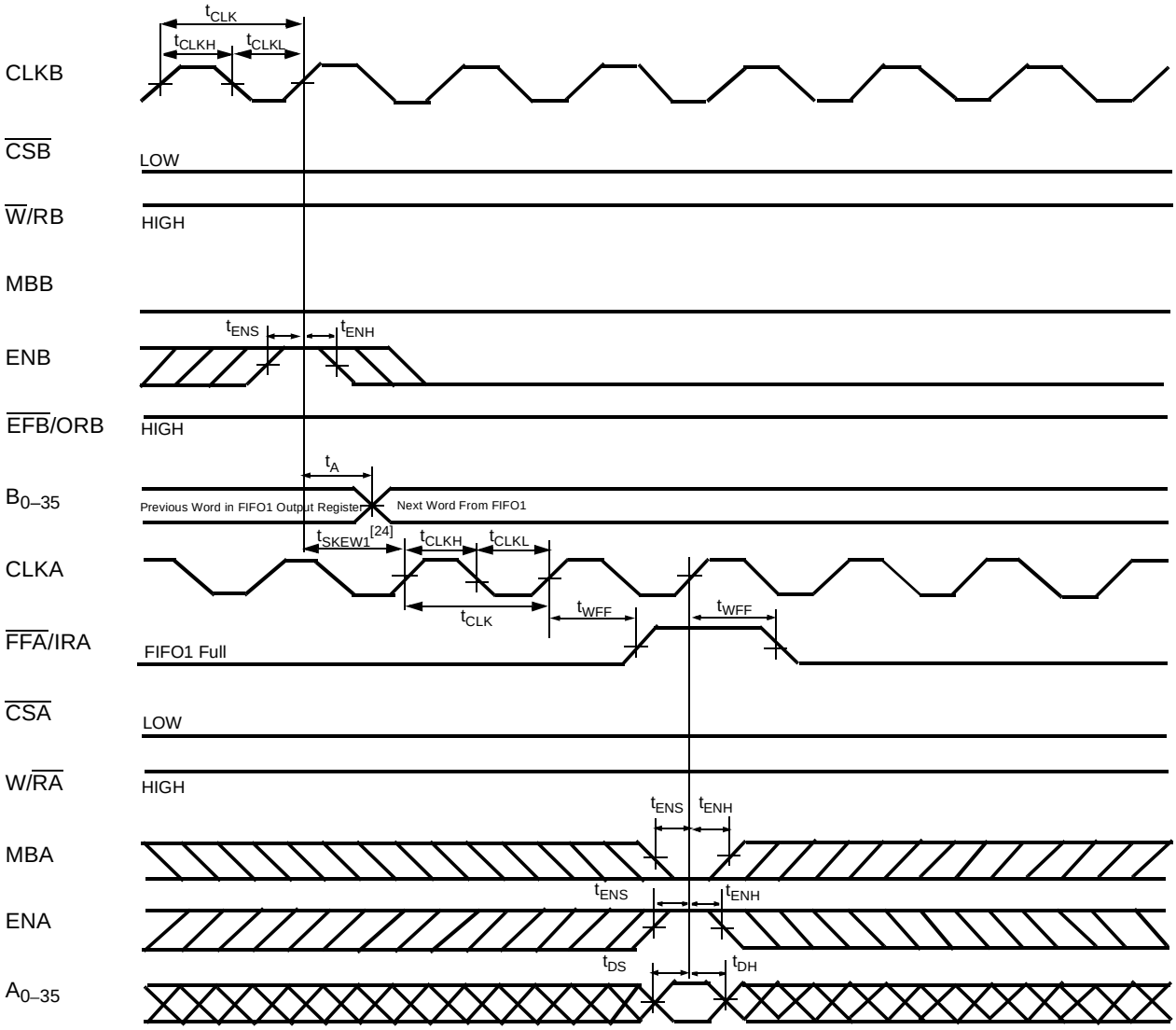


Note:

23. t_{SKEW1} is the minimum time between a rising CLKB edge and a rising CLKA edge for IRA to transition HIGH in the next CLKA cycle. If the time between the rising CLKB edge and rising CLKA edge is less than t_{SKEW1}, then IRA may transition HIGH one CLKA cycle later than shown.

Switching Waveforms (continued)

$\overline{FFA}$ Flag Timing and First Available Write when FIFO1 is Full (CY Standard Mode)

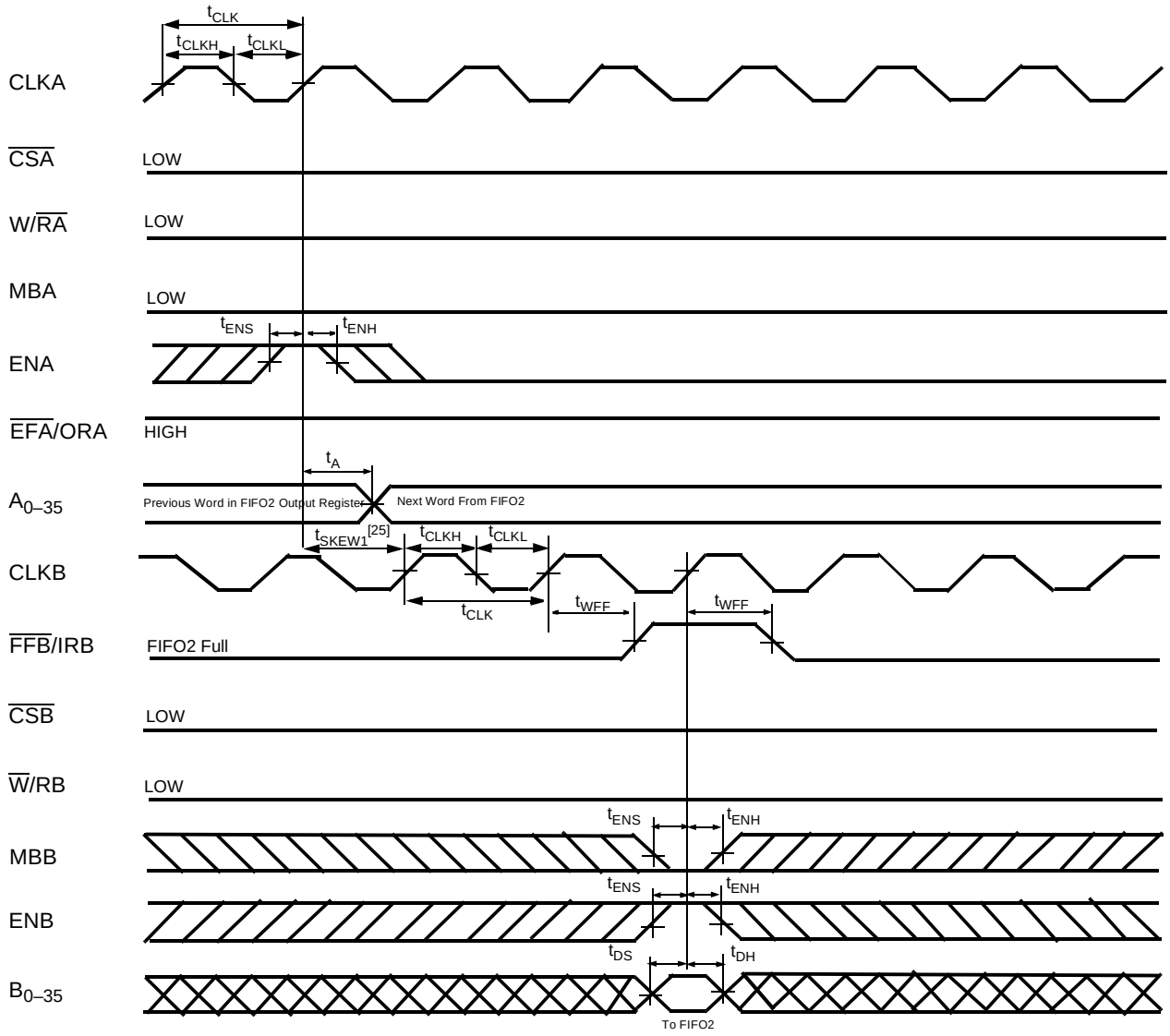


Note:

24. t_{SKEW1} is the minimum time between a rising CLKB edge and a rising CLKA edge for $\overline{FFA}$ to transition HIGH in the next CLKA cycle. If the time between the rising CLKB edge and rising CLKA edge is less than t_{SKEW1}, then the transition of $\overline{FFA}$ HIGH may occur one CLKA cycle later than shown.

Switching Waveforms (continued)

IRB Flag Timing and First Available Write when FIFO2 is Full (FWFT Mode)

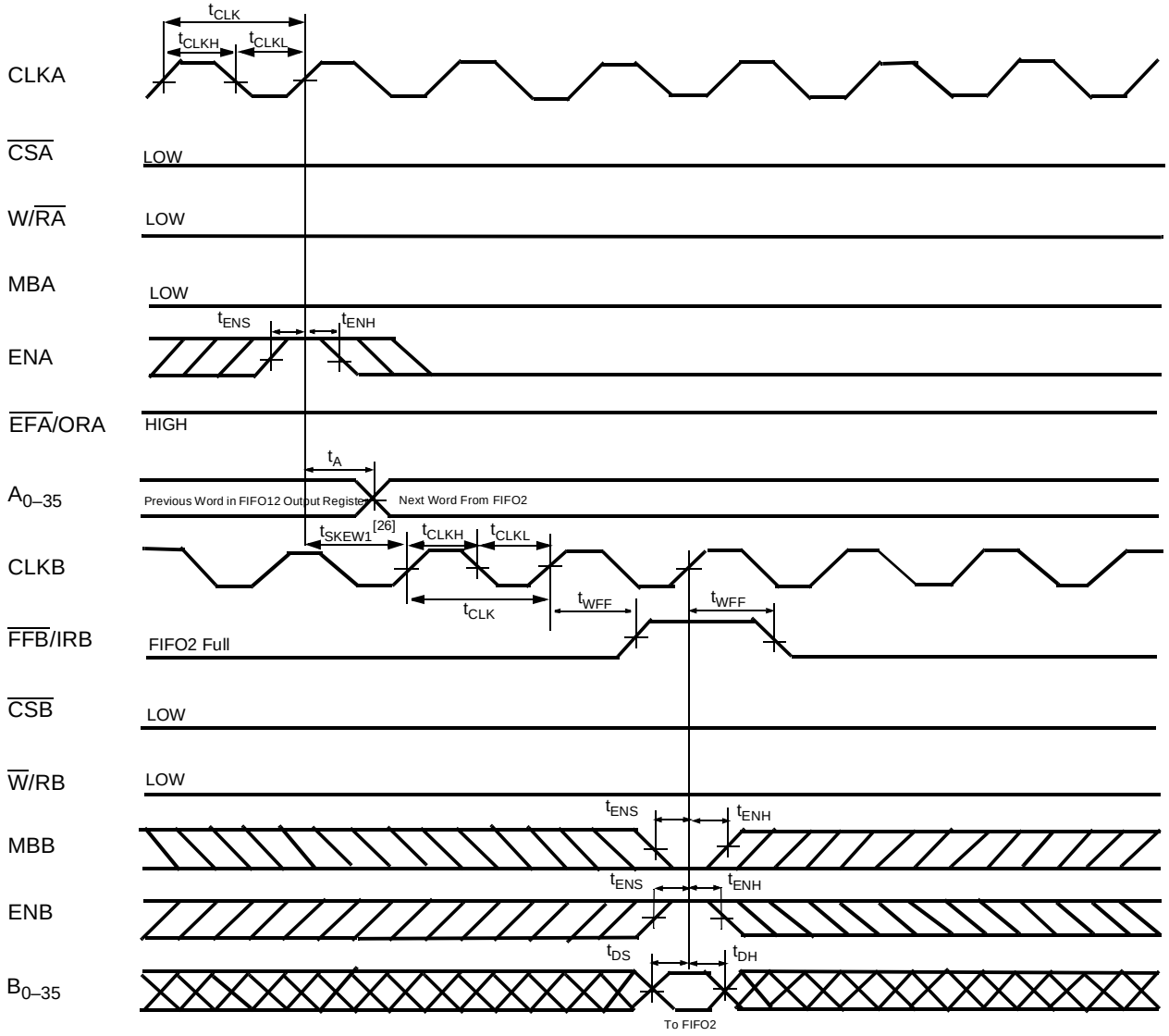


Note:

25. t_{SKEW1} is the minimum time between a rising CLKA edge and a rising CLKB edge for IRB to transition HIGH in the next CLKB cycle. If the time between the rising CLKA edge and rising CLKB edge is less than t_{SKEW1}, then the transition of IRB HIGH may occur one CLKB cycle later than shown.

Switching Waveforms (continued)

$\overline{FFB}$ Flag Timing and First Available Write when FIFO2 is Full (CY Standard Mode)

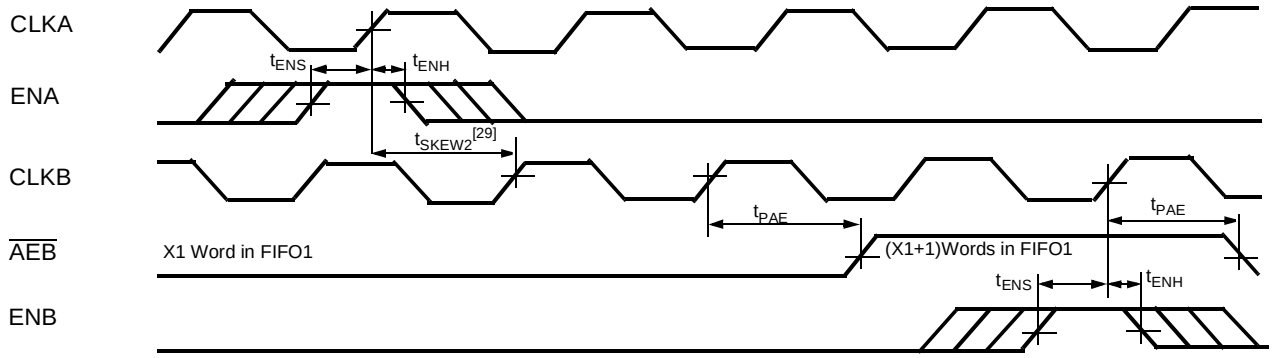


Note:

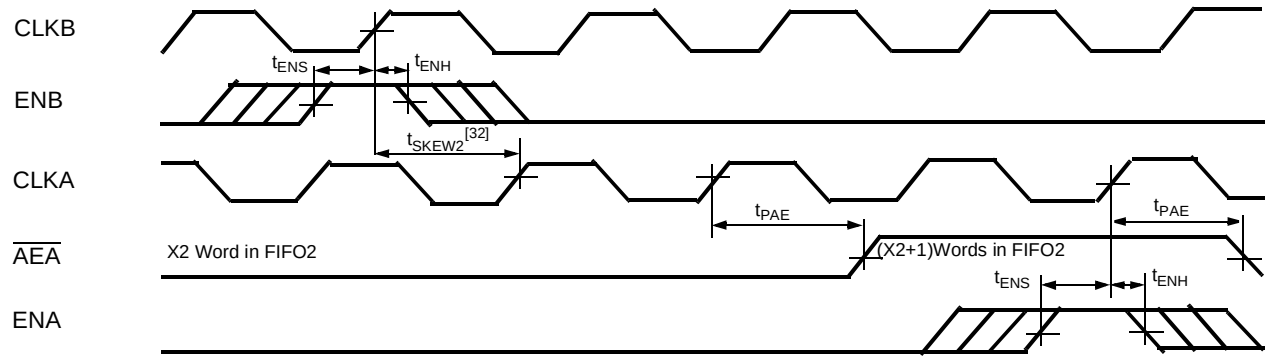
26. t_{SKEW1} is the minimum time between a rising CLKA edge and a rising CLKB edge for $\overline{FFB}$ to transition HIGH in the next CLKB cycle. If the time between the rising CLKA edge and rising CLKB edge is less than t_{SKEW1}, then the transition of $\overline{FFB}$ HIGH may occur one CLKB cycle later than shown.

Switching Waveforms (continued)

Timing for $\overline{AEB}$ when FIFO2 is Almost Empty (CY Standard and FWFT Modes) [27, 28]



Timing for $\overline{AEA}$ when FIFO2 is Almost Empty (CY Standard and FWFT Modes) [30, 31]

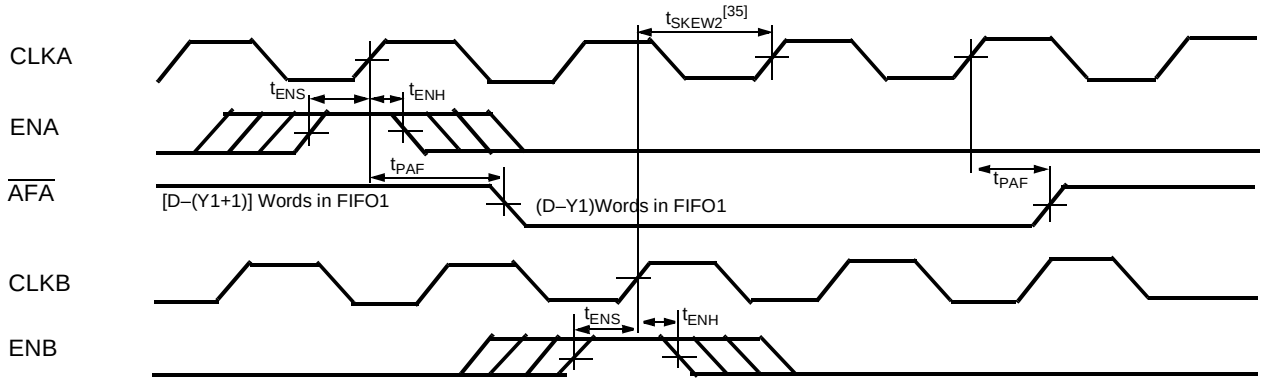


Notes:

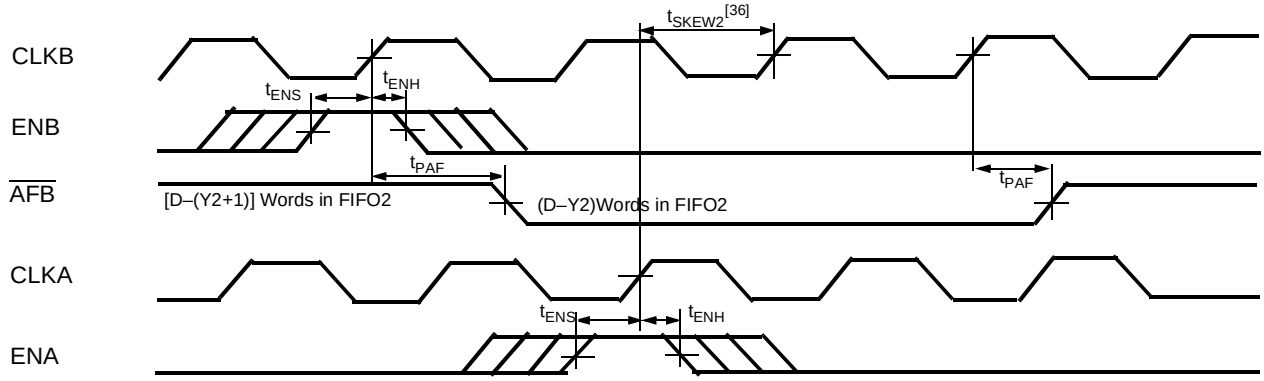
27. FIFO1 Write ($\overline{CSA}$ = LOW, W/$\overline{RA}$ = LOW, MBA = LOW), FIFO1 Read ($\overline{CSB}$ = LOW, $\overline{W}$/RB = HIGH, MBB = LOW). Data in the FIFO1 output register has been read from the FIFO.
28. If Port B size is word or byte, $\overline{AEB}$ is set LOW by the last word or byte read from FIFO1, respectively.
29. t_{SKEW2} is the minimum time between a rising CLKA edge and a rising CLKB edge for $\overline{AEB}$ to transition HIGH in the next CLKB cycle. If the time between the rising CLKA edge and rising CLKB edge is less than t_{SKEW2}, then $\overline{AEB}$ may transition HIGH one CLKB cycle later than shown.
30. FIFO2 Write ($\overline{CSB}$ = LOW, $\overline{W}$/RB = LOW, MBB = LOW), FIFO2 Read ($\overline{CSA}$ = LOW, W/$\overline{RA}$ = LOW, MBA = LOW). Data in the FIFO2 output register has been read from the FIFO.
31. If Port B size is word or byte, t_{SKEW2} is referenced to the rising CLKB edge that writes the last word or byte of the long word, respectively.
32. t_{SKEW2} is the minimum time between a rising CLKB edge and a rising CLKA edge for $\overline{AEA}$ to transition HIGH in the next CLKA cycle. If the time between the rising CLKB edge and rising CLKA edge is less than t_{SKEW2}, then $\overline{AEA}$ may transition HIGH one CLKA cycle later than shown.

Switching Waveforms (continued)

Timing for $\overline{AFA}$ when FIFO1 is Almost Full (CY Standard and FWFT Modes)[31, 33, 34]



Timing for $\overline{AFB}$ when FIFO2 is Almost Full (CY Standard and FWFT Modes)[30, 34]

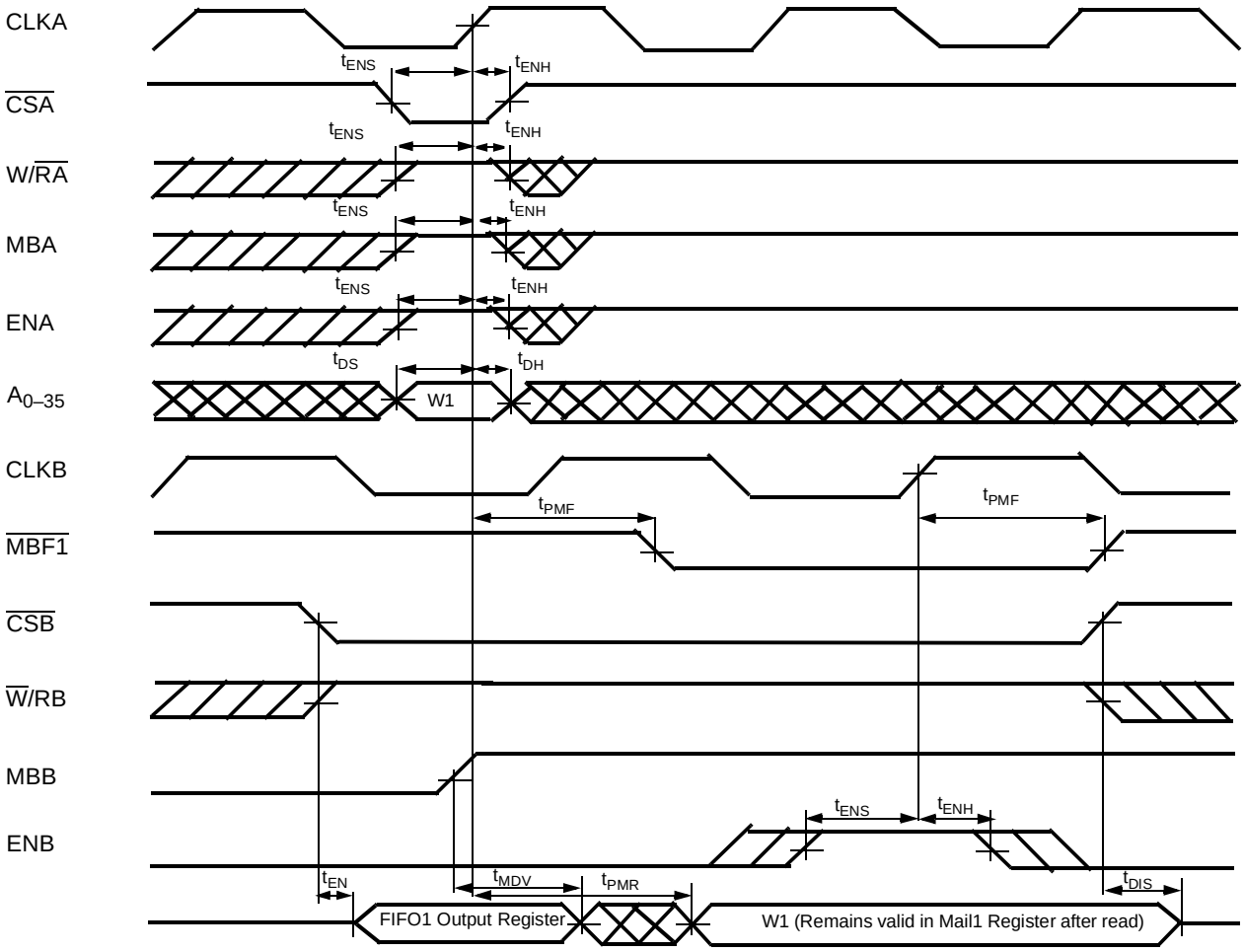


Notes:

33. FIFO1 Write ($\overline{CSA}$ = LOW, W/$\overline{RA}$ = HIGH, MBA = LOW), FIFO1 Read ($\overline{CSB}$ = LOW, $\overline{W}$/RB = HIGH, MBB = LOW). Data in the FIFO1 output register has been read from the FIFO.
34. D = Maximum FIFO Depth = 256 for the CY7C43622, 512 for the CY7C43632, 1K for the CY7C43642, 4K for the CY7C43662, and 16K for the CY7C43682.
35. t_{SKEW2} is the minimum time between a rising CLKA edge and a rising CLKB edge for $\overline{AFA}$ to transition HIGH in the next CLKA cycle. If the time between the rising CLKA edge and rising CLKB edge is less than t_{SKEW2}, then $\overline{AFA}$ may transition HIGH one CLKB cycle later than shown.
36. t_{SKEW2} is the minimum time between a rising CLKB edge and a rising CLKA edge for $\overline{AFB}$ to transition HIGH in the next CLKB cycle. If the time between the rising CLKB edge and rising CLKA edge is less than t_{SKEW2}, then $\overline{AFB}$ may transition HIGH one CLKA cycle later than shown.

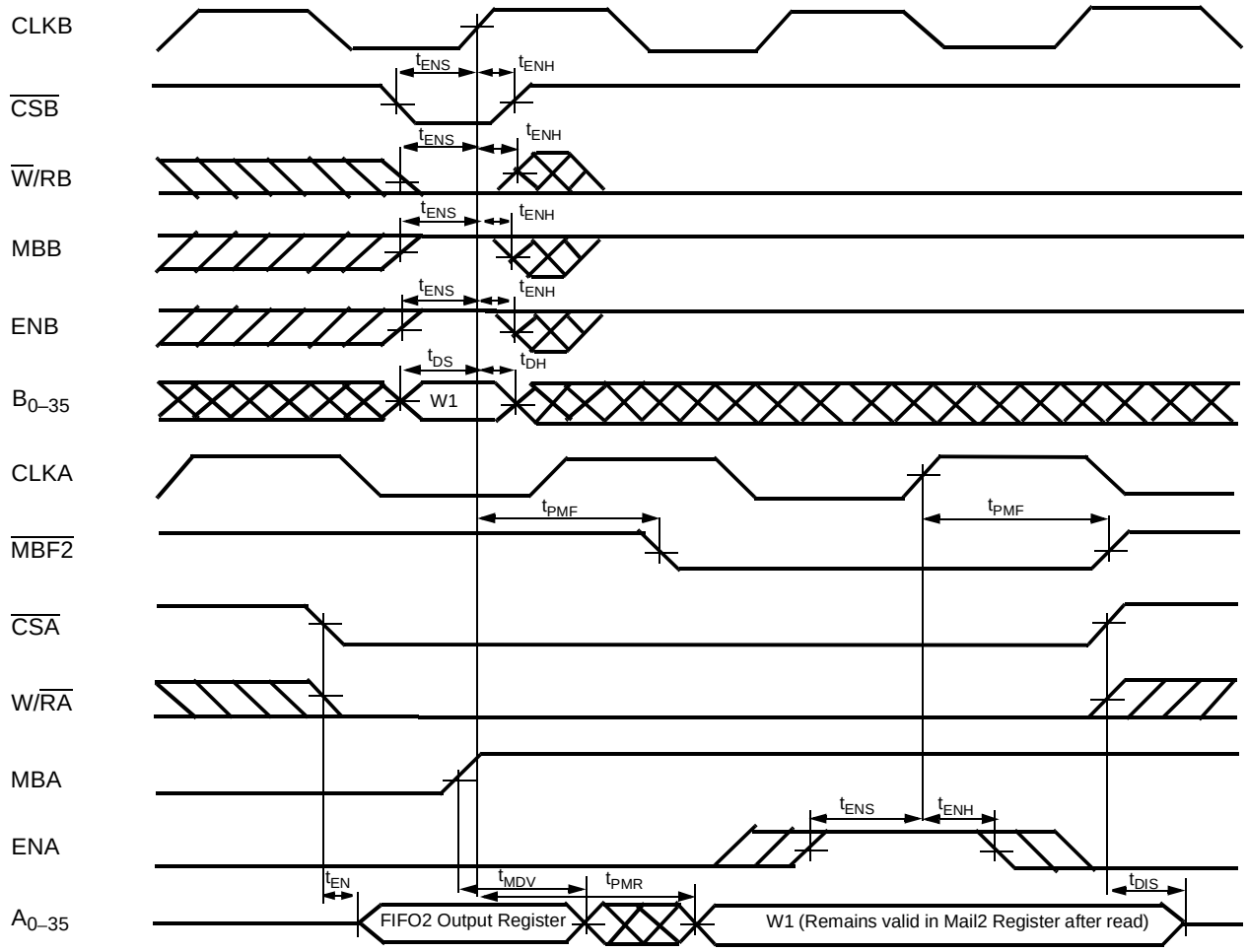
Switching Waveforms (continued)

Timing for Mail1 Register and $\overline{MBF1}$ Flag (CY Standard and FWFT Modes)

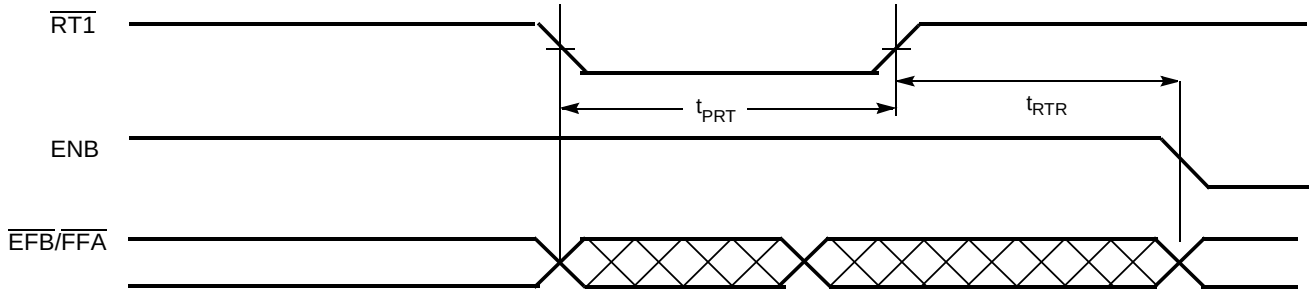


Switching Waveforms (continued)

Timing for Mail2 Register and $\overline{MBF2}$ Flag (CY Standard and FWFT Modes)



FIFO1 Retransmit Timing [37, 38, 39, 40]



Notes:
37. Retransmit is performed in the same manner for FIFO2.
38. Clocks are free-running in this case.
39. The flags may change state during Retransmit as a result of the offset of the read and write pointers, but flags will be valid at t_{RTR}.
40. For the synchronous PAE and PAF flags (SMODE), an appropriate clock cycle is necessary after t_{RTR} to update these flags.

Signal Description

Reset ($\overline{RST1}$, $\overline{RST2}$)

Each of the two FIFO memories of the CY7C436X2 undergoes a complete reset by taking its associated Master Reset ($\overline{RST1}$, $\overline{RST2}$) input LOW for at least four Port A clock (CLKA) and four Port B clock (CLKB) LOW-to-HIGH transitions. The Master Reset inputs can switch asynchronously to the clocks. A Master Reset initializes the internal read and write pointers and forces the Full/Input Ready flag ($\overline{FFA}$/IRA, $\overline{FFB}$/IRB) LOW, the Empty/Output Ready flag ($\overline{EFA}$/ORA, $\overline{EFB}$/ORB) LOW, the Almost Empty flag ($\overline{AEA}$, $\overline{AEB}$) LOW, and the Almost Full flag ($\overline{AFA}$, $\overline{AFB}$) HIGH. A Master Reset also forces the Mailbox flag (MBF1, MBF2) of the parallel mailbox register HIGH. After a Master Reset, the FIFO's Full/Input Ready flag is set HIGH after two clock cycles to begin normal operation. A Master Reset must be performed on the FIFO after power-up, before data is written to its memory.

A LOW-to-HIGH transition on a FIFO reset ($\overline{RST1}$, $\overline{RST2}$) input latches the values of the Flag select (FS0, FS1) for choosing the Almost Full and Almost Empty offset programming method (see Almost Empty and Almost Full flag offset programming below).

First-Word Fall-Through ($\overline{FWFT}$/STAN)

After Master Reset, the FWFT select function is active, permitting a choice between two possible timing modes: CY Standard Mode or First-Word Fall-Through (FWFT) Mode. Once the Master Reset ($\overline{RST1}$, $\overline{RST2}$) input is HIGH, a HIGH on the $\overline{FWFT}$/STAN input during the next LOW-to-HIGH transition of CLKA (for FIFO1) and CLKB (for FIFO2) will select CY Standard Mode. This mode uses the Empty Flag function ($\overline{EFA}$, $\overline{EFB}$) to indicate whether or not there are any words present in the FIFO memory. It uses the Full Flag function ($\overline{FFA}$, $\overline{FFB}$) to indicate whether or not the FIFO memory has any free space for writing. In CY Standard mode, every word read from the FIFO, including the first, must be requested using a formal read operation.

Once the Master Reset ($\overline{RST1}$, $\overline{RST2}$) input is HIGH, a LOW on the $\overline{FWFT}$/STAN input during the next LOW-to-HIGH transition of CLKA (for FIFO1) and CLKB (for FIFO2) will select FWFT Mode. This mode uses the Output Ready function (ORA, ORB) to indicate whether or not there is valid data at the data outputs ($A_{0–35}$ or $B_{0–35}$). It also uses the Input Ready function (IRA, IRB) to indicate whether or not the FIFO memory has any free space for writing. In the FWFT mode, the first word written to an empty FIFO goes directly to data outputs, no read request necessary. Subsequent words must be accessed by performing a formal read operation.

Following Master Reset, the level applied to the $\overline{FWFT}$/STD input to choose the desired timing mode must remain static throughout the FIFO operation.

Programming the Almost Empty and Almost Full Flags

Four registers in the CY7C436X2 are used to hold the offset values for the Almost Empty and Almost Full flags. The Port B Almost Empty flag ($\overline{AEB}$) offset register is labeled X1 and the Port A Almost Empty flag ($\overline{AEA}$) offset register is labeled X2. The Port A Almost Full flag ($\overline{AFA}$) offset register is labeled Y1 and the Port B Almost Full flag ($\overline{AFB}$) offset register is labeled Y2. The index of each register name corresponds with preset values during the reset of a FIFO, programmed in parallel using the FIFO's Port A data inputs (see *Table 1*).

To program the X1, X2, Y1, and Y2 registers from Port A, perform a Master Reset on both FIFOs simultaneously with FS0 and FS1 LOW during the LOW-to-HIGH transition of $\overline{RST1}$ and $\overline{RST2}$. After this reset is complete, the first four writes to FIFO1 do not store data in RAM but load the offset registers in the order Y1, X1, Y2, X2. The Port A data inputs used by the offset registers are ($A_{0–7}$), ($A_{0–8}$), ($A_{0–9}$), ($A_{0–11}$), or ($A_{0–13}$), for the CY7C436X2, respectively. The highest numbered input is used as the most significant bit of the binary number in each case. Valid programming values for the registers range from 1 to 252 for the CY7C43622; 1 to 508 for the CY7C43632; 1 to 1012 for the CY7C43642; 1 to 4092 for the CY7C43662; 1 to 16380 for the CY7C43682. After all the offset registers are programmed from Port A, the Port B Full/Input Ready ($\overline{FFB}$/IRB) is set HIGH and both FIFOs begin normal operation.

FS0 and FS1 function the same way in both CY Standard and FWFT modes.

FIFO Write/Read Operation

The state of the Port A data ($A_{0–35}$) lines is controlled by Port A Chip Select ($\overline{CSA}$) and Port A Write/Read Select (W/$\overline{RA}$). The $A_{0–35}$ lines are in the high-impedance state when either $\overline{CSA}$ or W/$\overline{RA}$ is HIGH. The $A_{0–35}$ lines are active outputs when both $\overline{CSA}$ and W/$\overline{RA}$ are LOW.

Data is loaded into FIFO1 from the $A_{0–35}$ inputs on a LOW-to-HIGH transition of CLKA when $\overline{CSA}$ is LOW, W/$\overline{RA}$ is HIGH, ENA is HIGH, MBA is LOW, and $\overline{FFA}$/IRA is HIGH. Data is read from FIFO2 to the $A_{0–35}$ outputs by a LOW-to-HIGH transition of CLKA when $\overline{CSA}$ is LOW, W/$\overline{RA}$ is LOW, ENA is HIGH, MBA is LOW, and $\overline{EFA}$/ORA is HIGH (see *Table 2*). FIFO reads and writes on Port A are independent of any concurrent Port B operation.

The Port B control signals are identical to those of Port A with the exception that the Port B Write/Read select ($\overline{W}$/RB) is the inverse of the Port A Write/Read Select (W/$\overline{RA}$). The state of the Port B data ($B_{0–35}$) lines is controlled by the Port B Chip Select ($\overline{CSB}$) and Port B Write/Read Select ($\overline{W}$/RB).The $B_{0–35}$ lines are in the high-impedance state when either $\overline{CSB}$ is HIGH or $\overline{W}$/RB is LOW. The $B_{0–35}$ lines are active outputs when $\overline{CSB}$ is LOW and $\overline{W}$/RB is HIGH.

Data is loaded into FIFO2 from the $B_{0–35}$ inputs on a LOW-to-HIGH transition of CLKB when $\overline{CSB}$ is LOW, $\overline{W}$/RB is LOW, ENB is HIGH, MBB is LOW, and $\overline{FFB}$/IRB is HIGH. Data is read from FIFO1 to the $B_{0–35}$ outputs by a LOW-to-HIGH transition of CLKB when $\overline{CSB}$ is LOW, $\overline{W}$/RB is HIGH, ENB is HIGH, MBB is LOW, and $\overline{EFB}$/ORB is HIGH (see *Table 3*). FIFO reads and writes on Port B are independent of any concurrent Port A operation.

The set-up and hold time constraints to the port clocks for the port Chip Selects and Write/Read Selects are only for enabling write and read operations and are not related to high-impedance control of the data outputs. If a port enable is LOW during a clock cycle, the port's Chip Select and Write/Read select may change states during the set-up and hold time window of the cycle.

When operating the FIFO in FWFT Mode and the Output Ready flag is LOW, the next word written is automatically sent to the FIFO's output register by the LOW-to-HIGH transition of the port clock that sets the Output Ready flag HIGH, data re-

siding in the FIFO's memory array is clocked to the output register only when a read is selected using the port's Chip Select, Write/Read Select, Enable, and Mailbox select.

When operating the FIFO in CY Standard Mode, regardless of whether the Empty Flag is LOW or HIGH, data residing in the FIFO's memory array is clocked to the output register only when a read is selected using the port's Chip Select, Write/Read Select, Enable, and Mailbox Select.

Synchronized FIFO Flags

Each FIFO is synchronized to its port clock through at least two flip-flop stages. This is done to improve flag-signal reliability by reducing the probability of the metastable events when CLKA and CLKB operate asynchronously to one another. $\overline{EFA}$/ORA, $\overline{AEA}$, $\overline{FFA}$/IRA, and $\overline{AFA}$ are synchronized to CLKA. $\overline{EFB}$/ORB, $\overline{AEB}$, $\overline{FFB}$/IRB, and $\overline{AFB}$ are synchronized to CLKB. *Table 4* and *Table 5* show the relationship of each port flag to FIFO1 and FIFO2.

Empty/Output Ready Flags ($\overline{EFA}$/ORA, $\overline{EFB}$/ORB)

These are dual-purpose flags. In the FWFT Mode, the Output Ready (ORA, ORB) function is selected. When the Output-Ready flag is HIGH, new data is present in the FIFO output register. When the Output Ready flag is LOW, the previous data word is present in the FIFO output register and attempted FIFO reads are ignored.

In the CY Standard Mode, the Empty Flag ($\overline{EFA}$, $\overline{EFB}$) function is selected. When the Empty Flag is HIGH, data is available in the FIFO's RAM memory for reading to the output register. When the Empty Flag is LOW, the previous data word is present in the FIFO output register and attempted FIFO reads are ignored.

The Empty/Output Ready flag of a FIFO is synchronized to the port clock that reads data from its array. For both the FWFT and CY Standard modes, the FIFO read pointer is incremented each time a new word is clocked to its output register. The state machine that controls an Output Ready flag monitors a write pointer and read pointer comparator that indicates when the FIFO SRAM status is empty, empty+1, or empty+2.

In FWFT Mode, from the time a word is written to a FIFO, it can be shifted to the FIFO output register in a minimum of three cycles of the Output Ready flag synchronizing clock. Therefore, an Output Ready flag is LOW if a word in memory is the next data to be sent to the FIFO output register and three cycles have not elapsed since the time the word was written. The Output Ready flag of the FIFO remains LOW until the third LOW-to-HIGH transition of the synchronizing clock occurs, simultaneously forcing the Output Ready flag HIGH and shifting the word to the FIFO output register.

In the CY Standard Mode, from the time a word is written to a FIFO, the Empty flag will indicate the presence of data available for reading in a minimum of two cycles of the Empty flag synchronizing clock. Therefore, an Empty Flag is LOW if a word in memory is the next data to be sent to the FIFO output register and two cycles have not elapsed since the time the word was written. The Empty flag of the FIFO remains LOW until the second LOW-to-HIGH transition of the synchronizing clock occurs, forcing the Empty flag HIGH; only then can data be read.

A LOW-to-HIGH transition on an Empty/Output Ready flag synchronizing clock begins the first synchronization cycle of a write if the clock transition occurs at time t_{SKEW1} or greater after the write. Otherwise, the subsequent clock cycle can be the first synchronization cycle.

Full/Input Ready Flags ($\overline{FFA}$/IRA, $\overline{FFB}$/IRB)

This is a dual-purpose flag. In FWFT Mode, the Input Ready (IRA and IRB) function is selected. In CY Standard Mode, the Full Flag ($\overline{FFA}$ and $\overline{FFB}$) function is selected. For both timing modes, when the Full/Input Ready flag is HIGH, a memory location is free in the SRAM to receive new data. No memory locations are free when the Full/Input Ready flag is LOW and attempted writes to the FIFO are ignored.

The Full/Input Ready flag of a FIFO is synchronized to the port clock that writes data to its array. For both FWFT and CY Standard modes, each time a word is written to a FIFO, its write pointer is incremented. The state machine that controls a Full/Input Ready flag monitors a write pointer and read pointer comparator that indicates when the FIFO SRAM status is full, full–1, or full–2. From the time a word is read from a FIFO, its previous memory location is ready to be written to in a minimum of two cycles of the Full/Input Ready flag synchronizing clock. Therefore, an Full/Input Ready flag is LOW if less than two cycles of the Full/Input Ready flag synchronizing clock have elapsed since the next memory write location has been read. The second LOW-to-HIGH transition on the Full/Input Ready flag synchronizing clock after the read sets the Full/Input Ready flag HIGH.

A LOW-to-HIGH transition on a Full/Input Ready flag synchronizing clock begins the first synchronization cycle of a read if the clock transition occurs at time t_{SKEW1} or greater after the read. Otherwise, the subsequent clock cycle can be the first synchronization cycle.

Almost Empty Flags ($\overline{AEA}$, $\overline{AEB}$)

The Almost Empty flag of a FIFO is synchronized to the port clock that reads data from its array. The state machine that controls an Almost Empty flag monitors a write pointer and read pointer comparator that indicates when the FIFO SRAM status is almost empty, almost empty+1, or almost empty+2. The Almost Empty state is defined by the contents of register X1 for $\overline{AEB}$ and register X2 for $\overline{AEA}$. These registers are loaded with preset values during a FIFO reset, programmed from Port A, or programmed serially (see Almost Empty flag and Almost Full flag offset programming above). An Almost Empty flag is LOW when its FIFO contains X or less words and is HIGH when its FIFO contains (X+1) or more words. A data word present in the FIFO output register has been read from memory.

Two LOW-to-HIGH transitions of the Almost Empty flag synchronizing clock are required after a FIFO write for its Almost Empty flag to reflect the new level of fill. Therefore, the Almost Full flag of a FIFO containing (X+1) or more words remains LOW if two cycles of its synchronizing clock have not elapsed since the write that filled the memory to the (X+1) level. An Almost Empty flag is set HIGH by the second LOW-to-HIGH transition of its synchronizing clock after the FIFO write that fills memory to the (X+1) level. A LOW-to-HIGH transition of an Almost Empty flag synchronizing clock begins the first synchronization cycle if it occurs at time t_{SKEW2} or greater after the write that fills the FIFO to (X+1) words. Otherwise, the subsequent synchronizing clock cycle may be the first synchronization cycle.

Almost Full Flags ($\overline{AFA}$, $\overline{AFB}$)

The Almost Full flag of a FIFO is synchronized to the port clock that writes data to its array. The state machine that controls an Almost Full flag monitors a write pointer and read pointer comparator that indicates when the FIFO SRAM status is almost full, almost full–1, or almost full–2. The Almost Full state is defined by the contents of register Y1 for $\overline{AFA}$ and register Y2 for $\overline{AFB}$. These registers are loaded with preset values during a FIFO reset, programmed from Port A, or programmed serially (see Almost Empty flag and Almost Full flag offset programming above). An Almost Full flag is LOW when the number of words in its FIFO is greater than or equal to (256–Y), (512–Y), (1024–Y), (4096–Y), or (16384–Y) for the CY7C436X2 respectively. An Almost Full flag is HIGH when the number of words in its FIFO is less than or equal to [256–(Y+1)], [512–(Y+1)], [1024–(Y+1)], [4096–(Y+1)], or [16384–(Y+1)], for the CY7C436X2 respectively. Note that a data word present in the FIFO output register has been read from memory.

Two LOW-to-HIGH transitions of the Almost Full flag synchronizing clock are required after a FIFO read for its Almost Full flag to reflect the new level of fill. Therefore, the Almost Full flag of a FIFO containing [256/512/1024/4096/16384–(Y+1)] or less words remains LOW if two cycles of its synchronizing clock have not elapsed since the read that reduced the number of words in memory to [256/512/1024/4096/16384–(Y+1)]. An Almost Full flag is set HIGH by the second LOW-to-HIGH transition of its synchronizing clock after the FIFO read that reduces the number of words in memory to [256/512/1024/4096/16384–(Y+1)]. A LOW-to-HIGH transition of an Almost Full flag synchronizing clock begins the first synchronization cycle if it occurs at time t_{SKEW2} or greater after the read that reduces the number of words in memory to [256/512/1024/4096/16384–(Y+1)]. Otherwise, the subsequent synchronizing clock cycle may be the first synchronization cycle.

Mailbox Registers

Each FIFO has a 36-bit bypass register to pass command and control information between Port A and Port B without putting it in queue. The Mailbox Select (MBA, MBB) inputs choose between a mail register and a FIFO for a port data transfer operation. The usable width of both the Mail1 and Mail2 registers matches the selected bus size for Port B.

A LOW-to-HIGH transition on CLKA writes $A_{0–35}$ data to the Mail1 Register when a Port A write is selected by $\overline{CSA}$, W/$\overline{RA}$, and ENA with MBA HIGH. If the selected Port A bus size is also 36 bits, then the usable width of the Mail1 Register employs data lines $A_{0–35}$. If the selected Port A bus size is 18 bits, then the usable width of the Mail1 Register employs data lines $A_{0–17}$. (In this case, $A_{18–35}$ are don't care inputs.) If the selected Port A bus size is 9 bits, then the usable width of the Mail1 Register employs data lines $A_{0–8}$. (In this case, $A_{9–35}$ are don't care inputs.)

A LOW-to-HIGH transition on CLKB writes $B_{0–35}$ data to the Mail2 Register when a Port B write is selected by $\overline{CSB}$, $\overline{W}$/RB, and ENB with MBB HIGH. If the selected Port B bus size is also 36 bits, then the usable width of the Mail2 Register employs data lines $B_{0–35}$. If the selected Port B bus size is 18 bits, then the usable width of the Mail2 Register employs data lines $B_{0–17}$. (In this case, $B_{18–35}$ are don't care inputs.) If the selected Port B bus size is 9 bits, then the usable width of the Mail2 Register employs data lines $B_{0–8}$. (In this case, $B_{9–35}$ are don't care inputs.)

Writing data to a mail register sets its corresponding flag ($\overline{MBF1}$ or $\overline{MBF2}$) LOW. Attempted writes to a mail register are ignored while the mail flag is LOW.

When data outputs of a port are active, the data on the bus comes from the FIFO output register when the port Mailbox Select input is LOW and from the mail register when the port Mailbox Select input is HIGH.

The Mail1 Register flag ($\overline{MBF1}$) is set HIGH by a LOW-to-HIGH transition on CLKB when a Port B read is selected by $\overline{CSB}$, $\overline{W}$/RB, and ENB with MBB HIGH. For a 36-bit bus size, 36 bits of mailbox data are placed on $B_{0–35}$. For an 18-bit bus size, 18 bits of mailbox data are placed on $B_{0–17}$. (In this case, $B_{18–35}$ are indeterminate.) For a 9-bit bus size, 9 bits of mailbox data are placed on $B_{0–8}$. (In this case, $B_{9–35}$ are indeterminate.)

The Mail2 Register flag ($\overline{MBF2}$) is set HIGH by a LOW-to-HIGH transition on CLKA when a Port A read is selected by $\overline{CSA}$, W/$\overline{RA}$, and ENA with MBA HIGH.

For a 36-bit bus size, 36 bits of mailbox data are placed on $A_{0–35}$. For an 18-bit bus size, 18 bits of mailbox data are placed on $A_{0–17}$. (In this case, $A_{18–35}$ are indeterminate.) For a 9-bit bus size, 9 bits of mailbox data are placed on $A_{0–8}$. (In this case, $A_{9–35}$ are indeterminate.)

The data in a mail register remains intact after it is read and changes only when new data is written to the register. The Endian Select feature has no effect on the mailbox data.

Retransmit ($\overline{RT1}$, $\overline{RT2}$)

The retransmit feature is beneficial when transferring packets of data. It enables the receipt of data to be acknowledged by the receiver and retransmitted if necessary.

The retransmit feature is intended for use when a number of writes equal to or less than the depth of the FIFO have occurred and at least one word has been read since the last reset cycle. A LOW pulse on $\overline{RT1}$, $\overline{RT2}$ resets the internal read pointer to the first physical location of the FIFO. CLKA and CLKB may be free running but must be disabled during and t_{RTR} after the retransmit pulse. With every valid read cycle after retransmit, previously accessed data is read and the read pointer is incremented until it is equal to the write pointer. Flags are governed by the relative locations of the read and write pointers and are updated during a retransmit cycle. Data written to the FIFO after activation of $\overline{RT1}$, $\overline{RT2}$ are transmitted also.

Table 1. Flag Programming

FS1	FS0	$\overline{RST1}$	$\overline{RST2}$	X1 and Y1 Registers[41]	X2 and Y2 Registers[42]
H	H	↑	X	64	X
H	H	X	↑	X	64
H	L	↑	X	16	X
H	L	X	↑	X	16
L	H	↑	X	8	X
L	H	X	↑	X	8
L	L	↑	↑	Programming via Port A	Programming via Port A

Table 2. Port A Enable Function

$\overline{CSA}$	W/$\overline{RA}$	ENA	MBA	CLKA	A_{0-35} Outputs	Port Function
H	X	X	X	X	In high-impedance state	None
L	H	L	X	X	In high-impedance state	None
L	H	H	L	↑	In high-impedance state	FIFO1 write
L	H	H	H	↑	In high-impedance state	Mail1 write
L	L	L	L	X	Active, FIFO2 output register	None
L	L	H	L	↑	Active, FIFO2 output register	FIFO2 read
L	L	L	H	X	Active, Mail2 register	None
L	L	H	H	↑	Active, Mail2 register	Mail2 read (set $\overline{MBF2}$ HIGH)

Table 3. Port B Enable Function

$\overline{CSB}$	$\overline{W}$/RB	ENB	MBB	CLKB	B_{0-35} Outputs	Port Function
H	X	X	X	X	In high-impedance state	None
L	L	L	X	X	In high-impedance state	None
L	L	H	L	↑	In high-impedance state	FIFO2 write
L	L	H	H	↑	In high-impedance state	Mail2 write
L	H	L	L	X	Active, FIFO1 output register	None
L	H	H	L	↑	Active, FIFO1 output register	FIFO1 read
L	H	L	H	X	Active, Mail1 register	None
L	H	H	H	↑	Active, Mail1 register	Mail1 read (set $\overline{MBF1}$ HIGH)

Notes:
41. X1 register holds the offset for $\overline{AEB}$; Y1 register holds the offset for $\overline{AFA}$.
42. X2 register holds the offset for $\overline{AEA}$; Y2 register holds the offset for $\overline{AFB}$.

Table 4. FIFO1 Flag Operation (CY Standard and FWFT modes)

Number of Words in FIFO Memory[43, 44, 45, 46]					Synchronized to CLKB		Synchronized to CLKA	
CY7C43622	CY7C43632	CY7C43642	CY7C43662	CY7C43682	$\overline{EFB}$/ORB	$\overline{AEB}$	$\overline{AFA}$	$\overline{FFA}$/IRA
0	0	0	0	0	L	L	H	H
1 TO X1	1 TO X1	1 TO X1	1 TO X1	1 TO X1	H	L	H	H
(X1+1) to [256–(Y1+1)]	(X1+1) to [512–(Y1+1)]	(X1+1) to [1024–(Y1+1)]	(X1+1) to [4096–(Y1+1)]	(X1+1) to [16384–(Y1+1)]	H	H	H	H
(256–Y1) to 255	(512–Y1) to 511	(1024–Y1) to 1023	(4096–Y1) to 4095	(16384–Y1) to 16383	H	H	L	H
256	512	1024	4096	16384	H	H	L	L

Table 5. FIFO2 Flag Operation (CY Standard and FWFT modes)

Number of Words in FIFO Memory[44, 45, 46, 47]					Synchronized to CLKA		Synchronized to CLKB	
CY7C43622	CY7C43632	CY7C43642	CY7C43662	CY7C43682	$\overline{EFA}$/ORA	$\overline{AEA}$	$\overline{AFB}$	$\overline{FFB}$/IRB
0	0	0	0	0	L	L	H	H
1 TO X2	1 TO X2	1 TO X2	1 TO X2	1 TO X2	H	L	H	H
(X2+1) to [256–(Y2+1)]	(X2+1) to [512–(Y2+1)]	(X2+1) to [1024–(Y2+1)]	(X2+1) to [4096–(Y2+1)]	(X2+1) to [16384–(Y2+)1]	H	H	H	H
(256–Y2) to 255	(512–Y2) to 511	(1024–Y2) to 1023	(4096–Y2) to 4095	(16384–Y2) to 16383	H	H	L	H
256	512	1024	4096	16384	H	H	L	L

Notes:

43. X1 is the Almost Empty offset for FIFO1 used by $\overline{AEB}$. Y1 is the Almost Full offset for FIFO1 used by $\overline{AFA}$. Both X1 and Y1 are selected during a FIFO1 reset or port A programming.
44. When a word loaded to an empty FIFO is shifted to the output register, its previous FIFO memory location is free.
45. Data in the output register does not count as a “word in FIFO memory.” Since in FWFT mode, the first word written to an empty FIFO goes unrequested to the output register (no read operation necessary), it is not included in the FIFO memory count.
46. The ORA and IRB functions are active during FWFT mode; the $\overline{EFA}$ and $\overline{FFB}$ functions are active in CY Standard Mode.
47. X2 is the Almost Empty offset for FIFO2 used by $\overline{AEA}$. Y2 is the Almost Full offset for FIFO2 used by $\overline{AFB}$. Both X2 and Y2 are selected during a FIFO2 reset or port A programming.

Ordering Information

256 x36 x2 Bidirectional Synchronous FIFO

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
7	CY7C43622–7AC	A120	120-Lead Thin Quad Flat Package	Commercial
10	CY7C43622–10AC	A120	120-Lead Thin Quad Flat Package	Commercial
15	CY7C43622–15AC	A120	120-Lead Thin Quad Flat Package	Commercial

512 x36 x2 Bidirectional Synchronous FIFO

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
7	CY7C43632–7AC	A120	120-Lead Thin Quad Flat Package	Commercial
10	CY7C43632–10AC	A120	120-Lead Thin Quad Flat Package	Commercial
15	CY7C43632–15AC	A120	120-Lead Thin Quad Flat Package	Commercial

1K x36 x2 Bidirectional Synchronous FIFO

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
7	CY7C43642–7AC	A120	120-Lead Thin Quad Flat Package	Commercial
10	CY7C43642–10AC	A120	120-Lead Thin Quad Flat Package	Commercial
15	CY7C43642–15AC	A120	120-Lead Thin Quad Flat Package	Commercial

4K x36 x2 Bidirectional Synchronous FIFO

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
7	CY7C43662–7AC	A120	120-Lead Thin Quad Flat Package	Commercial
10	CY7C43662–10AC	A120	120-Lead Thin Quad Flat Package	Commercial
15	CY7C43662–15AC	A120	120-Lead Thin Quad Flat Package	Commercial

16K x36 x2 Bidirectional Synchronous FIFO

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
7	CY7C43682–7AC	A120	120-Lead Thin Quad Flat Package	Commercial
10	CY7C43682–10AC	A120	120-Lead Thin Quad Flat Package	Commercial
15	CY7C43682–15AC	A120	120-Lead Thin Quad Flat Package	Commercial
15	CY7C43682–15AI	A120	120-Lead Thin Quad Flat Package	Industrial

Shaded area contains advance information.

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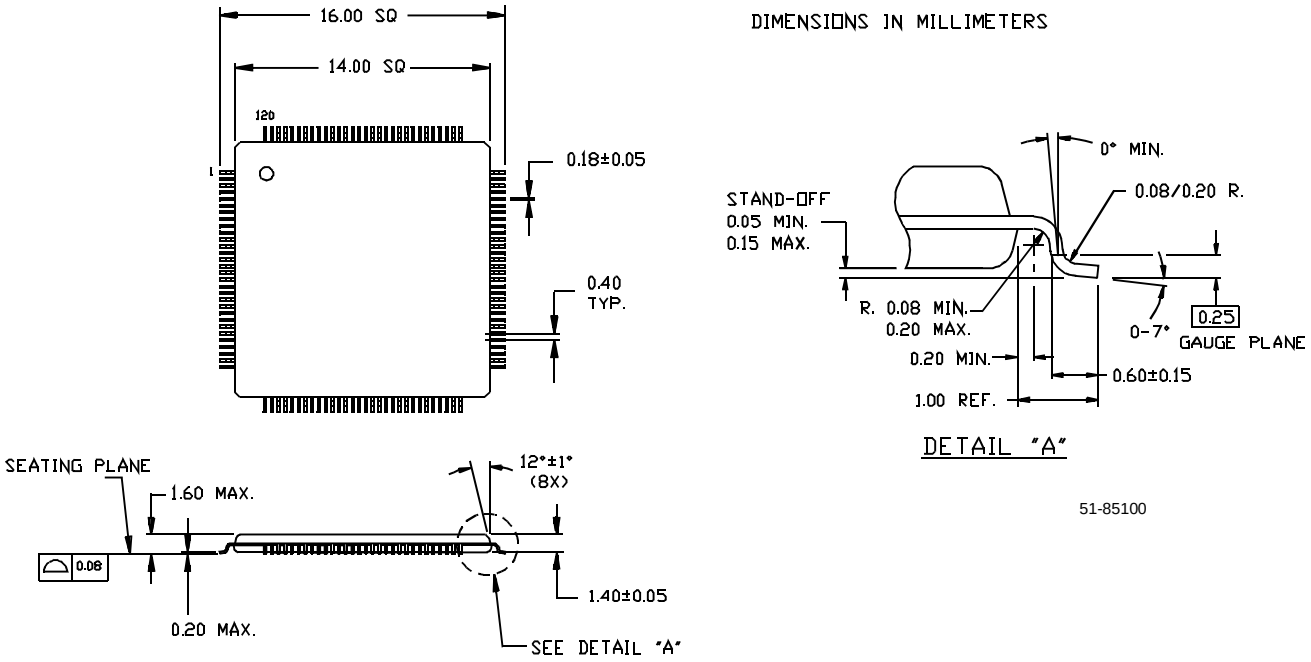
Package Diagram

120-Pin Thin Quad Flatpack (14 x 14 x 1.4 mm) A120



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