CRYSTAL
Semiconductor Corporation

CS5516
CS5520

16-Bit/20-Bit Bridge Transducer A/D Converters

Features

- On-chip Instrumentation Amplifier
- On-chip Programmable Gain Amplifier
- On-Chip 4-Bit D/A For Offset Removal
- Dynamic Excitation Options
- Linearity Error: ±0.0015% FS Max
  Offset and Full-Scale Errors: ±8 LSB_{20}
  20-Bit No Missing Codes
- CMRR at 50 / 60Hz >200dB
- System Calibration Capability with calibration read/write option
- 3, 4 or 5 wire Serial Communications Port
- Low Power Consumption: under 30mW
  10µW Standby Mode for Portable applications

General Description

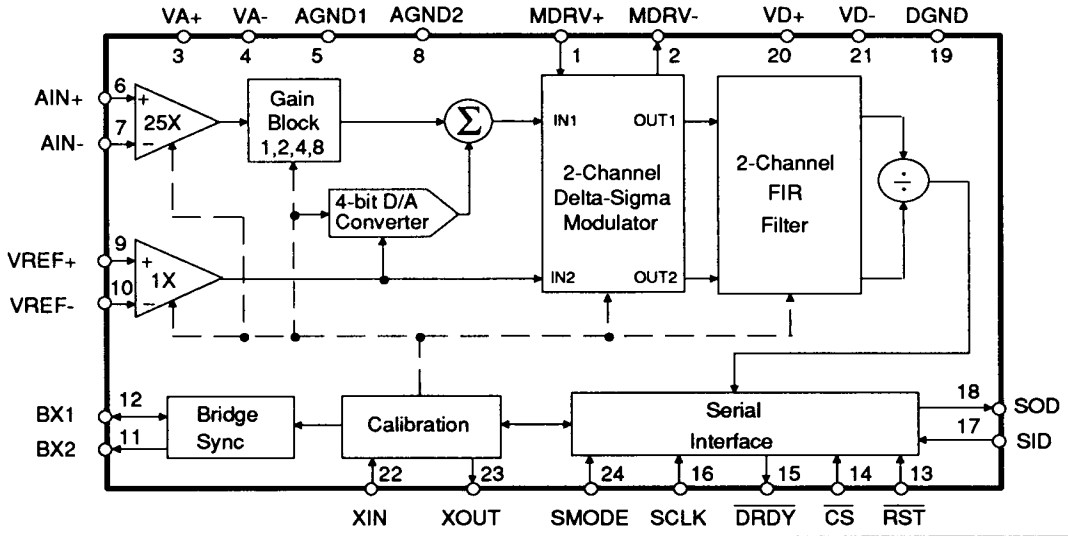
The CS5516 and CS5520 are complete solutions for digitizing low level signals from strain gauges, load cells, and pressure transducers. Any family of mV output transducers, including those requiring bridge excitation, can be interfaced directly to the CS5516 or CS5520. The devices offer an on-chip software programmable instrumentation amplifier block, choice of DC or AC bridge excitation, and software selectable reference and signal demodulation.

The CS5516 uses delta-sigma modulation to achieve 16-bit resolution at output word rates up to 60Hz. The CS5520 achieves 20-bit resolution at word rates up to 60Hz.

The CS5516 and CS5520 sample at a rate set by the user in the form of either an external CMOS clock or a crystal. On-chip digital filtering provides rejection of all frequencies above 12Hz for a 4.096 MHz clock.

The CS5516 and CS5520 include system calibration to null offset and gain errors in the input channel. The digital values associated with the system calibration can be written to, or read from, the calibration RAM locations at any time via the serial communications port. The 4-bit DC offset D/A converter, in conjunction with digital correction, is initially used to zero the input offset value.

ORDERING INFORMATION: Page 31



Preliminary Product Information | This document contains information for a new product. Crystal Semiconductor reserves the right to modify this product without notice.

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ANALOG CHARACTERISTICS (T_A = T_{MIN} to T_{MAX}; VA+, VD+ = 5V; VA-, VD- = -5V; VREF= 2.5V(external differential voltage across VREF+ and VREF-); f_{CLK} = 4.9152 MHz; AC Excitation 300 Hz; Gain = 25; Bipolar Mode; R_{source} = 300Ω with a 4.7nF to AGND at AIN (see Note 1); unless otherwise specified.)

Parameter *		CS5516-A Min	CS5516-A Typ	CS5516-A Max	CS5516-S Min	CS5516-S Typ	CS5516-S Max	Units
Specified Temperature Range			-40 to +85			-55 to +125		°C
Accuracy								
Linearity Error			0.0015	0.003		0.0015	0.003	±%FS
Differential Nonlinearity			±0.25	±0.5		±0.25	±0.5	LSB_{16}
Unipolar Gain Error	(Note 2)		±1	TBD		±1	TBD	LSB_{16}
Bipolar Gain Error	(Note 2)		±1			±1		LSB_{16}
Unipolar/Bipolar Gain Drift			±1			±1		ppm/°C
Unipolar Offset	(Note 2)		±1	TBD		±1	TBD	LSB_{16}
Bipolar Offset	(Note 2)		±1	TBD		±1	TBD	LSB_{16}
Offset Drift			±0.005			±0.005		µV/°C
Noise (Referred to Input)	Gain = 25 (25 x 1)		250			250		nVrms
	Gain = 50 (25 x 2)		200			200		nVrms
	Gain = 100 (25 x 4)		150			150		nVrms
	Gain = 200 (25 x 8)		150			150		nVrms

Notes: 1. The AIN pin presents a very high input resistance at dc and a minor dynamic load which scales to the master clock frequency. Both source resistance and shunt capacitance are therefore critical in determining the source impedance requirements of the CS5516 and CS5520.
2. Applies after system calibration at the temperature of interest.

	Unipolar Mode			Bipolar Mode		
uV	LSB's	% FS	ppm FS	LSB's	% FS	ppm FS
0.4	0.26	0.0004	4	0.13	0.0002	2
0.76	0.50	0.0008	8	0.26	0.0004	4
1.52	1.00	0.0015	15	0.50	0.0008	8
3.04	2.00	0.0030	30	1.00	0.0015	15
6.08	4.00	0.0061	61	2.00	0.0030	30

VREF = 2.5 V **PGA gain = 1**

CS5516; 16-Bit Unit Conversion Factors

* Refer to the Specification Definitions immediately following the Pin Description Section.

Specifications are subject to change without notice.

ANALOG CHARACTERISTICS (Continued)

Parameter*		CS5520-B Min	CS5520-B Typ	CS5520-B Max	CS5520-S Min	CS5520-S Typ	CS5520-S Max	Units
Specified Temperature Range			-40 to +85			-55 to +125		°C
Accuracy								
Linearity Error			0.0007	0.0015		0.0015	0.003	±%FS
Differential Nonlinearity (No Missing Codes)		20			20			Bits
Unipolar Gain Error	(Note 2)		±16	TBD		±16	TBD	LSB_{20}
Bipolar Gain Error	(Note 2)		±8			±8		LSB_{20}
Unipolar/Bipolar Gain Drift			±1			±1		ppm/°C
Unipolar Offset	(Note 2)		±16	±TBD		±16	TBD	LSB_{20}
Bipolar Offset	(Note 2)		±16	TBD		±16	TBD	LSB_{20}
Offset Drift			±0.005			±0.005		µV/°C
Noise (Referred to Input)	Gain = 25 (25 x 1)		250			250		nVrms
	Gain = 50 (25 x 2)		200			200		nVrms
	Gain = 100 (25 x 4)		150			150		nVrms
	Gain = 200 (25 x 8)		150			150		nVrms

	Unipolar Mode			Bipolar Mode		
uV	LSB's	% FS	ppm FS	LSB's	% FS	ppm FS
0.025	0.26	0.0000238	0.25	0.13	0.0000119	0.125
0.047	0.50	0.0000477	0.50	0.26	0.0000238	0.25
0.095	1.00	0.0000954	1.0	0.50	0.0000477	0.5
0.190	2.00	0.0001907	2.0	1.00	0.0000954	1.0
0.380	4.00	0.0003814	4.0	2.00	0.0001907	2.0

VREF = 2.5 V PGA gain = 1

CS5520; 20-Bit Unit Conversion Factors

* Refer to the Specification Definitions immediately following the Pin Description Section.

Specifications are subject to change without notice.

ANALOG CHARACTERISTICS (Continued)

Parameter		CS5516-A CS5520-B Min	Typ	Max	CS5516-S CS5520-S Min	Typ	Max	Units
Specified Temperature Range			-40 to +85			-55 to +125		°C
Analog Input								
Analog Input Range:	Unipolar Bipolar		12.5, 25, 50, 100 ±12.5, ±25, ±50, ±100			12.5, 25, 50, 100 12.5, ±25, ±50, ±100		mV mV
Common Mode Rejection:	dc 50,60 Hz		165 200			165 200		dB dB
Input Capacitance			5			5		pF
Input Bias Current	(Note 1)		100			100		pA
Instrumentation Amplifier								
Gain			25			25		
Bandwidth			200			200		kHz
Unity Gain Bandwidth			5			5		MHz
Output Slew Rate			1.5			1.5		V/µsec
Noise @ 10 Hz BW			100			100		nVrms
PSRR @ 50/60 Hz	(Note 3)		120			120		dB
Common Mode Range	(Note 4)		±3			±3		V
Chopping Frequency			XIN/128			XIN/128		Hz
Programmable Gain Amplifier								
Gain Tracking	(Note 5)		±1			±1		%
4-Bit Offset Trim DAC								
Accuracy			±5			±5		%
Voltage Reference Input								
Range	(Note 6)	2.0	2.5	3.8	2.0	2.5	3.8	V
Common Mode Rejection:	dc 50,60 Hz		165 200			165 200		dB dB
Input Capacitance			15			15		pF
Input Bias Current	(Note 1)		100			100		pA

Notes: 3. This includes the on-chip digital filtering.

4. The maximum magnitude of the differential input voltage, Vdiff(in) is determined by the following:
   Vdiff(in) < 300 mV - |Vcm/12.5 |
   Vcm is the common mode voltage which is applied to the instrumentation amplifier inputs.
   The above equations should be used to calculate the allowable common mode voltage for a given differential voltage applied to the first gain stage inputs.
   These limits ensure that the instrumentation amplifier does not saturate.
5. Gain tracking accuracy can be significantly improved by uploading a calibrated gain word to the gain register for each PGA gain selection.
6. The common mode voltage on the Voltage Reference Input, plus the reference range, [(VREF+) - (VREF-)]/2, must not exceed ±3 volts.

ANALOG CHARACTERISTICS (Continued)

Parameter		Min	Typ	Max	Min	Typ	Max	Units
Modulator Differential Voltage Reference								
Nominal Output Voltage			(MDRV+) - 3.75			(MDRV+) - 3.75		V
Initial Output Voltage Tolerance			100			100		mV
Temperature Coefficient			100			TBD		ppm/°C
Line Regulation	(4.75V < VA < 5.25V)		1			1		mV/Volt
Output Voltage Noise	0.1 to 15 Hz		10			10		μV_{p-p}
Output Current Drive:	Source Current			20			20	µA
	Sink Current			20			20	µA
Power Supplies								
DC Power Supply Currents:	I_{A+}		2.5	TBD		2.5	TBD	mA
	I_{A-}		2.5	TBD		2.5	TBD	mA
	I_{D+}		0.5	TBD		0.5	TBD	mA
	I_{D-}		0.1	TBD		0.1	TBD	mA
Power Dissipation:	Normal Operation		28	TBD		28	TBD	mW
(Note 7)	Standby Mode		10	TBD		10	TBD	µW
Power Supply Rejection:	Positive Supplies		90			90		dB
	Negative Supplies		90			90		dB
System Calibration Specifications								
Positive Full Scale Calibration Range (Note 8)	Unipolar Mode				0.8T		1.2T	V
	Bipolar Mode				0.8T		1.2T	V
Maximum Offset Calibration Range (Note 8)	Unipolar Mode				-2T		+2T	V
	Bipolar Mode				-2T		+2T	V
Differential Input Voltage Range (Notes 8, 9, 10)	Unipolar Mode					Voffset + (1.2T)		V
	Bipolar					Voffset ± (1.2T)		V

Notes:
7. All outputs unloaded. All inputs CMOS levels.
8. T=VREF/(Gx25), where T is the full scale span, where VREF is the differential voltage across VREF+ and VREF- in volts, and G is the gain setting of the second gain block. G can be set to 1, 2, 4, 8. This sets the overall gain to 25, 50, 100, 200. The gain can then be fine tuned by using the calibration of the full scale point.
9. When calibrated.
10. V_{offset} is the offset corrected by the offset calibration routine. V_{offset} may be as large as 2T.

DYNAMIC CHARACTERISTICS

Parameter	Symbol	Ratio	Units
Modulator Sampling Frequency	f_S	$f_{clk}/256$	Hz
Output Update Rate	f_{out}	$f_{clk}/81,920$	Hz
Filter Corner Frequency	f_{-3dB}	$f_{clk}/341,334$	Hz
Settling Time to ±0.0007% (FS Step)	t_s	$6/f_{out}$	s

DIGITAL CHARACTERISTICS ($T_A = T_{min}$ to T_{max}; VA+, VD+ = 5V ± 5%; VA-, VD- = -5V ± 5%; DGND = 0). All measurements below are performed under static conditions.

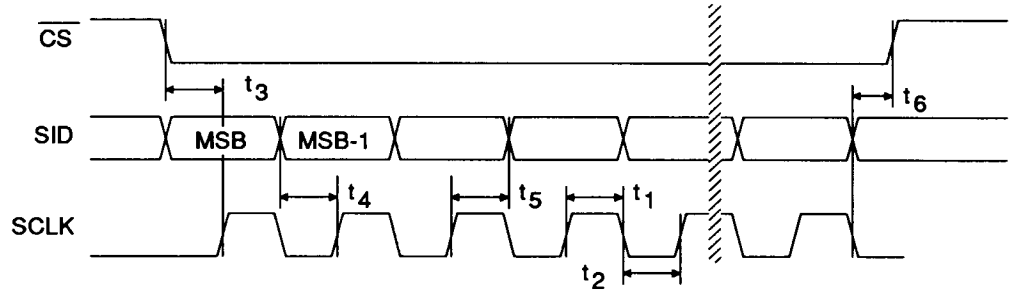
Parameter		Symbol	Min	Typ	Max	Units
High-Level Input Voltage:	XIN	V_{IH}	4.5			V
	All Pins Except XIN	V_{IH}	2.0			V
Low-Level Input Voltage	XIN	V_{IL}			0.5	V
	All pins Except XIN	V_{IL}			0.8	V
High-Level Output Voltage	(Note 11)	V_{OH}	(VD+)-1.0			V
Low Level Output Voltage	I_{out} = 1.6mA	V_{OL}			0.4	V
Input Leakage Current		I_{in}		1	10	µA
3-State Leakage Current		I_{OZ}			±10	µA
Digital Output Pin Capacitance		C_{out}		9		pF

11. I_{out} = -100 µA. This guarantees the ability to drive one TTL load. (V_{OH} = 2.4V @ I_{out} = -40 µA).

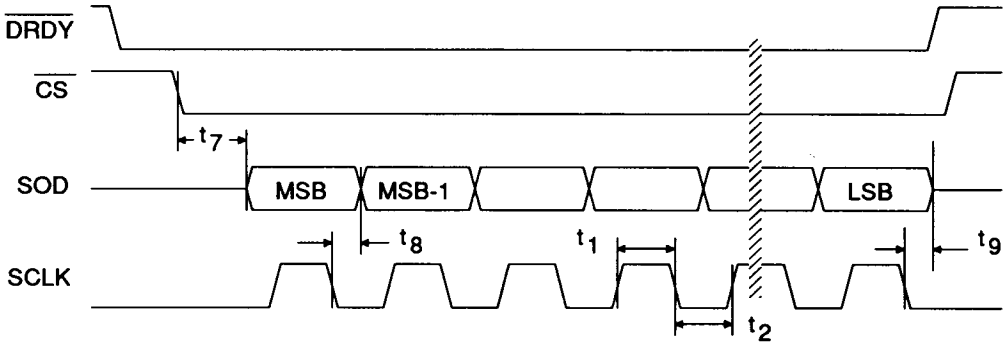
SWITCHING CHARACTERISTICS ($T_A = T_{min}$ to T_{max}; VA+, VD+ = 5V ± 5%; VA-, VD- = -5V±5%; Input Levels: Logic 0 = 0V, Logic 1 = VD+; C_L = 50 pF)

Parameter		Symbol	Min	Typ	Max	Units
Master Clock frequency:	Internal Oscillator:	XIN or f_{clk}	1.0	4.096	5.0	MHz
	External Clock:		TBD	4.096	5.0	MHz
Master Clock Duty Cycle			40		60	%
Rise Times: (Note 12)	Any Digital Input	t_{rise}			1.0	µs
	Any Digital Output			50		ns
Fall Times: (Note 12)	Any Digital Input	t_{fall}			1.0	µs
	Any Digital Output			50		ns
Start-Up						
Power-on Reset Period		t_{por}		100		ms
Oscillator Start-up Time	XTAL = 4.9152 MHz (Note 13)	t_{ost}		60		ms
$\overline{RST}$ Pulse Width		t_{res}	1/XIN			ns
Serial Port Timing						
Serial Clock Frequency		SCLK			2.4	MHz
Serial Clock	Pulse Width High	t_1	200			ns
	Pulse Width Low	t_2	200			ns
SID Write Timing						
$\overline{CS}$ Enable to Valid Latch Clock		t_3	150			ns
Data Set-up Time prior to SCLK rising		t_4	50			ns
Data Hold Time After SCLK Rising		t_5	50			ns
SCLK Falling Prior to $\overline{CS}$ Disable		t_6	50			ns
SOD Read Timing						
$\overline{CS}$ to Data Valid		t_7			150	ns
SCLK Falling to New Data Bit		t_8			150	ns
SCLK Falling to SOD Hi-Z		t_9			150	ns
$\overline{DRDY}$ Falling to Valid Data ($\overline{CS}$ = 0)		t_{10}			150	ns
$\overline{CS}$ Rising to SOD Hi-Z		t_{11}			150	ns
$\overline{CS}$ Disable Hold Time		t_{12}	50			ns
$\overline{CS}$ Enable Set-up Time		t_{13}	150			ns
$\overline{CS}$ Enable Hold Time		t_{14}	50			ns
$\overline{CS}$ Disable Set-up Time		t_{15}	150			ns

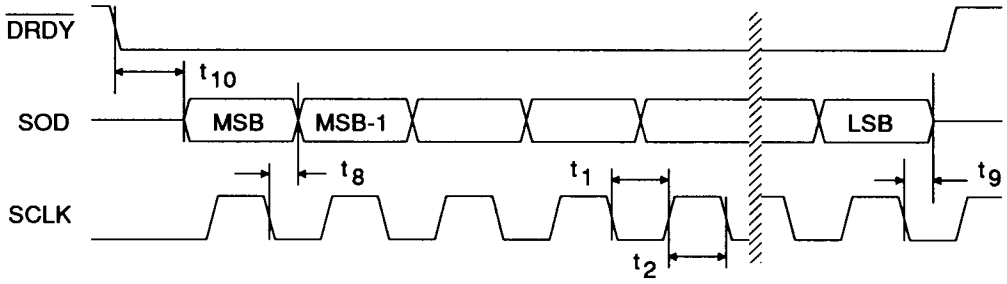
Notes: 12. Specified using 10% and 90% points on waveform of interest. Output loaded with 50 pF.
13. Oscillator start-up time varies with crystal parameters. This specification does not apply when using an external clock source.



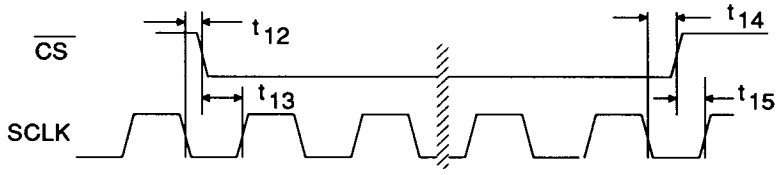
SID Write Timing (Not to Scale)



SOD Read Timing (Not to Scale)



SOD Read Timing with $\overline{CS}$ = 0 (Not to Scale)



$\overline{CS}$ with Continuous SCLK (Not to Scale)

RECOMMENDED OPERATING CONDITIONS (DGND = 0V, see Note 15.)

Parameter	Symbol	Min	Typ	Max	Units
DC Power Supplies: Positive Digital	VD+	4.5	5.0	5.5	V
Negative Digital	VD-	-4.5	-5.0	-5.5	V
Positive Analog	VA+	4.5	5.0	5.5	V
Negative Analog	VA-	-4.5	-5.0	-5.5	V
Differential Analog Reference Voltage	(VREF+)-(VREF-)	2.0	2.5	3.8	V
Analog Input Voltage: (Note 15)					
Unipolar	VAIN	0		+T	V
Bipolar	VAIN	-T		+T	V

Notes: 14. All voltages with respect to ground.

15. The CS5516 and CS5520 can accept input voltages up to +T in unipolar mode and -T to +T in bipolar mode where T=VREF/(Gx25). G is the gain setting at the second gain block. When the inputs exceed these values, the CS5516 and CS5520 will output positive full scale for any input above T, and negative full scale for inputs below AGND in unipolar and -T in bipolar mode. This applies when the analog input does not exceed ±2T overrange..

ABSOLUTE MAXIMUM RATINGS*

Parameter			Symbol	Min	Typ	Max	Units
DC Power Supplies:	Digital Ground	(Note 16)	DGND	-0.3		(VA+)+0.3	V
	Positive Digital	(Note 17)	VD+	-0.3		(VA+)+0.3	V
	Negative Digital		VD-	-0.3		-5.5	V
	Positive Analog		VA+	-0.3		5.5	V
	Negative Analog		VA-	+0.3		-5.5	V
Input Current, Any Pin Except Supplies		(Notes 18, 19)	I_{in}			±10	mA
Analog Input Voltage	AIN and VREF pins		V_{INA}	(VA-)-0.3		(VA+)+0.3	V
Digital Input Voltage			V_{IND}	-0.3		(VD+)+0.3	V
Ambient Operating Temperature			T_A	-55		125	°C
Storage Temperature			T_{stg}	-65		150	°C

Notes: 16. No pin should go more positive than (VA+)+0.3V.

17. VD+ must always be less than (VA+)+0.3 V,and can never exceed 6.0V.

18. Applies to all pins including continuous overvoltage conditions at the analog input pins.

19. Transient currents of up to 100mA will not cause SCR latch-up. Maximum input current for a power supply pin is ± 50 mA.

* WARNING: Operation beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

GENERAL DESCRIPTION

The CS5516 and CS5520 are monolithic CMOS A/D converters which include an instrumentation amplifier input, an on-chip programmable gain amplifier, and a DAC for offset trimming. While the devices are optimized for ratiometric measurement of Wheatstone bridge applications, they can be used for general purpose low level signal measurement.

Each of the devices includes a two-channel differential delta-sigma modulator (the signal measurement input and the reference input are digitized independently before a digital output word is computed), a calibration microcontroller, a two-channel digital filter, a programmable instrumentation amplifier block, a 4 bit DAC for coarse offset trimming, circuitry for generation and demodulation of AC (actually switched DC) bridge excitation, and a serial port. The CS5516 outputs 16-bit words; the CS5520 outputs 20-bit words.

The CS5516/20 devices can measure either unipolar or bipolar signals. Self-calibration is utilized to maximize performance of the measurement system. To better understand the capabilities of the CS5516/20, it is helpful to examine some of the error sources in bridge measurement systems.

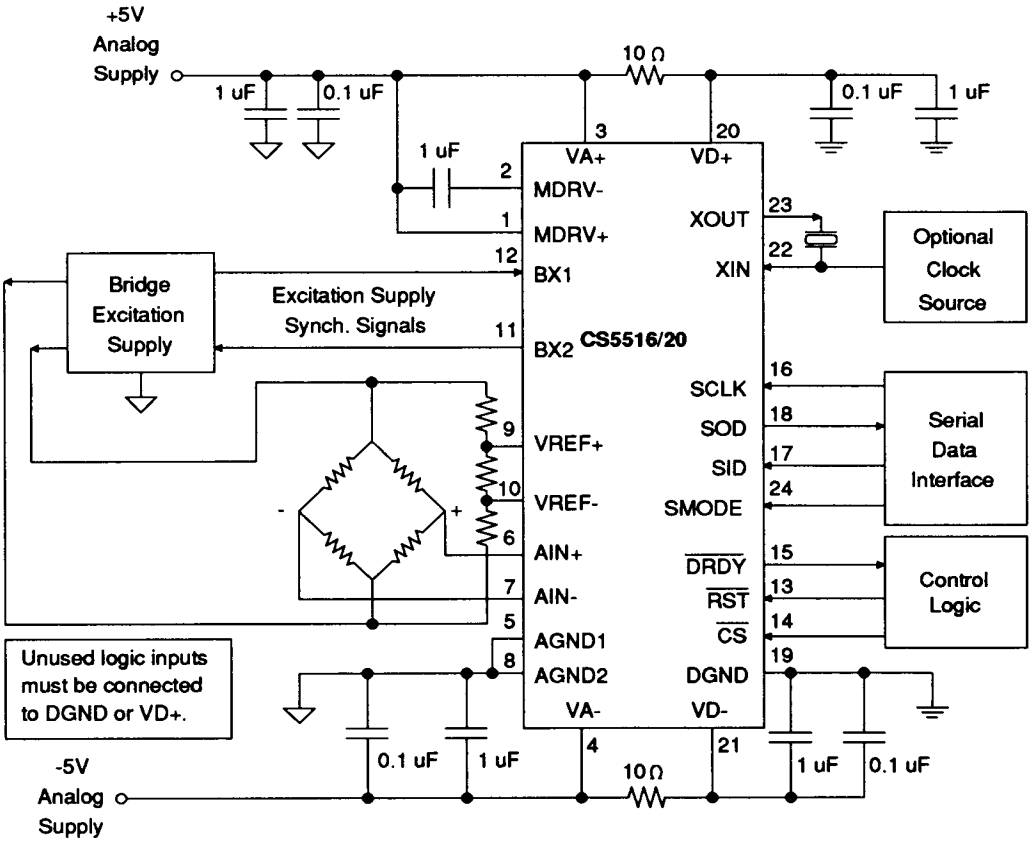


Figure 1. System Connection Diagram: AC Excitation Mode Using External Excitation

ENEMIES OF THE STRAIN GAUGE

The CS5516 and CS5520 address many common error sources encountered when digitizing bridge transducers. The following sections describe these error sources and the CS5516/20 features which allow for their control.

IR Drops

Strain gauges are low impedance devices (300Ω typical) and the bridge may be connected to the excitation source by long wires (R_{p1} and R_{p2}). This situation is illustrated in Figure 2.

Resistors R_{p1} and R_{p2} change the gain of the bridge, A_V:

$$A_V = \frac{(AIN+) - (AIN-)}{(VEXC+) - (VEXC-)} \quad (1)$$

Gauges are often purchased including interconnection cables, allowing errors due to R_{p1} and R_{p2} to be included in the gauge manufacturer's specification.

R_{p1} and R_{p2} include parasitic resistances of copper wire and various interconnections. These parasitics will not track the gauge resistance over temperature, and A_V will drift as a result. Generally, a gauge with a lower A_V drift will be more expensive.

A six-wire gauge allows for force and sense (Kelvin connection) of the excitation voltage. This allows all errors due to R_{p1} and R_{p2} to be removed by the ratiometric conversion of the CS5516/20. Figure 3 illustrates the solution.

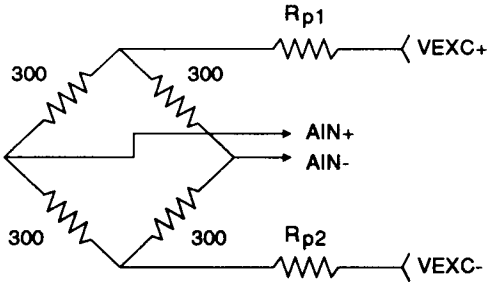


Figure 2. Four-Wire Bridge

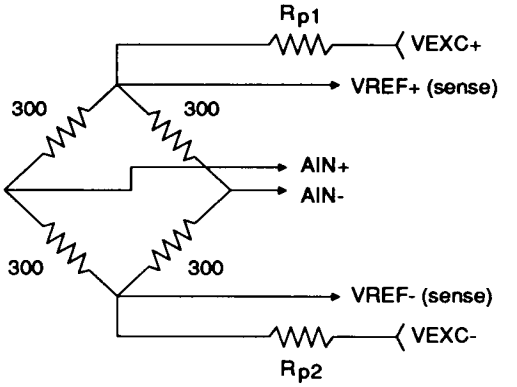


Figure 3. Six-Wire Bridge

Since the VREF inputs to the CS5516/20 provide very high impedance, no IR drops occur in the sense lines.

Pan Weight Offsets

Measuring zero weight in practice means measuring the weighing pan or surface itself. When the pan alone is measured, the bridge produces a differential output at AIN+ and AIN-.

At first glance, the CS5516's and CS5520's ratiometric offset calibration allows for easy removal of pan weight offsets. But the CS5516/20 is even more powerful than that. The internal 4-bit digital-to-analog converter allows for the removal of up to ±200% of the selected range's full scale, avoiding loss of resolution due to pan weight offsets.

Of critical importance here is the feature that the pan weight subtraction automatically scales with VREF+ and VREF-. Ratiometric, non-reference-sensitive operation is preserved even when the pan weight removal DAC is utilized.

50Hz/60Hz Pickup

Twisted pair interconnections should always be used to minimize 50/60Hz pickup into the VREF+, VREF- and AIN+, AIN- pairs. None the less, some 60Hz pickup into these pairs is inevitable.

The CS5516/20 remove pickup at either 50Hz (and harmonics) or 60Hz (and harmonics) by digital filters. Master clock frequencies of 4.096 MHz and 4.9152 MHz allow for removal of 50Hz and 60Hz, respectively.

Why bother to remove interference from the VREF input? The average value of the following expression:

$$V_{OUT} = \frac{V_{IN} + \alpha \sin(2\pi 60t)}{V_{REF} + \beta \sin(2\pi 60t)} \quad (2)$$

is NOT equal to V_{IN}/V_{REF}, so dc measurement errors result.

The CS5516 and CS5520 are different from most ADC systems because they convert both AIN and VREF with respect to an independent internal reference. Digital filters first remove the 50Hz and 60Hz (and harmonics). Then, and only then, is AIN ratioed to VREF. The result is significantly improved robustness when operating in harsh 50/60Hz environments.

Radio Frequency Interference (RFI)

The narrowband digital filters of the CS5516/20 also provide improved ADC performance in the presence of RFI. Just as 60Hz ac pickup into a traditional ADC reference input can cause shifts in the mean ADC output, RFI can produce the same effect.

The digital lowpass filters of the CS5516/20 remove all interference EXCEPT that present in narrow frequency bands centered around multiples of $f_{clk}/256$, where f_{clk} is the master clock to the converter. The delta-sigma modulator provides additional filtering at odd multiples of $f_{clk}/256$ and $f_{clk}/128$. The converter passband is illustrated on a linear frequency scale in Figure 4.

If RFI energy is present on AIN or VREF at multiples of $f_{clk}/64$, analog antialiasing filters should be evaluated for RFI control.

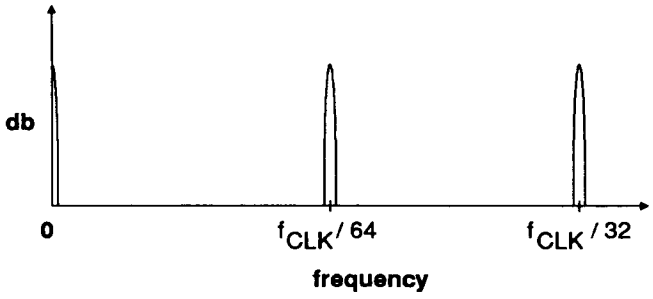


Figure 4. Filter Passband

Non-ratiometric Errors

For strain gauges operated with dc excitation voltages, voltage and current offsets impair measurement accuracy. The first such offset considered is shown as V_{OS} in Figure 5.

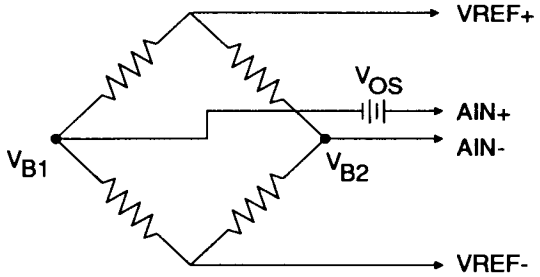


Figure 5. V_{OS} Offset

The fixed offset voltage obviously produces a signal at AIN+ and AIN- that does not scale with the excitation voltage; hence, the name "non-ratiometric error". Let's examine the significance of these errors with a little algebra. First, for convenience, let:

$$V_{REF} \equiv (VREF+) - (VREF-) \quad (3)$$

$$V_{IN} \equiv (AIN+) - (AIN-) \quad (4)$$

$$V_B \equiv V_{B1} - V_{B2} \quad (5)$$

Finally, the ideal bridge output is determined by the bridge gain, A_V:

$$V_B = A_V V_{REF} \quad (6)$$

But, thanks to the unwanted presence of V_{OS},

$$V_{IN} = A_V V_{REF} + V_{OS} \quad (7)$$

If the strain gauge ADC were perfectly ratiometric, its digital output would represent:

$$V_{OUT} = V_{IN}/V_{REF} = A_V + V_{OS}/V_{REF} \quad (8)$$

When $V_{OS} \neq 0$, the value of V_{OUT} depends on V_{REF}. The sensitivity, S_1, is given by:

$$S_1 \equiv \frac{\delta V_{OUT}/V_{OUT}}{\delta V_{REF}/V_{REF}} = \frac{-V_{OS}}{A_V V_{REF} + V_{OS}} \quad (9)$$

Some practical values illustrate the significance of equation 9. Suppose A_V = 0.002, (2mV/volt sensitivity), V_{REF} = 10V, and V_{OS} = 100 µV. Then, $S_1 \approx 5E-3$, implying a 10% change in V_{REF} will cause a $S_1 \times 10\% = 0.05\%$ change in V_{OUT}. A significant error indeed at the 16-bit level.

Equation 9 suggests three methods for reducing these non-ratiometric errors:

1) Buy a gauge with large A_V.
2) Use a large V_{REF}.
3) Measure V_{OS}, calibrate it out, and eliminate the problem.

The non-ratiometric offset calibration modes of the CS5520 make item #3 quite simple.

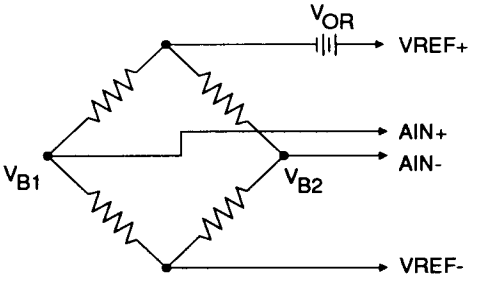


Figure 6. V_{OR} Offset

A second non-ratiometric error source is illustrated in Figure 6. The offset V_{OR} is picked up in the reference sense line. Thus,

$$V_B = A_V (V_{REF} - V_{OR}) \quad (10)$$

$$V_{OUT} = A_V - (A_V V_{OR})/V_{REF} \quad (11)$$

The sensitivity, S_2 is given by:

$$S_2 \equiv \frac{\delta V_{OUT}/V_{OUT}}{\delta V_{REF}/V_{REF}} = \frac{-V_{OR}}{V_{REF} - V_{OR}} \quad (12)$$

Not surprisingly, in this case increasing A_V doesn't help. Using the values of the previous example, $S_2 \approx 1E-5$.

Sensitivities S_1 and S_2 simply confirm that, when non-ratiometric errors (V_{OS} and V_{OR}) are non-zero, THE OUTPUT MEASUREMENT WILL VARY WITH VOLTAGE REFERENCE. A zero tempco, zero aging, perfect line regulation reference can avoid this variation, but one major advantage of ratiometric measurement techniques should be that no precise, stable reference is necessary.

The non-ratiometric offset and gain calibrations allow the user to "zero-out" the bridge excitation voltage and measure V_{OS} and V_{OR}, respectively. The voltages measured during this calibration step are subtracted from their respective inputs prior to the digital ratiometric operation. This calibration step can be performed whenever desired and contributes to the robustness of the CS5516/20 measurement system.

Thermocouples

A common source of non-ratiometric error is parasitic thermocouples. The differential reference and analog input paths should keep such thermocouples common mode. Route differential inputs next to each other, use low thermal emf interconnections and relays, etc. While perfectly matched thermocouple chains produce zero differential inputs, thermal gradients exist in any "real world" measurement system. Temperature-dependent non-ratiometric offsets result.

Use of non-ratiometric offset calibrations can substantially reduce thermocouple errors. None-

theless, temperature gradient fluctuations are difficult to eliminate.

AC excitation, shown in Figure 7, alternately flips the excitation voltages at the top and bottom of the bridge.

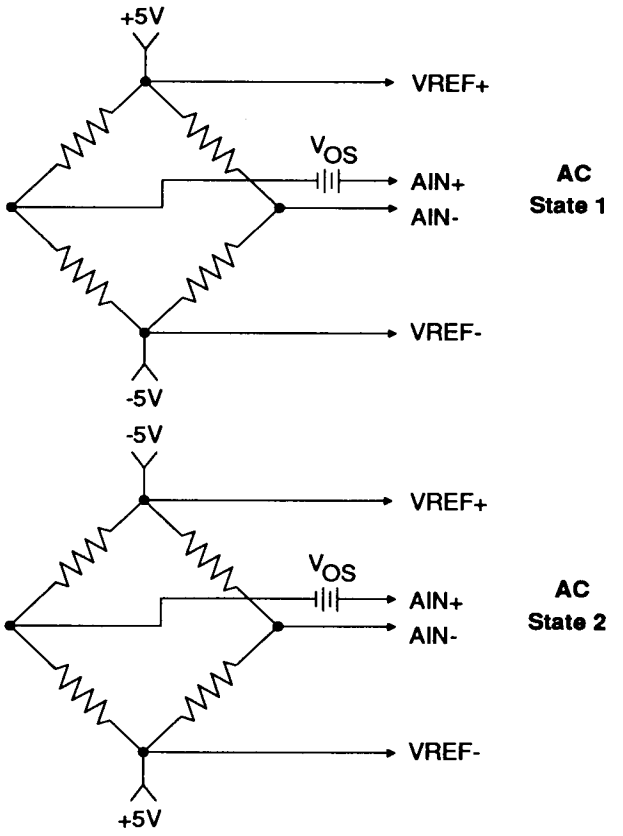


Figure 7. AC Excitation

With ac excitation, the desired signal V_B flips in polarity as the excitation voltage flips. The analog input becomes a square wave at the excitation frequency. V_{OS} doesn't flip. When the CS5516/20 synchronously demodulates the square wave in ac excitation mode, V_{OS} is modulated up into the digital filter's rejection band. V_{OS} problems are just filtered away.

Any systems designs that can exploit the benefits of ac excitation probably should. Accuracy fluctuations with temperature can be virtually eliminated. Any remaining non-ratiometric errors can still be attacked with non-ratiometric calibrations when ac excitation is used. The CS5516/20's BX1 and BX2 pins provide for both internally and externally controlled excitation signals.

Offsets due to leakages

Moisture or other contaminants in load cell cables or on the printed circuit board can cause current leakage paths, one of which is illustrated in Figure 8.

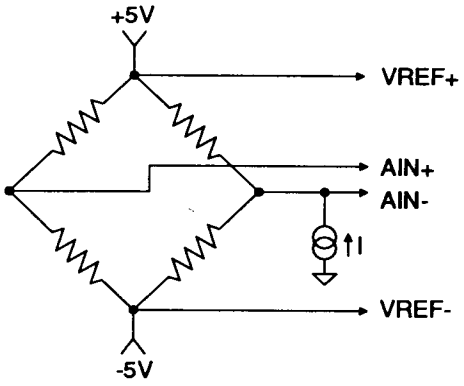


Figure 8. Leakage Effects Offset

The current source model is appropriate since the resistance of the leakage path is often much larger than that of the gauge. Comparison with Figure 7 reveals that both ac excitation and non-ratiometric calibration serve to reduce measurement errors due to these leakage current paths.

THEORY OF OPERATION

The front page of this data sheet illustrates the block diagram of the CS5516 and CS5520 A/D converter. The device includes an intrumentation amplifier with a fixed gain of 25. This chopper-stabilized instrumentation amplifier is followed by a programmable gain stage with gain settings of 1, 2, 4, and 8. The sensitivity of the input is a function of the programmable gain setting and of the reference voltage connected between the VREF+ and VREF- pins of the device. The full scale sensitivity of the instrumentation amplifier is VREF/(G x 25) in unipolar, or ±VREF/(G x 25) in bipolar, where VREF is the reference voltage between the VREF+ and VREF- pins, G is the gain setting of the programmable gain amplifier, and 25 is the gain of the instrumentation amplifier.

After the programmable gain block, the output of a 4-bit DAC is combined with the input signal. The DAC can be used to add or subtract offset from the analog input signal. Offsets as large as ±200 % of full scale can be trimmed from the input signal.

The CS5516 and CS5520 are optimized to perform ratiometric measurement of bridge-type transducers. The devices support dc bridge excitation or two modes of ac (switched dc) bridge excitation. In the switched-dc modes of operation the converter fully demodulates both the reference voltage and the analog input signal from the bridge.

The CS5516/20 includes a microcontroller which manages operation of the chip. Included in the microcontroller are eight different registers as-

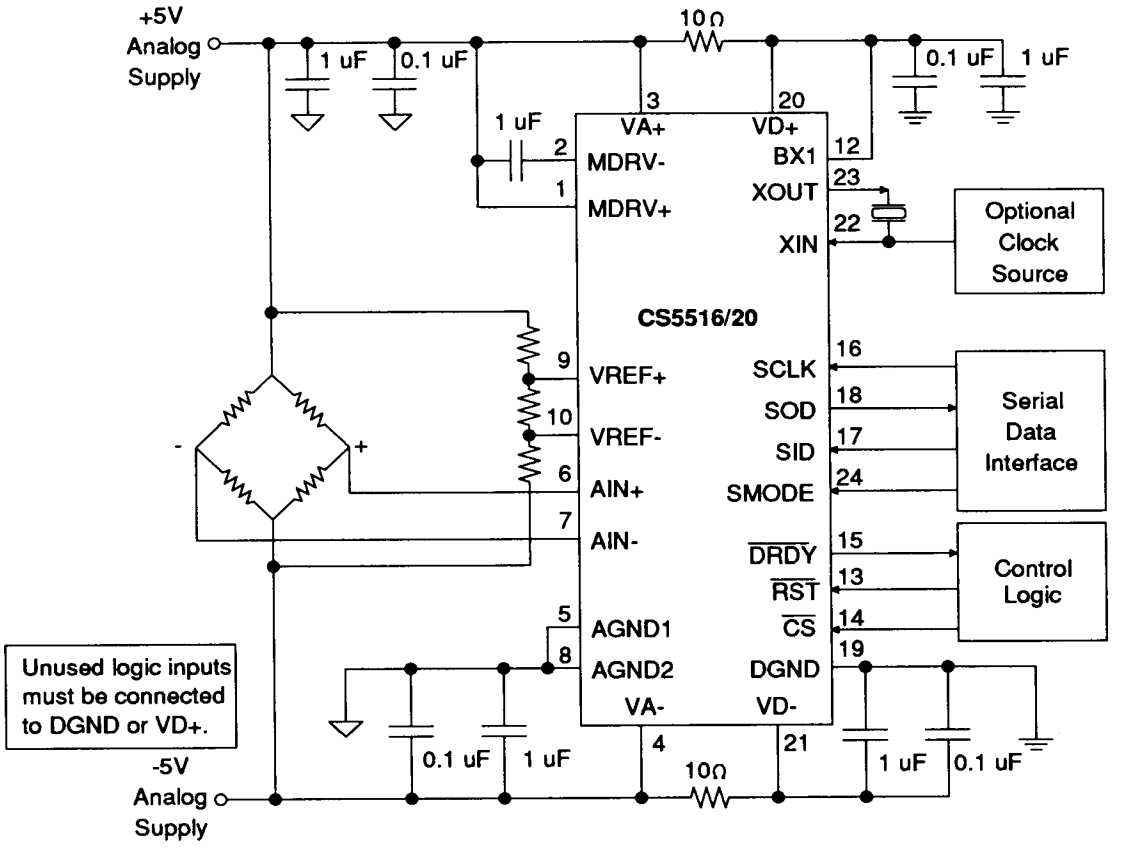


Figure 9. System Connection Diagram: DC Excitation Mode (EXC bit = 1)

Register[1]	Read	Write
Conversion Data Register [2]	88(H)	
Configuration Register	98(H)	90(H)[3]
DAC Register	B8(H)	B0(H)
Gain Register	A8(H)	A0(H)
AIN Ratiometric Offset Register	C8(H)	C0(H)
AIN Nonratiometric Offset Register	D8(H)	D0(H)
VREF Nonratiometric Offset Register	E8(H)	E0(H)

Notes: 1. 24 SCLKs are required to read or write all registers.
2. CS5516 has 16 data bits, CS5520 has 20 data bits.
3. The four DAC bits cannot be overwritten by this command.

Table 1. CS5516 and CS5520 Commands

sociated with the operation of the device. An 8-bit command register is used to interpret instructions received via the serial port. When power is applied, and the device has been reset, the serial port is initialized into the command mode. In this mode it is waiting to receive an 8-bit command via its serial port. The first 8 bits into the serial port are placed into the command register. Table 1 lists all the valid command words for reading from or writing to internal registers of the converter. Once a valid 8-bit command word has been received and decoded, the serial port goes into data mode. In data mode the next 24 serial clock pulses as shifting data either into or out of the serial port. When writing data to the port, the data may immediately follow the command word. When reading data from the port, the user must pause after clocking in the 8-bit command word to allow the microcontroller time to decode the command word, access the appropriate register to be read, and present its 24-bit word to the port. The microcontroller will signal when the 24-bit read data is available by causing the $\overline{\text{DRDY}}$ pin to go low.

The user must write or read the full 24-bit word except in the case of reading conversion data. In read data conversion mode, the user may read less than 24 bits if $\overline{\text{CS}}$ is then made inactive ($\overline{\text{CS}}$ = 1). $\overline{\text{CS}}$ going inactive releases user control over the port and allows new data updates to the port.

The user can instruct the on-chip microcontroller to perform certain operations via the configuration register. Whenever a new word is written to the 24-bit configuration register, the microcontroller then interprets the word and executes the configuration register instructions. Table 2 illustrates the bits of the configuration register. The bits in the configuration register will be discussed in various sections of this data sheet.

Configuration Register

DAC Bits, bits 23 - 20

23	22	21	20
D3	D2	D1	D0

D3-D0 Offset , increments of 25% of Full Scale
D3 is sign bit (0 = add offset;
1 = subtract offset)
D2 is the MSB, D0 represents 25% F.S.
e.g. 0001 = +25% F.S.
0111 = +175% F.S.
0000 = 0 % F.S.
1111 = -175% F.S.

Note: The DAC bits can only be written into the DAC register, but can be read via the configuration or DAC register.

Bridge Excitation, Bits 19-16

19	18	17	16
EXC	F1	F0	0

EXC Selects external or internal mode.
1 = External
0 = Internal

F1-F0 Select Internal mode Frequency
00 = dc
10 = XIN/16384 kHz
01 = XIN/8192 kHz
11 = XIN/4096 kHz

Bit 16 must be set to a logic 0

PGA Gain, Unipolar/Bipolar, Awake/Sleep Bits 15-11

15	14	13	12	11
G1	G0	U/B	0	A/S

G1-G0 Select gain setting
00 = 1 (x 25)
10 = 2 (x 25)
01 = 4 (x 25)
11 = 8 (x 25)

U/B Unipolar/Bipolar mode select
1 = Unipolar mode
0 = Bipolar mode

Bit 12 must be set to a logic 0

A/S Awake/Sleep mode select
0 = Awake mode
1 = Sleep mode

Execute Calibration and Calibration Control, Bits 10-4

10	9	8	7	6	5	4
EC	0	0	CC3	CC2	CC1	CC0

EC Execute calibration, EC must be set to 1 to execute calibration. See text for explanation of calibration steps.
Note: EC must be written back to 0 after calibration is completed.

Bits 9 and 8 must be set to 0.

CC3-CC0 Calibration Control Bits
1000 = Calibrate non-rationmetric offset, VREF
0100 = Calibrate non-ratiometric offset, AIN
0010 = Calibrate ratiometric offset, AIN
0001 = Calibrate gain, AIN

Reset Filter, Bit 0

3	2	1	0
0	0	0	RF

Bits 3 through 1 must be set to 0.

RF 1 = Reset Filter
0 = Normal Operation

MSB

23	22	21	20	19	18	17	16
D3	D2	D1	D0	EXC	F1	F0	0

15	14	13	12	11	10	9	8
G1	G0	U/B	0	A/S	EC	0	0

7	6	5	4	3	2	1	0
CC3	CC2	CC1	CC0	0	0	0	RF

Bits 16, 9, 8, 3, 2 and 1 must always be logic 0.

Table 2. Configuration Register

System Initialization

Whenever power is applied to the CS5516/CS5520 A/D converters, the devices must be reset to a known condition before proper operation can occur. The devices include an internal power-on reset function that initializes the internal logic. The internal reset is applied after power is established and lasts for approximately 100 ms. The RST pin can also be used to establish a reset condition. The reset signal should remain low for at least one XIN clock cycle to ensure adequate reset time. It is recommended that the RST pin be used to reset the converter if the power supplies rise very slowly or with poor startup characteristics. The RST signal can be generated by a microcontroller output, or by use of an R-C circuit.

The reset function initializes the configuration register, all five of the calibration registers, and places the microcontroller in command mode ready to accept a command from the serial port. Whenever the device is reset the DRDY pin will be set to a logic 1 and the on-chip registers are initialized to the following states:

Configuration	000000(H)
Calibration registers:	
DAC	0(H)
Gain	800000(H)
AIN Ratiometric Offset	000000(H)
AIN Non-ratiometric Offset	000000(H)
VREF Non-ratiometric Offset	000000(H)

CALIBRATION

After the CS5516/20 is reset, the device is functional and can perform measurements without being calibrated. The converter will utilize the initialized values of four of the five calibration registers to calculate output words.

The converter uses the two outputs (AIN & VREF) of the dual channel converter along with the contents of the calibration registers to compute the conversion data word. The following equation indicates the computation.

$$R0 = R4 \left[\left[\frac{D_{AIN} - R1}{D_{VREF} - R2} \right] - R3 \right]$$

Where R0 is the output data, D_{AIN} and D_{VREF} are the digital output words from the AIN and VREF digital filter channels, and R1, R2, R3 and R4 are the contents of the following calibration registers:
R1 = AIN non-ratiometric offset
R2 = VREF non-ratiometric offset
R3 = AIN ratiometric offset
R4 = Gain

The computed output word, R0, is a two's complement number which represents the percentage of full scale signal measured.

Calibration minimizes the errors in the converted output data. If calibration has not been performed, the measurements will include offset and gain errors of the entire system.

The converter may be calibrated each time it is used, or calibration words from a previous calibration may be uploaded into the appropriate calibration registers from some type of E^2PROM by the system microcontroller.

The converter uses five different registers to store specific calibration information. Each of the calibration registers stores information pertinent to correcting a specific source of error

Configuration Register					CAL Type	Calibration Time
EC	CC3	CC2	CC1	CC0		
1	1	0	0	0	VREF Non-ratiometric Offset	573,440/fclk
1	0	1	0	0	AIN Non-ratiometric Offset	573,440/fclk
1	0	0	1	0	AIN Ratiometric Offset	2,211,840/fclk
1	0	0	0	1	AIN System Gain	573,440/fclk
1	1	1	0	0	VREF & AIN Non-Ratiometric Offset	573,440/fclk
0	X	X	X	X	End Calibration	-

$\overline{\text{DRDY}}$ remains high throught calibration sequence. In all modes, $\overline{\text{DRDY}}$ falls immediately upon completion of the calibration sequence.

Table 3. CS5516/CS5520 Calibration Control

associated with either the converter or with the input transducer and its wiring. The method by which calibration is initiated is common to each of the calibration registers. The configuration register controls the execution of the calibration process. Bits CC3--CC0 in the configuration register determine which type of calibration will be performed and which of the five calibration registers will be affected. To execute a calibration will require that one of the bits (CC3--CC0) be set to a logic 1 to select the type of calibration to be performed. The EC bit of the same 24-bit configuration word is also set to a logic 1. On the falling edge of the 24th SCLK, the configuration word will be latched into the configuration register and the selected calibration will be executed. The time required to perform a calibration is listed in Table 3. The $\overline{\text{DRDY}}$ pin will remain a logic 1 during calibration, and will go low when the calibration step is completed.

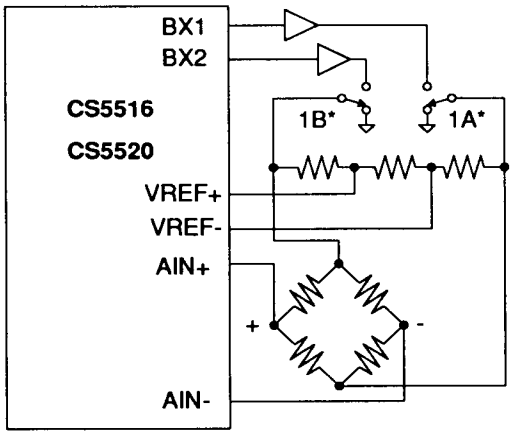
The serial port should remain inactive while a calibration is in progress. The EC bit of the configuration register remains a logic 1 until it is overwritten by a new configuration word (EC = 0). Consequently, if EC is left active, any write (the falling edge of the 24th SCLK) to any register inside the converter will cause a re-execution of the calibration sequence. This occurs because the internal microcontroller executes the contents of the configuration register every time the 24th SCLK falls after writing a 24-bit word to any internal register. To be certain that calibrations will not be re-executed each time a new word is written or read via the serial port, the EC bit of the configuration register must be written back to a logic 0 after the final calibration step has been completed.

The CC3--CC0 bits of the configuration register determine the type of calibration to be performed. The order in which the calibration steps are performed is important. A proper calibration sequence of all calibration steps should be performed in the following sequence. First, the non-ratiometric offset errors of the VREF and AIN input channels should be calibrated. Then the ratiometric offset of the AIN channel should be calibrated. And finally, the AIN channel gain should be calibrated.

To calibrate out the VREF and AIN non-ratiometric errors, the input channels to the VREF path into the converter and the AIN path into the converter must be grounded (this may occur at the pins of the IC, or at the bridge excitation as shown in Figure 10.). Then the EC, CC2 and CC3 bits of the configuration register must be set to logic 1. The converter will then perform a non-ratiometric calibration and place the proper 24 bit calibration words in the VREF and AIN non-ratiometric registers. Note that the two non-ratiometric offsets can be calibrated simultaneously or independently, but they must

be calibrated prior to the other calibration steps if the user wants to minimize the effect of these non-ratiometric offset errors. If the effects of the non-ratiometric errors are not significant enough to affect the user application, they can be left uncalibrated (after a reset, the non-ratiometric offset registers will contain 000000(H).

Once the non-ratiometric errors have been calibrated, the ratiometric offset error of the AIN channel should be calibrated next. To perform this calibration step, a reference voltage must be applied to the VREF+ and VREF- pins. Then, place "zero" weight on the scale platform. This will result in an offset voltage into the converter which will represent the offset of the bridge, the wiring, and the AIN input of the converter itself. A configuration word with the EC and CC1 bits set to logic 1 is then written into the configuration register. During the ratiometric offset calibration of AIN the microcontroller first uses a successive approximation algorithm to compute the correct values for the D3-D0 bits of the DAC register. This accommodates any large offsets on the AIN input signal. Once the four DAC bits are computed, this amount of offset is removed from the input signal. The microcontroller then computes the appropriate 24 bit number to place in the AIN ratiometric offset register to calibrate out the remaining offset not removed by the DAC.



*Note: The bridge can be grounded with a relay or with jumpers to perform non-ratiometric calibration.

Figure 10. Non-ratiometric System Calibration using Internal Excitation

After the AIN ratiometric offset has been calibrated, the next step is to perform a gain calibration. Gain calibration is performed with "full scale" weight on the scale platform. The EC and CC0 bits of the configuration register are set to logic 1. The gain calibration of the AIN channel is the final calibration step. After DRDY falls to signal the completion of this calibration step, the EC bit of the configuration register must be set back to logic 0 to terminate the calibration mode. The calibration word in the gain register spans 2^{-23} to 2 as illustrated.

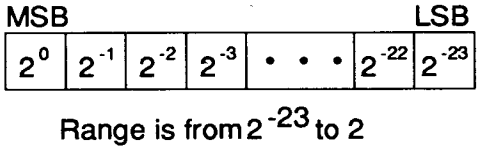


Figure 11. Gain Calibration Range

In a typical weigh scale application, the CS5516/CS5520 will be calibrated in combination with a load cell at the factory. Once calibrated, the calibration words are off-loaded from the converter and stored in E^2PROM. When powered-up in the field the calibration words are up-loaded into the appropriate registers. This is viable because the AIN and VREF input to the converter are "chopper-stabilized"and maintain excellent stability when subjected to changes in temperature.

Programmable Gain Amplifier

The programmable gain amplifier inside the CS5516/20 offers gains of 1, 2, 4, and 8. This is in addition to the fixed gain of × 25 in the input instrumentation amplifier. The gain tracking of the PGA is about one per cent between ranges. The user can remove this error by performing a gain calibration at the factory with a full scale signal on each range. The gain calibration word for each gain range can be off-loaded into E^2PROM and uploaded into the gain register

whenever a new gain setting is selected for the PGA. Gain stability over temperature for the converter itself is approximately 1 ppm/°C when the device is used ratiometrically.

Serial Interface Modes

The CS5516/20 support either 5, 4 or 3 pin serial interfacing. The SMODE pin sets the operating mode of the serial interface. With SMODE = 0, the device assumes the user is operating with either a 5 or 4 wire interface. The five wire mode includes SOD, SID, SCLK, DRDY, and CS. In the four wire mode, CS is connected to DGND as a logic 0. The user would then interface to the SOD, SID, SCLK, and DRDY pins.

Reading a register in the converter requires a command word to be written to the SID pin. For example, to read the conversion data register, the following command sequence should be performed. First, the command word 88(H) would be issued to the port. In the 5 wire interface mode, this would involve activating CS low, followed by 8 SCLKs (note that SCLK must always start low and transition from low to high to latch the transmit data, and then back low again) to input the 8-bit command word. CS must be low for the serial port to recognize SCLKs during a write or a read, but it is actually the first rising SCLK during command time that gives the user control over the port. After writing the command word, the user must pause and wait until the CS5520 presents the selected register data to the serial port. The DRDY signal will fall when the data is available. When reading the conversion data register, it may take up to 112,000 XIN clock cycles for DRDY to fall after the 88(H) command word is recognized. See Figure 12 for an illustration of command and data word timing.

The conversion data register is actually the accumulator of the post-processor which computes the output data. At the end of each filter convolution cycle, the internal microcontroller checks to see if a read conversion data register command has been interpreted. If so, it transfers the accumulator result to the serial port.

Whenever registers other than the conversion data register are read, the DRDY pin will fall within 256 XIN clock cycles (62.5 µs with XIN = 4.096 MHz) after the command word is recognized. When DRDY falls, 24 SCLKs are then issued to the port to read the 24-bit output data word. DRDY will return high after all 24 bits have been clocked out. The SOD pin will be in a Hi-Z state whenever CS is high, or after all 24 output data bits have been clocked out of the port.

If SMODE = 1 (tied to VD+), the interface operates as a 3 wire interface using only SOD, SID, and SCLK. In the 3 wire mode CS must be tied to DGND. DRDY operates normally but is not used. Instead, the DRDY signal modifies the behavior of the SOD signal, allowing it to signal to the user when data is available. To read data from the converter requires a command word to be written to the SID pin. The SOD output is normally high (never Hi-Z). When output data is available, the SOD signal will go low. The user would then issue 8 SCLKs to the SCLK pin to clear this data ready signal. On the falling edge of the 8th SCLK the SOD pin will present the first bit of the 24 bit output word.

The CS5516/20 is designed such that it can output conversion data words continuously, without issuing a new command word prior to each data read. Under the following circumstances, continuous conversion data can be read from the port after issuing only one 88(H) command word. Once the command to read the conversion data register is issued, DRDY must be allowed to go low, after which 24 SCLKs are issued to read the data. This will cause DRDY to return high.

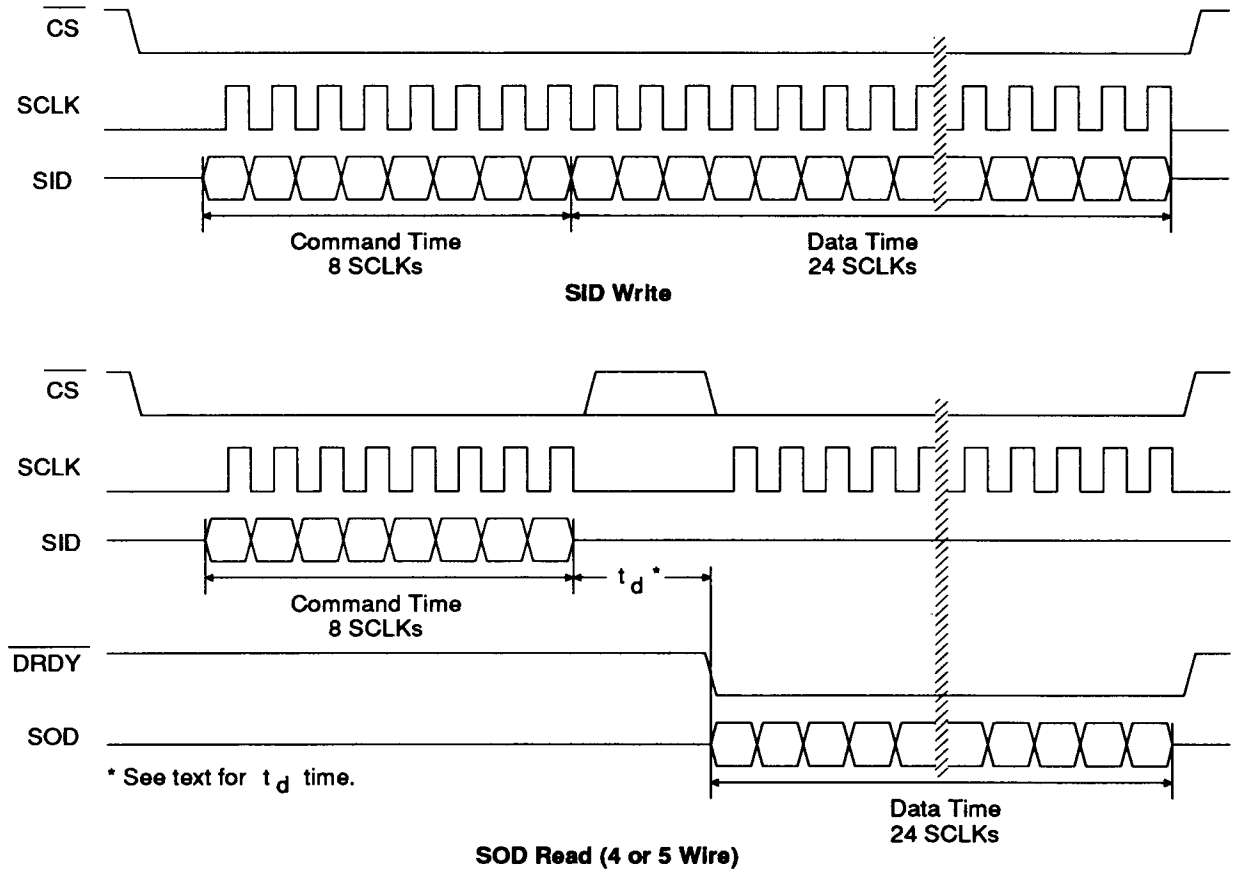


Figure 12. Command and Data Word Timing

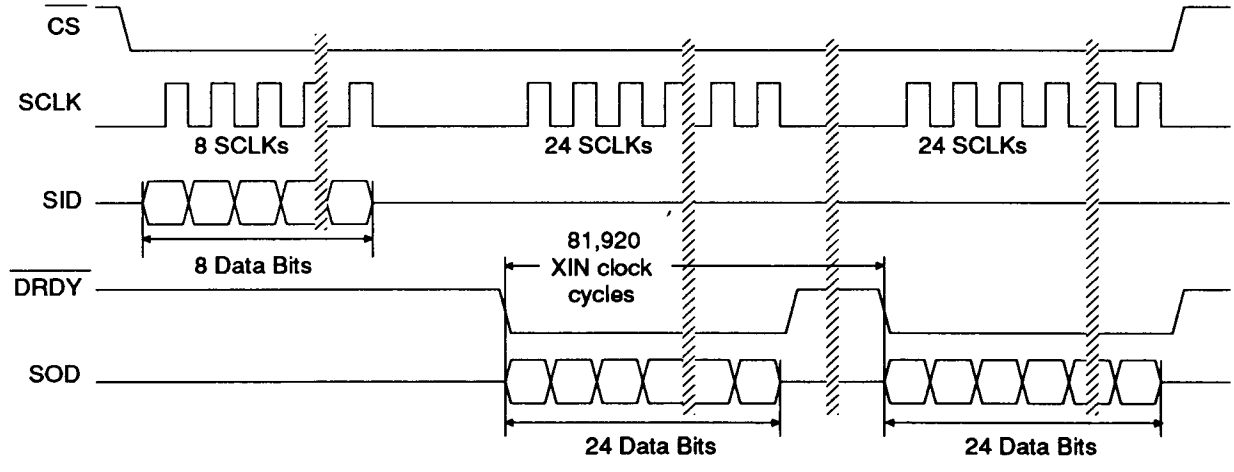


Figure 13. Continuous Read Conversion Data Mode (4 or 5 Wire)

The converter will continue to output conversion words at the update rate as long as a different command word is not started prior to DRDY falling again. The user is not required to read every output word to remain in the continuous update mode. DRDY will toggle high, and then low as each new output word becomes available. If a command word is issued immediately after a data word is read, the converter will end the read conversion mode. Figure 13 illustrates the continuous data mode.

The user should perform all data reads and command writes within 51,000 XIN clock cycles after DRDY falls to avoid ambiguity as to who controls the serial port.

Serial Port Initialization

If for any reason the off-chip microcontroller fails to know whether the serial port of the CS5516/20 is in data mode or command mode the following initialization procedure can be issued to the port to force the CS5516/20 into the command mode. Write 128 or more 1's to the SID pin. Then issue a single 0 to the SID pin. The port will then be initialized into the command mode and will be waiting for an 8-bit command word.

Bridge Excitation Options

The CS5516/CS5520 A/D converters are optimized for Wheatsone bridge applications. The converters support either dc or ac (switched dc) bridge excitation.

DC Bridge Excitation

The CS5516/CS5520 can be configured for dc bridge excitation in either of two ways. The EXC bit of the configuration register can be set for either internal or for external excitation. If set to internally-controlled mode (EXC = 0), the F1 and F0 bits must be set to logic 0s. In this condition, the bridge can be excited from a dc supply with a resistor divider to develop the appropriate reference voltage for the VREF+ and VREF- pins. Note that the bridge excitation should not be applied prior to the CS5516/CS5520 being powered-up. With EXC, F1, and F0 set to logic 0, the BX1 output will be logic 0 (0 volts) and the BX2 output will be a logic 1 (+5 volts).

A second method for configuring the converter for dc excitation is by setting EXC = 1, and connecting BX1 (pin 12) to VD+ (pin 20). This sets the converter for use with external excitation which uses the BX1 pin as an input to set the excitation frequency. With BX1 = VD+, the external excitation frequency is zero, or dc.

AC Bridge Excitation

AC bridge excitation involves using a clock signal to generate a square wave which repetitively reverses the excitation polarity on the bridge. Advantages of this type of excitation are explained in the "Enemies of the Strain Gauge" section of the data sheet. To excite the bridge dynamically requires some type of bridge driver external to the CS5516/CS5520 converter. This driver is driven by a square wave clock. The source of this clock depends upon whether the converter is set for internal excitation or for external excitation. Figure 14 illustrates a sample bridge drive circuit when operating in the external AC mode.

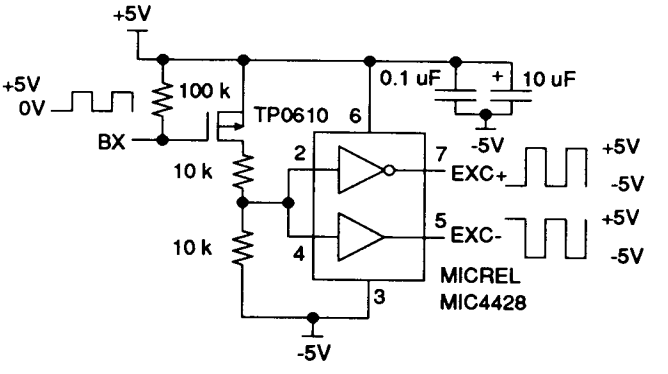
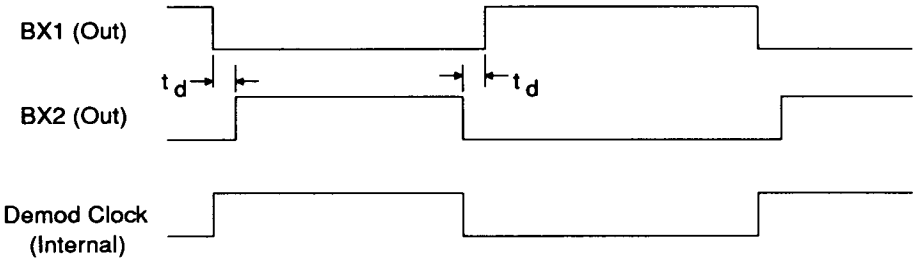


Figure 14. Sample AC Bridge Driver

Using internal excitation involves setting the EXC bit of the configuration register to 0, and setting the F1 and F0 bits to select the excitation frequency for the bridge. In this mode the excitation frequency is a sub-multiple of the XIN clock frequency. The excitation clock is output from the BX1 and BX2 pins of the converter in the form of a two-phase non-overlapping clock. The converter is capable of demodulating this clocked excitation. For proper operation the bridge must be driven so that its output signals into the AIN+ and VREF+ pins of the converter are in phase with the demodulation clock inside the converter (see Figure 15). The non-overlapping clock signals from BX1 and BX2 are CMOS level outputs (0 to VD+ volts) and are capable of driving one TTL load. A buffer amplifier MUST be used to drive the bridge.

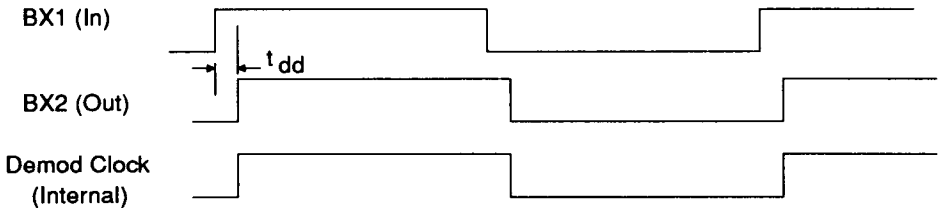
Whenever the internal mode is used for dynamic bridge excitation the signals are non-overlapping. The non-overlapping time is one XIN clock cycle.

The converter can also be configured to provide dynamic bridge excitation when operating in the external-controlled bridge excitation mode. With the EXC bit of the configuration register set to logic 1, the BX1 pin becomes an input which determines the bridge excitation frequency and phase. BX1 should be near 50% duty cycle. The user can select the excitation frequency with the following restrictions. The excitation frequency



Note: The signals from the bridge into AIN+ and VREF+ of the converter must be in phase with the demodulation clock.
t_d is 1 cycle of XIN clock.

Figure 15. Internal Excitation Clock Phasing



Note: The signals from the bridge into AIN+ and VREF+ of the converter must be in phase with the demodulation clock.
$t_{dd} \leq 64/XIN$.

Figure 16. External Excitation Space Clock Phasing

must be synchronous with the XIN frequency of the converter and must be chosen using the following equation:

$$F_{exc} = (N \times XIN)/81{,}920$$

where N is an integer and lies in the range including 1 to 160. F_{exc} is the desired bridge excitation frequency. Other asynchronous frequencies are possible but may introduce a jitter component in the BX output signals.It is desirable not to choose an excitation frequency where interference components are present, such as 50 or 60 Hz or their harmonics. The XIN frequency would be divided down using a counter IC external to the A/D converter. F_{exc} would be input to the BX1 pin of the converter to synchronize the internal operations of the amplifiers and synchronous detection circuitry and to generate a clock output from the BX2 pin. The BX2 output is then used to drive the bridge amplifier with a signal of proper phase for detection by the converter. Figure 16 indicates the necessary phase of the signals to insure proper demodulation.

Whenever the dynamic excitation clock output from either the BX1 and BX2 pins (during internal exciation) or from the BX2 pin (during external excitation) changes states, the converter waits 64 XIN cycles before sampling the AIN and VREF signal inputs. The delay allows some time for the signal to settle from the modulation event.

Input Filtering

Some load cells are located a distance from the input to the converter. Under these conditions, separate twisted pair cabling is recommended for the excitation drive to the bridge, the excitation sense leads (if used) and for the AIN± signal leads. If the AIN± leads to the converter and the VREF± leads to the converter are filtered, care should be exercised in the choice of components. With either dc or ac excitation, one should limit

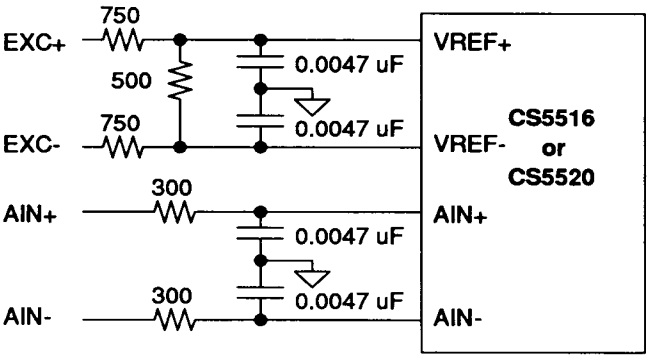


Figure 17. External AC Excitation Filter Components

any input filtering resistors on AIN or on VREF to below 1 kΩ. Values greater than this will degrade noise performance of the converter. In ac excitation applications, any filtering must be broadband enough that the switched dc excitation signal can settle within 10 µsecs. Failure to meet this settling requirement will affect measurement accuracy. Figure 17 illustrates acceptable filter components for ac excitation. If only differential filtering is required, a single capacitor can be placed between AIN+ and AIN- (and VREF+ and VREF-) in place of two capacitors to ground.

Voltage Reference Considerations

The CS5516/20 include an on-chip voltage reference which is output on the MDRV- and referenced from the MDRV+ pin. The converter is designed to be operated as a ratiometric measurement device. The 2-channel delta-sigma converter uses the internal MDVR (Modulator Differential Voltage Reference) as its reference. Since the MDVR is used for converting both the AIN and VREF signals at the same time, the absolute value of the MDVR and its tempco are not important when the CS5516/20 is used in the ratiometric measurement mode. The voltage reference output, MDVR-, should be decoupled using a 1 uF capacitor which is connected to the MDRV+ supply line. Voltage reference decoupling is shown on the system connection diagrams.

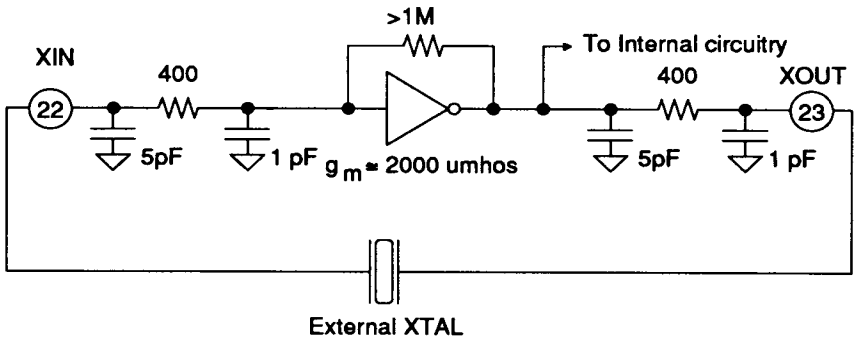


Figure 18. On-Chip Gate Oscillator Model

If absolute measurements are to be made by the CS5516/20, then a precision reference should be input into the VREF+ and VREF- terminals.

Clock Generator

The CS5516/20 includes a gate which can be connected as a crystal oscillator to provide the master clock to run the chip. Alternatively, an external (CMOS compatible) clock can be input into the XIN pin. Figure 18 illustrates a simple model for the on-chip gate oscillator. The on-chip oscillator is designed to typically operate with crystal frequencies between 4.0 and 5.0 MHz without additional loading capacitors. If other crystal frequencies, or if ceramic resonators are used, additional loading capacitance may be necessary.

The XOUT pin can be used to drive one CMOS gate for system clock requirements. Be sure to include the gate's input capacitance and stray capacitance as part of the loading capacitance for the resonating element.

Digital Filter

The delta-sigma A/D converter consists of a third order modulator and a digital filter. The device is optimized to operate with clock frequencies of 4.096 MHz or 4.9152 MHz. These result in the filter having a 3dB bandwidth of 12 Hz or 15 Hz, with output word rates of 50 or 60Hz. The rejection at 50Hz ± 3Hz is 70 dB minimum with a 4.096 MHz clock. Similar rejection is obtained at 60 Hz with a 4.9152 MHz clock. The user can further decimate the output without aliasing down to the DC to 3Hz band. Rejection of line frequencies is therefore ensured over the normal frequency

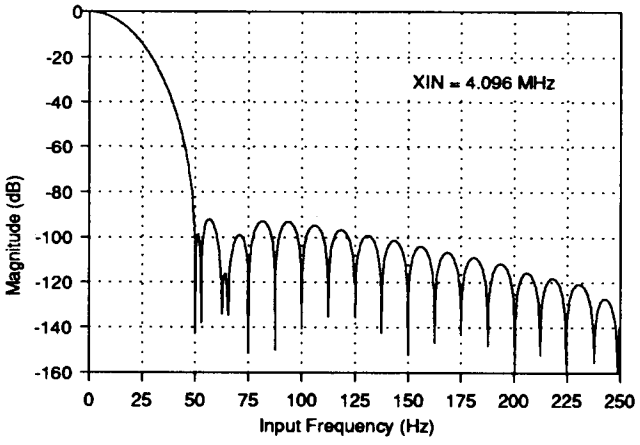


Figure 19. Filter Magnitude Response

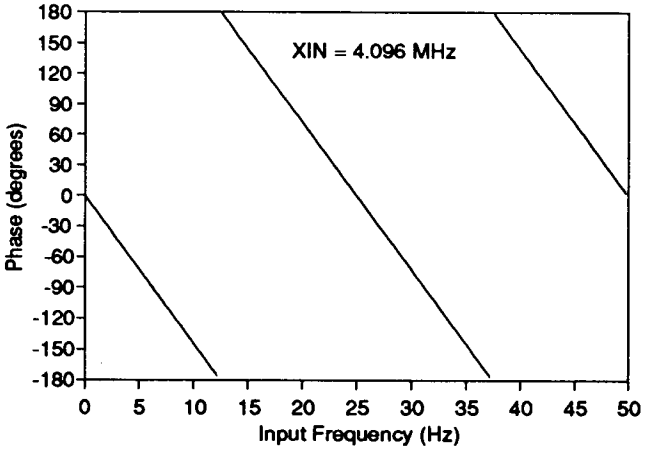


Figure 20. Filter Phase Response.

variation of the power system. Figures 19 and 20 illustrate the magnitude and phase of the filter when using a 4.096 MHz clock.

The digital filter computes a new output data word every 81,920 XIN clock cycles. If the input experiences a large change in amplitude, the PGA gain is changed, or the DAC calibration registers are changed, it may take up to six filter cycles (81,920 X 6 clock cycles) for the filter to compute an output word which is fully settled to the input signal.

Output Coding

The CS5516/20 converters output data in binary format when operating in unipolar mode and in two's complement when operating in bipolar mode. Table 4 illustrates the output coding for the converters. Note that when reading conversion data from the converter the data word is output MSB or sign bit first. Falling edges on SCLK advance the data word to the next lower bit.

The output conversion words from both the CS5516 and the CS5520 are 24 bits long. The CS5516 has 16 data bits followed by 8 flag bits (all identical). The CS5520 has 20 data bits followed by 4 flag bits (all identical). To read the conversion data, including the error flag information will require at least 17 SCLKs for the CS5516 and at least 21 SCLKs for the CS5520.

Under large overrange conditions, approximately two times full scale, (for example: when the converter is set-up for a full scale sensitivity of 25 mV, an input of 50 mV would be an excessive overrange condition) the flag bits of the output conversion word will be set. If an excessive overrange condition exists, whether it be a positive or negative overrange, the converter may not be able to yield a proper output code. Under this condition the flag bits will be set to all 1's. Under normal operating conditions flag bits will remain 0's.

Unipolar Input Voltage	Offset Binary	Bipolar Input Voltage	Two's Complement
>(VFS-1.5 LSB)	FFFF	>(VFS-1.5 LSB)	7FFF
VFS-1.5 LSB	FFFF ----- FFFE	VFS-1.5 LSB	7FFF ----- 7FFE
VFS/2-0.5 LSB	8000 ----- 7FFF	-0.5 LSB	0000 ----- FFFF
+0.5 LSB	0001 ----- 0000	-VFS+0.5 LSB	8001 ----- 8000
<(+0.5 LSB)	0000	<(-VFS+0.5 LSB	8000

CS5516 Output Coding

Unipolar Input Voltage	Offset Binary	Bipolar Input Voltage	Two's Complement
>(VFS-1.5 LSB)	FFFFF	>(VFS-1.5 LSB)	7FFFF
VFS-1.5 LSB	FFFFF ----- FFFFE	VFS-1.5 LSB	7FFFF ----- 7FFFE
VFS/2-0.5 LSB	80000 ----- 7FFFF	-0.5 LSB	00000 ----- FFFFF
+0.5 LSB	00001 ----- 00000	-VFS+0.5 LSB	80001 ----- 80000
<(+0.5 LSB)	00000	<(-VFS+0.5 LSB	80000

CS5520 Output Coding

Note: VFS in the table equals the full scale voltage between +VREF/(G x 25) and ground for unipolar mode; and between ±VREF/(G x 25) for bipolar mode. The signal input to the A/D section of the converter has been amplified by the instrumentation amplifier (x25) and the PGA gain, G (1, 2, 4 or 8). See text about error flags under overrange conditions.

Table 4. CS5516/20 Output Coding

After the converter is first powered-up, a $\overline{RST}$ is issued, or the device comes out of the SLEEP mode, the first conversion data read may erroneously have its error flag bits set to "1".

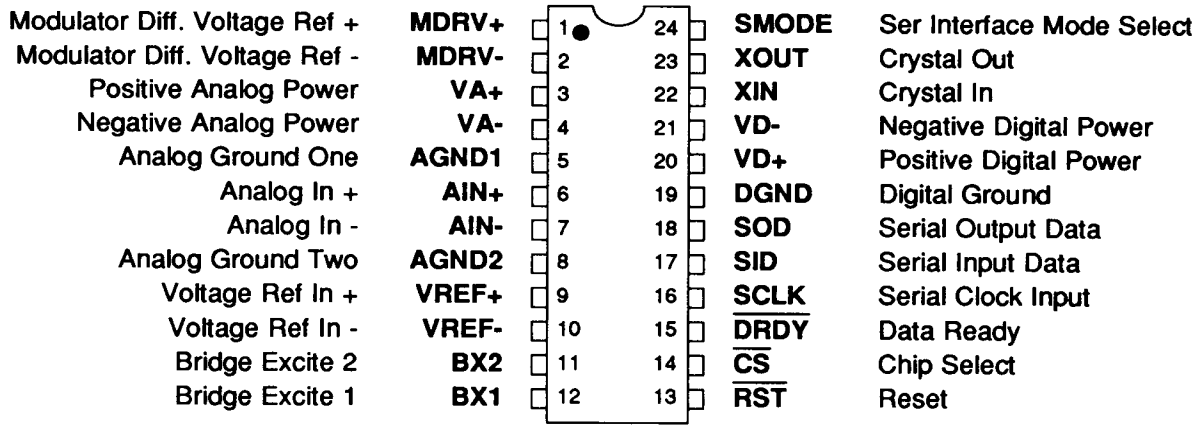
Synchronizing Multiple Converters

Multiple converters can be made to output their conversion words at the same time if they are operated from the same clock signal at XIN. To synchronize multiple converters requires that they all have their RF bit of the configuration register written to a logic 1 and then back to 0. The filters will be allowed to start convolutions after the falling edge of the 24th SCLK used to write the RF bit to the configuration register. The filter will start a new convolution on the next rising edge of the XIN clock after the 24th SCLK falls.

Sleep Mode

The CS5516/20 configuration register has an A/S bit which allows the users to put the device in a sleep condition to lower quiescent power. Upon reset the A/S bit device is set to a logic 0 which places the device in the 'awake' condition. Writing a 1 to the A/S bit will shutdown most of the chip, including the oscillator. It is desirable to use the following sequence when coming out of sleep. Write a logic 0 to the A/S bit of the configuration register. In the same configuration word write a logic 1 to the RF bit of the configuration register. Then wait until it is certain that the oscillator has started. After the oscillator has started or a clock present on the XIN pin, set the RF bit back to 0. The user should then wait at least 6 output word update periods before expecting a valid output data word.

PIN DESCRIPTIONS



Power Supply Connections

VD+ - Positive Digital Power, PIN 20.
Positive digital supply voltage. Nominally +5 volts.

VD- - Negative Digital Power, PIN 21.
Negative digital supply voltage. Nominally -5 volts.

DGND - Digital Ground, PIN 19.
Digital ground.

VA+ - Positive Analog Power, PIN 3.
Positive analog supply voltage. Nominally +5 volts.

VA- - Negative Analog Power, PIN 4.
Negative analog supply voltage. Nominally -5 volts.

AGND1, AGND2 - Analog Ground, PINS 5, 8.
Analog ground.

Clock Generator

XIN; XOUT - Crystal In; Crystal Out, Pins 22, 23
An internal gate is connected to these pins enabling the use of either a crystal or a ceramic resonator to provide the master clock for the device. Alternatively, an external (CMOS compatible) clock can be input to the XIN pin as the master clock for the device.

Digital Inputs

$\overline{RST}$ - Reset, PIN 13.

Reset pin initializes all calibration registers to a known condition and places the serial port into the command mode.

$\overline{CS}$ - Chip Select, PIN 14.

An input which can be enabled by an external device to gain control over the serial port. When this pin is high, SOD is in a high impedance state if SMODE = 0.

SCLK - Serial Data Clock, PIN 16.

A clock signal at this pin determines the output rate of the data from the SOD pin and the input data rate on the SID pin.

SID - Serial Input Data, PIN 17.

This pin is used for inputing command and configuration words or inputing calibration words. Data is input at a rate determined by SCLK. SID is in a don't care state when no data is being clocked in.

SMODE - Serial Interface Mode Select, PIN 24.

Selects the operating mode of the serial port. When low the serial port operates in the 5 or 4 wire interface mode. When high the chip will enter the 3 wire interface mode.

Analog Inputs

AIN+ and AIN- - Analog Inputs, PINS 6, 7.

The analog input signals from the transducer. These are true differential inputs.

VREF+ and VREF- - Voltage Reference Inputs, PINS 9,10.

These are the differential analog reference voltage inputs.

MDRV+ - Modulator Differential Voltage Reference, PIN 1.

Positive terminal of the internal differential voltage reference which can be tied to the positive supply (VA+) or ground (AGND).

MDRV- - Modulator Differential Voltage Reference, PIN 2.

This is the -3.75V modulator differential voltage reference output and can be used to generate an analog reference. Note this is with reference to the MDRV+ line.

Digital Outputs

BX1 and BX2 - AC Bridge Excitation Signals, PINS 12, 11.

These can be buffered to drive the transducer or used as synchronizing signals for a transducer drive circuit. BX1 and BX2 are 0 to +5V signals.

$\overline{\text{DRDY}}$ - Data Ready, PIN 15.

$\overline{\text{DRDY}}$ goes low every 81,920 cycles of XIN (when in read conversion data mode) to indicate that new data has been placed in the output port. $\overline{\text{DRDY}}$ goes high when all the serial port data is clocked out, when the serial port is being updated with new data, when a calibration is in progress, or when the device is in SLEEP.

SOD - Serial Output Data, PIN 18.

Data from the serial port will be output from this pin at a rate determined by SCLK . The data will either be conversion data, or, calibration values, dependent upon the command word that has been previously input on the SID pin. The SOD pin furnishes a high impedance output state when not transmitting data (SMODE = 0).

Ordering Guide

Model Number	Linearity Error (Max)	Temperature Range	Package
CS5516-AP	0.003%	-40 to +85°C	24-pin 0.3" Plastic DIP
CS5516-AS	0.003%	-40 to +85°C	24-pin 0.3" SOIC
CS5516-SD	0.003%	-55 to +125°C	24-pin 0.3" Cerdip
CDB5516	CS5516 evaluation board		
CS5520-BP	0.0015%	-40 to +85°C	24-pin 0.3" Plastic DIP
CS5520-BS	0.0015%	-40 to +85°C	24-pin 0.3" SOIC
CS5520-SD	0.003%	-55 to +125°C	24-pin 0.3" Cerdip
CDB5520	CS5520 evaluation board		

SPECIFICATION DEFINITIONS

Linearity Error

The deviation of a code from a straight line which extends between two fixed points on the A/D converter transfer function. In unipolar mode, the straight line extends from one point located ½ LSB below the first code transition, one count above all zeros; to the second point located ½ LSB beyond the code transition to all ones. In bipolar mode, the straight line extends from one point located ½ LSB beyond the code transition to all ones, passing through a point ½ LSB below code 8000(H) (16-bit); 80000(H) (20-bit); extending to beyond negative full scale. Units are in percent of full-scale.

Differential Nonlinearity

The deviation of a code's width from the ideal width. Units in LSBs.

Full Scale Error

The deviation of the last code transition form the ideal [{(VREF+)-(VREF-)}-3½ LSB]. Units are in LSBs.

Unipolar Offset

The deviation of the first code transition from the ideal (½ LSB above AGND) when in unipolar mode (BP/$\overline{UP}$ low). Units are in LSBs.

Bipolar Offset

The deviation of the mid-scale transition (011...111 to 100...000) from the ideal (½ LSB below AGND) when in bipolar mode (BP/$\overline{UP}$ high). Units are in LSBs.

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