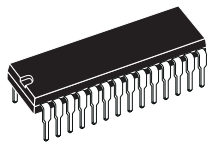
TDA7343

DIGITALLY CONTROLLED AUDIO PROCESSOR

- INPUT MULTIPLEXER
  - TWO STEREO AND ONE MONO INPUTS
  - SELECTABLE INPUT GAIN FOR OPTIMAL ADAPTATION TO DIFFERENT SOURCES
- FULLY PROGRAMMABLE LOUDNESS FUNCTION
- VOLUME CONTROL IN 0.3dB STEPS INCLUDING GAIN UP TO 20dB
- ZERO CROSSING MUTE AND DIRECT MUTE
- SOFT MUTE CONTROLLED BY SOFTWARE OR HARDWARE PIN
- BASS AND TREBLE CONTROL
- FOUR SPEAKER ATTENUATORS
  - FOUR INDEPENDENT SPEAKERS CONTROL IN 1.25dB STEPS FOR BALANCE AND FADER FACILITIES
  - INDEPENDENT MUTE FUNCTION
- ALL FUNCTIONS PROGRAMMABLE VIA SERIAL I^2 CBUS



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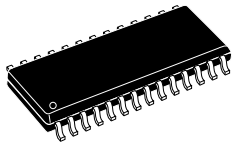


SO28

ORDERING NUMBER: TDA7343 (DIP28)
TDA7343D (SO28)

DESCRIPTION

The TDA7343 is an upgrade of the TDA7313 audioprocessor.

Thanks to the used BIPOLAR/CMOS technology, very low distortion, low noise and DC-stepping are obtained.

Due to a highly linear signal processing, using CMOS-switching techniques instead of standard bipolar multipliers, very low distortion and very low noise are obtained Several new features like softmute, zero-crossing mute and pause detector are implemented.

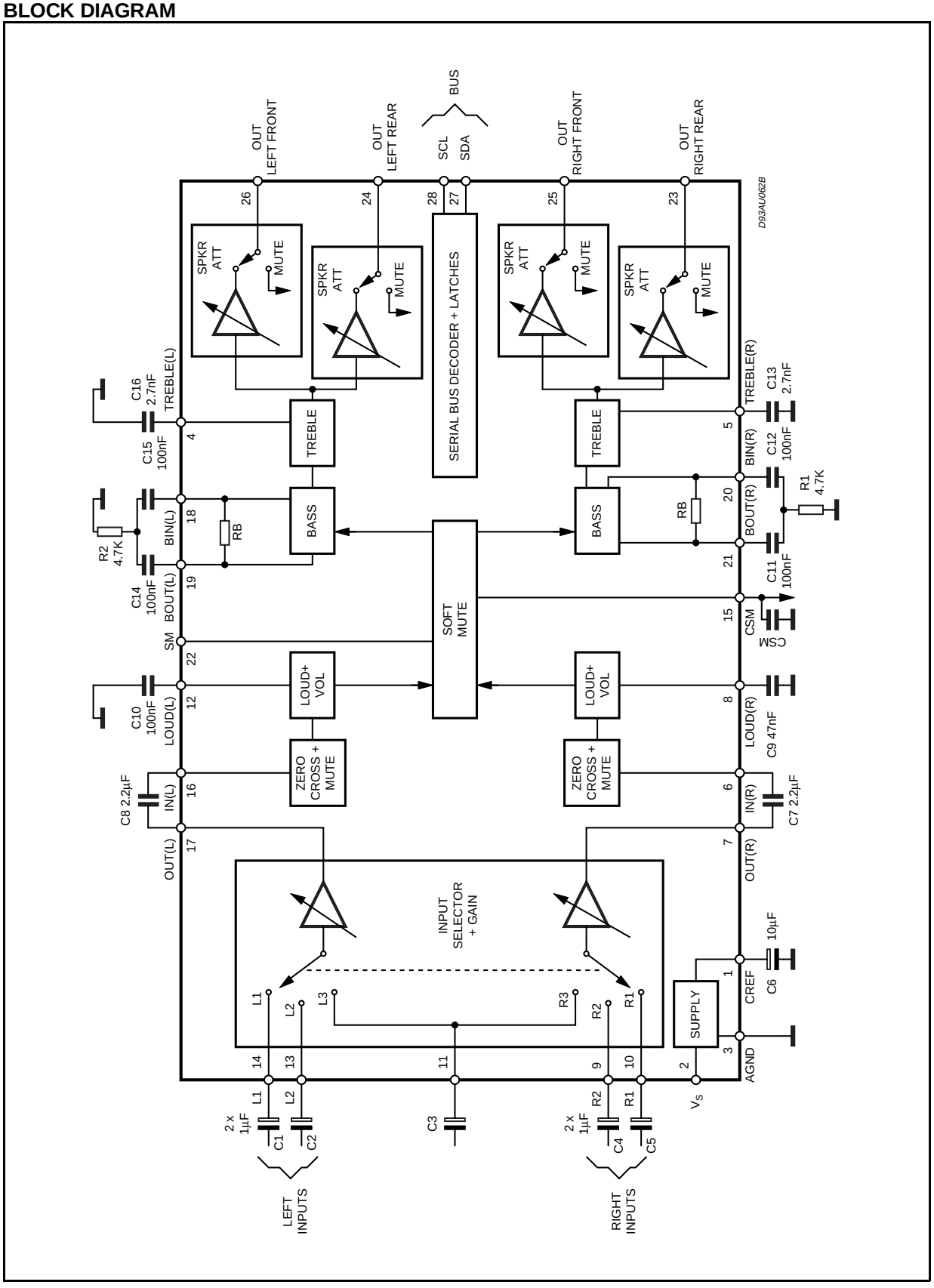
The Soft Mute function can be activated in two ways:

1 Via serial bus (bit D0, Mute Byte)

2 Directly on pin 22 through an I/O line of the microcontroller

Very low DC stepping is obtained by use of a BICMOS technology.

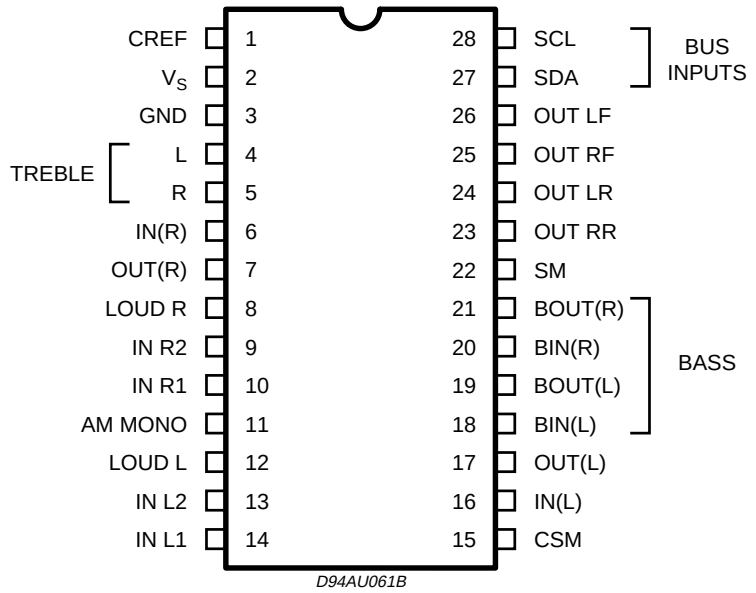
BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_S	Operating Supply Voltage	10.5	V
T_{amb}	Operating Ambient Temperature	-40 to 85	°C
T_{stg}	Storage Temperature Range	-55 to 150	°C

PIN CONNECTION



D94AU061B

THERMAL DATA

Symbol	Parameter	DIP28	SO28	Unit
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-pins	85	65	°C/W

QUICK REFERENCE DATA

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_S	Supply Voltage	6	9	10.2	V
V_{CL}	Max. input signal handling	2.1	2.6		Vrms
THD	Total Harmonic Distortion V = 1Vrms f = 1KHz		0.01	0.08	%
S/N	Signal to Noise Ratio		106		dB
S_C	Channel Separation f = 1KHz		100		dB
	Volume Control 0.3dB step	-59.7		20	dB
	Treble Control 2dB step	-14		+14	dB
	Bass Control 2dB step	-10		+18	dB
	Fader and Balance Control 1.25dB step	-38.75		0	dB
	Input Gain 3.75dB step	0		11.25	dB
	Mute Attenuation		100		dB

ELECTRICAL CHARACTERISTICS (V_S = 9V; R_L = 10KΩ; R_g = 50Ω; T_{amb} = 25°C; all controls flat (G - 0dB); f = 1KHz. Refer to the test circuit, unless otherwise specified.)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
INPUT SELECTOR						
R_I	Input Resistance		70	100	130	KΩ
V_{CL}	Clipping Level	d ≤ 0.3%	2.1	2.6		V_{RMS}
S_I	Input Separation		80	100		dB
R_L	Output Load Resistance		2			KΩ
$G_{I\ MIN}$	Minimum Input Gain		-0.75	0	0.75	dB
$G_{I\ MAX}$	Maximum Input Gain		10.25	11.25	12.25	dB
G_{step}	Step Resolution		2.75	3.75	4.75	dB
e_N	Input Noise	20Hz to 20 KHz unweighted		2.3		µV
V_{DC}	DC Steps	Adiacent Gain Steps		1.5	10	mV
		G_{IMIN} to G_{IMAX}		3		mV
VOLUME CONTROL						
R_I	Input Resistance		35	50		KΩ
G_{MAX}	Maximum Gain		18.75	20	21.25	dB
A_{MAX}	Maximum Attenuation		57.7	59.7	62.7	dB
A_{STEPC}	Step Resolution Coarse Attenuation		0.5	1.25	2.0	dB
A_{STEPF}	Step Resolution Fine Attenuation		0.11	0.31	0.51	dB
E_A	Attenuation Set Error	G = 20 to -20dB	-1.25	0	1.25	dB
		G = -20 to -58dB	-3		2	dB
E_t	Tracking Error				2	dB
V_{DC}	DC Steps	Adiacent Attenuation Steps	-3	0	3	mV
		From 0dB to A_{MAX}		0.5	5	mV
LOUDNESS CONTROL						
R_I	Internal Resistor	Loud = ON	35	50	65	KΩ
A_{MAX}	Maximum Attenuation		17.5	18.75	20.0	dB
A_{step}	Step Resolution		0.5	1.25	2.0	dB
ZERO CROSSING MUTE						
V_{TH}	Zero Crossing Threshold (note 1)	WIN = 11		20		mV
		WIN = 10		40		mV
		WIN = 01		80		mV
		WIN = 00		160		mV
A_{MUTE}	Mute Attenuation		80	100		dB
V_{DC}	DC Step	0dB to Mute		0	3	mV
SOFT MUTE						
A_{MUTE}	Mute Attenuation			60		dB
T_{DON}	ON Delay Time	C_{CSM} = 22nF; 0 to -20dB; I = I_{MAX}	0.7	1	1.7	ms
		C_{CSM} = 22nF; 0 to -20dB; I = I_{MIN}	20	35	55	ms
T_{DOFF}	OFF Delay Time	V_{CSM} = 0V; I = I_{MAX}	25	50	75	µA
		V_{CSM} = 0V; I = I_{MIN}		1		µA
V_{THSM}	Soft Mute Threshold		1.5	2.5	3.5	V
R_{INT}	Pullup Resistor (pin 22)	(note 2)	35	50	65	KΩ
V_{SMH}	(pin 22) Level High	Soft Mute Active	3.5			V
V_{SML}	(pin 22) Level Low				1	V

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
BASS CONTROL						
B_{BOOST}	Max Bass Boost		15	18	20	dB
B_{CUT}	Max Bass Cut		-8.5	-10	-11.5	dB
A_{step}	Step Resolution		1	2	3	dB
R_g	Internal Feedback Resistance		45	65	85	KΩ
TREBLE CONTROL						
C_{RANGE}	Control Range		±13	±14	±15	dB
A_{step}	Step Resolution		1	2	3	dB
SPEAKER ATTENUATORS						
C_{RANGE}	Control Range		35	37.5	40	dB
A_{step}	Step Resolution		0.5	1.25	2.0	dB
A_{MUTE}	Output Mute Attenuation	Data Word = XXX11111	80	100		dB
E_A	Attenuation Set Error				1.25	dB
V_{DC}	DC Steps	Adjacent Attenuation Steps		0	3	mV
AUDIO OUTPUT						
V_{clip}	Clipping Level	d = 0.3%	2.1	2.6		Vrms
R_L	Output Load Resistance		2			KΩ
R_O	Output Impedance			30	100	Ω
V_{DC}	DC Voltage Level		3.5	3.8	4.1	V
GENERAL						
V_{CC}	Supply Voltage		6	9	10.2	V
I_{CC}	Supply Current		5	10	15	mA
PSRR	Power Supply Rejection Ratio	f = 1KHz	60	80		dB
		B = 20 to 20kHz "A" weighted		65		dB
e_{NO}	Output Noise	Output Muted (B = 20 to 20kHz flat)		2.5		µV
		All Gains 0dB (B = 20 to 20kHz flat)		5	15	µV
E_t	Total Tracking Error	A_V = 0 to -20dB		0	1	dB
		A_V = -20 to -60dB		0	2	dB
S/N	Signal to Noise Ratio	All Gains = 0dB; $V_O = 1V_{rms}$		106		dB
S_C	Channel Separation		80	100		dB
d	Distortion	V_{in} = 1V		0.01	0.08	%
BUS INPUTS						
V_{IL}	Input Low Voltage				1	V
V_{IN}	Input High Voltage		3			V
I_{IN}	Input Current	VIN = 0.4V	-5		5	µA
V_O	Output Voltage SDA Acknowledge	I_O = 1.6mA		0.4	0.8	V

Note 1: WIN represents the MUTE programming bit pair D_6, D_5 for the zero crossing window threshold
Note 2: Internal pullup resistor to Vs/2; "LOW" = softmute active

I²C BUS INTERFACE

Data transmission from microprocessor to the TDA7343 and viceversa takes place thru the 2 wires I²C BUS interface, consisting of the two lines SDA and SCL (pull-up resistors to positive supply voltage must be externally connected).

Data Validity

As shown in fig. 3, the data on the SDA line must be stable during the high period of the clock. The HIGH and LOW state of the data line can only change when the clock signal on the SCL line is LOW.

Start and Stop Conditions

As shown in fig.4 a start condition is a HIGH to LOW transition of the SDA line while SCL is HIGH. The stop condition is a LOW to HIGH transition of the SDA line while SCL is HIGH.

A STOP conditions must be sent before each START condition.

Byte Format

Every byte transferred to the SDA line must contain 8 bits. Each byte must be followed by an acknowledge bit. The MSB is transferred first.

Acknowledge

The master (µP) puts a resistive HIGH level on the SDA line during the acknowledge clock pulse (see fig. 5). The peripheral (audioprocessor) that acknowledges has to pull-down (LOW) the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during this clock pulse.

The audioprocessor which has been addressed has to generate an acknowledge after the reception of each byte, otherwise the SDA line remains at the HIGH level during the ninth clock pulse time. In this case the master transmitter can generate the STOP information in order to abort the transfer.

Transmission without Acknowledge

Avoiding to detect the acknowledge of the audioprocessor, the µP can use a simplier transmission: simply it waits one clock without checking the slave acknowledging, and sends the new data.

This approach of course is less protected from misworking and decreases the noise immunity.

Figure 3: Data Validity on the I²CBUS

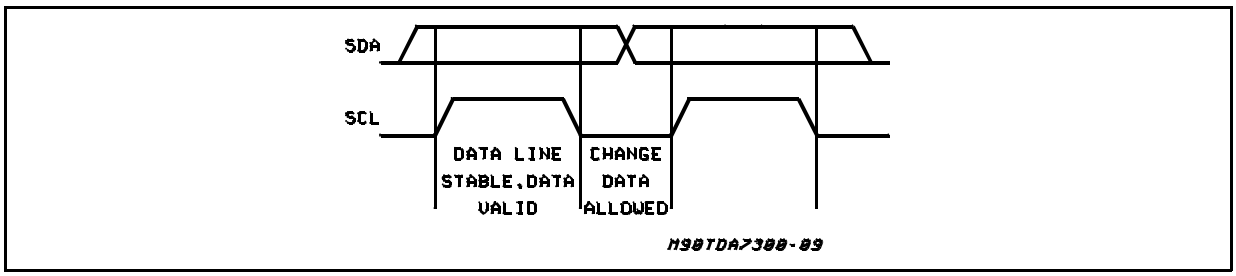


Figure 4: Timing Diagram of I²CBUS

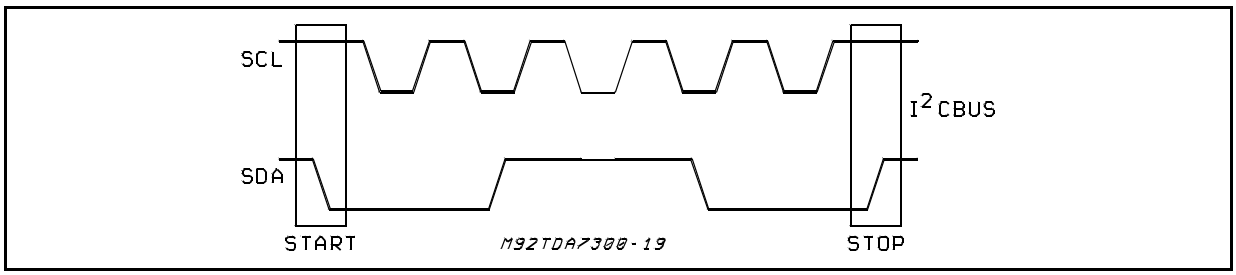
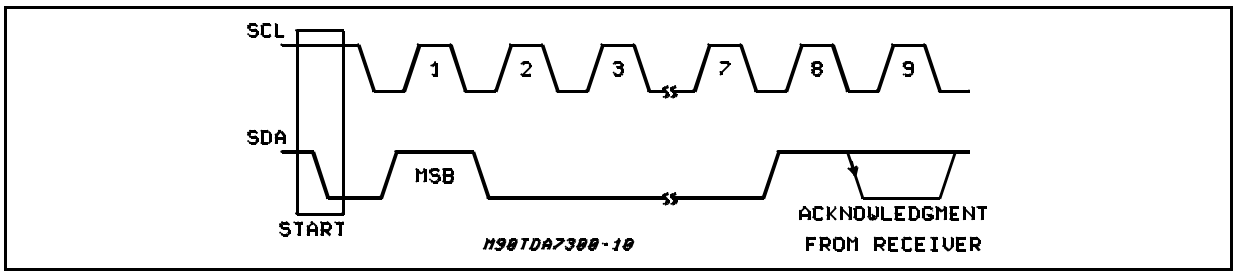


Figure 5: Acknowledge on the I²CBUS

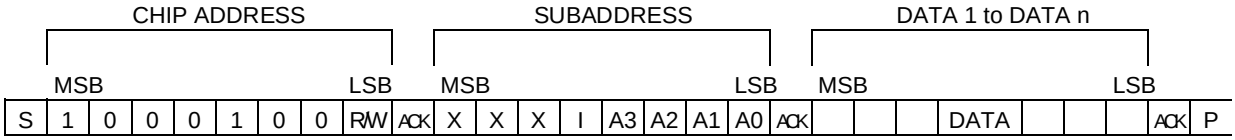


SOFTWARE SPECIFICATION

Interface Protocol

The interface protocol comprises:

- A start condition (s)
- A chip address byte,(the LSB bit determines read/write transmission)
- A subaddress byte.
- A sequence of data (N-bytes + acknowledge)
- A stop condition (P)



ACK = Acknowledge
S = Start
P = Stop
I = Auto Increment
X = Not used

MAX CLOCK SPEED 500kbits/s

AUTO INCREMENT

If bit I in the subaddress byte is set to "1", the autoincrement of the subaddress is enabled

SUBADDRESS (receive mode)

MSB							**LSB**	**FUNCTION**
X	X	X	I	A3	A2	A1	A0	
				0	0	0	0	Input Selector
				0	0	0	1	Loudness
				0	0	1	0	Volume
				0	0	1	1	Bass, Treble
				0	1	0	0	Speaker Attenuator LF
				0	1	0	1	Speaker Attenuator LR
				0	1	1	0	Speaker Attenuator RF
				0	1	1	1	Speaker Attenuator RR
				1	0	0	0	Mute

TRANSMITTED DATA

Send Mode

MSB							LSB
X	X	X	X	X	SM	ZM	X

ZM = Zero crossing muted (HIGH active)
SM = Soft mute activated (HIGH active)
X = Not used

The transmitted data is automatically updated after each ACK.
Transmission can be repeated without new chip address.

DATA BYTE SPECIFICATION

X = not relevant; set to "1" during testing

Input Selector

MSB							LSB	FUNCTION
D7	D6	D5	D4	D3	D2	D1	D0	
X	X	1			0	0	0	not used
X	X	1			0	0	1	IN 2
X	X	1			0	1	0	IN 1
X	X	1			0	1	1	AM mono
X	X	1			1	0	0	not used
X	X	1			1	0	1	not used
X	X	1			1	1	0	not allowed
X	X	1			1	1	1	not allowed
X	X	1	0	0				11.25dB gain
X	X	1	0	1				7.5dB gain
X	X	1	1	0				3.75dB gain
X	X	1	1	1				0dB gain

For example to select the IN 2 input with a gain of 7.5dB the Data Byte is: X X 1 0 1 0 0 1

Loudness

MSB							LSB	FUNCTION
D7	D6	D5	D4	D3	D2	D1	D0	
X	X	X	0	0	0	0	0	0dB
X	X	X	0	0	0	0	1	-1.25dB
X	X	X	0	0	0	1	0	-2.5dB
X	X	X	0	0	0	1	1	-3.75dB
X	X	X	0	0	1	0	0	-5dB
X	X	X	0	0	1	0	1	-6.25dB
X	X	X	0	0	1	1	0	-7.5dB
X	X	X	0	0	1	1	1	-8.75dB
X	X	X	0	1	0	0	0	-10dB
X	X	X	0	1	0	0	1	-11.25dB
X	X	X	0	1	0	1	0	-12.5dB
X	X	X	0	1	0	1	1	-13.75dB
X	X	X	0	1	1	0	0	-15dB
X	X	X	0	1	1	0	1	-16.25dB
X	X	X	0	1	1	1	0	-17.5dB
X	X	X	0	1	1	1	1	-18.75dB
X	X	X	1	D3	D2	D1	D0	Loudness OFF (1)

For example to select -17.5dB attenuation, loudness OFF, the Data Byte is: X X X1 1 1 1 0

NOTE 1:
If the loudness is switched OFF, the loudness stage is acting like a volume attenuator with flat frequency response. D0 to D3 determine the attenuation level.

Mute

MSB							LSB	FUNCTION
D7	D6	D5	D4	D3	D2	D1	D0	
							1	Soft Mute On
						0	1	Soft Mute with fast slope ($I = I_{MAX}$)
						1	1	Soft Mute with slow slope ($I = I_{MIN}$)
				1				Direct Mute
			0		1			Zero Crossing Mute On
			0		0			Zero Crossing Mute Off (delayed until next zerocrossing)
			1					Zero Crossing Mute and Pause Detector Reset
	0	0						160mV ZC Window Threshold (WIN = 00)
	0	1						80mV ZC Window Threshold (WIN = 01)
	1	0						40mV ZC Window Threshold (WIN = 10)
	1	1						20mV ZC Window Threshold (WIN = 11)
0								Nonsymmetrical Bass Cut (note 4)
1								Symmetrical Bass Cut

An additional direct mute function is included in the Speaker Attenuators.

Note 4: Bass cut for very low frequencies; should not be used at +16 and +18dB bass boost (DC gain)

Speaker Attenuators

MSB							LSB	SPEAKER ATTENUATOR LF, LR, RF, RR
D7	D6	D5	D4	D3	D2	D1	D0	
								1.25dB step
X	X	X			0	0	0	0dB
X	X	X			0	0	1	-1.25dB
X	X	X			0	1	0	-2.5dB
X	X	X			0	1	1	-3.75dB
X	X	X			1	0	0	-5dB
X	X	X			1	0	1	-6.25dB
X	X	X			1	1	0	-7.5dB
X	X	X			1	1	1	-8.75dB
								10dB step
X	X	X	0	0				0dB
X	X	X	0	1				-10dB
X	X	X	1	0				-20dB
X	X	X	1	1				-30dB
X	X	X	1	1	1	1	1	Speaker Mute

For example an attenuation of 25dB on a selected output is given by: X X X1 0 1 0 0

Bass/Treble

MSB							LSB	FUNCTION
D7	D6	D5	D4	D3	D2	D1	D0	
								TREBLE STEP
				0	0	0	0	-14dB
				0	0	0	1	-12dB
				0	0	1	0	-10dB
				0	0	1	1	-8dB
				0	1	0	0	-6dB
				0	1	0	1	-4dB
				0	1	1	0	-2dB
				0	1	1	1	0dB
				1	1	1	1	0dB
				1	1	1	0	2dB
				1	1	0	1	4dB
				1	1	0	0	6dB
				1	0	1	1	8dB
				1	0	1	0	10dB
				1	0	0	1	12dB
				1	0	0	0	14dB
								BASS STEPS
0	0	1	0					-10dB
0	0	1	1					-8dB
0	1	0	0					-6dB
0	1	0	1					-4dB
0	1	1	0					-2dB
0	1	1	1					-0dB
1	1	1	1					-0dB
1	1	1	0					2dB
1	1	0	1					4dB
1	1	0	0					6dB
1	0	1	1					8dB
1	0	1	0					10dB
1	0	0	1					12dB
1	0	0	0					14dB
0	0	0	1					146B
0	0	0	0					18dB

For example 12dB Treble and -8dB Bass give the following DATA BYTE: 0 0 1 1 1 0 0 1

Volume

MSB							LSB	FUNCTION
D7	D6	D5	D4	D3	D2	D1	D0	
								0.31dB Fine Attenuation Steps
						0	0	0dB
						0	1	-0.31dB
						1	0	-0.62dB
						1	1	-0.94dB
								1.25dB Coarse Attenuation Steps
			0	0	0			0dB
			0	0	1			-1.25dB
			0	1	0			-2.5dB
			0	1	1			-3.75dB
			1	0	0			-5dB
			1	0	1			-6.25dB
			1	1	0			-7.5dB
			1	1	1			-8.75dB
								10dB Gain / Attenuation Steps
0	0	0						20dB
0	0	1						10dB
0	1	0						0dB
0	1	1						-10dB
1	0	0						-20dB
1	0	1						-30dB
1	1	0						-40dB
1	1	1						-50dB

For example to select -47.81dB Volume the Data Byte is: 1 1 0 1 1 0 0 1

Power on RESET: All Bytes Set to 1 1 1 1 1 1 1 0

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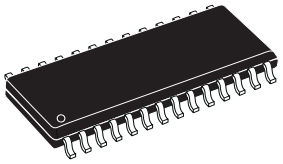
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			2.65			0.104
a1	0.1		0.3	0.004		0.012
b	0.35		0.49	0.014		0.019
b1	0.23		0.32	0.009		0.013
C		0.5			0.020	
c1	45° (typ.)					
D	17.7		18.1	0.697		0.713
E	10		10.65	0.394		0.419
e		1.27			0.050	
e3		16.51			0.65	
F	7.4		7.6	0.291		0.299
L	0.4		1.27	0.016		0.050
S	8 ° (max.)					

OUTLINE AND MECHANICAL DATA



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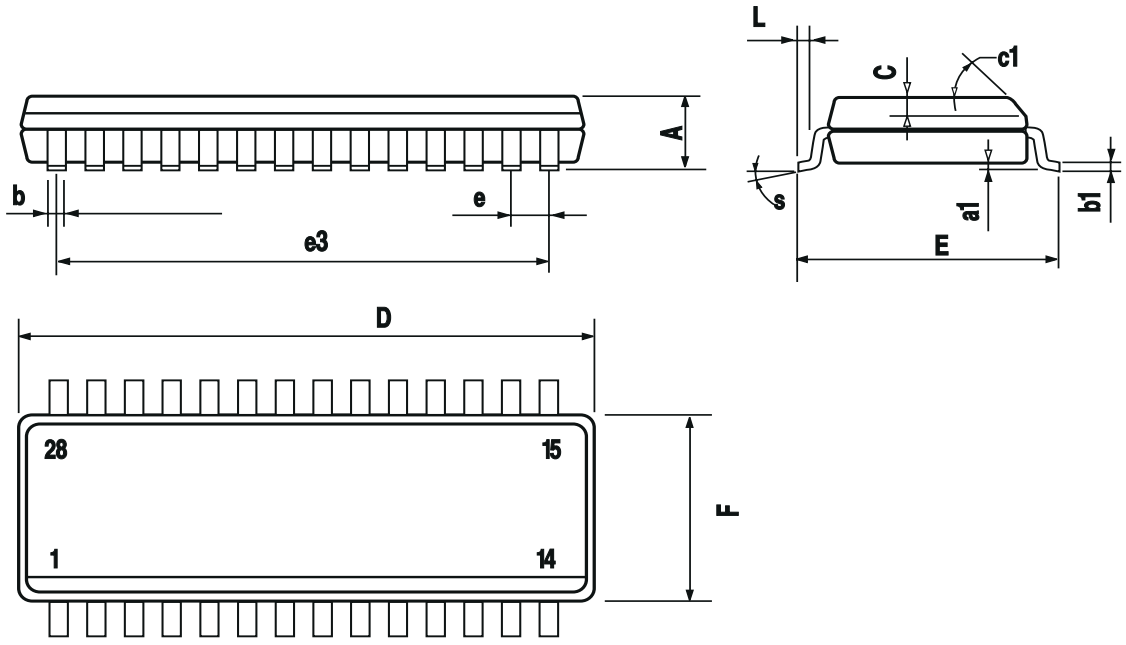
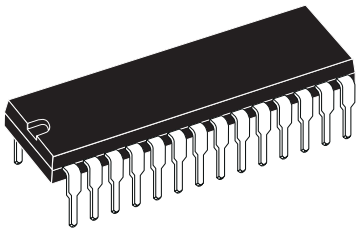


DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1		0.63			0.025	
b		0.45			0.018	
b1	0.23		0.31	0.009		0.012
b2		1.27			0.050	
D			37.34			1.470
E	15.2		16.68	0.598		0.657
e		2.54			0.100	
e3		33.02			1.300	
F			14.1			0.555
I		4.445			0.175	
L		3.3			0.130	

OUTLINE AND MECHANICAL DATA



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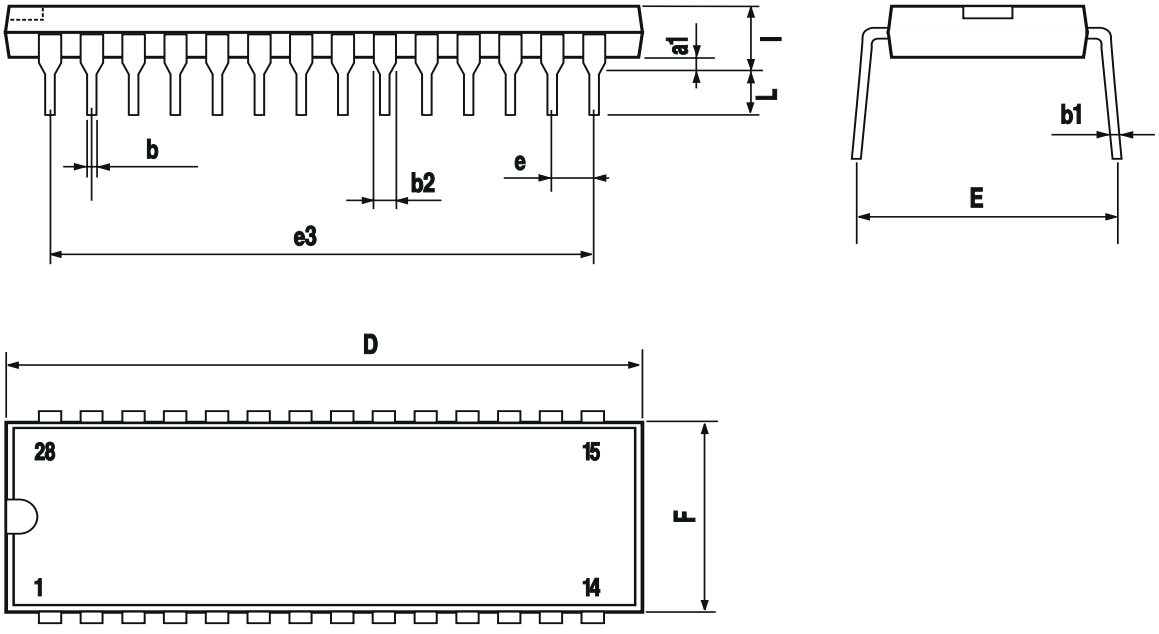

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