Complementary 20-V (D-S) MOSFET

PRODUCT SUMMARY			
	V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
N-Channel	20	0.040 @ V_{GS} = 4.5 V	5.9
		0.045 @ V_{GS} = 2.5 V	5.6
		0.052 @ V_{GS} = 1.8 V	5.2
P-Channel	–20	0.086 @ V_{GS} = –4.5 V	–4.1
		0.121 @ V_{GS} = –2.5 V	–3.4
		0.171 @ V_{GS} = –1.8 V	–2.9

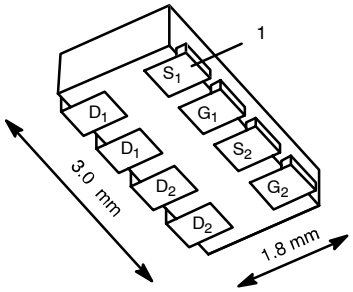
FEATURES

- TrenchFET® Power MOSFETS
- Ultra Low $r_{DS(on)}$ and Excellent Power Handling In Compact Footprint

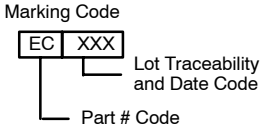
APPLICATIONS

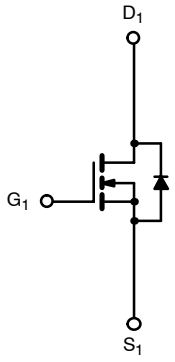
- Load Switching for Portable Devices

1206-8 ChipFET®

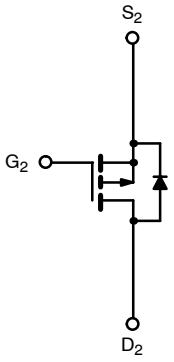


Bottom View





N-Channel MOSFET



P-Channel MOSFET

Ordering Information: Si5515DC-T1—E3

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C UNLESS OTHERWISE NOTED)							
Parameter		Symbol	N-Channel		P-Channel		Unit
			5 secs	Steady State	5 secs	Steady State	
Drain-Source Voltage		V_{DS}	20		–20		V
Gate-Source Voltage		V_{GS}	±8				
Continuous Drain Current (T_J = 150°C)[a]	T_A = 25°C	I_D	5.9	4.4	–4.1	–3	A
	T_A = 85°C		4.2	3.1	–2.9	–2.2	
Pulsed Drain Current		I_{DM}	20		–15		
Continuous Source Current (Diode Conduction)[a]		I_S	1.8	0.9	–1.8	–0.9	
Maximum Power Dissipation[a]	T_A = 25°C	P_D	2.1	1.1	2.1	1.1	W
	T_A = 85°C		1.1	0.6	1.1	0.6	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	–55 to 150				°C
Soldering Recommendations (Peak Temperature)[b, c]			260				

THERMAL RESISTANCE RATINGS					
Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient[a]	t ≤ 5 sec	R_{thJA}	50	60	°C/W
	Steady State		90	110	
Maximum Junction-to-Foot (Drain)	Steady State	R_{thJF}	30	40	

Notes
a. Surface Mounted on 1" x 1" FR4 Board.
b. See Reliability Manual for profile. The ChipFET is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
c. Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.

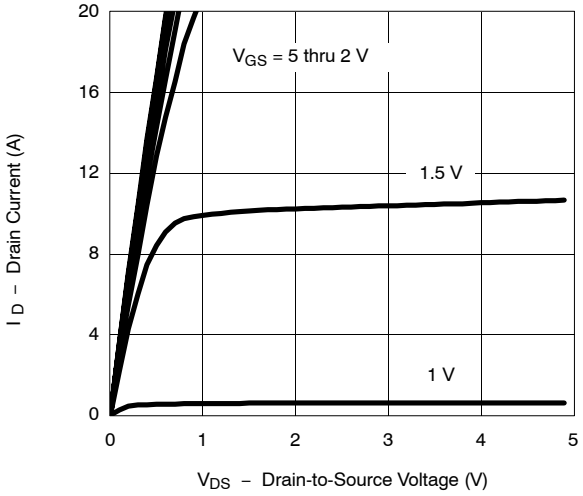
SPECIFICATIONS (T_J = 25°C UNLESS OTHERWISE NOTED)

Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
Static							
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 μA	N-Ch	0.4		1.0	V
		V_{DS} = V_{GS}, I_D = −250 μA	P-Ch	−0.4		−1.0	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±8 V	N-Ch			±100	nA
			P-Ch			±100	
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 20 V, V_{GS} = 0 V	N-Ch			1	μA
		V_{DS} = −20 V, V_{GS} = 0 V	P-Ch			−1	
		V_{DS} = 20 V, V_{GS} = 0 V, T_J = 85°C	N-Ch			5	
		V_{DS} = −20 V, V_{GS} = 0 V, T_J = 85°C	P-Ch			−5	
On-State Drain Current[a]	$I_{D(on)}$	V_{DS} ≥ 5 V, V_{GS} = 4.5 V	N-Ch	20			A
		V_{DS} ≤ −5 V, V_{GS} = −4.5 V	P-Ch	−15			
Drain-Source On-State Resistance[a]	$r_{DS(on)}$	V_{GS} = 4.5 V, I_D = 4.4 A	N-Ch		0.032	0.040	Ω
		V_{GS} = −4.5 V, I_D = −3.0 A	P-Ch		0.069	0.086	
		V_{GS} = 2.5 V, I_D = 4.1 A	N-Ch		0.036	0.045	
		V_{GS} = −2.5 V, I_D = −2.5 A	P-Ch		0.097	0.121	
		V_{GS} = 1.8 V, I_D = 1.9 A	N-Ch		0.042	0.052	
		V_{GS} = −1.8 V, I_D = −0.6 A	P-Ch		0.137	0.171	
Forward Transconductance[a]	g_{fs}	V_{DS} = 10 V, I_D = 4.4 A	N-Ch		22		S
		V_{DS} = −10 V, I_D = −3 A	P-Ch		8		
Diode Forward Voltage[a]	V_{SD}	I_S = 0.9 A, V_{GS} = 0 V	N-Ch		0.8	1.2	V
		I_S = −0.9 A, V_{GS} = 0 V	P-Ch		−0.8	−1.2	
Dynamic[b]							
Total Gate Charge	Q_g	N-Channel V_{DS} = 10 V, V_{GS} = 4.5 V, I_D = 4.4 A P-Channel V_{DS} = −10 V, V_{GS} = −4.5 V, I_D = −3 A	N-Ch		5	7.5	nC
			P-Ch		5.5	8.5	
Gate-Source Charge	Q_{gs}		N-Ch		0.85		
			P-Ch		0.91		
Gate-Drain Charge	Q_{gd}		N-Ch		1		
			P-Ch		1.6		
Turn-On Delay Time	$t_{d(on)}$	N-Channel V_{DD} = 10 V, R_L = 10 Ω I_D ≅ 1 A, V_{GEN} = 4.5 V, R_G = 6 Ω P-Channel V_{DD} = −10 V, R_L = 10 Ω I_D ≅ −1 A, V_{GEN} = −4.5 V, R_G = 6 Ω	N-Ch		20	30	ns
			P-Ch		18	30	
Rise Time	t_r		N-Ch		36	55	
			P-Ch		32	50	
Turn-Off Delay Time	$t_{d(off)}$		N-Ch		30	45	
			P-Ch		42	65	
Fall Time	t_f		N-Ch		12	20	
			P-Ch		26	40	
Source-Drain Reverse Recovery Time	t_{rr}	I_F = 0.9 A, di/dt = 100 A/μs	N-Ch		45	90	
		I_F = −0.9 A, di/dt = 100 A/μs	P-Ch		30	60	

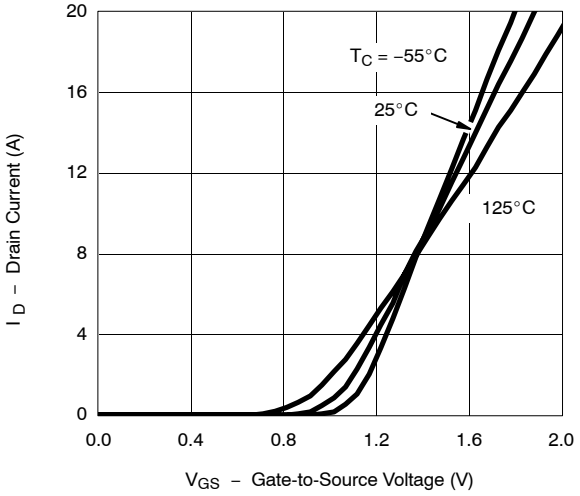
Notes
a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%,
b. Guaranteed by design, not subject to production testing.

TYPICAL CHARACTERISTICS (25°C UNLESS NOTED) N-CHANNEL

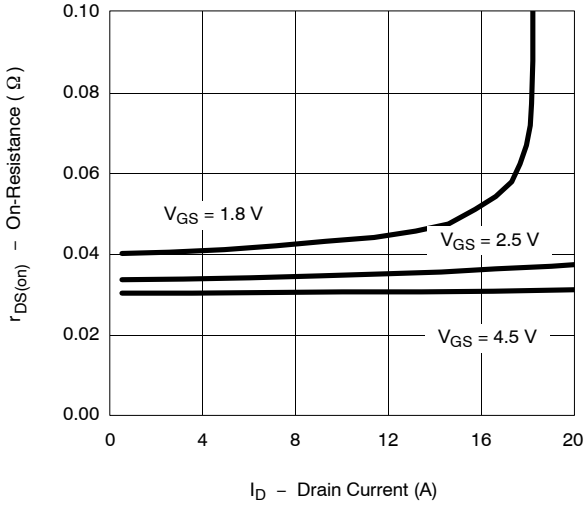
Output Characteristics



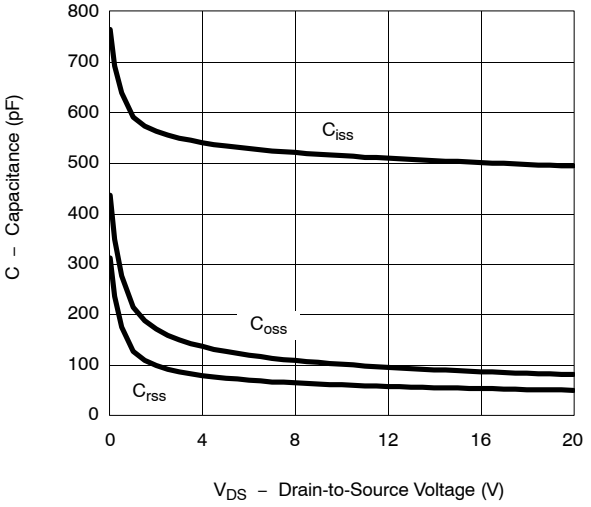
Transfer Characteristics



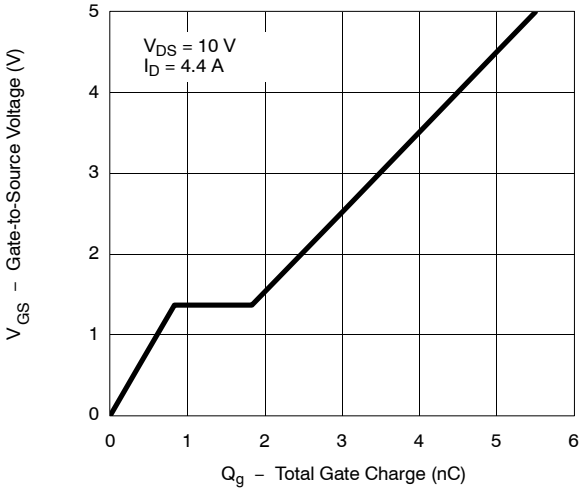
On-Resistance vs. Drain Current



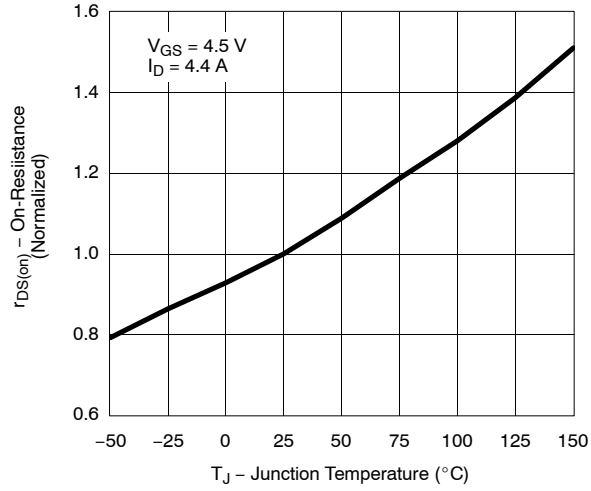
Capacitance



Gate Charge

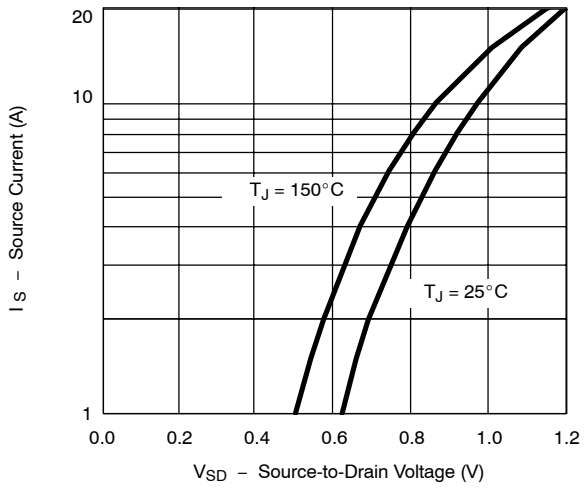


On-Resistance vs. Junction Temperature

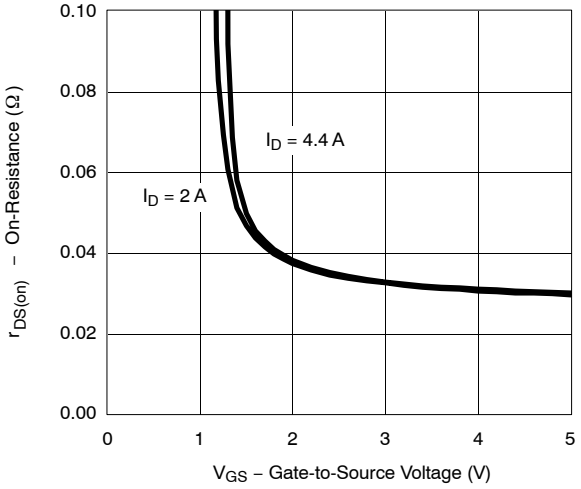


TYPICAL CHARACTERISTICS (25°C UNLESS NOTED) N-CHANNEL

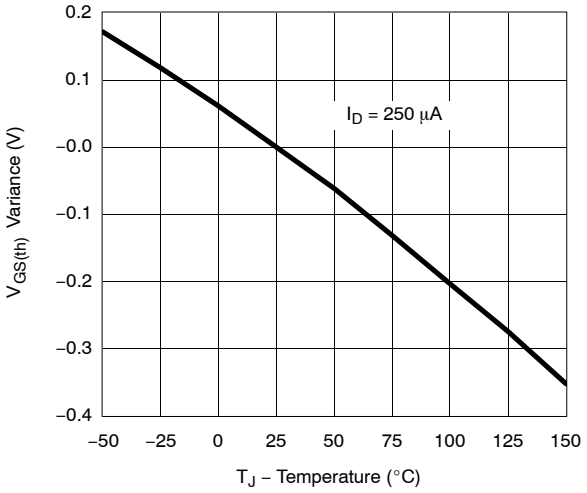
Source-Drain Diode Forward Voltage



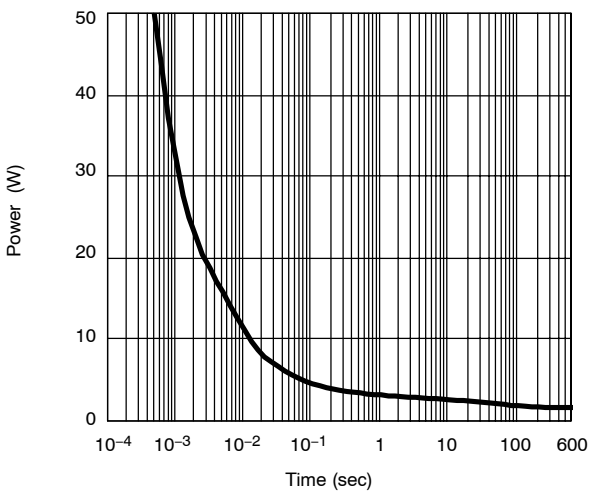
On-Resistance vs. Gate-to-Source Voltage



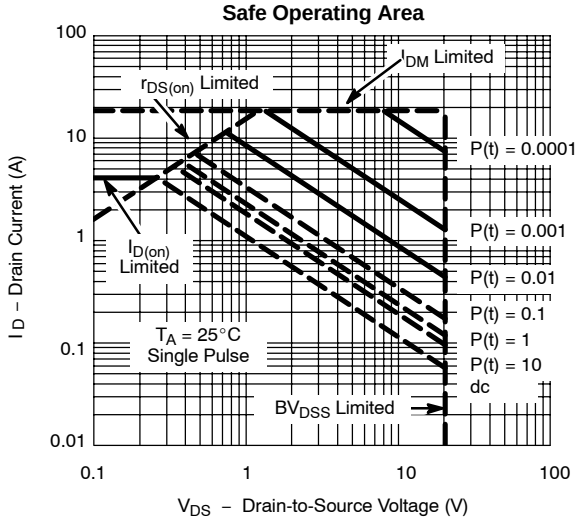
Threshold Voltage



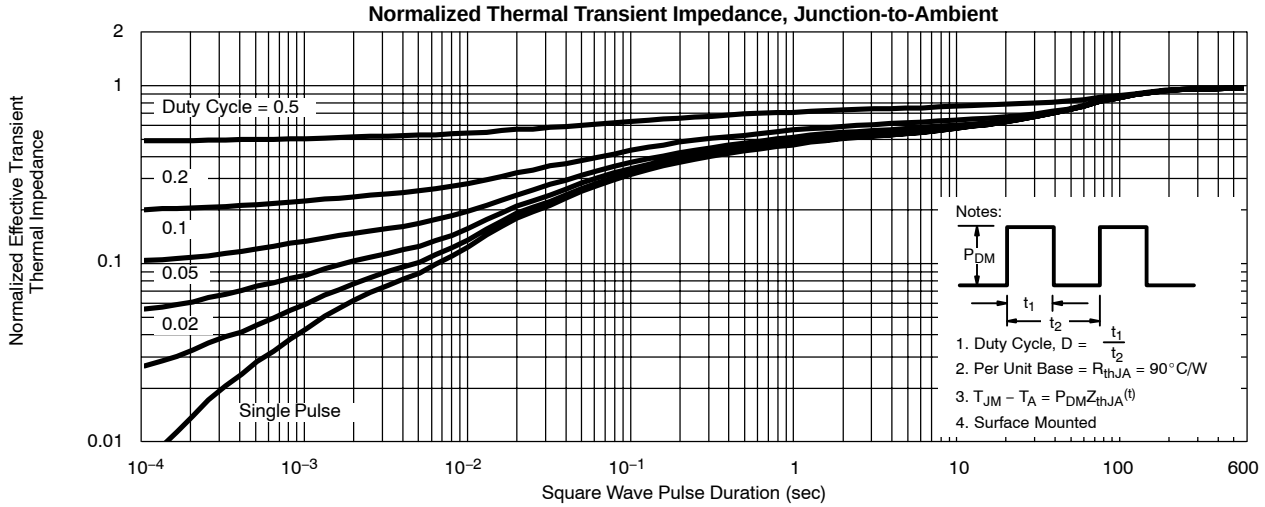
Single Pulse Power

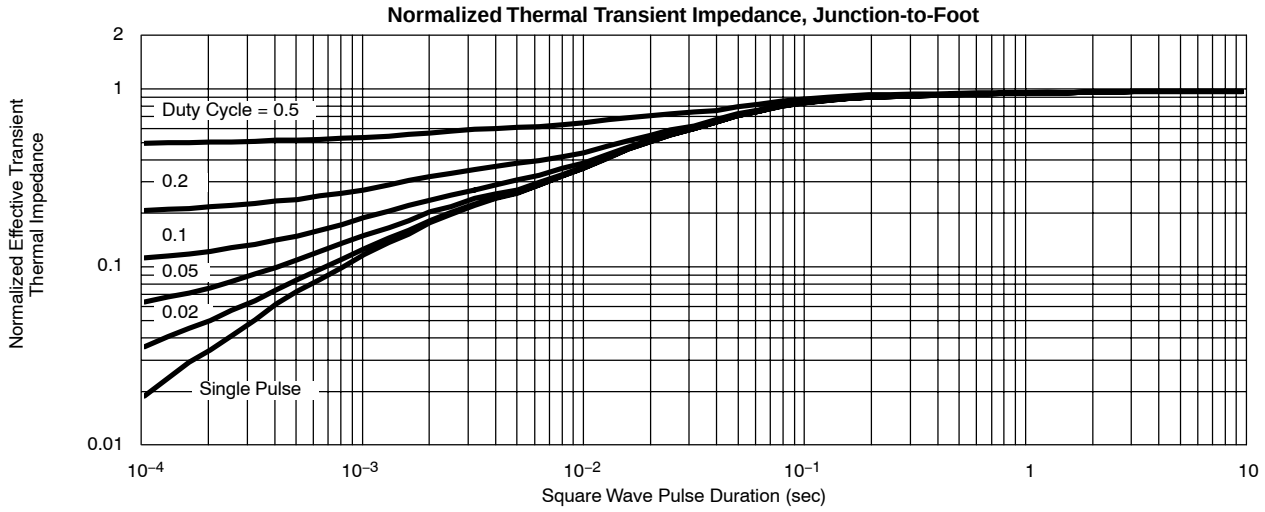


Safe Operating Area

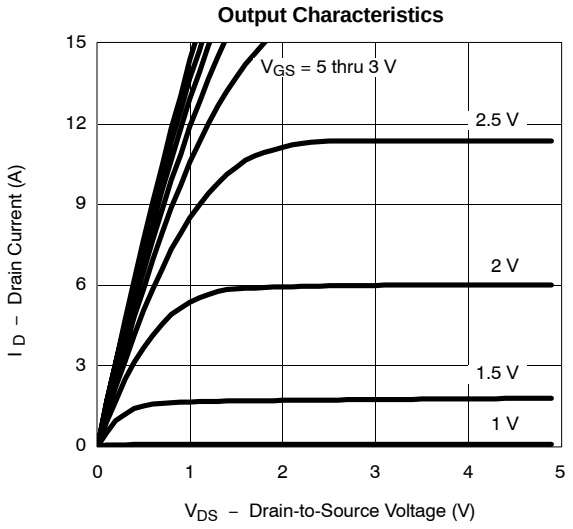


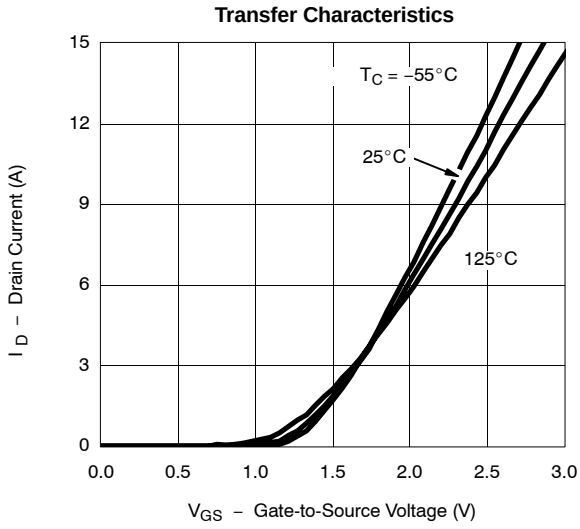
TYPICAL CHARACTERISTICS (25°C UNLESS NOTED) N-CHANNEL





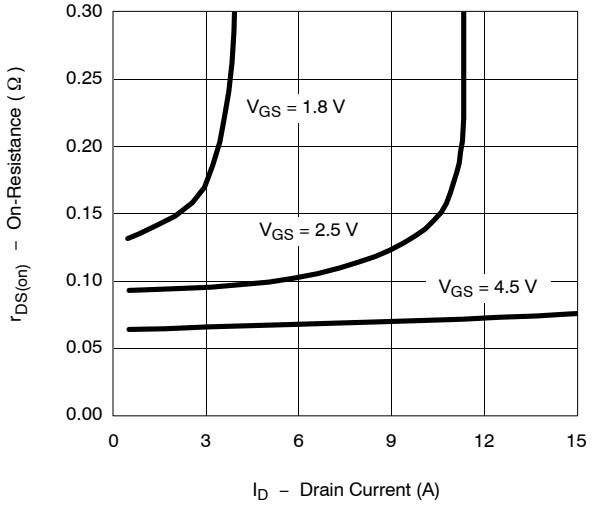
TYPICAL CHARACTERISTICS (25°C UNLESS NOTED) P-CHANNEL



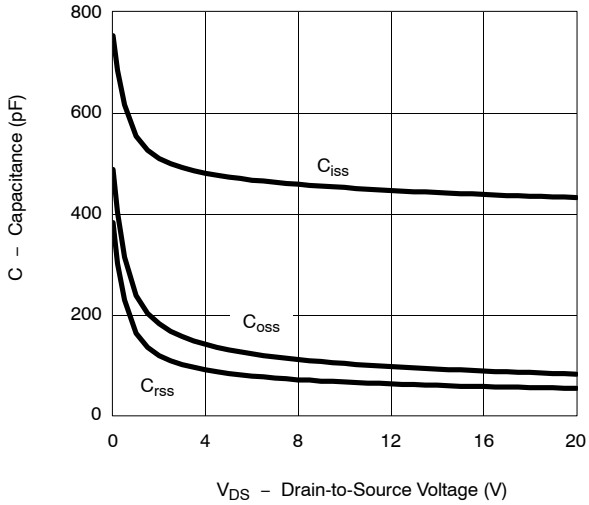


TYPICAL CHARACTERISTICS (25°C UNLESS NOTED) P-CHANNEL

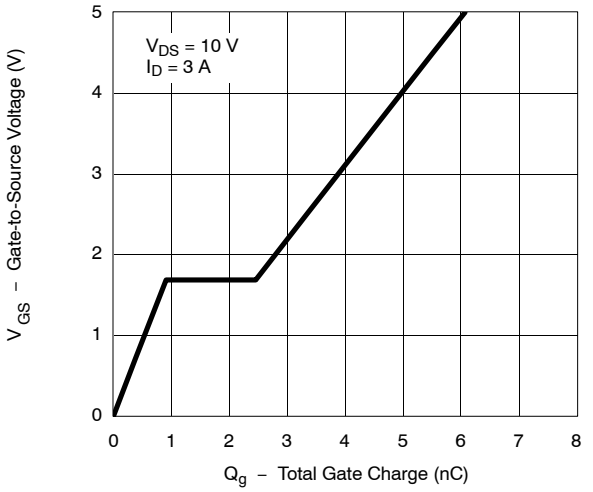
On-Resistance vs. Drain Current



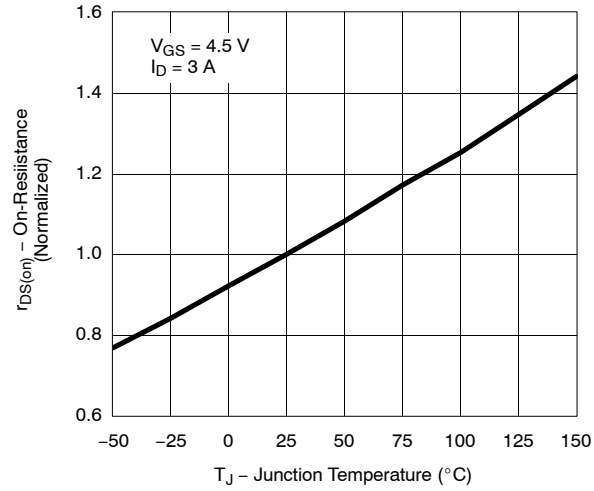
Capacitance



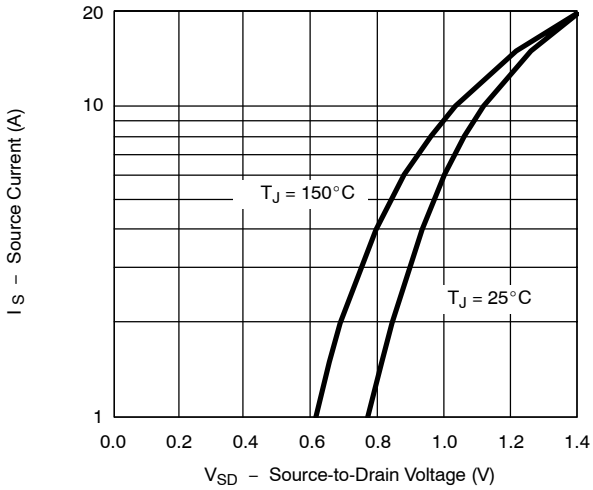
Gate Charge



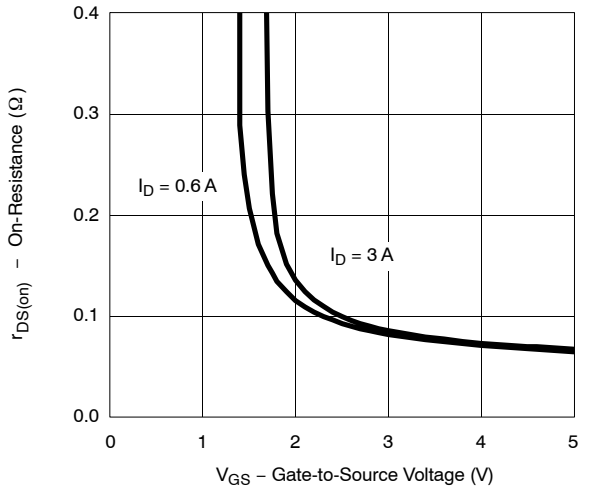
On-Resistance vs. Junction Temperature



Source-Drain Diode Forward Voltage

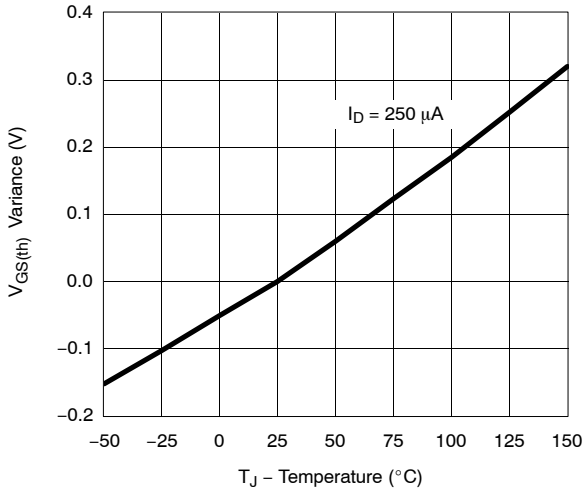


On-Resistance vs. Gate-to-Source Voltage

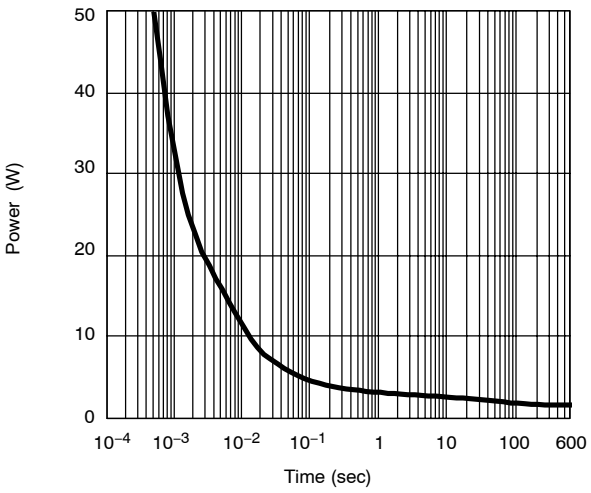


TYPICAL CHARACTERISTICS (25°C UNLESS NOTED) P-CHANNEL

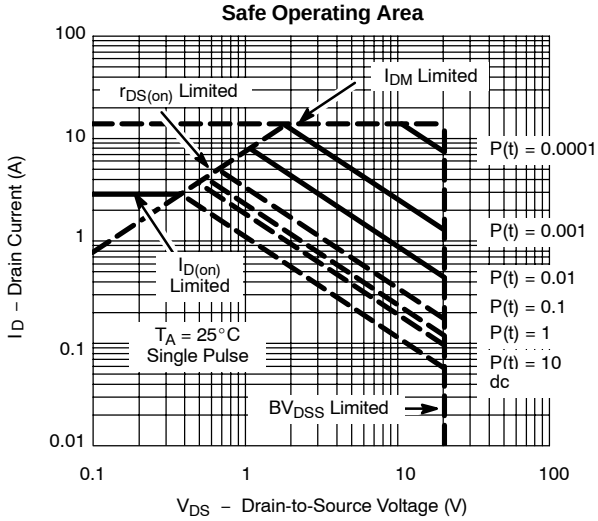
Threshold Voltage



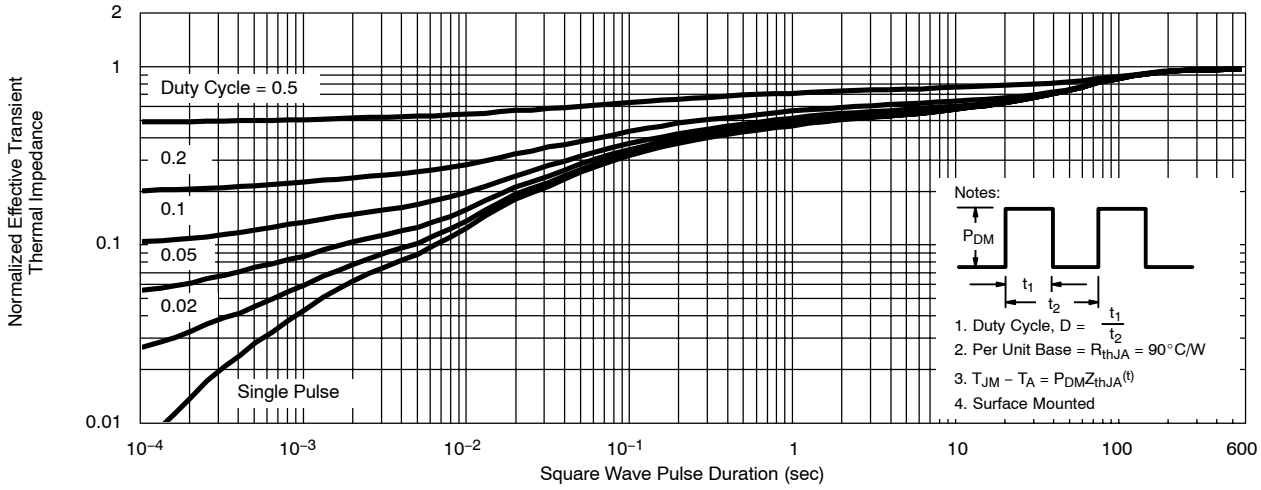
Single Pulse Power



Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Ambient



TYPICAL CHARACTERISTICS (25°C UNLESS NOTED) P-CHANNEL

Normalized Thermal Transient Impedance, Junction-to-Foot