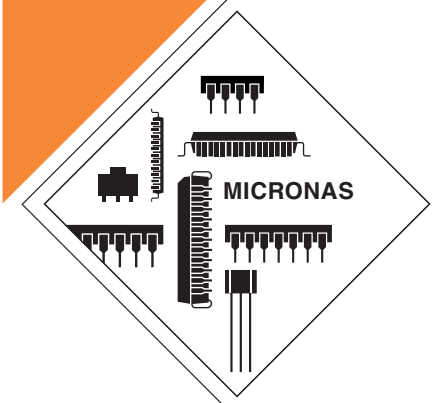

DATA SHEET

MAS 35x9F
MPEG Layer 2/3, AAC Audio Decoder, G.729 Annex A Codec

MICRONAS
BASS

June 30, 2004
6251-505-1DS

MICRONAS

Contents

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Contents, continued

MPEG Layer 2/3, AAC Audio Decoder, G.729 Annex A Codec

Release Note: Revision bars indicate significant changes to the previous edition. This data sheet applies to the MAS 35x9F version B4.

1. Introduction

The MAS 35x9F is a single-chip, low-power MPEG layer 2/3 and MPEG2-AAC audio stereo decoder. It also contains the G.729 Annex A speech compression and decompression technology for use in memory-based or broadcast applications. Additional functionality is achievable via download software (e.g., CELP voice decoder, Micronas SC4 (ADPCM) encoder/ decoder).

The MAS 35x9F decoding block accepts compressed digital data streams as serial bit streams or in parallel format, and provides serial PCM and S/PDIF output of decompressed audio. In addition to the signal processing function, the IC incorporates a high-performance stereo D/A converter, headphone amplifiers, a stereo A/D converter, a microphone amplifier, and two DC/DC converters.

Thus, the MAS 35x9F provides a true **"all-in-one"** solution that is ideally suited for highly optimized memory-based portable music players with integrated speech recording and playback function.

In MPEG 1 (ISO 11172-3), three hierarchical layers of compression have been standardized. The most sophisticated and complex, layer 3, allows compression rates of approximately 12:1 for mono and stereo signals while still maintaining CD audio quality. Layer 2 (widely used, e.g., in DVD) achieves a compression of 8:1 without significant losses in audio quality.

The MAS 35x9F supports the "Advanced Audio Coding" (AAC) that is defined as a part of MPEG 2. AAC provides compression rates up to 16:1. It defines several profiles for different applications. This IC decodes the "low complexity profile" that is especially optimized for portable applications.

The MAS 35x9F also implements a voice encoder and decoder that is compliant to the ITU Standard G.729 Annex A.

SC4 is a proprietary Micronas speech codec technology that can be downloaded to the MAS 35x9F, to allow recording and playing back speech at various sampling rates.

1.1. Features

Firmware

- MPEG 1/2 layer 2 and layer 3 decoder
- Extension to MPEG 2 layer 3 for low sampling rates (“MPEG 2.5”)
- Extraction of MPEG Ancillary Data
- MPEG 2 AAC decoder (low-complexity profile)
- Micronas G.729 Annex A speech compression and decompression
- Master or slave clock operation
- Adaptive bit rates (bit rate switching)
- Intelligent power management (processor clock is dependent on sampling frequencies)
- SDMI-compliant security technology
- Stereo channel mixer
- Bass, treble, and loudness function
- Micronas Bass (MB)
- Automatic Volume Control (AVC)

Interfaces

- Two serial asynchronous interfaces for bit streams and uncompressed digital audio
- Parallel handshake bit stream input
- Serial audio output via I^2S and related formats
- S/PDIF data input and output
- Controlling via I^2C interface

Hardware Features

- Two independent embedded DC/DC converters, (e.g., for DSP and flash RAM supply)
- Low DC/DC converter start-up voltage (0.9 V)
- DC converter efficiency up to 95%
- Battery voltage monitor
- Low supply voltage down to 2.2 V
- Low power dissipation, e.g., 87 mW (128kBit/s, 44.1 kHz, Headphone playback)
- High-performance RISC DSP core
- On-chip crystal oscillator
- Hardware power management and power-off functions
- Microphone amplifier
- Stereo A/D converter for FM/AM-radio and speech input
- CD quality stereo D/A converter
- Headphone amplifier
- Noise and power-optimized volume
- External clock or crystal frequency of 13...28 MHz
- Standby current < 10 µA

1.2. Features of the MAS 35x9F Family

Feature	3509	3519	3529	3539	3549	3559
Layer 3 Decoder	X	X	X	X		
G.729 Encoder/Decoder	X	X			X	
AAC Decoder	X		X			X

1.3. Application Overview

The following block diagram shows an example application for the MAS 35x9F in a portable audio player device. Besides a simple controller and the external flash memories, all required components are integrated in the MAS 35x9F. The MAS 35x9F supports both speech and radio quality audio encoding, as well as compressed-audio decoding tasks.

Fig. 1–1 depicts a portable power-optimized audio application. The two embedded DC/DC converters of the MAS 35x9F generate optimum power supply voltages for the DSP core and also for state-of-the art flash memories that typically require 2.7 to 3.3 V supply. The performance of the DC/DC converters reaches efficiencies of up to 95%.

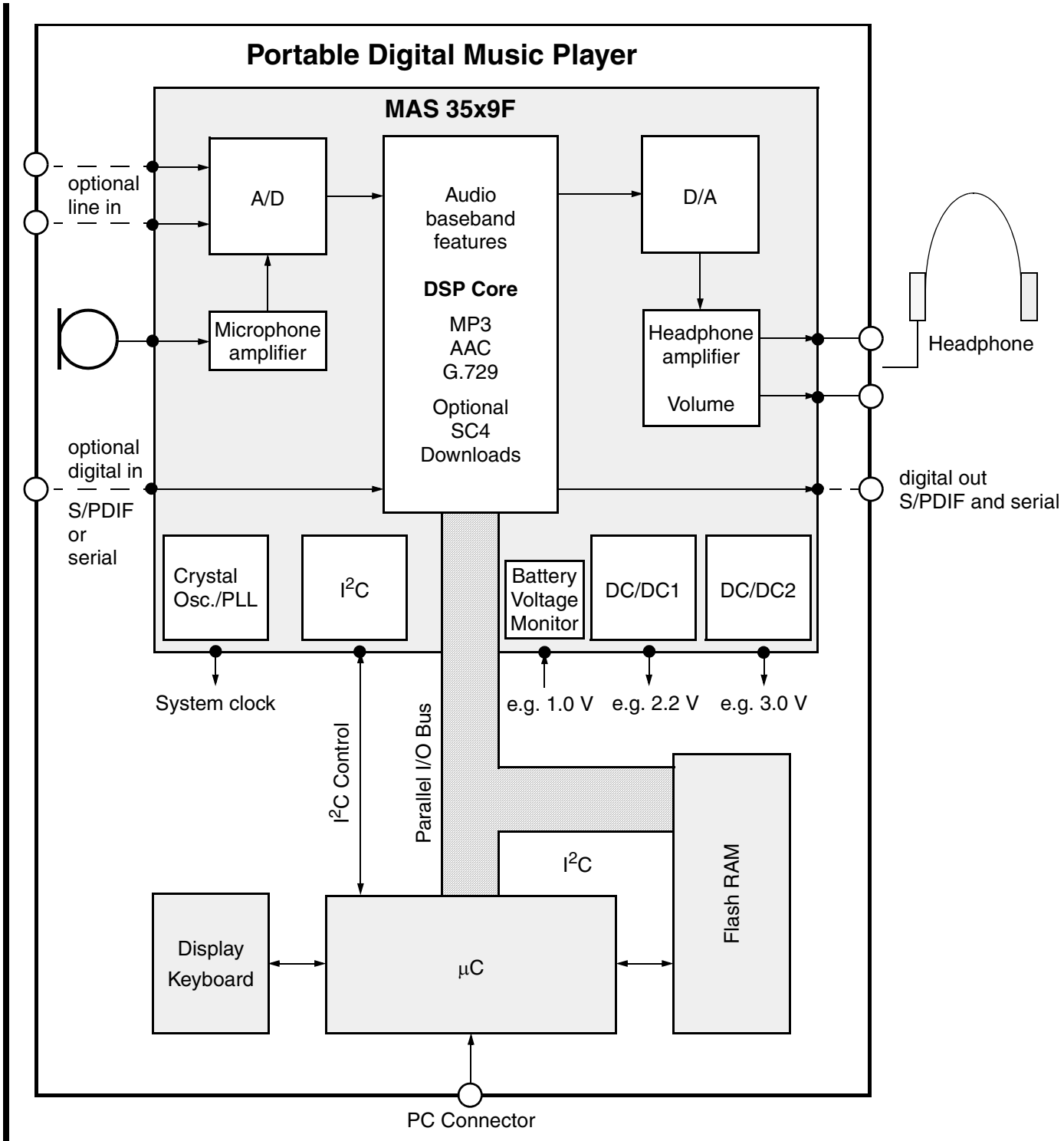


Fig. 1–1: Example of an application for the MAS 35x9F in a portable audio player device

2. Functional Description

2.1. Overview

The MAS 35x9F is intended for use in portable consumer audio applications. It receives parallel or serial data streams and decodes MPEG Layer 2 and 3 (including the low sampling frequency extensions) and MPEG 2 AAC. A low bit-rate speech codec, compliant to the ITU Standard G.729 Annex A, is integrated. Additional downloadable software modules (SDMI, other audio/speech encoders/decoders) are available on request.

2.2. Architecture of the MAS 35x9F

The hardware of the MAS 35x9F consists of a high-performance RISC Digital Signal Processor (DSP), and appropriate interfaces. A hardware overview of the IC is shown in Fig. 2–1.

2.3. DSP Core

The internal processor is a dedicated DSP for advanced audio applications.

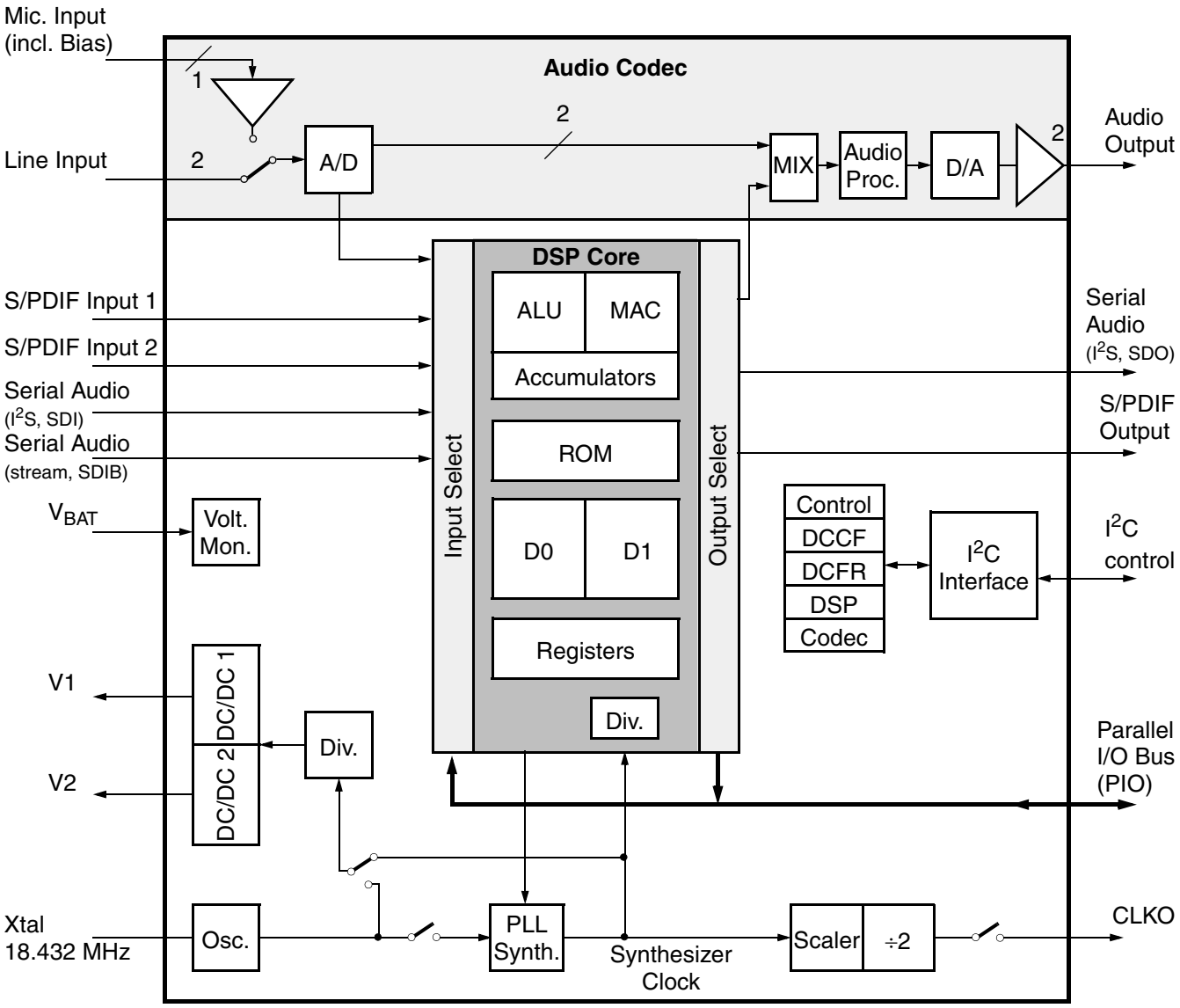


Fig. 2–1: The MAS 35x9F architecture

2.3.1. RAM and Registers

The DSP core has access to two RAM banks denoted D0 and D1. All RAM addresses can be accessed in a 20-bit or a 16-bit mode via I^2C bus. For fast access of internal DSP states the processor core has an address space of 256 data registers which also can be accessed via I^2C bus. For more details, please refer to Section 3.3. on page 27.

2.3.2. Firmware and Software

2.3.2.1. Internal Program ROM and Firmware, MPEG-Decoding

The firmware implemented in the program ROM of the MAS 35x9F provides MPEG 1/2 Layer 2, MPEG 1/2/2.5 Layer 3 and MPEG 2 AAC-decoding as well as a G.729 encoder and decoder.

The DSP operating system starts the firmware in the “Application Selection Mode”. By setting the appropriate bit in the Application Select memory cell (see Table 3–8 on page 32), the MPEG audio decoder or the G.729 Codec can be activated.

The MPEG decoder provides an automatic standard detection mode. If all MPEG audio decoders are selected, the Layer 2, Layer 3 or AAC bit stream is recognized and decoded automatically.

To add/remove MPEG layers while running in MPEG decoding mode (e.g. Layer 2, Layer 3 (0x0c) to Layer 2, Layer 3, AAC (0x1c)), the application selection has to be reset before writing the new value.

For general control purposes, the operation system provides a set of I^2C instructions that give access to internal DSP registers and memory areas.

An auxiliary digital volume control and mixer matrix is applied to the digital stereo audio data. This matrix is capable of performing the balance control and a simple kind of stereo basewidth enhancement. All four factors LL, LR, RL, and RR are adjustable, please refer to Fig. 3–3 on page 44.

2.3.2.2. Program Download Feature

The standard functions of the MAS 35x9F can be extended or substituted by downloading up to 4 kWords (1 Word = 20 bits) of program code and additionally up to 4 kWords of coefficients into the internal RAM.

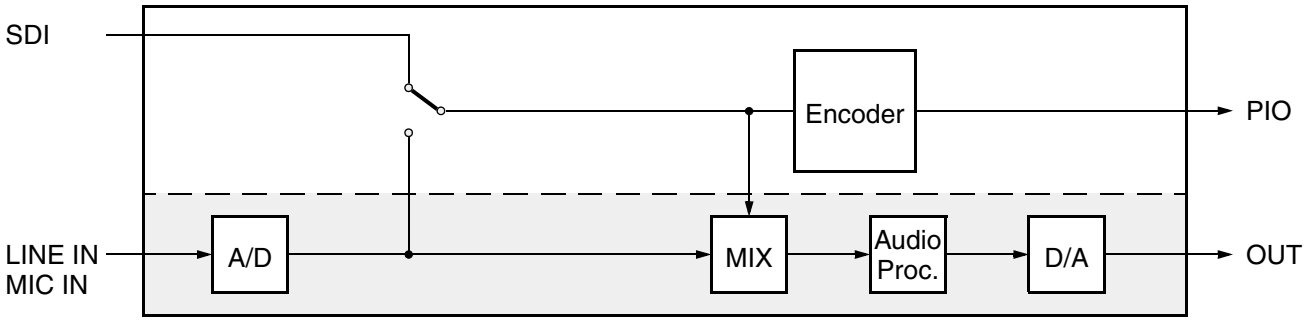


Fig. 2–2: Encoder signal flow

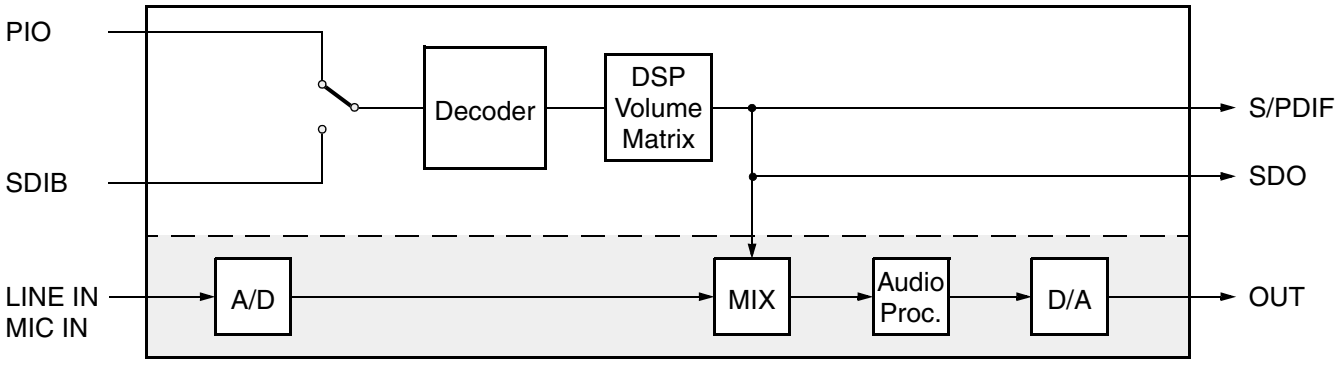


Fig. 2–3: Decoder signal flow

2.4. Audio Codec

A sophisticated set of audio converters and sound features has been implemented to comply with various kinds of operating environments that range up to high-end equipment (see Fig. 2–4).

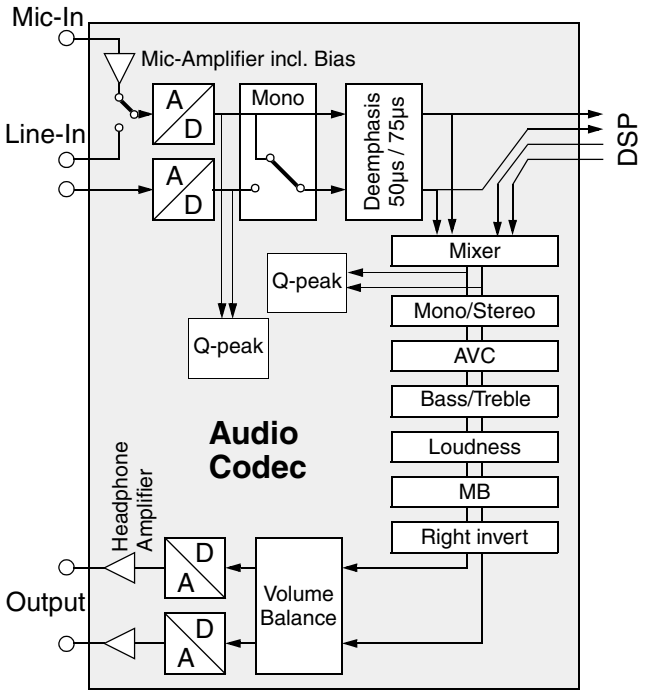


Fig. 2–4: Signal flow block diagram of Audio Codec

2.4.1. A/D Converter and Microphone Amplifier

A pair of A/D converters is provided for recording or loop-through purposes. In addition, a microphone amplifier including voltage supply function for an electret type microphone has been integrated.

2.4.2. Baseband Processing

The several baseband functions are applied to the digital audio signal immediately before D/A conversion.

2.4.2.1. Bass, Treble, and Loudness

Standard baseband functions such as bass, treble, and loudness are provided (refer to Table 3–16 for details).

2.4.2.2. Micronas Bass (MB)

The Micronas Bass system (MB) was developed to extend the frequency range of loudspeakers or headphones below the cutoff frequency of the speakers. Apart from dynamically amplifying the low-frequency bass signals, the MB exploits the psycho-acoustic phenomenon of the 'missing fundamental'. Adding harmonics of the frequency components below the cutoff frequency gives the impression of actually hearing the low frequency fundamental, while at the same time retaining the loudness of the original signal. Due to the parametric implementation of the MB, it can be customized to create different bass effects and adapted to various loudspeaker characteristics (see Section 3.4.4. and Table 3–16).

2.4.2.3. Automatic Volume Control (AVC)

In a collection of tracks from different sources fairly often the average volume level varies. Especially in a noisy listening environment the user must adjust the volume to comfortably enjoy listening. The Automatic Volume Correction (AVC) solves this problem by equalizing the volume level.

To prevent clipping, the AVC's gain decreases quickly in dynamic boost conditions. To suppress oscillation effects, the gain increases rather slowly for low level inputs. The decay time is programmable by means of the AVC register (see Table 3–16 on page 46).

For input levels of -18 dBr to 0 dBr, the AVC maintains a fixed output level of -9 dBr. Fig. 2–5 shows the AVC output level versus its input level. For volume and baseband registers set to 0 dB, a level of 0 dBr corresponds to full scale input/output.

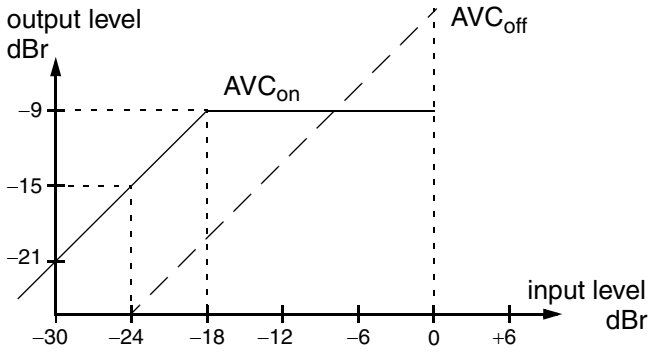


Fig. 2–5: Simplified AVC characteristics

2.4.2.4. Balance and Volume

To minimize quantization noise, the main volume control is automatically split into a digital and an analog part. The volume range is –114...+12 dB with an additional mute position. A balance function is provided.

2.4.3. D/A Converters

One pair of Micronas' unique multibit sigma-delta D/A converters is used to convert the audio data with high linearity and a superior S/N. In order to attenuate high-frequency noise caused by noise-shaping, internal low-pass filters are included. They require additional external capacitors between pins FILTx and OUTx (see Section 5.1. on page 89).

2.4.4. Output Amplifiers

The integrated output amplifiers are capable of directly driving stereo headphones or loudspeakers of 16 to 32 Ω impedance via 22 Ω series resistors. If more output power is required, the right output signal can be inverted and a single loudspeaker can be connected as a bridge between pins OUTL and OUTR. In this case, the source should be set to mono for optimized power.

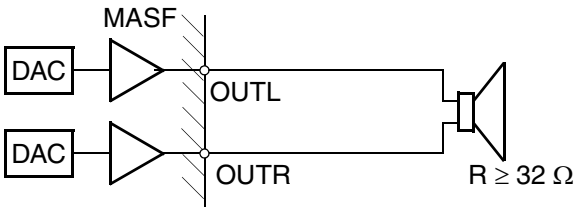


Fig. 2–6: Bridge operation mode

2.5. Clock Management

The MAS 35x9F is driven by a single crystal-controlled clock with a frequency of 18.432 MHz. It is possible to drive the MAS 35x9F with other reference clocks. In this case, the nominal crystal frequency must be written into memory location D0:348. The crystal clock acts as a reference for the embedded synthesizer that generates the internal clock.

For compressed audio data reception, the MAS 35x9F may act either as the clock master (Demand Mode) or as a slave (Broadcast Mode) as defined by bit[1] in IOControlMain memory cell (see Table 3–8 on page 32). In both modes, the output of the clock synthesizer depends on the sample rate of the decoded data stream as shown in Table 2–1.

In the BROADCAST MODE (PLL on), the incoming audio data controls the clock synthesizer via a PLL.

In the DEMAND MODE (PLL off) the MAS 35x9F acts as the system master clock. The data transfer is triggered by a demand signal at pin $\overline{EOD}$.

2.5.1. DSP Clock

The DSP clock has a separate divider. In order to reduce the power consumption, it is set to the lowest acceptable rate of the synthesizer clock which is capable to allow the processor core to perform all tasks.

2.5.2. Clock Output At CLKO

If the DSP or audio codec functions are enabled (bits[11] or [10] in the Control Register at I^2C subaddress $6A_{hex}$), the reference clock at pin CLKO is derived from the synthesizer clock.

Dependent on the sample rate of the decoded signal a scaler is applied which automatically divides the clock-out by 1, 2, or 4, as shown in Table 2–1. An additional division by 2 may be selected by setting bit[17] of the OutClkConfig memory cell (see Table 3–8 on page 32). The scaler can be disabled by setting bit[8] of this cell.

The controlling at OutClkConfig is only possible as long as the DSP is operational (bit[10] of the Control Register). Settings remain valid if the DSP is disabled by clearing bit[10].

Table 2–1: Settings of bits[8] and [17] in OutClkConfig and resulting CLKO output frequencies

	Output Frequency at CLKO/MHz				
	Synth. Clock bit[8]=1	Scaler On bit[8]=0, bit[17]=0		Scaler Plus Extra Division bit[8]=0, bit[17]=1	
f_s/kHz					
48	24.576	512·f_s	24.576	256·f_s	12.288
44.1	22.5792		22.5792		11.2896
32	24.576	768·f_s	24.576	384·f_s	12.288
24		512·f_s	12.288	256·f_s	6.144
22.05	22.5792		11.2896		5.6448
16	24.576	768·f_s	12.288	384·f_s	6.144
12		512·f_s	6.144	256·f_s	3.072
11.025	22.5792		5.6448		2.8224
8	24.576	768·f_s	6.144	384·f_s	3.072

2.6. Power Supply Concept

The MAS 35x9F was designed for minimal power dissipation. In order to optimize the battery management in portable players, two DC/DC converters were implemented to supply the complete portable audio player with regulated voltages.

2.6.1. Power Supply Regions

The MAS 35x9F has five power supply regions.

The VDD/VSS pin pair supplies all digital parts including the DSP core, the XVDD/XVSS pin pair is connected to the digital signal pin output buffers, the AVDD0/AVSS0 supply is for the analog output amplifiers, AVDD1/AVSS1 for all other analog circuits like clock oscillator, PLL circuits, system clock synthesizer and A/D and D/A converters. The I^2C interface has an own supply region via pin I2CVDD. Connecting this to the microcontroller supply assures that the I^2C bus always works as long as the microcontroller is alive so that the operating modes can be selected.

Beside these regions, the DC/DC converters have start-up circuits of their own which get their power via pin VSENSx.

2.6.2. DC/DC Converters

The MAS 35x9F has two embedded high-performance step-up DC/DC converters with synchronous rectifiers to supply both the DSP core itself and external circuitry such as a controller or flash memory at two different voltage levels. An overview is given in Fig. 2–7 on page 13.

The DC/DC converters are designed to generate an output voltage between 2.0 V and 3.5 V which can be programmed separately for each converter via the I^2C interface (see table 3.3). Both converters are of bootstrapped type allowing to start up from a voltage down to 0.9 V for use with a single battery or NiCd/NiMH cell. The default output voltages are 3.0 V. Both converters are enabled with a high level at pin DCEN and enabled/disabled by the I^2C interface.

The MAS 35x9F DC/DC converters feature a constant-frequency, low noise pulse width modulation (PWM) mode and a low quiescent current, pulse frequency modulation (PFM) mode for improved efficiencies at low current loads. Both modes – PWM or PFM – can be selected independently for each converter via I^2C interface. The default mode is PWM.

In PWM mode the switching frequency of the power-MOSFET-switches is derived from the crystal oscillator. Switching harmonics generated by constant frequency operation are consistent and predictable. When the audio codec is enabled, the switching frequency of the converters is synchronised to the audio codec clock to avoid interferences into the audio band. The actual switching frequency can be selected via the I^2C-interface between 300 kHz and 580 kHz (for details see DCFR Register in Table 3–3 on page 24).

In the PFM operation mode, the switching frequency is controlled by the converters themselves. It will be just high enough to service the output load, thus resulting in the best possible efficiency at low current loads. The PFM mode does not need a clock signal from the crystal oscillator. If both converters do not use the PWM-mode, the crystal clock will be shut down as long it is not needed by other internal blocks.

The synchronous rectifier bypasses the external Schottky diode to reduce losses caused by the diode forward voltage providing up to 5% efficiency improvement. By default, the P-channel synchronous rectifier switch is turned on when the voltage at pin(s) DCSOn exceeds the converter's output voltage at pin(s) VSENSn, and is turned off when the inductor current drops below a threshold. If one or both converters are disabled, the corresponding P-channel switch will be turned on, connecting the battery voltage to the DC/DC converters output voltage at pin VSENSn. However, it is possible to individually disable both synchronous rectifier switches by setting the corresponding bits (bit[8] and [0] in DCCF-register).

If both DC/DC-converters are off, a high signal may be applied at pin DCEN. This will start the converters in their default mode (PWM with 3.0 V output voltage). The PUP signal will change from low to high when both converters have reached their nominal output voltage and will return to low when both converters output voltages have dropped 200 mV below their programmed output voltage. The signal at pin PUP can be used to control the reset of an external microcontroller (see Section 2.11.2. on page 18 for details on the start-up procedure).

If only DC/DC-converter 1 is used, the output of the unused converter 2 (VSENS2) must be connected to the output of converter 1 (VSENS1) to make the PUP signal work properly. Also, if a DC/DC-converter is not used (no inductor connected), the pin DCSO must be left vacant.

2.6.3. Power Supply Configurations

One of the following supply configurations may be used:

– Power-optimized solution (recommended operation). DC/DC 1 (e.g. 2.2 V) drives the MAS 35x9F DSP and the audio circuitry, DC/DC 2 (e.g. 2.7 V) supplies controller and flash (see Fig. 2–8 on page 14)

– Volume-optimized solution. DC/DC 1 (e.g. 2.7 V) supplies controller, flash and MAS 35x9F audio parts, DC/DC 2 generates e.g. 2.2 V for the MAS 35x9F DSP (see Fig. 2–9 on page 14).

– Minimized external components. DC/DC 1 operates on, e.g., 2.7 V and feeds all components, DC/DC 2 remains off (see Fig. 2–10 on page 14).

– External power supply. All components are powered by an external source, no DC/DC converter is used (see Fig. 2–11 on page 14).

If DC/DC converter 1 is used, it must supply the analog circuits (pins AVDD0, AVDD1) of the MAS 35x9F.

If only one DC/DC converter is required, DC/DC1 must be used. Pin DCSO2 must be left vacant, pin VSENS2 should be connected to pin VSENS1.

If the DC/DC converters are not used, pin DCEN must be connected to VSS, DCSOx must be left vacant.

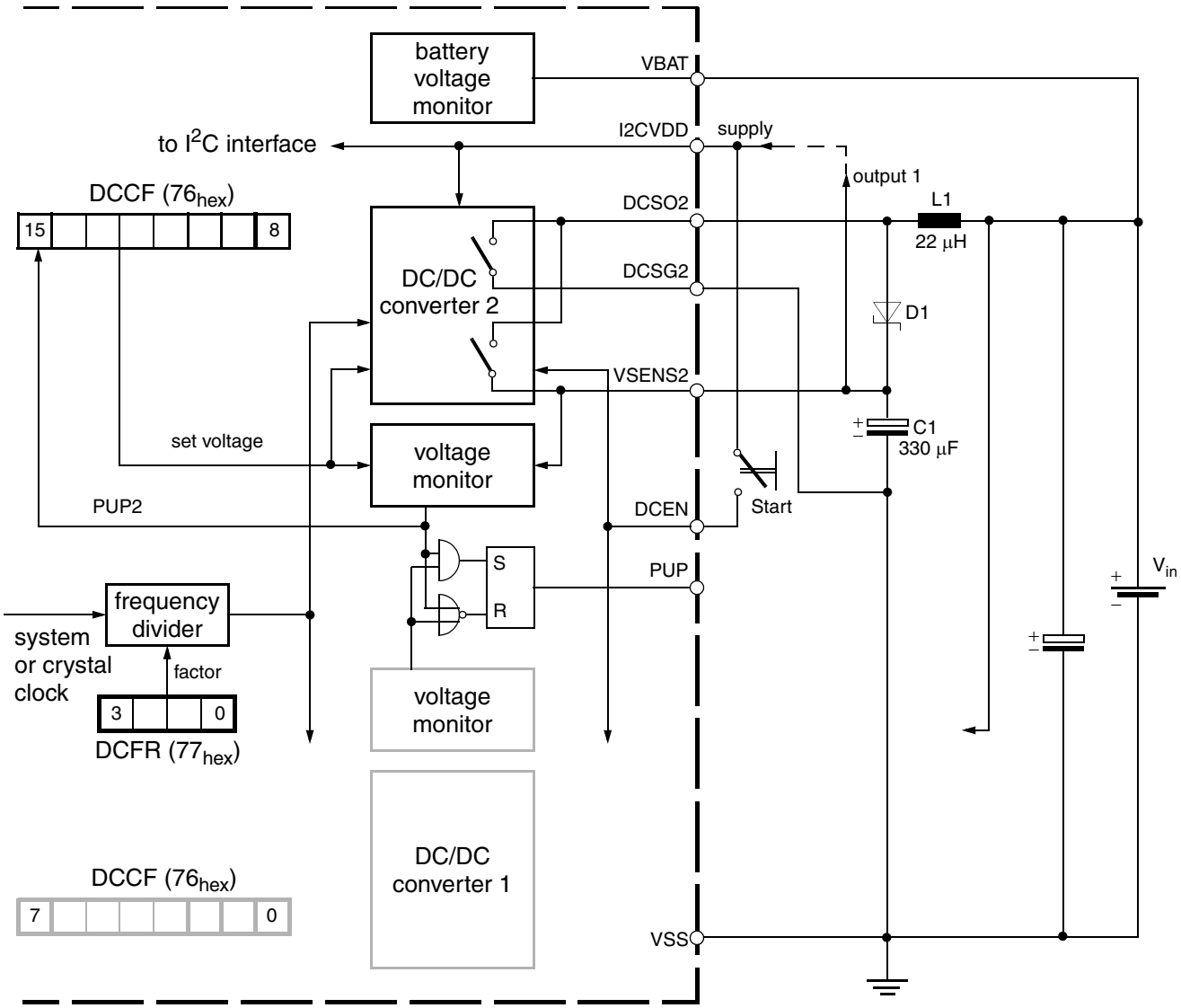


Fig. 2–7: DC/DC converter overview. The DCEN input must be connected to pin I2CVDD via start-up push button.

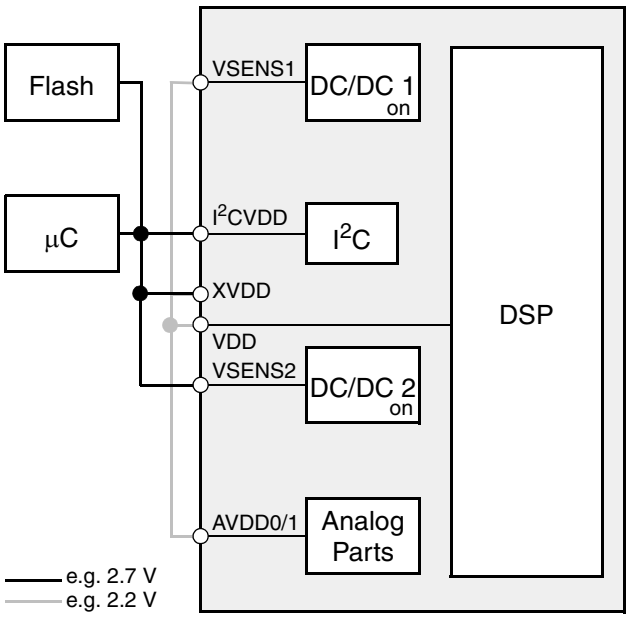


Fig. 2–8: Solution 1: Power-optimized

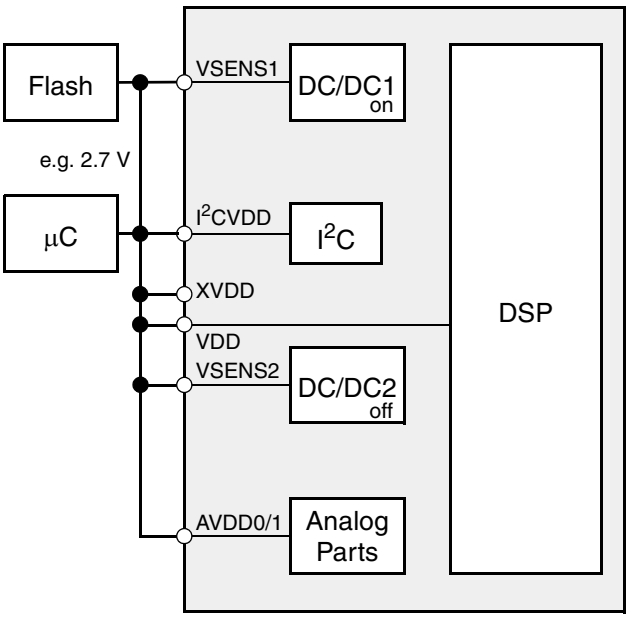


Fig. 2–10: Solution 3: Minimized components

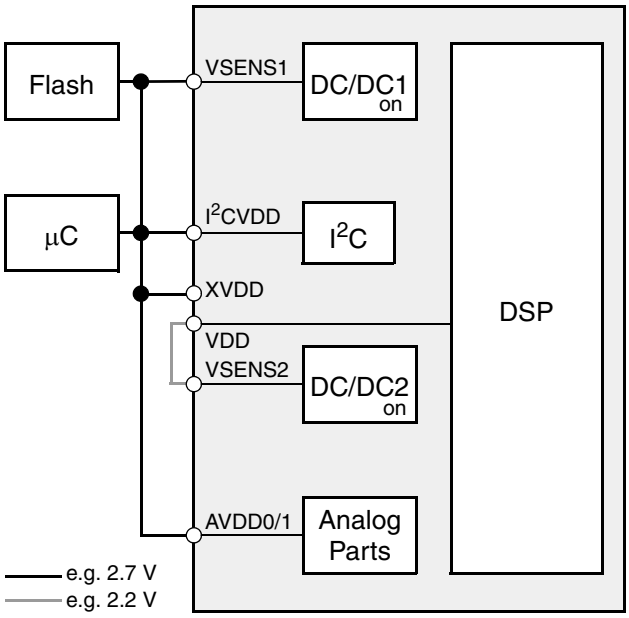


Fig. 2–9: Solution 2: Volume-optimized

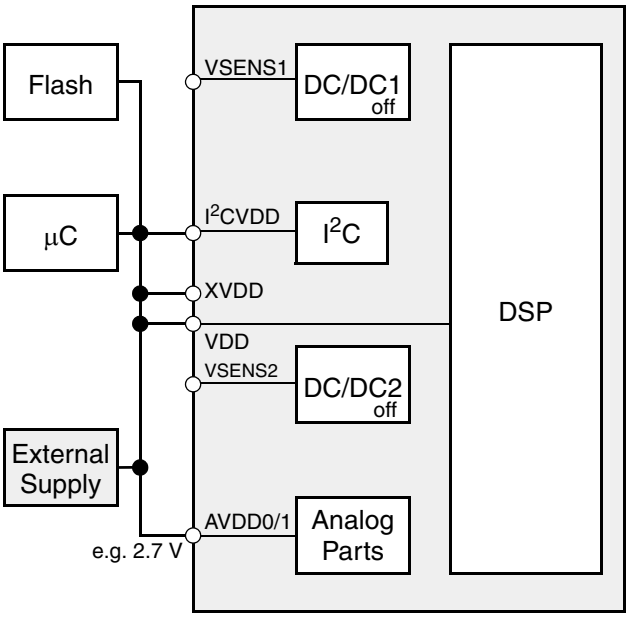


Fig. 2–11: Solution 4: External power supply

2.7. Battery Voltage Supervision

Independent of the DC/DC converters, a battery voltage supervision circuit (at pin VBAT) is provided. It can be programmed to supervise one or two battery cells. The voltage is measured by subsequently setting a series of voltage thresholds and checking the respective comparison result in register 77_{hex}.

2.8. Interfaces

The MAS 35x9F uses an I^2C control interface, a serial input interface for MPEG bit streams, and digital audio output interfaces for the decoded audio data (I^2S and S/PDIF). S/PDIF input is available after Software download. A parallel I/O interface (PIO) may be used for fast data exchange.

2.8.1. I^2C Control Interface

For controlling and program download purposes, a standard I^2C slave interface is implemented. A detailed description of all functions can be found in Section 3.

2.8.2. S/PDIF Input Interface

The S/PDIF interface receives a one-wire serial bus signal. In addition to the signal input pin SPDI1/SPDI2, a reference pin SPDIR is provided to support balanced signal sources or twisted pair transmission lines.

The synchronization time on the input signal is < 50 ms.

S/PDIF input is not supported for MPEG 1/2 Layer 2/3 and MPEG 2 AAC.

Micronas has developed a download software for flexible usage of the S/PDIF I/O and SDI/SDO interfaces. It is described in Download Software Supplement I2SPDIF (6251-505-1PDS).

2.8.3. S/PDIF Output

The S/PDIF output of the baseband audio signals is implemented at pin SPDO since version B4.

The channel status bits can be set as described in Table 3–8.

2.8.4. Multiline Serial Audio Input (SDI, SDIB)

There are two multiline serial audio input interfaces (SDI, SDIB) each consisting of the three pins SI(B)C, SI(B)I, and SI(B)D. The standard firmware only supports SDIB for bit-stream signals, while PCM-inputs should be routed to SDI.

The interfaces can be configured as continuous bit-stream or word-oriented inputs. For the MPEG bit streams, the word strobe pin SIBI must always be connected to V_{SS}; bits must be sent MSB first as created by the encoder.

If the download software (refer to Download Software Supplement I2SPDIF (6251-505-1PDS)) is used, the interface acts as an I^2S-type with SI(B)I as a word-strobe for PCM data.

For the Demand Mode (see Section 2.5.), the signal clock coming from the data source must be higher than the nominal data transmission rate (e.g. 128 kbit/s). Pin $\overline{EOD}$ is used to interrupt the data flow whenever the input buffer of the MAS 35x9F is filled.

For controlling details, please refer to Table 3–8 on page 32.

2.8.5. Multiline Serial Output (SDO)

The serial audio output interface of the MAS 35x9F is a standard I^2S-like interface consisting of the data lines SOD, the word strobe SOI and the clock signal SOC. It is possible to choose between two standard interface configurations (16-bit data words with word strobe time offset or 32-bit data words with inverted SOI signal).

If the serial output generates 32 bits per audio sample, only the first 20 bits will carry valid audio data. The 12 trailing bits are set to zero by default.

2.8.6. Parallel Input/Output Interface (PIO)

The parallel interface of the MAS 35x9F consists of the 8 data lines PI12...PI19 (MSB) and the control lines $\overline{PCS}$, PR, $\overline{PRTR}$, $\overline{PRTW}$, and $\overline{EOD}$. It can be used for data exchange with an external memory, for fast program download and for other special purposes as defined by the DSP software.

For MPEG data input, the PIO interface is activated by setting bits[9] and [8] in D0:346 to 01. For the handshake protocol, please refer to Section 4.6.2.8. on page 80.

2.9. MPEG Synchronization Output

The signal at pin SYNC is set to ‘1’ after the internal decoding for the MPEG header has been finished for one frame. The rising edge of this signal can be used as an interrupt input for the controller that triggers the read out of the control information and ancillary data. As soon as the MAS 35x9F has received the SYNC reset command (see Section 4.6.2.6. on page 77), the SYNC signal is cleared. If the controller does not issue a reset command, the SYNC signal returns to ‘0’ as soon as the decoding of the next MPEG frame is started. MPEG status and ancillary data become invalid until the frame is completely decoded and the signal at pin SYNC rises again. The controller must have finished reading all MPEG information before it becomes invalid. The MPEG Layer 2/3 frame lengths are given in Table 2–2. AAC has no fixed frame length.

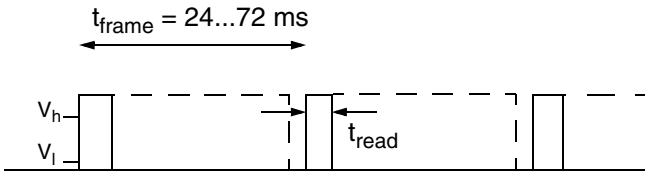


Fig. 2–12: Schematic timing of the signal at pin SYNC. The signal is cleared at t_{read} when the controller has issued a Clear SYNC Signal command (see Section 4.6.2.6. on page 77). If no command is issued, the signal returns to ‘0’ just before the decoding of the next MPEG frame.

Table 2–2: Frame length in MPEG Layer 2/3

f_s/kHz	Frame Length Layer 2	Frame Length Layer 3
48	24 ms	24 ms
44.1	26.12 ms	26.12 ms
32	36 ms	36 ms
24	24 ms	24 ms
22.05	26.12 ms	26.12 ms
16	36 ms	36 ms
12	not available	48 ms
11.025	not available	52.24 ms
8	not available	72 ms

2.10.MP3 Block Input Mode

A new so-called **MP3 block input** mode is now available which improves the input timing behavior of the MAS 35x9F MPEG 1/2/2.5 Layer 3 decoder. The following sections provide a detailed description of this new mode.

2.10.1.Functional Description of the MP3 Block Input Mode

In MP3 block input, the MAS 35x9F generates a demand for new input data each time one of its two input buffers becomes available. The controller then has to send one block of input data via the serial interface SDIB. The block size is 2048 byte. The demand is signalized via a pulse on the $\overline{\text{EOD}}$ pin.

Fig. 2–13 shows that the number of interrupts per second does not depend on the data rate at the serial interface. The maximum input data bit clock rate supported by the MAS 35x9F for all MPEG audio sampling rates is 1.4 MHz.

Table 2–3 shows the average number of interrupts per second for several typical MP3 bit rates.

The time period between two interrupts may vary slightly even for fixed bit rate input streams due to the MP3 specific bit reservoir.

Table 2–3: MP3 bit rate vs. number of interrupts

Bit Rate [kbit/s]	Number of Interrupts [1/s]
320	20
256	16
224	14
192	12
160	10
128	8
112	7
96	6
80	5
64	4

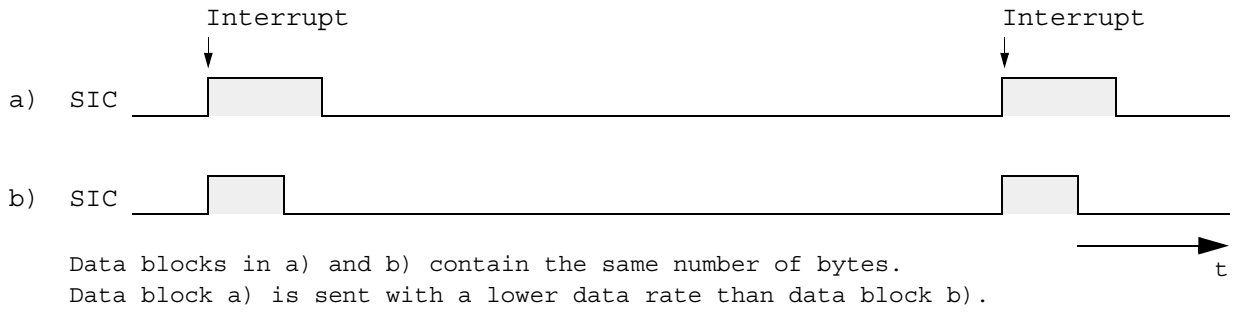


Fig. 2–13: Data Block Timing Diagram

2.10.2. Setup

Table 3–10 on page 39 lists the new bits, UIC cells, and registers to setup the MP3 block input mode.

2.10.2.1. Resync Timeout

In case the MP3 decoder loses the synchronization (e.g. due to corrupted input data), the output is softly muted and a resync loop is entered where the MAS 35x9F can be accessed via I^2C. The loop is left and the re-synchronization procedure continues in any of the following cases:

– the last input data block is fully sent,

– the Validate bit of IOControlMain is set (D0:346, bit[0]),

– the timeout is reached (ResyncTimeout in Table 3–10), the end bit is set (this bit will be reset by the MAS 35x9F).

2.10.2.2. Detailed Setup

After the MPEG audio decoder application has been selected, the following settings enable the MP3 block decoding process.

Play MP3

1. Write 0x318 into SerialInConfig.
2. Write IOControlMain with bit[2] and bit[0] equal one.
3. Write IOControlMain with bit[2] equals zero and bit[0] equals one.
4. Write 0x0 into ResyncTimeout.
5. Write 0x0 into SoftMute.
6. Enable EODQ interrupt for sending data in controller.
7. Set StartBit in MP3BlockConfig.
8. Send data block of 2048 byte when EODQ goes high.

Stop/Pause MP3

1. Write 0x1 into SoftMute.
2. Clear start bit in MP3BlockConfig.

2.11. Default Operation

This sections refers to the standard operation mode “power-optimized solution” (see Section 2.6.3.).

2.11.1. Stand-by Functions

After applying the battery voltage, the system will remain stand-by, as long as the DCEN pin level is kept low. Due to the low stand-by current of CMOS circuits, the battery may remain connected to DCSOn/VSENSn at all times.

2.11.2. Power-Up of the DC/DC Converters and Reset

The battery voltage must be applied to pin DCSOn via the 22 µH inductor and, furthermore, to the sense pin VSENSn via a Schottky diode (see Fig. 2–7 on page 13).

For start-up, the pin DCEN must be connected via an external “start” push button to the I2CVDD supply, which is equivalent to the battery supply voltage (> 0.9 V) at start-up.

The supply at DCEN must be applied until the DC/DC converters have started up (signal at pin PUP) and then removed for normal operation.

As soon as the output voltage at VSENSn reaches the default voltage monitor reset level of 3.0 V, the respective internal PUPn bit will be set. When both PUPn bits are set, the signal at pin PUP will go high and can be used to start and reset the microcontroller.

Before transmitting any I^2C commands, the controller must issue a power-on reset to pin $\overline{POR}$. The separate supply pin I2CVDD ensures that the I^2C interface works independently from the DSP or the audio codec. Now the desired supply voltage can be programmed at I^2C subaddress 76_{hex}.

2.11.2.1. Important Advice for Turn-on and Operating Voltage

Before the 2.2 V are programmed at the DCDC converter, DSP+Codec must be enabled.
Operating and Turn-Off is possible down to 2.2 V.
The sequence should be similar to the following:

1. Start DCDC
2. Set DCDC to 2.5 V
   Turn on DSP+Codec
   Write App-Select memory cell
   Read App-Running Mem cell
   If okay: Set DCDC to 2.2 V
   Set other mem cells
   Set other codec registers
   .....
3. Demute...send data
4. Mute...stop data.....loop "3)" "4)"...
5. Turn off DSP+Codec
   goto "2)"
   etc.....

The signal at pin PUP will return to low only when both PUPn flags (I^2C subaddress 76_{hex}) have returned to zero. Care must be taken when changing both DC/DC output voltages to higher values. In this case, both output voltages are momentarily insufficient to keep the PUPn flags up; the resulting dip in the signal at the PUP pin may, in turn, reset the microcontroller. To avoid this condition, only one DC/DC output voltage should be changed at a time. Before modifying the second voltage, the microcontroller must wait for the PUPn flag of the first voltage to be set again.

If only DC/DC converter 1 is used, the reference voltage of the second, unused converter should be set to a lower value than that of converter 1, and its pin VSENS2 should be connected to VDD.

The operating mode pulse width modulation, or pulse frequency modulation, are controlled at I^2C subaddress 76_{hex}, the operating frequency at I^2C subaddress 77_{hex}.

2.11.3. Reset Signal Specification

After power-up, a reset signal should be applied to the pin $\overline{POR}$ by the microcontroller as follows:

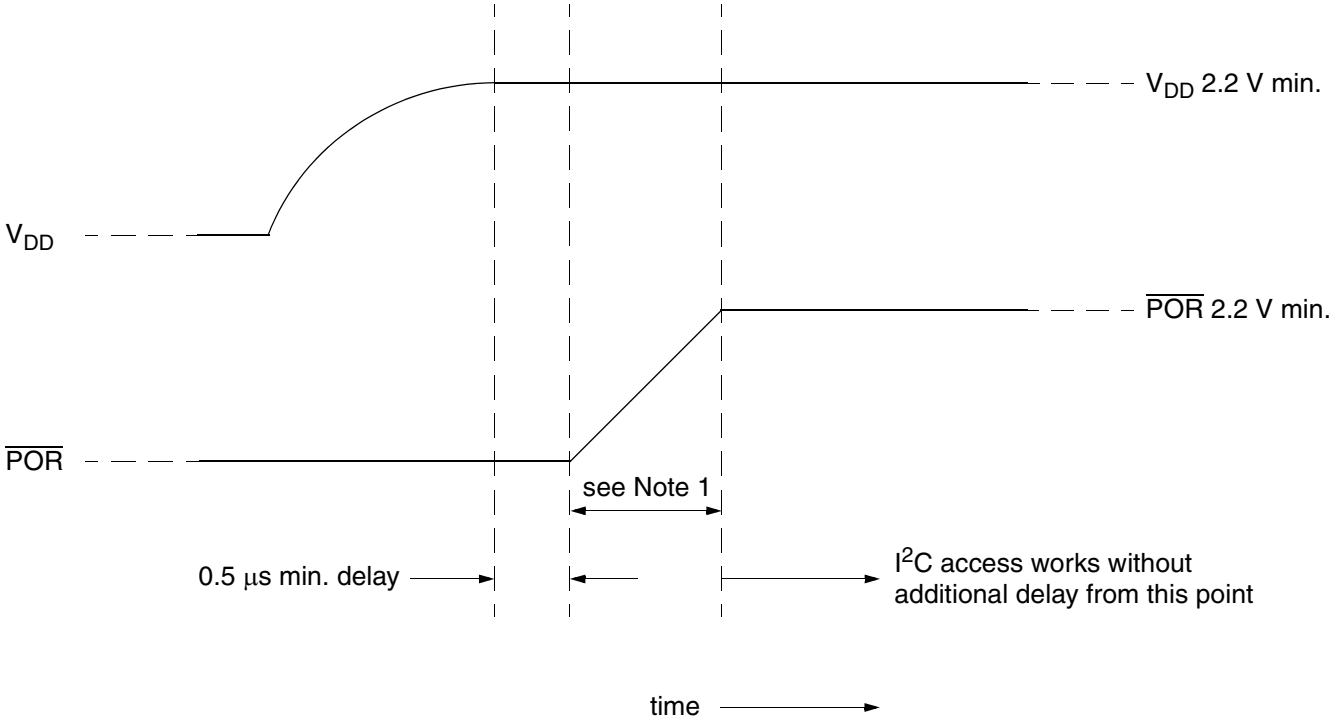


Fig. 2–14: Reset signal at pin $\overline{POR}$

Note: The slew rate of $\overline{POR}$ should be as high as possible, but **must be glitch-free in any case**.

Slew rate typ.: 1 µs for 10% to 90% level transition,
Slew rate max.: 20 µs for 10% to 90% level transition.

2.11.4.Control of the Signal Processing

Before starting the DSP, the controller should check for a sufficient voltage supply (respective flag PUPn at I^2C subaddress 76_{hex}). The DSP is enabled by setting the appropriate bit in the Control register (I^2C subaddress $6A_{hex}$). The nominal frequency of the crystal oscillator must be written into D0:348. After an initialization phase of 5 ms, the DSP data registers can be accessed via I^2C.

Input and output control is performed via memory location D0:346 and D0:347. The serial input interface SDIB is the default. The decoded audio can be routed to either the S/PDIF, the SDO and the analog outputs. The output clock signal at pin CLKO is defined in D0:349.

All changes in the D0 memory cells become effective synchronously upon setting the LSB of Main I/O Control (see Table 3–8 on page 32). Therefore, this cell should always be written last.

The digital volume control (see Table 3–8 on page 32) is applied to the output signal of the DSP. The decoded audio data will be available at the SPDO output interface in the next version.

The DSP does not have to be started if its functions are not required, e.g., for routing audio through the codec part of the IC via the A/D and the D/A converters.

2.11.5.Start-up of the Audio Codec

Before enabling the audio codec, the controller should check for a sufficient voltage supply (respective flag PUPn at I^2C subaddress 76_{hex}).

The audio codec is enabled by setting the appropriate bit at the Control register (I^2C subaddress $6A_{hex}$). After an initialization phase of 5 ms, the DSP data registers can be accessed via I^2C. The A/D and the D/A converters must be switched on explicitly (register 00 00_{hex} at I^2C subaddress $6C_{hex}$). The D/A converters may either accept data from the A/D converters or the output of the DSP, or a mix of both[1)] (register 00 06_{hex} and 00 07_{hex} at I^2C subaddress $6C_{hex}$). Finally, an appropriate output volume (register 00 10_{hex} at I^2C subaddress $6C_{hex}$) must be selected.

2.11.6.Power-Down

All analog outputs should be muted and the A/D and the D/A converters must be switched off (register 00 10_{hex} and 00 00_{hex} at I^2C subaddress $6C_{hex}$). The DSP and the audio codec must be disabled (clear DSP_EN and CODEC_EN bits in the Control register, I^2C subaddress $6A_{hex}$). By clearing both DC/DC enable flags in the Control register (I^2C subaddress $6A_{hex}$), the microcontroller can power down the complete system.

1) mixer available in version A2 and later; in version A1, please use selector 00 $0F_{hex}$.

3. Controlling

3.1. I²C Interface

Controlling between the MAS 35x9F and the external controller is done via an I²C slave interface.

3.1.1. Device Address

The device addresses are $3C/3E_{hex}$ (device write "DW") and $3D/3F_{hex}$ (device read, "DR") as shown in Table 3–1. The device address pair $3C/3D_{hex}$ applies if the DVS pin is connected to VSS, the device address pair $3E/3F_{hex}$ applies if the DVS pin is connected to I2CVDD.

Table 3–1: I²C device address

A7	A6	A5	A4	A3	A2	A1	W/R
0	0	1	1	1	1	DVS	0/1

I²C clock synchronization is used to slow down the interface if required.

3.1.2. I²C Registers and Subaddresses

The interface uses one level of subaddresses. The MAS 35x9F interface has 7 subaddresses allocated for the corresponding I²C registers. The registers can be divided into three categories as shown in Table 3–2.

The address $6A_{hex}$ is used for basic control, i.e. reset and task select. The other addresses are used for data transfer from/to the MAS 35x9F.

The I²C registers of the MAS 35x9F are 16 bits wide, the MSB is denoted as bit[15]. Transmissions via I²C bus have to take place in 16-bit words (two byte transfers, MSB sent first); thus, for each register access, two 8-bit data words must be sent/received via I²C bus.

3.1.3. Naming Convention

The description of the various controller commands uses the following formalism:

– **Abbreviations** used in the following descriptions:
  a address
  d data value
  n count value
  o offset value
  r register number
  x don't care

– Memory addresses, like D1:89f, are always in hexadecimal notation.

– A data value is split into 4-bit nibbles which are numbered beginning with 0 for the least significant nibble.

– Data values in nibbles are always shown in hexadecimal notation.

– A hexadecimal 20-bit number **d** is written, e.g. as **d** = $17C63_{hex}$, its five nibbles are d0 = 3_{hex}, d1 = 6_{hex}, d2 = C_{hex}, d3 = 7_{hex}, and d4 = 1_{hex}.

– **Variables** used in the following descriptions:
  I²C address:
  DW3C/$3E_{hex}$ I²C device write
  DR3D/$3F_{hex}$ I²C device read
  DSP core:
  data_write68_{hex} DSP data write
  data_read69_{hex} DSP data read
  Codec:
  codec_write$6C_{hex}$ codec write
  codec_read$6D_{hex}$ codec read

– **Bus signals**
  S Start
  P Stop
  A ACK = Acknowledge
  N NAK = Not acknowledge
  W Wait = I²C clock line is held low while the MAS 35x9F is processing the current I²C command

– **Symbols** in the telegram examples
  < Start Condition
  > Stop
  dd data bytes
  xx ignore
  All telegram numbers are hexadecimal, data originating from the MAS 35x9F are represented as gray letters.
  Example:
  `<DW 68 dd dd >` write data to DSP
  `<DW 69 <DR dd dd >` read data from DSP

Fig. 3–1 shows I²C bus protocols for write and read operations of the interface; the read operations require an extra start condition and repetition of the chip address with the device read command (DR). Fields with signals/data originating from the MAS 35x9F are marked by a gray background.

Note: In some cases the data reading process must be concluded by a NAK condition.

3.2. Direct Configuration Registers

The task selection of the DSP and the DC/DC converters are controlled in the direct configuration registers CONTROL, DCCF, and DCFR.

Table 3–2: I²C subaddresses

Sub-address (hex)	I²C-Register Name	Function
Direct Configuration		
6A	CONTROL	Controller writes to MAS 35x9F CONTROL register
76	DCCF	Controller writes to first DC/DC configuration register
77	DCFR	Controller writes to second DC/DC configuration register
DSP Core Access		
68	data_write	Controller writes to MAS 35x9F DSP
69	data_read	Controller reads from MAS 35x9F DSP
Codec Access		
6C	codec_write	Controller writes to MAS 35x9F codec register
6D	codec_read	Controller reads from MAS 35x9F codec register

3.2.1. Write Direct Configuration Registers

S	DW	W	A	subaddr.	A	d3,d2	A	d1,d0	A	P

The write protocol for the direct configuration registers only consists of device address, subaddress and one 16-bit data word.

3.2.2. Read Direct Configuration Register

S	DW	W	A	subaddr.	A	S	DR	W	A	
						d3,d2	A	d1,d0	N	P

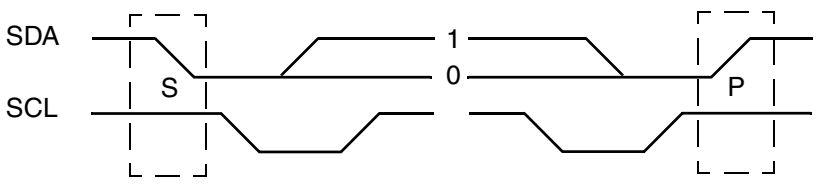
To check the PUP1 and PUP2 power-up flags, it is necessary to read back the content of the direct configuration registers.

Example: I2C write access

S	DW	W	A	subaddress	A	high byte data	A	low byte data	W	A	P

Example: I²C read access

S	DW	W	A	subaddress	A	S	DR	W	A
						high byte data	A	low byte data	W	N	P



W = Wait
A = Acknowledge (Ack)
N = Not Acknowledge (NAK)
S = Start
P = Stop

Fig. 3–1: Example of an I²C bus protocol for the MAS 35x9F (MSB first; data must be stable while clock is high)

Table 3–3: Direct configuration registers

I^2C Sub-address (hex)	Function	Name
6A	**Control Register** (reset value = 3000_{hex}) bit[15:14] Analog supply voltage range Code / AGNDC / recommended for voltage range of AVDD 00 / 1.1 V / 2.0 ... 2.4 V (reset) 01 / 1.3 V / 2.4 ... 3.0 V 10 / 1.6 V / 3.0 ... 3.6 V 11 / reserved / reserved Higher voltage ranges permit higher output levels and thus a better signal-to-noise ratio. bit[13] Enable DC/DC 2 (reset=1) bit[12] Enable DC/DC 1 (reset=1) Both DC/DC converters are switched on by default with DCEN = high (1). bit[11] Enable and reset audio codec[2)] bit[10] Enable and reset DSP core[2)] For normal operation (MPEG-decoding and D/A conversion), both, the DSP core and the audio codec have to be enabled after the power-up procedure. The DSP can be left off if an audio signal is routed from the analog inputs to the analog outputs (set bit[15] in codec register 00 $0F_{hex}$). The audio codec can be left off if the DSP uses digital inputs and outputs only. bit[9] Reset codec bit[8] Reset DSP core bit[7] Enable crystal input clock divider of 1.5 (extended range up to 28 MHz)[1)] bit[6:0] Reserved, must be set to zero	CONTROL

[1)] refer to Section 4.6.3. on page 81
[2)] refer to Section 2.11.2.1.

Table 3–3: Direct configuration registers, continued

I^2C Sub-address (hex)	Function	Name
76	**DCCF Register** (reset = 5050_{hex})	DCCF

DC/DC Converter 2

bit[15] PUP2: Voltage monitor 2 flag (readback)

bit[14:11] Converter 2 output voltage with respect to VREF[2)]

Code	Nominal output volt.	set level of PUP2	reset level of PUP2
1111	3.5 V	3.4 V	3.3 V
1110	3.4 V	3.3 V	3.2 V
1101	3.3 V	3.2 V	3.1 V
1100	3.2 V	3.1 V	3.0 V
1011	3.1 V	3.0 V	2.9 V
1010	3.0 V	2.9 V	2.8 V (reset)
1001	2.9 V	2.8 V	2.7 V
1000	2.8 V	2.7 V	2.6 V
0111	2.7 V	2.6 V	2.5 V
0110	2.6 V	2.5 V	2.4 V
0101	2.5 V	2.4 V	2.3 V
0100[1)]	2.4 V	2.3 V	2.2 V
0011[1)]	2.3 V	2.2 V	2.1 V
0010[1)]	2.2 V	2.1 V	2.0 V

bit[10] Mode

1	pulse frequency modulation (PFM)
0	pulse width modulation (PWM) (reset)

bit[9:8] Reserved, must be set to zero

The DC/DC converters are up-converters only. Thus, if the battery voltage is higher than the selected nominal voltage, the output voltage will exceed the nominal voltage.

DC/DC Converter 1

bit[7] PUP1: Voltage monitor 1 flag (readback)

bit[6:3] Converter 1 output voltage at VSENS1 with respect to VREF (see bits 14 to 11)[2)]

bit[2] Mode

1	pulse frequency modulation (PFM)
0	pulse width modulation (PWM) (reset)

bit[1:0] Reserved, must be set to zero

Note, that the reference voltage for DC/DC converter 1 is derived from the main reference source supplied via pin AVDD1. Therefore, if this DC/DC converter is used, its output must be connected to the analog supply.

The DC/DC converters are up-converters only. Thus, if the battery voltage is higher than the selected nominal voltage, the output voltage will exceed the nominal voltage.

[1)] refer to Section 4.3.3. on page 60
[2)] refer to Section 2.11.2.1.

Table 3–3: Direct configuration registers, continued

I^2C Sub-address (hex)	Function	Name
77	**DCFR Register** (reset = 00_{hex})	DCFR

Battery Voltage Monitor

bit[15] Comparison result (readback)
- 1 input voltage at pin VBAT above defined threshold
- 0 input voltage at pin VBAT below defined threshold

bit[14] Number of battery cells
- 0 1 cell (range 0.8...1.5 V) (reset)
- 1 2 cells (range 1.6...3.0 V)

bit[13:10] Voltage threshold level

	1 cell	2 cells
1111	1.5	3.0 V
1110	1.45	2.9 V
...		
0010	0.85	1.7 V
0001	0.8	1.6 V
0000	battery voltage supervision off (reset)	

bit[9:8] Reserved, must be set to 0

The result is stable 1 ms after enabling. The setup time for switching between two thresholds is negligibly small.

For power management reasons, the battery voltage monitor should be switched off by setting bit[13:10] to zero when the measurement is completed.

DC/DC Converter Frequency Control (PWM)

bit[7:4] Reserved, must be set to 0

bit[3:0] Frequency of DC/DC converter

Reference: 24.576	22.5792	18.432 MHz
0111	315.1	289.5	297.3 kHz
0110	323.4	297.1	307.2 kHz
0101	332.1	305.1	317.8 kHz
0100	341.3	313.6	329.1 kHz
0011	351.1	322.6	341.3 kHz
0010	361.4	332.0	354.5 kHz
0001	372.4	342.1	368.6 kHz
0000	384.0	352.8	384.0 kHz (reset)
1111	396.4	364.2	400.7 kHz
1110	409.6	376.3	418.9 kHz
1101	423.7	389.3	438.9 kHz
1100	438.9	403.2	460.8 kHz
1011	455.1	418.1	485.1 kHz
1010	472.6	434.2	512.0 kHz
1001	491.5	451.6	542.1 kHz
1000	512.0	470.4	576.0 kHz

If the audio codec is not enabled (bit[11] of the CONTROL register at I^2C-sub-address $6A_{hex}$ is zero), the clock for the DC/DC converters is directly derived from the crystal frequency (nominal 18.432 MHz). Otherwise, the synthesizer clock is used as the reference (please refer to the respective column in Table 2–1 on page 11).

3.3. DSP Core

3.3.1. Access Protocol

The I^2C data register is used to communicate with the internal firmware of the MAS 35x9F. It is readable (subaddress “data_read”) and writable (subaddress “data_write”) and also has a length of 16 bits. The data transfer is done with the most significant bit (m) first.

Table 3–4: Data register bit assignment

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
m															l

A special command language is used that allows the controller to access the DSP registers and RAM cells and thus monitor internal states, set the parameters for the DSP firmware, control the hardware, and even provide a download of alternative software modules. The DSP commands consist of a “Code” which is sent to the I^2C data register together with additional parameters.

S	DW	W	A	data_write	A	**Code**,...	A	...,...	A	...

Fig. 3–2: General core access protocol

Table 3–5 gives an overview over the different commands which the DSP Core receives via the I^2C data register. The “Code” is always the first data nibble transmitted after the “data_write” subaddress byte. A second auxiliary code nibble is used for the short memory (16-bit) access commands.

The MAS 35x9F firmware scans the I^2C interface periodically and checks for pending or new commands.

The commands are then executed by the DSP during its normal operation without any loss or interruption of the incoming data or outgoing audio data stream. However, due to some time critical firmware parts, a certain latency time for the response has to be expected at the locations marked with a “W” (= wait). The theoretical worst case response time does not exceed 4 ms. However, the typical response time is less than 0.5 ms.

Due to the 16-bit width of the I^2C data register, all actions transmit telegrams with multiples of 16 data bits.

Table 3–5: Basic controller command codes

Code (hex)	Command	Function
0...3	Run	Start execution of an internal program. *Run* with start address 0 means freeze the operating system.
5	Read Ancillary Data	The controller reads a block of MPEG Ancillary Data from the MAS 35x9F
6	Fast Program Download	The controller downloads custom software via the PIO interface
7	Read IC Version	The controller reads the version information of the IC
a	Read from Register	The controller reads an internal register of the MAS 35x9F
b	Write to Register	The controller writes an internal register of the MAS 35x9F
c	Read D0 Memory	The controller reads a block of the DSP memory
d	Read D1 Memory	The controller reads a block of the DSP memory
e	Write D0 Memory	The controller writes a block of the DSP memory
f	Write D1 Memory	The controller writes a block of the DSP memory

3.3.2. Data Formats

The internal data word size is 20 bits. All RAM-addresses can be accessed in a 20-bit mode via I^2C bus. Because of the 16-bit width of the I^2C data register the full transfer of all 20 bits requires two 16-bit I^2C words. Some commands only access the lower 16 bits of a cell. For fast access of internal DSP states the processor core also has an address space of 256 data registers.

The internal data format is a 20 bit two's complement denoted "r". If in some cases a fixed point notation "v" is necessary. The conversion between the two forms of notation is done as follows:

r = v*524288.0+0.5; ($-1.0 \leq v < 1.0$)
v = r/524288.0; ($-524288 < r < 524287$)

3.3.2.1. Run and Freeze (Codes 0_{hex} to 3_{hex})

S	DW	W	A	data_write	A	a3,a2	A	a1,a0	W	A	P

The *Run* command causes the start of a program part at address **a** = (a3,a2,a1,a0). Since nibble a3 is also the command code (see Table 3–5), it is restricted to values between 0 and 3. This command is used to start alternate code or downloaded code from a RAM-area that has been configured as program RAM.

If the start address is $1000_{hex} \leq$ **a** $< 3FFF_{hex}$ and the respective RAM area has been configured as program RAM (see Table 3–7 on page 31), the MAS 35x9F continues execution with a custom program already downloaded to this area.

Example 1: Start program execution at address 345_{hex}:

```
<DW 68 03 45>
```

Example 2: Start execution of a downloaded code at address 1000_{hex}:

```
<DW 68 10 00>
```

Freeze is a special run command with start address 0. It suspends all normal program execution. The operating system will enter an idle loop so that all registers and memory cells can be watched. This state is useful for operations like downloading code or contents of memory cells because the internal program cannot overwrite these values. This freezing will be required if alternative software is downloaded into the internal RAM of the MAS 35x9F.

Freeze has the following I^2C protocol:

```
<DW 68 00 00>
```

The entry point of the default software will be accessed automatically after a reset, thus issuing a *Run* or *Freeze* command is only necessary for starting downloaded software or special program modules which are not part of the standard set.

3.3.2.2. Read Register (Code A_{hex})

1) send command

S	DW	W	A	data_write	A	**a**,r1	A	r0,0	W	A	P

2) get register value

S	DW	W	A	data_read	A	S	DR	W	A		
	x,x	A	x,d4	W	A	d3,d2	A	d1,d0	W	N	P

The MAS 35x9F has an address space of 256 DSP-registers. Some of the registers (**r** = r1,r0 in the figure above) are direct control inputs for various hardware blocks, others control the internal program flow. In Table 3–7, the registers of interest are described in detail. In contrast to memory cells, registers cannot be accessed as a block but must always be addressed individually.

Example:
Read the content of register $C8_{hex}$:

```
<DW 68 ac 80>                    define register
<DW 69 <DR xx xd dd dd >         and read
```

3.3.2.3. Write Register (Code B_{hex})

S	DW	W	A	data_write	A	**b**,r1	A	r0,d4	W	A	
						d3,d2	A	d1,d0	W	A	P

The controller writes the 20-bit value (**d** = d4,d3,d2, d1,d0) into the MAS 35x9F register (**r** = r1,r0). A list of registers needed for control purposes is given in Table 3–7.

Example: Writing the value 81234_{hex} into the register with the number AA_{hex}:

```
<DW 68 ba a8 12 34>
```

3.3.2.4. Read Memory (Codes C_{hex} and D_{hex})

The MAS 35x9F has 2 memory areas of 2048 words denoted D0 and D1. The memory areas D0 and D1 can be written by using the codes C_{hex} and D_{hex}, respectively.

1) send command (Read D0)

S	DW	W	A	data_write	A	**c**,0	A	0,0	W	A	
						n3,n2	A	n1,n0	W	A	
						a3,a2	A	a1,a0	W	A	P

2) get register value

S	DW	W	A	data_read	A	S	DR	W	A					
	x,x	A	x,d4	W	A	d3,d2	A	d1,d0	W	A				
	....repeat for n data values....													
	x,x	A	x,d4	W	A	d3,d2	A	d1,d0	W	N	P			

The *Read D0 Memory* command gives the controller access to all 20 bits of the D0/D1 memory cells. The telegram to read 3 words starting at location D1:100 is

```
<DW 68 d0 00 00 03 01 00>
<DW 69 <DR xx xd dd dd
           xx xd dd dd xx xd dd dd >
```

3.3.2.5. Short Read Memory (Codes $C4_{hex}$ and $D4_{hex}$)

Because most cells in the user interface are only 16 bits wide, it is faster and more convenient to access the memory locations with a special 16-bit mode for reading:

1) send command (e.g. Short Read D0)

S	DW	W	A	data_write	A	**c,4**	A	0,0	W	A	
						n3,n2	A	n1,n0	W	A	
						a3,a2	A	a1,a0	W	A	P

2) get register value

S	DW	W	A	data_read	A	S	DR	W	A					
						d3,d2	A	d1,d0	W	A				
	....repeat for n data values....													
						d3,d2	A	d1,d0	W	N	P			

This command is similar to the normal 20 bit read command and uses the same command code C_{hex} and D_{hex} for D0 and D1 memory, respectively, however it is followed by a 4_{hex} rather than a 0_{hex}.

Example: Read 16 bits of D1:123 has the following I^2C protocol:

```
<DW 68 d4 00          read 16 bits from D1
    00 01             1 word to be read
    01 23             start address
   <DW 69 DR          start reading
     dd dd >          and read
```

3.3.2.6. Write Memory (Codes E_{hex} and F_{hex})

The memory areas D0 and D1 can be written by using the codes E_{hex} and F_{hex}, respectively.

S	DW	W	A	data_write	A	**e**,0	A	0,0	W	A	
						n3,n2	A	n1,n0	W	A	
						a3,a2	A	a1,a0	W	A	
	x,x	A	x,d4	W	A	d3,d2	A	d1,d0	W	A	
	....repeat for n data values....										
	x,x	A	x,d4	W	A	d3,d2	A	d1,d0	W	A	P

With the *Write D0/D1 Memory* command n 20-bit memory cells in D0 can be initialized with new data.

Example: Write 80234_{hex} to D1:456 has the following I^2C protocol:

```
<3a 68 f0 00          write D1 memory
   00 01              1 word to write
   04 56              start address
   00 08              value = 80234hex
   02 34>
```

3.3.2.7. Short Write Memory (Codes $E4_{hex}$ and $F4_{hex}$)

S	DW	W	A	data_write	A	**e,4**	A	0,0	W	A
					A	n3,n2	A	n1,n0	W	A
					A	a3,a2	A	a1,a0	W	A
					A	d3,d2	A	d1,d0	W	A
	....repeat for n data values....									
					A	d3,d2	A	d1,d0	W	A	P

For faster access only the lower 16 bits of each memory cell are written. The 4 MSBs of the cell are cleared. The command uses the same codes E_{hex} and F_{hex} for D0/D1 as for the 20-bit command but followed by a 4 rather than a 0.

3.3.2.8. Clear SYNC Signal (Code 5_{hex})

S	DW	W	A	data_write	A	**5**,0	A	0,0	W	A	P

After a successful decoding of an MPEG frame the signal at pin SYNC rises and thus generates an interrupt event for the microcontroller. Issuing this command lets the signal at pin SYNC return to '0'.

3.3.2.9. Default Read

The *Default Read* command is the fastest way to get information from the MAS 35x9F. Executing the *Default Read* in a polling loop can be used to detect a special state during decoding.

S	DW	W	A	data_read	A	S	DR	W	A			
							d3,d2	A	d1,d0	W	N	P

The *Default Read* command immediately returns the lower 16 bit content of a specific RAM location as defined by the pointer D0:ffb. The pointer must be loaded before the first *Default Read* action occurs. If the MSB of the pointer is set, it points to a memory location in D1 rather than to one in D0.

Example: For watching D1:123 the pointer D0:ffb must be loaded with 8123_{hex}:

```
<DW 68 e0 00          write to D0 memory
    00 01             1 word to write
    0f fb             start address ffb
    00 08             value = 8...
    01 23>                ...0123hex
```

Now the *Default Read* commands can be issued as often as desired:

```
<DW 69 <DR            Default Read command
  dd dd >             16 bit content of the
                      address as defined by the
                      pointer
<DW 69 <DR dd dd >    ... and do it again
```

3.3.2.10. Fast Program Download (Code 6_{hex})

S	DW	W	A	data_write	A	**6**,n2	A	n1,n0	W	A	
						a3,a2	A	a1,a0	W	A	P

The *Fast Program Download* command introduces a data transfer via the parallel port. **n** = n2,n1,n0 denotes the number of 20-bit data words to be transferred, **a** = a3,a2,a1,a0 gives the start address. The data must be organized in two times five nibbles to get two words of 20-bit length. If the number n of 20-bit data words is odd, the very last word has to be padded with one additional nibble.

The download must be initiated in the following order:

– Issue *Freeze* command

– Stop all DMA-transfers

– Issue *Fast Program Download* command

– Download code via PIO-interface

– Switch appropriate memory area to act as program RAM (register ED_{hex})

– Issue a *Run* command to start program execution at entry point of downloaded code

Example for *Fast Program Download* command:
Download 5 words starting at D0:800,
then download 4 words starting at D1:200:

```
<DW 68 00 00>          Freeze

<DW 68 b3 b0 03 18>Stop all internal transfers
<DW 68 b4 30 03 00>
<DW 68 b4 b0 00 00>
<DW 68 b5 30 03 18>
<DW 68 b6 b0 00 00>
<DW 68 bb b0 03 18>
<DW 68 bc 30 03 00>
<DW 68 b0 60 00 00>

<DW 68 60 05           initiate download of 5 words
    08 00>             start at address D0:800
```

Now transfer 5 20-bit words via the parallel PIO-port:

```
d4,d3  d2,d1  d0,d4  d3,d2  d1,d0
d4,d3  d2,d1  d0,d4  d3,d2  d1,d0
d4,d3  d2,d1  d0,x
```

```
<DW 68 60 05           initiate download of 4 words
    82 00>             start at address D1:200
```

Now transfer 4 20-bit words via the parallel PIO-port:

```
d4,d3  d2,d1  d0,d4  d3,d2  d1,d0
d4,d3  d2,d1  d0,d4  d3,d2  d1,d0
```

```
<DW 68 b6 bc 00 00>switch the memory area
                   D0:800 ... D0:fff from
                   data to program usage

<DW 68 10 0a>      start program execution at
                   address D0:100a
```

3.3.2.11. Serial Program Download

Program downloads may also be performed via the I^2C-interface by using the *Write D0/D1 Memory* commands. A similar command sequence as in the Fast Program Download (*Freeze*, stop transfers...) applies.

3.3.2.12.Read IC Version (Code 7_{hex})

1) send command

S	DW	W	A	data_write	A	7,0	A	0,0	W	A	P

2) get version information

S	DW	W	A	data_read	A	S	DR	W	A		
						n3,n2	A	n1,n0	W	A	
						d3,d2	A	d1,d0	W	N	P

With this command the version of the IC is read in two 16 bit words. The first word **n** = n3,n2,n1,n0 contains the IC's major number (one nibble for each digit). The second word (**d** = d3,d2,d1,d0) returns the version as shown in Table 3–6.

Table 3–6: Second word of version information

Bit	Nibble	Content
15:12	d3	IC family derivate
11:8	d2	Coded character of order version (add 41_{hex} to the content of d2 to get ASCII)
7:0	d1,d0	Digit of order version

Example:

Read the version information for MAS 35x9F, derivate 0, order version B2:

```
<DW 68 70 00          send version command
<DW 69 <DR            and read
35 09                 MAS 3509F
01 02 >               derivate 0, version B2
                      (see Section 2.2. on page 8)
```

0 1	0 2	(hex)
0		Derivate (0..F)
1		Version character (0 = “A”,.., F = “P”)
	0 2	Version number (01..FF)

3.3.3. List of DSP Registers

The PSelect_Shadow register in Table 3–7 is used to switch four RAM areas from data to program usage and thus enabling the DSP's program counter to access downloaded program code stored at these locations. For normal operation (firmware in ROM), this register must be kept to zero.

Note: DSP registers not given in Table 3–7 must not be written.

3.3.4. List of DSP Memory Cells

Among the user interface control memory cells there are some which have a global meaning and some which control application specific parts of the DSP core. In Table 3–8 and Table 3–9, this is reflected by the key words All, MPEG, and G.729.

Table 3–7: Program Download registers

Address (hex)	R/W	Function	Mode	Default (hex)	Name
6B	R/W	**Configuration of Variable RAM Areas** Affected RAM area bit[19] D0:800 ... D0:BFF bit[18] D0:C00 ... D0:FFF bit[17] D1:800 ... D1:BFF bit[16] D1:C00 ... D1:FFF For details of program code download please refer to Section 3.3.2.10. on page 30.	**Download**	0000	PSelect_Shadow

3.3.4.1. Application Selection and Application Running

The AppSelect cell is a global user interface configuration cell, which has to be written in order to start a specific application.

The AppRunning cell is a global user interface status cell, which indicates, which application loop is actually running.

1. Write “0” to AppSelect
2. Check AppRunning for “0”
3. Write value to AppSelect according to Table 3–8 (determines start time of Application program)
4. Apply necessary/wanted control settings (D0:346..357)

3.3.4.2. Application Specific Control

The configuration of the MPEG Layer 2/3, AAC decoding and the G.729 codec firmware is done via the control memory cells described in Table 3–9. The changes applied to any of the control memory cells have to be validated by setting bit[0] of memory cell Main I/O Control. This bit will be reset automatically after the changes have been taken over by the DSP.

The status memory cells in Table 3–11 are used to read the decoder status and to get additional MPEG bitstream information.

Note: DSP memory cells not given in Table 3–8 or Table 3–9 must not be written.

Table 3–8: D0 control memory cells: mode selection

Memory Address (hex)	Function	Name
D0:34b	**Application Selection** **All** AppSelect is used for selecting an application. This is done by setting the appropriate bit to one. It is principally allowed to set more than one bit to one, e.g. setting AppSelect to $1C_{hex}$ will select all MPEG audio decoders. The auto-detection feature will automatically detect the Layer 2, Layer 3, or AAC data. Setting bit[0] or bit[1] will make the DSP loop in the OS loop or the Top Level loop respectively. To add/remove MPEG layers while running in MPEG decoding mode (e.g. change from Layer 2, Layer 3 ($0C_{hex}$) to Layer 2, Layer 3, AAC ($1C_{hex}$)), the application selection has to be reset to 00_{hex} before writing the new value. bit[5] G.729 Codec bit[4] MPEG AAC Decoder bit[3] MPEG Layer 3 Decoder bit[2] MPEG Layer 2 Decoder bit[1] Top Level bit[0] Operating System	AppSelect
D0:34c	**Application Running** **All** The AppRunning cell is a global user interface status cell, that indicates which application loop is actually running. Prior to writing any of the configuration registers or memory cells (except AppSelect), it has to be checked whether the appropriate bit(s) in the AppRunning cell is set. bit[5] G.729 Codec bit[4] MPEG AAC Decoder bit[3] MPEG Layer 3 Decoder bit[2] MPEG Layer 2 Decoder bit[1] Top Level bit[0] Operating System	AppRunning

Table 3–9: D0 control memory cells

Memory Address (hex)	Function	Name
D0:346	**Main I/O Control** (reset = 8025_{hex}) **MPEG** IOControlMain is used for selecting/deselecting the appropriate data input interface and for setting up the serial data output interface. In serial input mode the coded audio data (Layer 2, Layer 3, AAC) is expected at the serial input interface SDIB (default). In the 8-bit-parallel input mode the PIO pins PI[19:12] are used. bit[15] MP3 block input selection 0: MP3 block input mode OFF 1: MP3 block input mode ON bit[14] Invert serial output clock (SOC) 0 (reset) do not invert SOC 1 invert SOC bit[13:12] Reserved, must be set to zero bit[11] Serial data output delay 0 (reset) no additional delay (reset) 1 additional delay of data related to word strobe bit[10] Reserved, must be set to zero bit[9:8] Input Select Main 00 (reset) serial input at interface B 01 parallel input at PIO pins PI[19...12] 10 reserved for future use 11 reserved for future use bit[7:6] Reserved, must be set to zero bit[5] SDO Word Strobe Invert 0 do not invert 1 (reset) invert outgoing word strobe signal bit[4] Bits per Sample at SDO 0 (reset) 32 bits/sample 1 16 bits/sample bit[3] Reserved, must be set to zero bit[2] Serial data input interface B clock invert (pin SIBC) 0 not inverted (data latched at rising clock edge) 1 (reset) incoming clock signal is inverted (data latched at falling clock edge) bit[1] 0 (reset) DEMAND MODE (PLL off, MAS 35x9F is clock master) 1 BROADCAST MODE (PLL on, clock of MAS 35x9F locks on data stream) bit[0] Validate 0 (reset) no forced evaluation of control memory cells 1 changes in control memory will become effective Bit[0] is reset after the DSP has recognized the changes. The controller should set this bit after the other D0 control memory cells have been initialized with the desired values.	IOControlMain

Table 3–9: D0 control memory cells, continued

Memory Address (hex)	Function	Name
D0:347	**Interface Status Control** (reset = 05_{hex}) **MPEG** This control cell allows to enable/disable the data I/O interfaces. In addition, the clock of the output data interface interfaces, S/PDIF and SDO, can be set to a low-impedance mode. bit[6] S/PDIF input selection (used for download modules) 0 (reset) select S/PDIF input 1 1 select S/PDIF input 2 bit[5] Enable/disable S/PDIF output 0 (reset) enable S/PDIF output 1 S/PDIF output (invalid) bit[4] Reserved, must be set to zero bit[3] Enable/disable serial data output SDO 0 (reset) SDO valid data 1 SDO invalid data bit[2] Output clock characteristic (SDO and S/PDIF outputs) 0 low impedance 1 (reset) high impedance bit[1] reserved, must be set to zero bit[0] Enable/Disable SDI[1)] 0 enable 1 (reset) disable Both digital outputs, S/PDIF and I^2S, and the D/A converters may use the decoded audio independent of each other. Changes at this memory address must be validated by setting bit[0] of D0:346_{hex}.	InterfaceControl
D0:348	**Oscillator Frequency** (reset = 18432_{dec}) **All** bit[19:0] oscillator frequency in kHz In order to achieve a correct internal operating frequency of the DSP, the nominal crystal frequency has to be deposited into this memory cell. Changes at this memory address must be validated by setting bit[0] of D0:346_{hex}.	OfreqControl

[1)] **Note:** The pins SIC, SII, SID are switched to output mode, if bit [0] = 1 (Reset value).

Table 3–9: D0 control memory cells, continued

Memory Address (hex)	Function	Name
D0:349	**Output Clock Configuration** (affects pin CLKO) (reset = 80000_{hex}) **All** bit[19] CLKO configuration 0 output clock signal at CLKO 1 (reset) CLKO is tristate The CLKO output pin of the MAS 35x9F can be disabled via bit[19]. bit[18] Reserved, must be set to zero bit[17] Additional division by 2 if scaler is on (bit[8] cleared) 0 (reset) oversampling factor 512/768 1 oversampling factor 256/384 bit[16:9] Reserved, must be set to zero bit[8] Output clock scaler 0 (reset) set output clock according to audio sample rate (see Table 2–1) 1 output clock fixed at 24.576 or 22.5792 MHz For a list of output frequencies at pin CLKO please refer to Table 2–1. bit[7:0] reserved, must be set to zero Changes at this memory address must be validated by setting bit[0] of D0:346.	OutClkConfig
D0:350	**Soft Mute** **MPEG** %0 (reset) mute off %1 mute on	SoftMute
D0:351	**S/PDIF channel status bits category code setting** (reset = 8200_{hex}) **All**	SpdOutBits

Table 3–9: D0 control memory cells, continued

Memory Address (hex)	Function	Name
D0:34d	**Operation Mode Selection** (reset = 0_{hex}) **G.729** The register is used to switch between basic G.729 operation modes. bit[19:7] Reserved, set to 0 bit[6] Page headers 0 enable 1 disable If the page headers bit is 0, a header frame is transfered before each page of 50 data frames. If the header bit is 1, all the frames are G.729 data frames. Please (see Section 3.3.8. on page 44). bit[5:4] Decoding speed 00 8 kHz (normal) 01 6 kHz (slow) 10 12 kHz (fast) 11 not allowed The recording (encoding) is always done with a sampling rate of 8 kHz. During decoding this control can be used to speed up or slow down the playback. bit[3] Reserved, set to 0 bit[2] Pause encoder/decoder 0 normal operation 1 pause If the pause bit is set, the processing continues until the current page is finished and then en-/decoding is paused. The pause mode lasts until the pause bit is cleared again or the mode is set to 0. bit[1:0] Mode 00 idle 01 decode 10 not allowed 11 encode To switch to **encoder** operation mode, UserControl has to be set to 3_{hex}. Then 50 frames are encoded and sent via the PIO interface. This is repeated until the UserControl register is changed. If the transmission of headers is enabled, each page of 50 frames is preceeded by a header frame as shown in Fig. 3–4 on page 44. To switch to **decoder** operation mode, UserControl has to be set to 1_{hex}. For decoding with slow speed, UserControl must be 11_{hex}, for decoding with fast speed it must be 21_{hex}. Then the decoder is requesting several frames via the PIO interface to fill its internal buffer. If enough data is available, 50 frames are decoded. This is repeated until the UserControl register is changed. If the transmission of headers is enabled, a header frame has to be sent before each page of 50 frames (see Fig. 3–4 on page 44). To switch off the encoder or decoder, UserControl has to be set to 0_{hex}. Then the encoding/decoding and sending/receiving of frames continues until the end of the current page and the operation mode is set to stop.	UserControl

Table 3–9: D0 control memory cells, continued

Memory Address (hex)	Function	Name
D0:34e	**I^2S Audio Input/Output Interface** (reset = 60_{hex}) **G.729** bit[19:15] Reserved, set to 0 bit[14] Output clock signal 0 standard signal 1 inverted signal bit[13] Reserved, set to 0 bit[12] Additional delay of input data related to word strobe 0 no delay 1 1 bit delay bit[11] Additional delay of output data related to word strobe 0 no delay 1 1 bit delay bit[10:7] Reserveded, set to 0 bit[6] Input word strobe signal 0 standard signal 1 inverted signal bit[5] Output word strobe signal 0 standard signal 1 inverted signal bit[4] Wordlength 0 32 bits/sample 1 16 bits/sample This setting affects the wordlength on the SDI and SDO interfaces. bit[3] Input clock signal 0 standard signal 1 inverted signal bit[2:0] Reserved, set to 0 Changes become effective when the codec is started or the mode is changed by writing to the UserControl memory cell.	SDISDOConfig

Table 3–9: D0 control memory cells, continued

Memory Address (hex)	Function		Name
D0:34f	**Interface Status Control** (reset = 25_{hex}) This control cell is used to enable/disable interfaces in G.729 mode. bit[6],[4] reserved, must be set to zero bit [5] reserved, must be set to one bit[3] Enable/disable serial data output SDO 0 (reset) SDO valid data 1 SDO invalid data bit[2] Output clock characteristic (SDO and S/PDIF outputs) 0 low impedance 1 (reset) high impedance bit[1] reserved, must be set to zero bit[0] Enable/Disable SDI[1)] 0 enable 1 (reset) disable	**G.729**	g729_InterfaceControl
D0:352	**Volume input control: left gain** (reset=80000_{hex})	**G.729**	in_L
D0:353	**Volume input control: right gain** (reset=0_{hex})	**G.729**	in_R
D0:354	**Volume output control: left → left gain** (reset=80000_{hex})	**All**	out_LL
D0:355	**Volume output control: left → right gain** (reset=0_{hex})	**All**	out_LR
D0:356	**Volume output control: right → left gain**(reset=0_{hex})	**All**	out_RL
D0:357	**Volume control: right → right gain** (reset=80000_{hex})	**All**	out_RR

[1)] **Note:** The pins SIC, SII, SID are switched to output mode, if bit [0] = 1 (Reset value).

Table 3–10: MP3 block input mode user interface (all addresses in hex notation)

Addr.	Name	Description
D0:346	IOControlMain	bit[15] MP3 block input select 0: MP3 block input mode OFF 1: MP3 block input mode ON works for input at serial input interface B (bit[9:8] of IOControlMain = 00_{bin}) Reset value is 0x8024 (see Table 3–2).
R0:68	MP3BlockConfig	bit[17] data end bit Disables resync timeout. Should be set by the controller at the end of an input file (file end, stop, or pause) when the last requested data block has been fully sent. 0: resync timeout enabled 1: resync timeout disable ↔ no wait for end of block bit[16] reserved, set to “0” bit[15] start data request 0: MP3 decoder does not send data requests (wait loop) 1: MP3 decoder in operational mode, new input data will be requested via pulses at the demand pin. bit[14:0] input block size specific value, do not modify Reset value is 0x6670. To set the start bit, the controller must write 0xe670.
R0:7e	PulseDelayCounter	bit[13:0] determines the variable fraction of the demand pulse length. pulseLenVar[ns] = value * 88.58.
D0:34e	ResyncTimeout	bit[19:0] timeout after resync: timeout[µs] = value * 3.32. The default value is 2^{19}-1, which results in a timeout of 1.74 seconds. For an optimized resync behavior, it is recommended to set this value to zero.
R0:5b	SerialInConfig	bit[14:0] configuration of the serial input interface
D0:350	SoftMute	bit[0] MP3 soft mute 0: audio output on 1: audio output soft muted

Table 3–11: D0 status memory cells

Memory Address	Function	Name
D0:FCF	**AAC bitrate in bit/s**	AACbitrate
D0:FD0	**MPEG Frame Counter** bit[19:0] number of MPEG frames after synchronization The counter will be incremented with every new frame that is decoded. With an invalid MPEG bit stream at its input (e.g. an invalid header is detected), the MAS 35x9F resets the MPEGFrameCount to '0'.	MPEGFrameCount
D0:FD1	**MPEG Header and Status Information** bit[15] reserved, must be set to zero bit[14:13] MPEG ID, Bits 12, 11 of the MPEG header 00 MPEG 2.5 01 reserved 10 MPEG 2 11 MPEG 1 not valid in case of AAC decoding (bit[12:11] = 00) bit[12:11] Bits 14 and 13 of the MPEG header 00 AAC 01 Layer 3 10 Layer 2 11 Layer 1 bit[10] CRC Protection 0 bitstream protected by CRC 1 bitstream not protected by CRC bit[9:2] Reserved bit[1] CRC error 0 no CRC error 1 CRC error bit[0] Invalid frame 0 no invalid frame´ 1 invalid frame This location contains bits 15...11 of the original MPEG header and other status bits. It will be set each frame directly after the header has been decoded from the bit stream.	MPEGStatus1

Table 3–11: D0 status memory cells, continued

Memory Address	Function	Name
D0:FD2	**MPEG Header Information** bit[15:12] MPEG Layer 2/3 Bitrate 0000 free / free / free 0001 32 / 32 / 8 0010 48 / 40 / 16 0011 56 / 48 / 24 0100 64 / 56 / 32 0101 80 / 64 / 40 0110 96 / 80 / 48 0111 112 / 96 / 56 1000 128 / 112 / 64 1001 160 / 128 / 80 1010 192 / 160 / 96 1011 224 / 192 / 112 1100 256 / 224 / 128 1101 320 / 256 / 144 1110 384 / 320 / 160 1111 forbidden / forbidden / forbidden (MPEG1, L2 / MPEG1, L3 / MPEG2+2.5, L2/3) bit[13:10] Sampling frequency for MPEG2-AAC in Hz 0000..0010 reserved 0011 48000 0100 44100 0101 32000 0110 24000 0111 22050 1000 16000 1001 12000 1010 11025 1011 8000 1100..1111 reserved ...	MPEGStatus2

Table 3–11: D0 status memory cells, continued

Memory Address	Function	Name
D0:FD2 (continued)	**MPEG Header Information, continued** bit[11:10] Sampling frequencies in Hz 00: MPEG1 44100, MPEG2 22050, MPEG2.5 11025 01: MPEG1 48000, MPEG2 24000, MPEG2.5 12000 10: MPEG1 32000, MPEG2 16000, MPEG2.5 8000 11: MPEG1 reserved, MPEG2 reserved, MPEG2.5 reserved bit[9] Padding Bit bit[8] reserved bit[7:6] Mode 00 stereo 01 joint_stereo (intensity stereo / m/s stereo) 10 dual channel 11 single channel bit[5:4] Mode extension (applies to joint stereo only) 00: intensity stereo off, m/s stereo off 01: intensity stereo on, m/s stereo off 10: intensity stereo off, m/s stereo on 11: intensity stereo on, m/s stereo on bit[3] Copyright Protect Bit 0/1 not copyright protected/copyright protected bit[2] Copy/Original Bit 0/1 bitstream is a copy/bitstream is an original bit[1:0] Emphasis, indicates the type of emphasis 00 none 01 50/15 µs 10 reserved 11 CCITT J.17 This memory cell contains the 16 LSBs of the MPEG header. It will be set directly after synchronizing to the bit stream. Note that for AAC four bits are needed to define the sampling frequency while for Layer2/Layer3 two bits are sufficient. This leads to an inconsistency in the format of bits 13...10.	MPEGStatus2
D0:FD3	**MPEG CRC Error Counter** The counter will be increased by each CRC error detected in the MPEG bis-stream. It will not be reset when losing the synchronization.	CRCErrorCount
D0:FD4	**Number of Bits in Ancillary Data** Number of valid ancillary bits in the current MPEG frame.	NumberOfAncillary-Bits
D0:FD5 ... D0:FF1	**Ancillary Data** (see Section 3.3.6. on page 43).	AncillaryData

3.3.5. Ancillary Data

The memory fields D0:FD5...D0:ff1 contain the ancillary data. It is organized in 28 words of 16 bit each. The last ancillary bit of a frame is placed at bit 0 in D0:FD5. The position of the first ancillary data bit received can be located via the content of NumberOfAncillaryBits because

int[(NumberOfAncillaryBits-1)/16] + 1

of memory words are used.

Example:

First get the content of 'NumberOfAncillaryBits'

```
<DW 68 c4 00 00 01 0f d4>
<DW 69 <DR dd dd>
```

Assume that the MAS 35x9F has received 19 ancillary data bits. Therefore, it is necessary to read two 16-bit words:

```
<DW 68 c4 00      Short Read from D0
  00 02 0f d5>    read 2 words starting at D0:fd5
<DW 69 <DR dd dd
           dd dd>
                  receive the 2 16-bit words
```

The first bit received from the MPEG source is at position 2 of D0:FD6; the last bit received is at the LSB of D0:fd5.

3.3.6. Reading of the Memory Cells "Number of Bits in Ancillary Data" and "Ancillary Data"

When in Broadcast Mode, reading of the cells "Number of Bits in Ancillary Data" and "Ancillary Data" will lead to unpredictable results. These cells are described in Table 3–11 on page 43.

The same applies to the "Number of Bits in Ancillary Data" and "Ancillary Data" of the preliminary data sheet MAS 3587F.

Table 3–12: Content of D0:fd5 after reception of 19 ancillary bits.

D0:fd5	MSB	14	13	12	11	10	9	8	7	6	5	4	3	2	1	LSB
Ancillary Data	4th bit	5th bit	6th bit	...	...	...	...	...	...	...	...	...	...	17th bit	18th bit	last bit

Table 3–13: Content of D0:fd6 after reception of 19 ancillary bits.

D0:fd6	MSB	14	13	12	11	10	9	8	7	6	5	4	3	2	1	LSB
Ancillary Data	x	x	x	x	x	x	x	x	x	x	x	x	x	first bit	2nd bit	3rd bit

3.3.7. DSP Volume Control

The digital baseband volume matrix is used for controlling the digital gain as shown in Fig. 3–3. This volume control is effective on both, the digital audio output and the data stream to the D/A converters. The values are in 20-bit 2's complement notation.

Table 3–14 shows the proposed settings for the 4 volume matrix coefficients for stereo, left and right mono. The gain factors are given in fixed point notation ($-1.0 \times 2^{19} = 80000_{hex}$).

If channels are mixed, care must be taken to prevent clipping at high amplitudes. Therefore, the sum of the absolute values of coefficients for one output channel must be less than 1.0.

For normal operating conditions it is recommended to use the main volume control of the audio codec instead (register 00 10_{hex} of the audio codec).

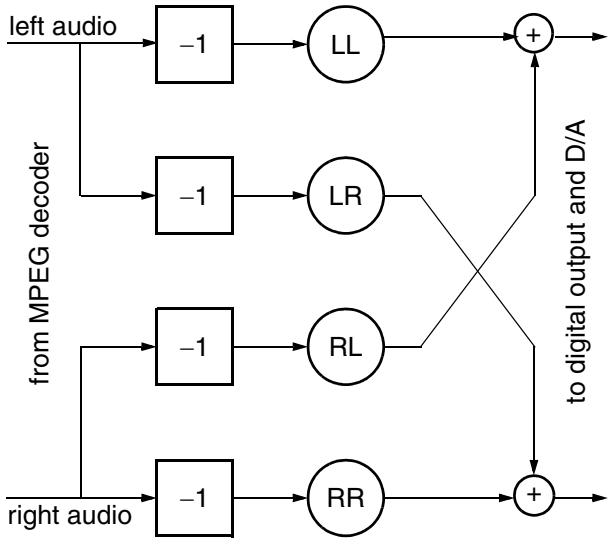


Fig. 3–3: Digital volume matrix

Table 3–14: Settings for the digital volume matrix

Memory	D0:354	D0:355	D0:356	D0:357
Name	LL	LR	RL	RR
Stereo (default)	−1.0	0	0	−1.0
Mono left	−1.0	−1.0	0	0
Mono right	0	0	−1.0	−1.0

3.3.8. Explanation of the G.729A Data Format

The codec is working on a page basis where the encoding and decoding is performed in blocks of 50 G.729 frames, whereas each frame consists of 10 bytes in byte-swapped order (see Fig. 3–4). Therefore most changes to the UserControl register become effective when processing of the current page is finished. The pages are optionally preceeded by 10 byte header frames (see Table 3–15).

Table 3–15: Content of page header

Byte	1	2	3	4	5	6	7	8	9	10
Value (hex)	64	6d	72	31	64	61	74	61	F4	01

Switching directly from encoding to decoding mode (or vice versa) is not allowed. Instead, the controller has to send a stop request to the MAS 35x9F (writing 0_{hex} to UserControl) and must keep on sending data in decoding mode or receive data in encoding mode until the current page of 50 frames is finished. After this run-out time, the encoding or decoding can be started again.

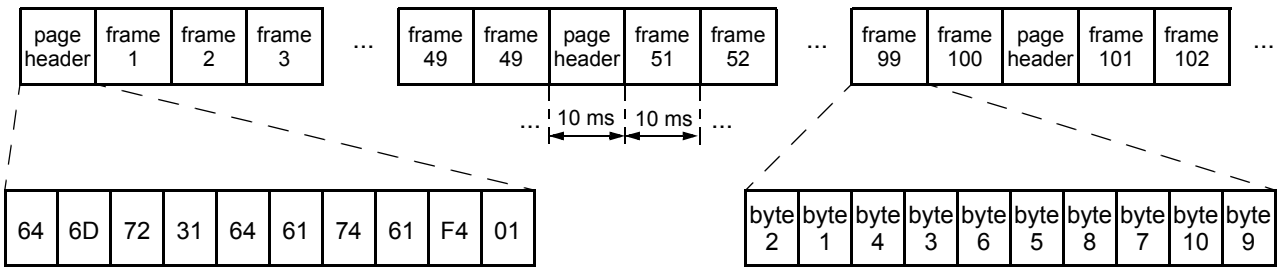


Fig. 3–4: Schematic timing of the data transmission with preceeding header

3.4. Audio Codec Access Protocol

The MAS 35x9F has 16-bit wide registers for the control of the audio codec. These registers are accessed via the I^2C subaddresses codec_write ($6C_{hex}$) and codec_read ($6D_{hex}$).

3.4.1. Write Codec Register

S	DW	W	A	codec_write	A	r3,r2	A	r1,r0	A	
						d3,d2	A	d1,d0	A	P

The controller writes the 16-bit value (**d** = d3,d2,d1,d0) into the MAS 35x9F codec register (**r** = r3,r2,r1,r0). A list of registers is given in Table 3–16.

Example: Writing the value 1234_{hex} into the codec register with the number 00 $1B_{hex}$:

```
<DW 6c 00 1b 12 34>
```

3.4.2. Read Codec Register

1) send command

S	DW	W	A	codec_write	A	r3,r2	A	r1,r0	A	P

2) get register value

S	DW	W	A	codec_read	A	S	DR	W	A	
					d3,d2	A	d1,d0	N	P	

Reading the codec registers also needs a set-up for the register address and an additional start condition during the actual read cycle. A list of status registers is given in Table 3–17.

3.4.3. Codec Registers

Table 3–16: Codec control registers on I^2C subaddress $6C_{hex}$

Register Address (hex)	Function	Name
CONVERTER CONFIGURATION		
00 00	**Audio Codec Configuration** 0 dB is related to the D/A full-scale output voltage Please refer to (see Section 4.6.3. on page 81). bit[15:12] A/D converter left amplifier gain = n*1.5−3 [dB] bit[11:8] A/D converter right amplifier gain = n*1.5−3 [dB] 1111 +19.5 dB 1110 +18.0 dB ... ... 0011 +1.5 dB 0010 0.0 dB 0001 −1.5 dB 0000 − 3.0 dB bit[7:4] Microphone amplifier gain = n*1.5+21 [dB] 1111 +43.5 dB 1110 +42.0 dB ... ... 0001 +22.5 dB 0000 +21.0 dB bit[3] Input selection for left A/D converter channel 0 line-in 1 microphone bit[2] Enable left A/D converter[1)] bit[1] Enable right A/D converter[1)] bit[0] Enable D/A converter[1)]	CONV_CONF

[1)] The generation of the internal DC reference voltage for the D/A converter is also controlled with this bit. In order to avoid click noise, the reference voltage at pin AGNDC should have reached a near ground potential before repowering the D/A converter after a short down phase.

Alternatively, at least one of the A/D converters (bits[2] or [1]) should remain set during short power-down phases of the D/A. Then the DC reference voltage generation for the D/A converter will not be interrupted.

Table 3–16: Codec control registers on I^2C subaddress $6C_{hex}$, continued

Register Address (hex)	Function	Name
INPUT MODE SELECT		
00 08	**Input Mode Setting** bit[15] Mono switch 0 stereo input mode 1 left channel is copied into the right channel bit[14:2] Reserved, must be set to 0 bit[1:0] Deemphasis select 0 deemphasis off 1 deemphasis 50 µs 2 deemphasis 75 µs	ADC_IN_MODE
OUTPUT MODE SELECT		
	D/A Converter Source Mixer	
00 06	**MIX ADC scale**	DAC_IN_ADC
00 07	**MIX DSP scale**	DAC_IN_DSP
	bit[15:8] Linear scaling factor (hex) 0 off 20 50 % (−6 dB gain) 40 100 % (0 dB gain) 7f 200 % (+6 dB gain) In the sum of both mixing inputs exceeds 100 %, clipping may occur in the successive audio processing.	
00 0E	**D/A Converter Output Mode** bit[15] Mono switch 0 stereo through 1 mono matrix applied bit[14] Invert right channel 0 through 1 right channel is inverted bit[1:0] Reserved, must be set to 0 In order to achieve more output power a single loudspeaker can be connected as a bridge between pins OUTL and OUTR. In this mode bit[15] and bit[14] must be set.	DAC_OUT_MODE

Table 3–16: Codec control registers on I^2C subaddress $6C_{hex}$, continued

Register Address (hex)	Function	Name
BASEBAND FEATURES		
00 14	**Bass** bit[15:8] Bass range 60_{hex} +12 dB 58_{hex} +11 dB ... 08_{hex} +1 dB 00_{hex} 0 dB $F8_{hex}$ −1 dB ... $A8_{hex}$ −11 dB $A0_{hex}$ −12 dB Higher resolution is possible, one LSB step results in a gain step of about 1/8 dB. With positive bass settings clipping of the output signal may occur. Therefore, it is not recommended to set bass to a value that, in conjunction with volume, would result in an overall positive gain. The settings require: max (bass, treble) + loudness + volume ≤ 0 dB bit[7:0] Not used, must be set to 0	BASS
00 15	**Treble** bit[15:8] Treble range 60_{hex} +12 dB 58_{hex} +11 dB ... 08_{hex} +1 dB 00_{hex} 0 dB $F8_{hex}$ −1 dB ... $A8_{hex}$ −11 dB $A0_{hex}$ −12 dB Higher resolution is possible, one LSB step results in a gain step of about 1/8 dB. With positive treble settings, clipping of the output signal may occur. Therefore, it is not recommended to set treble to a value that, in conjunction with loudness and volume, would result in an overall positive gain. The settings require: max (bass, treble) + loudness + volume ≤ 0 dB bit[7:0] Not used, must be set to 0	TREBLE

Table 3–16: Codec control registers on I^2C subaddress $6C_{hex}$, continued

Register Address (hex)	Function	Name
00 1E	**Loudness** bit[15:8] Loudness Gain 44_{hex} +17 dB 40_{hex} +16 dB ... 04_{hex} +1 dB 00_{hex} 0 dB bit[7:0] Loudness Mode 00_{hex} normal (constant volume at 1 kHz) 04_{hex} Super Bass (constant volume at 2 kHz) Higher resolution of Loudness Gain is possible: An LSB step results in a gain step of about 1/4 dB. Loudness increases the volume of low- and high-frequency signals, while keeping the amplitude of the 1-kHz reference frequency constant. The intended loudness has to be set according to the actual volume setting. Because loudness introduces gain, it is not recommended to set loudness to a value that, in conjunction with volume, would result in an overall positive gain. The settings should be: max (bass, treble) + loudness + volume $\leq$ 0 dB The corner frequency for bass amplification can be set to two different values. In Super Bass mode, the corner frequency is shifted up. The point of constant volume is shifted from 1 kHz to 2 kHz.	LDNESS

Table 3–16: Codec control registers on I^2C subaddress $6C_{hex}$, continued

Register Address (hex)	Function	Name
Micronas Bass (MB)		
00 22	**MB Effect Strength** bit[15:8] 00_{hex} MB off (default) $7F_{hex}$ maximum MB The MB effect strength can be adjusted in 1dB steps. A value of 40_{hex} will yield a medium MB effect.	MB_STR
00 23	**MB Harmonics** bit[15:8] 00_{hex} no harmonics are added (default) 64_{hex} 50% fundamentals + 50% harmonics $7F_{hex}$ 100% harmonics The MB exploits the psychoacoustic phenomenon of the 'missing fundamental by creating harmonics of the frequencies below the center frequency of the bandpass filter (MB_FC). This enables a loudspeaker to display frequencies that are below its cutoff frequency. The Variable MB_HAR describes the ratio of the harmonics towards the original signal.	MB_HAR
00 24	**MB Center Frequency** bit[15:8] 2 20 Hz 3 30 Hz ... 30 300 Hz The MB Center Frequency defines the center frequency of the MB bandpass filter (see Fig. 3–5 on page 52). The center frequency should approximately match the cutoff frequency of the loudspeakers. For high end loudspeakers, this frequency is around 50 Hz, for low end speakers around 90 Hz	MB_FC
00 21	**MB Shape** bit[15:8] 5...30 corner frequency in 10-Hz steps (range: 50...300 Hz) With a second lowpass filter the steepness of the falling edge of the MB bandpass can be increased (see Fig. 3–5 on page 52). Choosing the corner frequency of this filter close to the center frequency of the bandpass filter (MB_FC) results in a narrow MB frequency range. The smaller this range, the harder the bass sounds. The recommended value is around 1.5 × MB_FC	MB_SHAPE
	MB Switch bit[7:2] reserved, must be set to zero bit[1] MB switch 0 MB off 1 MB on bit [0] reserved,must be set to zero	MB_SWITCH

Table 3–16: Codec control registers on I^2C subaddress $6C_{hex}$, continued

Register Address (hex)	Function	Name
VOLUME		
00 12	**Automatic Volume Correction (AVC) Loudspeaker Channel** bit[15:12] 0_{hex} AVC off (and reset internal variables) 8_{hex} AVC on bit[11:8] 8_{hex} 8 s decay time 4_{hex} 4 s decay time 2_{hex} 2 s decay time 1_{hex} 20 ms decay time (intended for quick adaptation to the average volume level after track or source change) **Note:** To reset the internal variables, the AVC should be switched off and then on again during any track or source change. For standard applications, the recommended decay time is 4 s.	AVC
00 11	**Balance** bit[15:8] Balance range $7F_{hex}$ left −127 dB, right 0 dB $7E_{hex}$ left −126 dB, right 0 dB ... 01_{hex} left −1 dB, right 0 dB 00_{hex} left 0 dB, right 0 dB FF_{hex} left 0 dB, right −1 dB ... 81_{hex} left 0 dB, right −127 dB 80_{hex} left 0 dB, right −128 dB Positive balance settings reduce the left channel without affecting the right channel; negative settings reduce the right channel leaving the left channel unaffected.	BALANCE
00 10	**Volume Control** bit[15:8] Volume table with 1 dB step size $7F_{hex}$ +12 dB (maximum volume) $7E_{hex}$ +11 dB ... 74_{hex} +1 dB 73_{hex} 0 dB 72_{hex} −1 dB ... 02_{hex} −113 dB 01_{hex} −114 dB 00_{hex} mute (reset) bit[7:0] Not used, must be set to 0 This main volume control is applied to the analog outputs only. It is split between a digital and an analog function. In order to avoid noise due to large changes of the setting, the actual setting is internally low-pass filtered. With large scale input signals, positive volume settings may lead to signal clipping.	VOLUME

Table 3–17: Codec status registers on I^2C subaddress $6D_{hex}$

Register Address (hex)	Function	Name
INPUT QUASI-PEAK		
00 0A	**A/D Converter Quasi-Peak Detector Readout Left** bit[14:0] positive 15-bit value, linear scale 0000 0% 2000 25% (–12 dBFS) 4000 50% (–6 dBFS) 7FFF 100% (0 dBFS)	QPEAK_L
00 0B	**A/D Converter Quasi-Peak Detector Readout Right** bit[14:0] positive 15-bit value, linear scale 0000 0% 2000 25% (–12 dBFS) 4000 50% (–6 dBFS) 7FFF 100% (0 dBFS)	QPEAK_R
OUTPUT QUASI-PEAK		
00 0C	**Audio Processing Input Quasi-Peak Detector Readout Left** bit[14:0] positive 15-bit value, linear scale	DQPEAK_L
00 0D	**Audio Processing Input Quasi-Peak Detector Readout Right** bit[14:0] positive 15-bit value, linear scale	DQPEAK_R

3.4.4. Basic MB Configuration

With the parameters described in Table 3–16, the Micronas Bass system (MB) can be customized to create different bass effects, as well as to fit the MB to various loudspeaker characteristics. The easiest way to find a good set of parameter is by selecting one of the settings below, listening to music with strong bass content and adjusting the MB parameters:

- MB_STR: Increase/decrease the strength of the MB effect
- MB_HAR: Increase/decrease the content of low frequency harmonics
- MB_FC: Shift the MB effect to lower/higher frequencies
- MB_SHAPE: Widen/narrow MB frequency range (which results in a softer/harder bass sound), turn on/off the MB

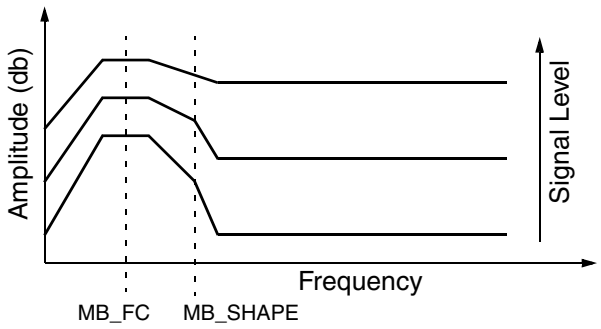


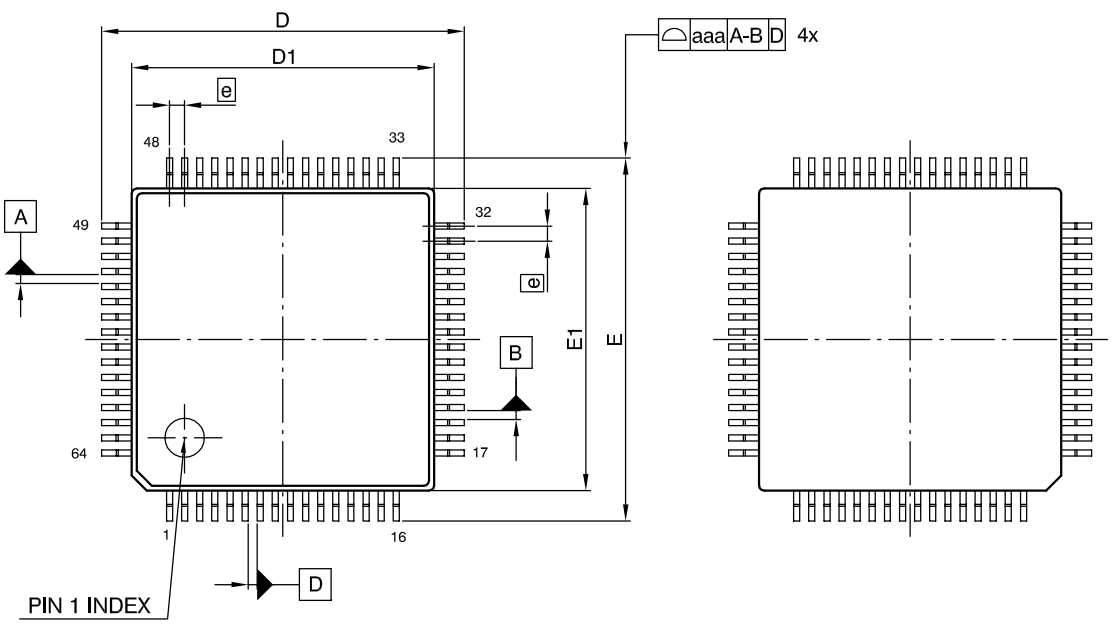
Fig. 3–5: Micronas Bass (MB): Bass boost in relation to input signal level

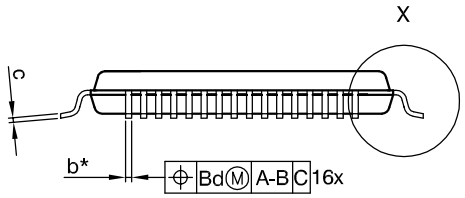
Table 3–18: Suggested MB settings

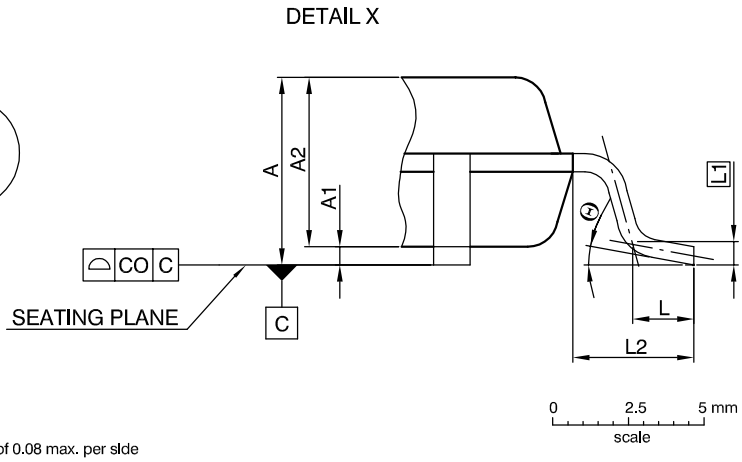
Function	MB_STR (22_{hex})	MB_HAR (23_{hex})	MB_FC (24_{hex})	MB_SHAPE (21_{hex})
MB off	$xxxx_{hex}$	$xxxx_{hex}$	$xxxx_{hex}$	$xx00_{hex}$
Low end headphones, medium effect	5000_{hex}	3000_{hex}	0600_{hex}	0902_{hex}

4. Specifications

4.1. Outline Dimensions







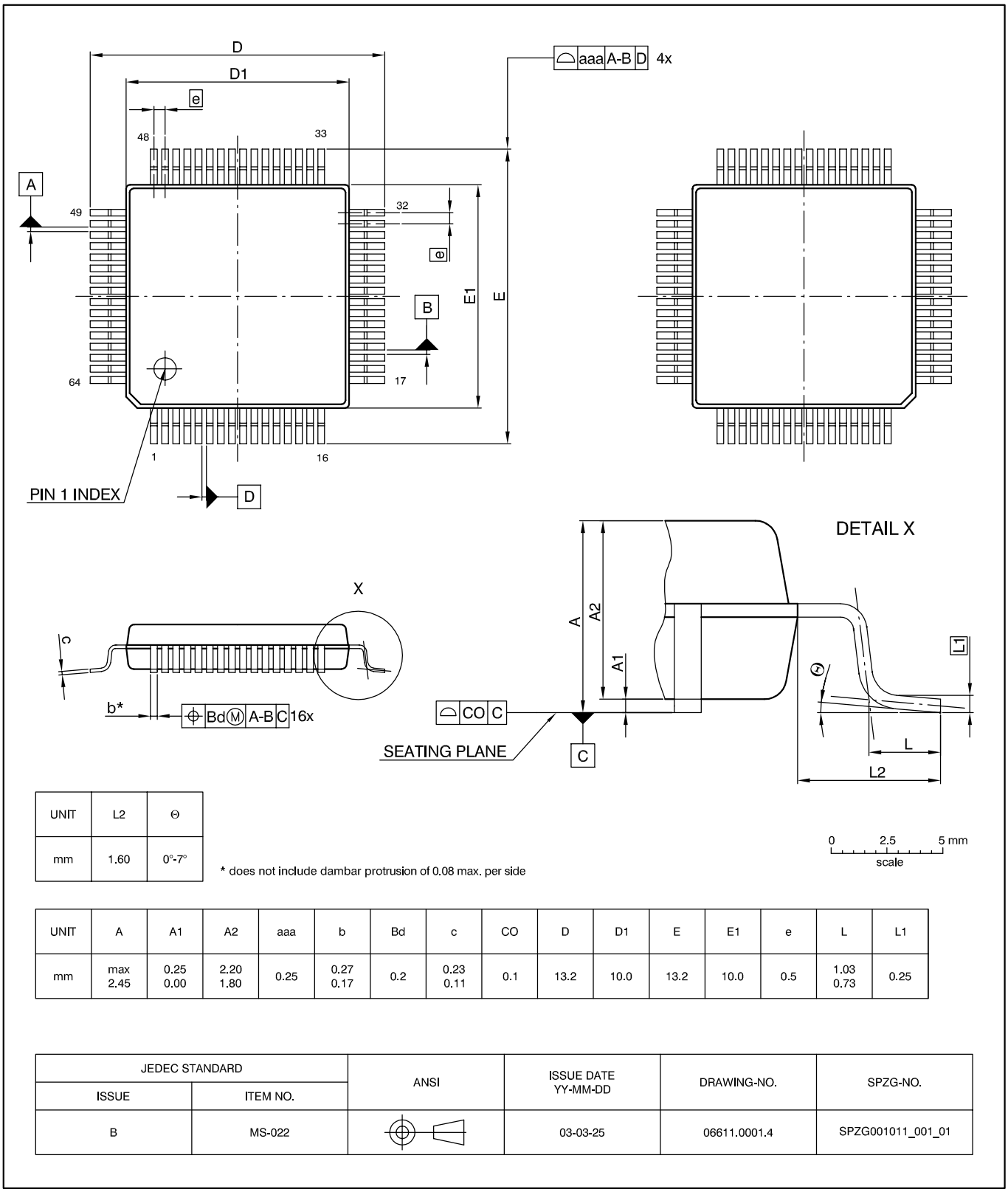
UNIT	L2	Θ
mm	1.0	0°-7°

* does not include dambar protrusion of 0.08 max. per side

UNIT	A	A1	A2	aaa	b	Bd	c	CO	D	D1	E	E1	e	L	L1
mm	max 1.6	0.15 0.05	1.45 1.35	0.2	0.27 0.17	0.08	0.20 0.09	0.08	12.0	10.0	12.0	10.0	0.5	0.75 0.45	0.25

JEDEC STANDARD		ANSI	ISSUE DATE YY-MM-DD	DRAWING-NO.	SPZG-NO.
ISSUE	ITEM NO.				
C	MS-026		03-04-17	06621.0001.4	SPZG001021_001_01

Fig. 4–1:
PLQFP64-1: Plastic **L**ow **Q**uad **F**lat **P**ackage, **64** leads, 10 × 10 × 1.4 mm^3
Ordering code: FH
Weight approximately 0.66 g



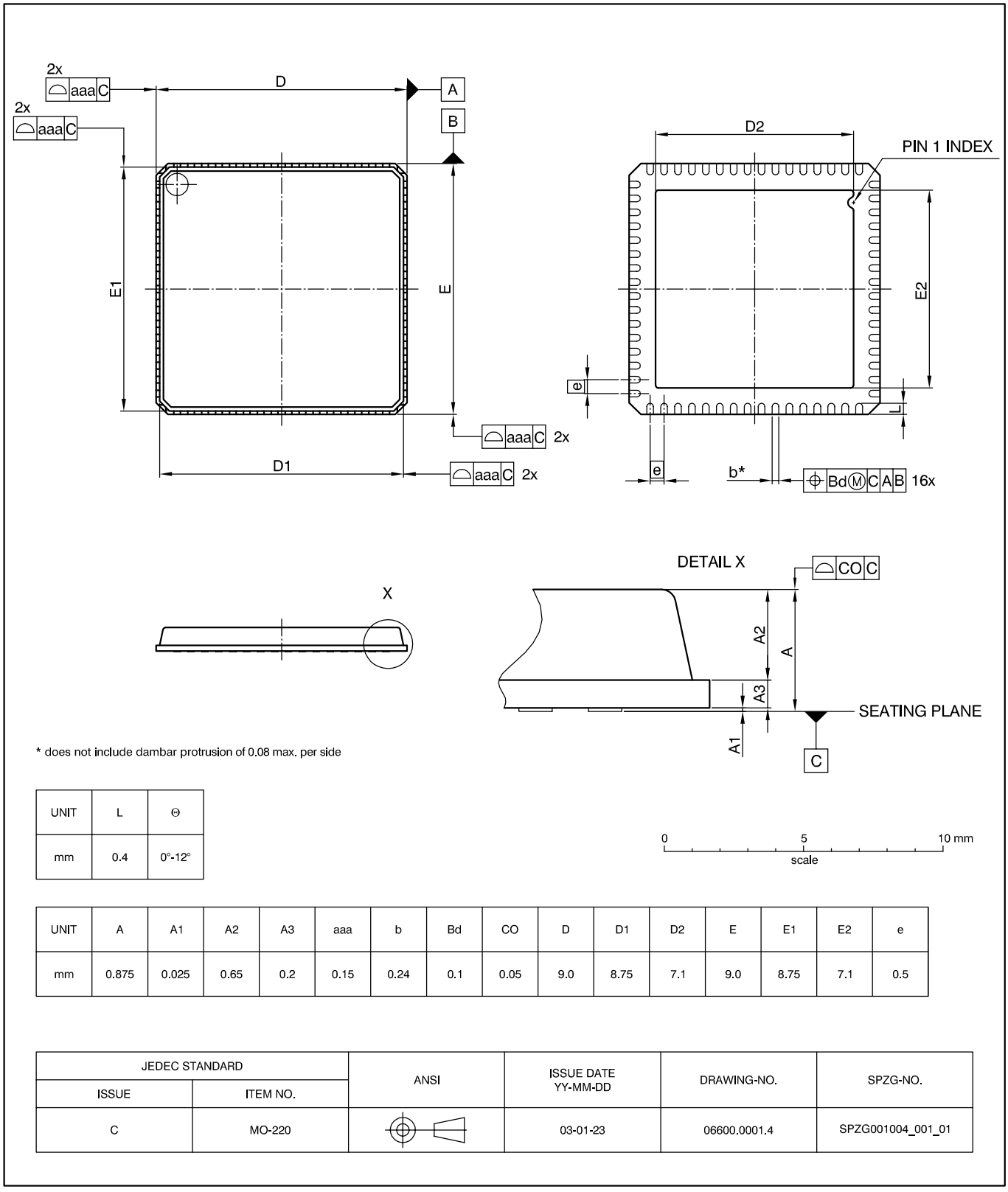
UNIT	L2	Θ
mm	1.60	0°-7°

* does not include dambar protrusion of 0.08 max. per side

UNIT	A	A1	A2	aaa	b	Bd	c	CO	D	D1	E	E1	e	L	L1
mm	max 2.45	0.25 0.00	2.20 1.80	0.25	0.27 0.17	0.2	0.23 0.11	0.1	13.2	10.0	13.2	10.0	0.5	1.03 0.73	0.25

JEDEC STANDARD		ANSI	ISSUE DATE YY-MM-DD	DRAWING-NO.	SPZG-NO.
ISSUE	ITEM NO.				
B	MS-022		03-03-25	06611.0001.4	SPZG001011_001_01

Fig. 4–2:
PMQFP64-2: Plastic **M**etric **Q**uad **F**lat **P**ackage, **64** leads, 10 × 10 × 2 mm^3
Ordering code: QI
Weight approximately 0.5 g



UNIT	L	Θ
mm	0.4	0°-12°

UNIT	A	A1	A2	A3	aaa	b	Bd	CO	D	D1	D2	E	E1	E2	e
mm	0.875	0.025	0.65	0.2	0.15	0.24	0.1	0.05	9.0	8.75	7.1	9.0	8.75	7.1	0.5

JEDEC STANDARD		ANSI	ISSUE DATE YY-MM-DD	DRAWING-NO.	SPZG-NO.
ISSUE	ITEM NO.				
C	MO-220		03-01-23	06600.0001.4	SPZG001004_001_01

Fig. 4–3:
PQFN64-1: Plastic **Q**uad **F**lat **N**on-leaded package, **64** pins, 9 × 9 × 0.85 mm^3, 0.5 mm pitch
Ordering code: XK
Weight approximately 0.23 g

4.2. Pin Connections and Short Descriptions

NC = not connected, leave vacant
LV = if not used, leave vacant
S.T.B. = shorted to BAGNDI if not used
DVSS = if not used, connect to DVSS
OBL = obligatory; connect as described in circuit diagram
AHVSS = connect to AHVSS

Pin No.			Pin Name	Type	Connection (If not used)	Short Description
PLQFP 64-1	PMQFP 64-2	PQFN 64-1				
1	1	1	AGNDC		OBL	Analog reference voltage
2	2	2	MICIN	IN	LV	Input for internal microphone amplifier
3	3	3	MICBI	IN	LV	Bias for internal microphone
4	4	4	INL	IN	LV	Left A/D input
5	5	5	INR	IN	LV	Right A/D input
6	6	6	TE	IN	OBL	Test enable
7	7	7	XTI	IN	OBL	Crystal oscillator (ext. clock) input
8	8	8	XTO	OUT	LV	Crystal oscillator output
9	9	9	$\overline{\text{POR}}$	IN	OBL	Power on reset, active low
10	10	10	VSS	SUPPLY	OBL	DSP supply ground
11	11	11	XVSS	SUPPLY	OBL	Digital output supply ground
12	12	12	VDD	SUPPLY	OBL	DSP supply
13	13	13	XVDD	SUPPLY	OBL	Digital output supply
14	14	14	I2CVDD	SUPPLY	OBL	I^2C supply
15	15	15	DVS	IN	OBL	I^2C device address selector
16	16	16	VSENS1	IN/OUT	VDD	Sense input and power output of DC/DC 1 converter
17	17	17	DCSO1	SUPPLY	LV	DC/DC 1 switch output
18	18	18	DCSG1	SUPPLY	VSS	DC/DC 1 switch ground
19	19	19	DCSG2	SUPPLY	VSS	DC/DC 2 switch ground
20	20	20	DCSO2	SUPPLY	LV	DC/DC 2 switch output
21	21	21	VSENS2	IN/OUT	VDD	Sense input and power output of DC/DC 2 converter
22	22	22	DCEN	IN	VSS	DC/DC enable (both converters)

Pin No. PLQFP 64-1	Pin No. PMQFP 64-2	Pin No. PQFN 64-1	Pin Name	Type	Connection (If not used)	Short Description
23	23	23	CLKO	OUT	LV	Clock output
24	24	24	I2CC	IN/OUT	OBL	I^2C clock
25	25	25	I2CD	IN/OUT	OBL	I^2C data
26	26	26	SYNC	OUT	LV	Sync output
27	27	27	VBAT	IN	LV	Battery voltage monitor input
28	28	28	PUP	OUT	LV	DC Converters Power-Up Signal
29	29	29	$\overline{EOD}$	OUT	LV	PIO end of DMA, active low
30	30	30	$\overline{PRTR}$	OUT	LV	PIO ready to read, active low
31	31	31	$\overline{PRTW}$	OUT	LV	PIO ready to write, active low
32	32	32	PR	IN	VDD	PIO DMA request, active high
33	33	33	$\overline{PCS}$	IN	VSS	PIO chip select, active low
34	34	34	PI19	IN/OUT	LV	PIO data bit[7] (MSB)
35	35	35	PI18	IN/OUT	LV	PIO data bit[6]
36	36	36	PI17	IN/OUT	LV	PIO data bit[5]
37	37	37	PI16	IN/OUT	LV	PIO data bit[4]
38	38	38	PI15	IN/OUT	LV	PIO data bit[3]
39	39	39	PI14	IN/OUT	LV	PIO data bit[2]
40	40	40	PI13	IN/OUT	LV	PIO data bit[1]
41	41	41	PI12	IN/OUT	LV	PIO data bit[0] (LSB)
42	42	42	SOD	OUT	LV	Serial output data
43	43	43	SOI	OUT	LV	Serial output word identification
44	44	44	SOC	OUT	LV	Serial output clock
45	45	45	SID	IN/OUT	OBL	Serial input data, interface A
46	46	46	SII	IN/OUT	OBL	Serial input word identification, interface A
47	47	47	SIC	IN/OUT	OBL	Serial input clock, interface A
48	48	48	SPDO	OUT	LV	S/PDIF output interface
49	49	49	SIBD	IN	VSS	Serial input data, interface B

Pin No. PLQFP 64-1	Pin No. PMQFP 64-2	Pin No. PQFN 64-1	Pin Name	Type	Connection (If not used)	Short Description
50	50	50	SIBC	IN	VSS	Serial input clock, interface B
51	51	51	SIBI	IN	VSS	Serial input word identification, interface B
52	52	52	SPDI2	IN	LV	Active differential S/PDIF input 2
53	53	53	SPDI1	IN	LV	Active differential S/PDIF input 1
54	54	54	SPDIR	IN	LV	Reference differential S/PDIF input 1 and 2
55	55	55	FILTL	IN	OBL	Feedback input for left amplifier
56	56	56	AVDD0	SUPPLY	OBL	Analog supply for output amplifiers
57	57	57	OUTL	OUT	LV	Left analog output
58	58	58	OUTR	OUT	LV	Right analog output
59	59	59	AVSS0	SUPPLY	OBL	Analog ground for output amplifiers
60	60	60	FILTR	IN	OBL	Feedback for right output amplifier
61	61	61	AVSS1	SUPPLY	OBL	Analog ground
62	62	62	VREF		OBL	Analog reference ground
63	63	63	PVDD	SUPPLY	OBL	Internal power supply
64	64	64	AVDD1	SUPPLY	OBL	Analog Supply

4.3. Pin Descriptions

4.3.1. Power Supply Pins

The use of all power supply pins is mandatory to achieve correct function of the MAS 35x9F.

VDD, VSS **SUPPLY**
Digital supply pins.

XVDD, XVSS **SUPPLY**
Supply for digital output pins.

I2CVDD **SUPPLY**
Supply for I^2C interface circuitry. This net uses VSS or XVSS as the ground return line.

PVDD **SUPPLY**
Auxiliary pin for analog circuitry. This pin has to be connected via a 3 nF capacitor to AVDD1. Extra care should be taken to achieve a low-inductance PCB line.

AVDD0/AVSS0 **SUPPLY**
Supply for analog output amplifier.

AVDD1/AVSS1 **SUPPLY**
Supply for internal analog circuits (A/D, D/A converters, clock, PLL, S/PDIF input).

AVDD0/AVSS0 and AVDD1/AVSS1 should receive the same supply voltages.

4.3.2. Analog Reference Pins

AGNDC
Internal analog reference voltage. This pin serves as the internal ground connection for the analog circuitry.

VREF
Analog reference ground. All analog inputs and outputs should drive their return currents using separate traces to a ground starpoint close to this pin. Connect to AVSS1. This reference pin should be as noise-free as possible.

4.3.3. DC/DC Converters and Battery Voltage Supervision

DCSG1/DCSG2 **SUPPLY**
DC/DC converters switch ground. Connect using separate wide trace to negative pole of battery cell. Connect also to AVSS0/1 and VSS/XVSS, VREF.

DCSO1/DCSO2 **SUPPLY**
DC/DC converter switch connection. If the respective DC/DC converter is not used, this pin must be left vacant.

VSENS1/VSENS2 **IN**
Sense input and power output of DC/DC converters. If the respective DC/DC converter is not used, this pin should be connected to a supply to enable proper function of the PUP-signals.

DCEN **IN**
Enable signal for both DC/DC converters. If none of the DC/DC converters is used, this pin must be connected to VSS.

PUP **OUT**
Power-up. This signal is set when the required voltages are available at both DC/DC converter output pins VSENS1 and VSENS2. The signal is cleared when both voltages have dropped below the reset level in the DCCF Register.

VBAT **IN**
Analog input for battery voltage supervision.

4.3.4. Oscillator Pins and Clocking

XTI **IN**
XTO **OUT**
The XTI pin is connected to the input of the internal crystal oscillator, the XTO pin to its output. Each pin should be directly connected to the crystal and to a ground-connected capacitor (see application diagram, Fig. 5–1 on page 89).

CLKO **OUT**
The CLKO can drive an output clock line.

4.3.5. Control Lines

I2CC **SCL** **IN/OUT**
I2CD **SDA** **IN/OUT**
Standard I^2C control lines.

DVS **IN**
I^2C device address selector. Connect this pin either to VDD (I^2C device address: $3E/3F_{hex}$) or VSS (I^2C device address: $3C/3D_{hex}$) to select a proper I^2C device address (see also Table 3–2 on page 23).

4.3.6. Parallel Interface Lines

PI12..PI19 **IN/OUT**
The PIO input pins PI12..PI19 are used as 8-bit I/O interface to a microcontroller in order to transfer compressed and uncompressed data. PI12 is the LSB, PI19 the MSB.

4.3.6.1. PIO Handshake Lines

$\overline{\text{PCS}}$ **IN**
The PIO chip select $\overline{\text{PCS}}$ must be set to '0' to activate the PIO in operation mode.

PR **IN**
Pin PR must be set to '1' to validate data output from MAS 35x9F PIO pins.

$\overline{\text{PRTR}}$ **OUT**
Ready to read. This signal indicates that the MAS 35x9F is able to receive data in PIO input mode.

$\overline{\text{PRTW}}$ **OUT**
Ready to write. This pin indicates that MAS 35x9F has data available for PIO output mode.

$\overline{\text{EOD}}$ **OUT**
$\overline{\text{EOD}}$ indicates the end of an DMA cycle in the IC's PIO input mode. In 'serial' input mode it is used as Demand signal, that indicates that new input data are required.

4.3.7. Serial Input Interface (SDI)

SID	**DATA**	**IN/OUT**
SII	**WORD STROBE**	**IN/OUT**
SIC	**CLOCK**	**IN/OUT**

I^2S compatible serial interface A for digital audio data. In the standard firmware this interface is not used.
Note: Please refer to Bit [0] of Table 3–5

4.3.8. Serial Input Interface B (SDIB)

SIBD	**DATA**	**IN**
SIBI	**WORD STROBE**	**IN**
SIBC	**CLOCK**	**IN**

The serial interface B is primarily used as bitstream input interface. The SIBI line must be connected to VSS in the standard application.

4.3.9. Serial Output Interface (SDO)

SOD	**DATA**	**OUT**
SOI	**WORD STROBE**	**OUT**
SOC	**CLOCK**	**IN/OUT**

Data, Frame Indication, and Clock line of the serial output interface. The SOI is reconfigurable and can be adapted to several I^2S compliant modes.

4.3.10. S/PDIF Input Interface

SPDI1 **IN**
SPDI2 **IN**
SPDIR **IN**
SPDIF1 and SPDIF2 are alternative input pins for S/PDIF sources according to the IEC 958 consumer specification are used in conjunction with download software only. A switch at D0:ff6 selects one of these pins at a time. The SPDIR pin is a common reference for both input lines (see Fig. 5–1 on page 89).

4.3.11. S/PDIF Output Interface

SPDO **OUT**
The SPDO pin provides an digital output with standard CMOS level that is compliant to the IEC 958 consumer specification.

4.3.12. Analog Input Interfaces

In the standard MPEG-decoding DSP firmware the analog inputs are not used. However, they can be selected as a source for the D/A converters
(set MIX ADC scale of the D/A Converter Source Mixer, Register 00 06_{hex} in Table 3–16).

MICIN **IN**
MICBI **IN**
The MICIN input may be directly used as electret microphone input, which should be connected as described in application information (see Fig. 5–1 on page 89). The MICBI signal provides the supply voltage for these microphones.

INL **IN**
INR **IN**
INL and INR are analog line-in input lines. They are connected to the embedded stereo A/D converter of the MAS 35x9F. The sources should be AC-coupled. The reference ground for these analog input pins is the VREF pin.

4.3.13. Analog Output Interfaces

OUTL **OUT**
OUTR **OUT**
OUTL and OUTR are left and right analog outputs, that may be directly connected to the headphones as described in the application information (see Fig. 5–1 on page 89).

FILTL **IN**
FILTR **IN**
Connection to input terminal of output amplifier.Can be used to connect a capacitance from OUTL respectively OUTR to FILTL respectively FILTR in parallel to feedback resistor and thus implement a low pass filter to reduce the out-of-band noise of the DAC.

4.3.14. Miscellaneous

SYNC **OUT**
The SYNC signal indicates the detection of a frame start in the input data of MAS 35x9F. Usually this signal generates an interrupt in the controller.

$\overline{\text{POR}}$ **IN**
The Power-On Reset pin is used to reset the whole MAS 35x9F. The $\overline{\text{POR}}$ is an active-low signal (see Fig. 5–1 on page 89).

TE **IN**
The TE pin is for production test only and must be connected with VSS in all applications.

4.4. Pin Configuration

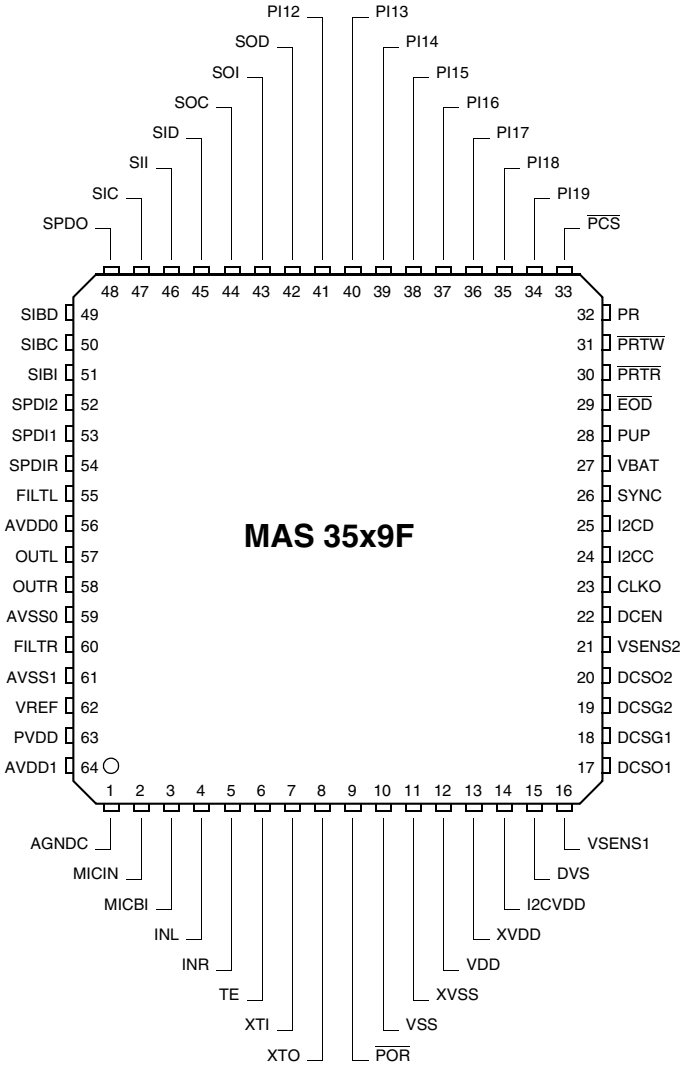


Fig. 4–4: PLQFP64-1/PMQFP64-2 and PQFN64-1 package

4.5. Internal Pin Circuits

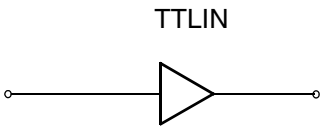


Fig. 4–5: Input pins $\overline{PCS}$, PR

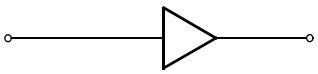


Fig. 4–6: Input pin TE, DVS, $\overline{POR}$

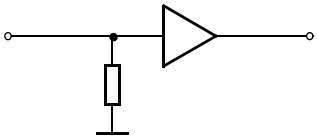


Fig. 4–7: Input pin DCEN

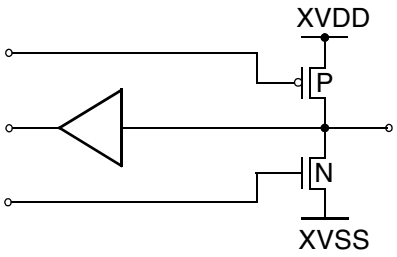


Fig. 4–8: Input/output pins SOC, SOI, SOD, PI12...PI19, SPDO

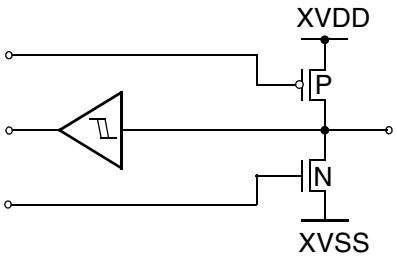


Fig. 4–9: Input pins SIC, SII, SID

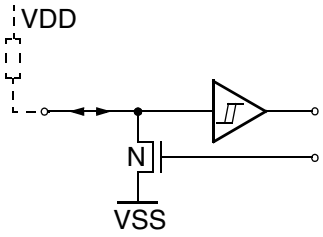


Fig. 4–10: Input/output pins I2CC, I2CD

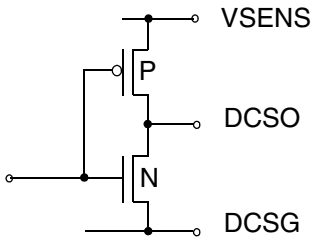


Fig. 4–11: Input/output pins DCSO1/2, DCSG1/2, VSENS1/2

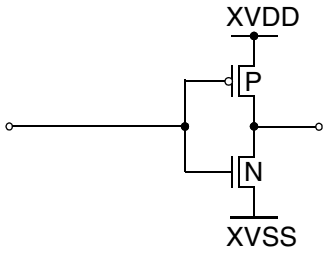


Fig. 4–12: Output pins $\overline{PRTW}$, $\overline{EOD}$, $\overline{PRTR}$, CLKO, SYNC, PUP

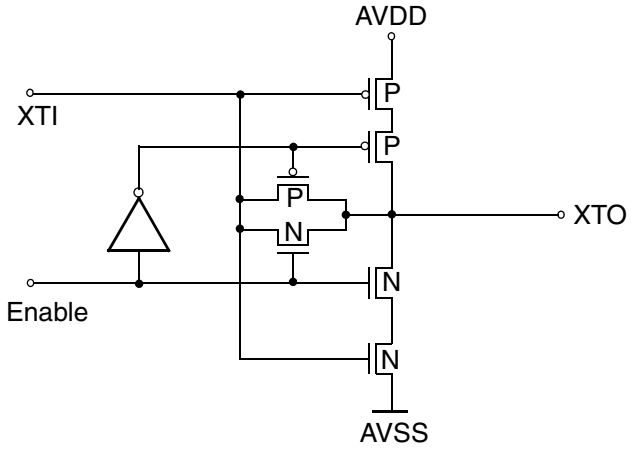


Fig. 4–13: Clock oscillator XTI, XTO

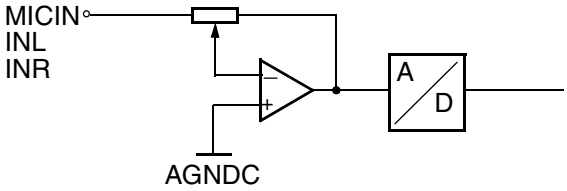


Fig. 4–14: Analog input pins MICIN, INL, INR

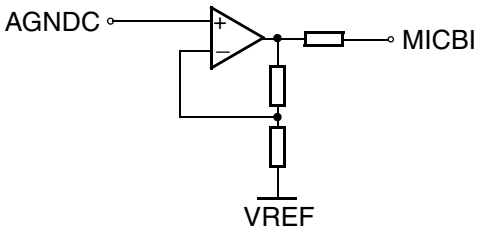


Fig. 4–15: Microphone bias pin (MICBI)

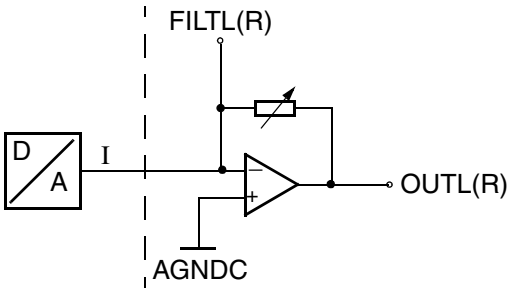


Fig. 4–16: Analog outputs OUTL(R) and connections for filter capacitors FILTL(R)

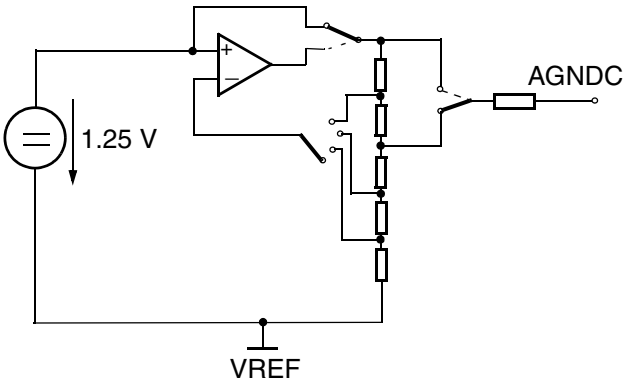


Fig. 4–17: Analog ground generation with pin to connect external capacitor

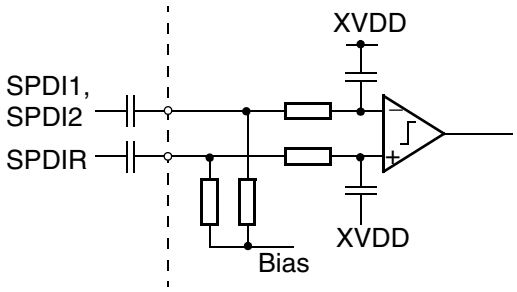


Fig. 4–18: S/PDIF inputs

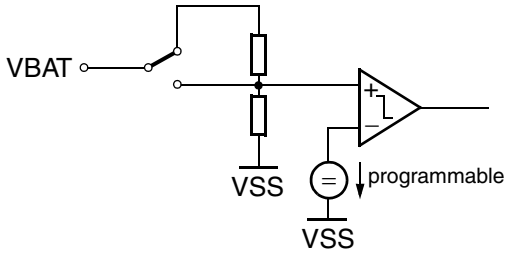


Fig. 4–19: Battery voltage monitor VBAT

4.5.1. Reset Pin Configuration for MAS 3529F and MAS 3539F

The Power-On Reset pin $\overline{\text{POR}}$ is used to reset the entire MAS 35x9F. The $\overline{\text{POR}}$ is an active-low signal.

Note: If a pull-up resistor is used for building a delay time here (see Fig. 5–1 on page 89), referred to the VDD pins, the maximum allowed value for this resistor is 3.3 kOhm!

4.6. Electrical Characteristics

Abbreviations:

tbd = to be defined
vacant = not applicable
positive current values mean current flowing into the chip

4.6.1. Absolute Maximum Ratings

Stresses beyond those listed in the “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only. Functional operation of the device at these conditions is not implied. Exposure to absolute maximum rating conditions for extended periods will affect device reliability.

This device contains circuitry to protect the inputs and outputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than absolute maximum-rated voltages to this high-impedance circuit.

All voltages listed are referenced to ground (V_{SUP1}, V_{SUP2}, V_{SUP3} = 0 V) except where noted.

All GND pins must be connected to a low-resistive ground plane close to the IC.

Do not insert the device into a live socket. Instead, apply power by switching on the external power supply. For power up/down sequences, see the instructions in Section 2.6. of this document.

Table 4–1: Absolute Maximum Ratings

Symbol	Parameter	Pin Name	Limit Values		Unit
			Min.	Max.	
T_A [1]	Ambient Temperature - operating conditions - extended temperature range [1]		 –10 –40	[2] 85 85	°C
T_C	Case Temperature PLQFP64-1 PMQFP64-2 PQFN64-1		 –10 –10 –10	 115 120 120	°C
T_S	Storage Temperature		–40	125	°C
P_{MAX}	Maximum Power Dissipation PLQFP64-1 PMQFP64-2 PQFN64-1	VDD, XVDD, AVDD0/1, I2CVDD		[3] 0.67 0.63 0.87	W
V_{SUP1}	Supply Voltage 1	VDD, XVDD, I2CVDD, AVDD0/1 [4]	–0.3	6	V

[1] Data sheet parameters are valid for “operating conditions” only. The functionality of the device in the “extended temperature range” was checked by electrical characterization on sample base.

[2] A power-optimized board layout is recommended. The Case Temperature mentioned in the “Absolute Maximum Ratings” must not be exceeded at worst case conditions of the application.

[3] Package limits

[4] Both AVDD0 and AVDD1 have to be connected together!

Table 4–1: Absolute Maximum Ratings, continued

Symbol	Parameter	Pin Name	Limit Values		Unit
			Min.	Max.	
V_{SUP2}	Supply Voltage 2	VDD, XVDD, I2CVDD, AVDD0/1 [1)]	−0.3	6	V
V_{SUP3}	Supply Voltage 3	VDD, XVDD, I2CVDD, AVDD0/1 [1)]	−0.3	6	V
V_{II2C}	Input Voltage, I^2C pins	I2CC, I2CD	−0.3	6	V
V_{ID}	Input Voltage	all digital inputs	−0.3	V_{SUP} + 0.3	V
I_{ID}	Input Current	all digital inputs	−20	+20	mA
V_{IA}	Input Voltage	all analog inputs	−0.3	V_{SUP} + 0.3	V
I_{IA}	Input Current	all analog inputs	−5	+5	mA
I_{Oaudio}	Output Current, audio output [2)]	OUTL/R	−0.2	0.2	A
I_{Odig}	Output Current, all digital outputs [3)]		−50	+50	mA
I_{Odcdc1}	Output Current DCDC converter 1	DCSO1		1.5	A
I_{Odcdc2}	Output Current DCDC converter 2	DCSO2		1.5	A

1) Both AVDD0 and AVDD1 have to be connected together!

2) These pins are not short-circuit-proof!

3) Total chip power dissipation must not exceed maximum rating.

4.6.1.1. Recommended Operating Conditions

Functional operation of the device beyond those indicated in the “Recommended Operating Conditions/Characteristics” is not implied and may result in unpredictable behavior, reduce reliability and lifetime of the device.

All voltages listed are referenced to ground (V_{SUP1}, V_{SUP2}, V_{SUP3} = 0 V) except where noted.

All GND pins must be connected to a low-resistive ground plane close to the IC.

Do not insert the device into a live socket. Instead, apply power by switching on the external power supply. For power up/down sequences, see the instructions in section Section 2.11.2. of this document.

Symbol	Parameter	Pin Name	Limit Values			Unit
			Min.	Typ.	Max.	
T_A	Ambient Operating Temperature PLQFP64-1 PMQFP64-2 PQFN64-1		 0 0 0	 25 25 25	[1] 85 85 85	°C
T_C	Case Operating Temperature PLQFP64-1 PMQFP64-2 PQFN64-1		 15 20 15	 95 100 95	 100 105 100	°C
P_{MAX_D1}	MP3 Decoder (SC4 En-/Decoder)	VDD		80		mW
P_{MAX_D2}	AAC Decoder/G729 Encoder	VDD		122		mW
P_{MAX_D3}	G.729 Decoder	VDD		50		mW
P_{MAX_A}	DAC-Headphone Playback	AVDD0/1		7		mW
V_{SUPD1} [1]	Digital supply voltage (MP3 decoder, G729 Decoder)	VDD	2.2	2.5	3.6	V
V_{SUPD2}	Digital supply voltage (G.729 A encoder/MP3 Decoder and SD Decryption/AAC Decoder)		2.5	2.7	3.6	
V_{SUPI2C}	I^2C bus supply voltage	I2CVDD	V_{SUPDn} [2] at VDD		3.9	V
V_{SUPx}	PIN supply voltage	XVDD	2.2	2.5	3.6	V
	PIN supply voltage in relation to digital supply voltage		0.62 * V_{SUPDn} [2]		1.6 * V_{SUPDn} [2]	V
V_{SUPA}	Analog audio supply voltage	AVDD0/1	2.2	2.7	3.6	V
	Analog audio supply voltage in relation to the digital supply voltage		0.62 * V_{SUPDn} [2]		1.6 * V_{SUPDn} [2]	V
V_{SUPDX}	Voltage differences within supply domains					V

[1] A power-optimized board layout is recommended. The Case Operating Temperatures mentioned in the “Recommended Operating Conditions” must not be exceeded at worst case conditions of the application. For turn-on voltage of DSP and codec, please refer to Section 2.11.2.1.

[2] n = 1 or 2

Table 4–2: Reference Frequency Generation and Crystal Recommendation

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit
External Clock Input Recommendations						
f_{CLK}	Clock frequency	XTI, XTO	13.00	18.432	20.00	MHz
V_{CLKI}	Clockamplitude of external clock fed into XTI at V_{AVDD} = 2.2 V	XTI	0.7		1.05	V_{PP}
	Clockamplitude of external clock fed into XTI at V_{AVDD} = 2.7 V		0.55		1.5	
	Clockamplitude of external clock fed into XTI at V_{AVDD} = 3.3 V		0.45		1.75	
	Clockamplitude of external clock fed into XTO at V_{AVDD} = 2.2 V	XTO	1.25		2.2	
	Clockamplitude of external clock fed into XTO at V_{AVDD} = 2.7 V		0.75		2.7	
	Clockamplitude of external clock fed into XTO at V_{AVDD} = 3.3 V		0.55		3.3	
	Duty cycle	XTI, XTO	45	50	55	%
Crystal Recommendations						
f_P	Load resonance frequency at C_I = 20 pF	XTI, XTO		18.432		MHz
$\Delta f/f_S$	Accuracy of frequency adjustment		–50		50	ppm
$\Delta f/f_S$	Frequency variation vs. temperature		–50		50	ppm
R_{EQ}	Equivalent series resistance			12	30	Ω
C_0	Shunt (parallel) capacitance			3	5	pF

Table 4–3: Input clock frequency

Symbol	Parameter	Pin Name	Limit Values			Unit
			Min.	Typ.	Max.	
f_{CLK} [1)]	G.729 Decoder G.729 Encoder	XTI, XTO	16.4 13.7			MHz MHz
	MPEG Decoder (SC4 En-Decoder)		11.0			MHz
[1)] Minimum F_{CLK} for SD-card decryption is defined in a supplement.						

Table 4–4: Input levels

Symbol	Parameter	Pin Name	Limit Values			Unit
			Min.	Typ.	Max.	
V_{IL}	Input low voltage	I2CC, I2CD			0.3	V
V_{IH}	Input high voltage		1.4			V
V_{IL}	Input low voltage	$\overline{POR}$, DCEN			0.2	V
V_{IH}	Input high voltage		0.9			V
V_{ILD}	Input low voltage	PI<I>, SI(B)I, SI(B)C, $\overline{SI(B)}$D, PR, $\overline{PCS}$, TE, DVS			0.3	V
V_{IHD}	Input high voltage		V_{SUPx} −0.5			V

Table 4–5: Analog input and output recommendations

Symbol	Parameter	Pin Name	Limit Values			Unit
			Min.	Typ.	Max.	
Analog Reference						
C_{AGNDC1}	Analog filter capacitor	AGNDC	1.0	3.3		µF
C_{AGNDC2}	Ceramic capacitor in parallel			10		nF
C_{PVDD}	Capacitor for analog circuitry	PVDD	3			nF
Analog Audio Inputs						
C_{inAD}	DC-decoupling capacitor at A/D-converter inputs	INL/R		390		nF
C_{inMI}	DC-decoupling capacitor at microphone-input	MICIN		390		nF
C_{LMICBI}	Minimum-Capacitance at microphone bias	MICBI	3.3			nF
Analog Audio Filter Outputs						
C_{FILT}	Filter capacitor for headphone amplifier high-Q type, NP0 or C0G material	FILTL/R OUTL/R	–20 %	470	+20 %	pF
Analog Audio Output						
Z_{AOL_HP}	Analog output load with stereo headphones	OUTL/R	16			Ω
				100		pF
DC/DC-Converter External Circuitry (please refer to application example)						
C_1	VSENS blocking (<100 mΩ ESR)	VSENS1/2		330		µF
V_{TH}	Schottky diode threshold voltage	DCSO1/2 VSENS1/2	0.39			V
L	Ferrite core coil inductance	DCSO1/2		22		µH
S/PDIF Interface Analog Input						
C_{SPI}	S/PDIF coupling capacitor	SPDI1/2 SPDIR		100		nF

4.6.2. Digital Characteristics

at T = T_A, V_{SUPD}, V_{SUPA} = 2.2 ... 3.6 V, $f_{Crystal}$ = 18.432 MHz, Typ. values for T_A = 25 °C in P(L/M)QFP package

Symbol	Parameter	Pin Name	Limit Values			Unit	Test Conditions
			Min.	Typ.	Max.		
Digital Supply Voltage							
I_{SUPD}	Current consumption	VDD, XVDD, I2CVDD		36		mA	2.2 V, sampling frequency ≥ 32 kHz
I_{SUPD}	Current consumption			23		mA	2.2 V, sampling frequency ≤ 24 kHz
I_{SUPD}	Current consumption			15		mA	2.2 V, sampling frequency ≤ 12 kHz
$I_{STANDBY}$	Total current at stand-by				10	µA	DSP off, Codec off, DC/DC off, AD and DAC off, no I^2C access
Digital Outputs and Inputs							
O_{DigL}	Output low voltage	PI<I>, SOI, SOC, $\overline{SOD}$, $\overline{EOD}$, $\overline{PRTR}$, $\overline{PRTW}$, CLKO, SYNC, PUP, SPDO			0.3	V	I_{load} = 2 mA
O_{DigH}	Output low voltage		V_{SUPx} −0.3			V	I_{load} = −2 mA
Z_{DigI}	Input impedance	ALL DIGITAL INPUTS			7	pF	
I_{DLeak}	Digital input leakage current		−1		1	µA	0 V < V_{pin} < V_{SUPD}

4.6.2.1. I²C Characteristics

at T = 25°C, V_{SUPI2C} = 2.2...3.6 V in P(L/M)QFP package

Symbol	Parameter	Pin Name	Limit Values			Unit	Test Conditions
			Min.	Typ.	Max.		
I²C Input Specifications							
f_{I2C}	Upper limit I²C bus frequency operation	I2CC	400			kHz	
t_{I2C1}	I²C START condition setup time	I2CC, I2CD	300			ns	
t_{I2C2}	I²C STOP condition setup time	I2CC, I2CD	300			ns	
t_{I2C3}	I²C clock low pulse time	I2CC	1250			ns	
t_{I2C4}	I²C clock high pulse time	I2CC	1250			ns	
t_{I2C5}	I²C data setup time before rising edge of clock	I2CC	80			ns	
t_{I2C6}	I²C data hold time after falling edge of clock	I2CC	80			ns	
V_{I2COL}	I²C output low voltage	I2CC, I2CD			0.4	V	I_{load} = 3 mA
I_{I2COH}	I²C output high leakage current	I2CC, I2CD			1	µA	
t_{I2COL1}	I²C data output hold time after falling edge of clock	I2CC, I2CD	20			ns	
t_{I2COL2}	I²C data output setup time before rising edge of clock	I2CC, I2CD	250			ns	f_{I2C} = 400 kHz
V_{I2CIL}	I²C input low voltage	I2CC, I2CD			0.3	V_{SUPI2C}	
V_{I2CIH}	I²C input high voltage	I2CC, I2CD	0.6			V_{SUPI2C}	
t_W	Wait time	I2CC, I2CD	0	0.5	4	ms	

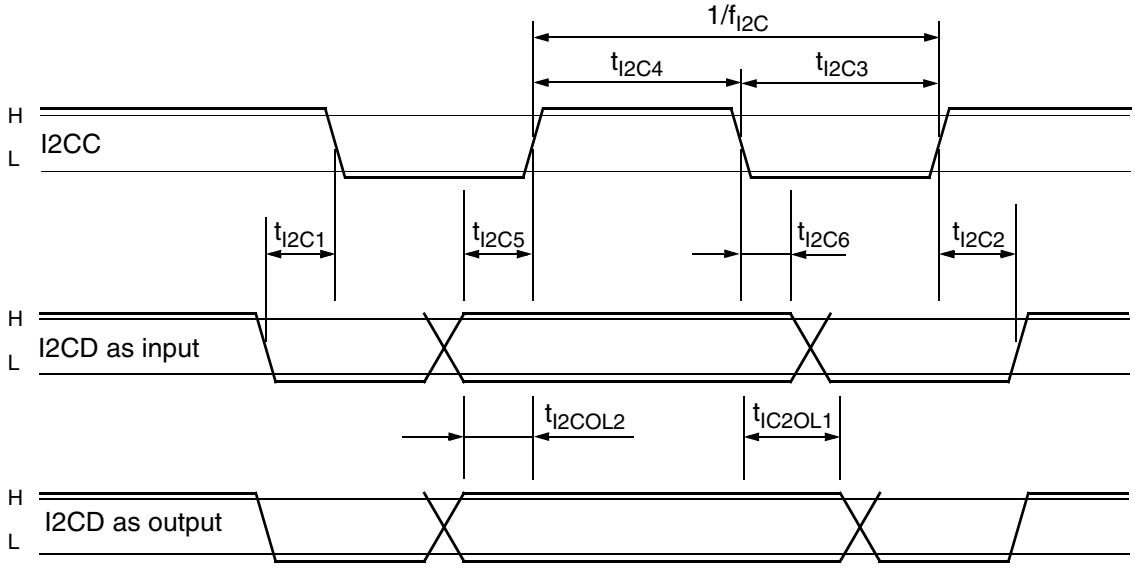


Fig. 4–20: I²C timing diagram

4.6.2.2. Serial (I^2S) Input Interface Characteristics (SDI, SDIB)

at T = T_A, V_{SUPD}, V_{SUPA} = 2.2 ... 3.6 V, $f_{CRYSTAL}$ = 18.432 MHz, Typ. values for T_A = 25 °C in P(L/M)QFP package

Symbol	Parameter	Pin Name	Limit Values			Unit	Test Conditions
			Min.	Typ.	Max.		
t_{SICLK}	I^2S clock input clock period	SI(B)C		325		ns	f_S = 48 kHz Stereo, 32 bits per sample (for demand mode see Table 4–6)
t_{SIDS}	I^2S data setup time before rising edge of clock (for continuous data stream: falling edge)	SI(B)C, SI(B)D	50			ns	
t_{SIDH}	I^2S data hold time	SI(B)D	50			ns	
t_{SIIS}	I^2S ident setup time before rising edge of clock (for continuous data stream: falling edge)	SI(B)C, SI(B)I	50			ns	
t_{SIIH}	I^2S ident hold time	SI(B)I	50			ns	
t_{bw}	Burst wait time	SI(B)C, SI(B)D	480				

Table 4–6: Maximum allowed sample clock frequency in Demand Mode

f_{Sample} (kHz)	f_C (MHz)	min. t_{SICLK} (ns)
48, 32	6.144	162
44.1	5.6448	177
24, 16	3.072	325
22.05	2.8224	354
12, 8	1.536	651
11.025	1.4112	708

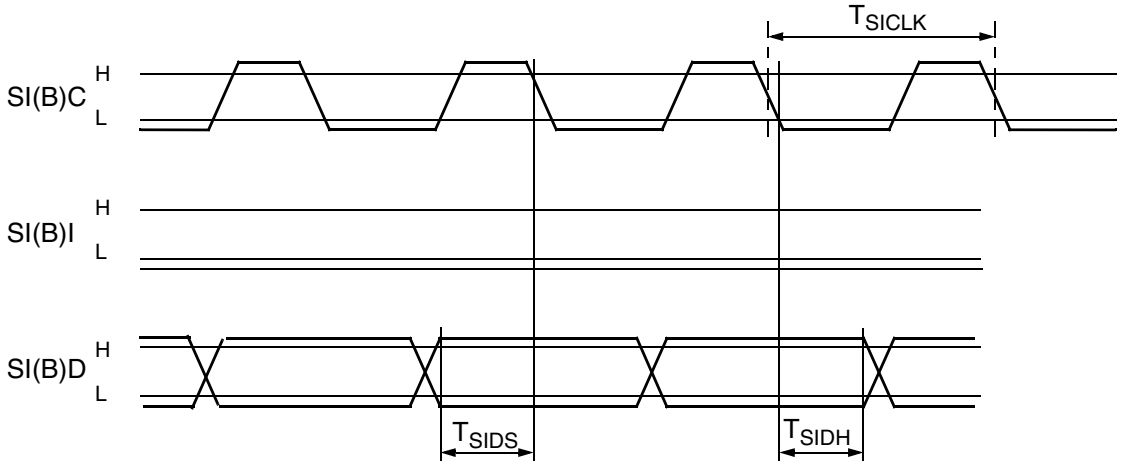


Fig. 4–21: Continuous data stream at serial input A or B. In this mode, the word strobe SI(B)I is not used and the data are read at the falling edge of the clock (bit[2] in D0:346 is set).

Table 4–7: Allowed transmission delays of external data source MPEG1/2 Layer 2/3

Symbol	Parameter	Pin Name	Limit Values			Unit	Test Conditions
			Min.	Typ.	Max.		
$t_{START48-320}$	Allowed delay time before start of serial data transmission after assertion of signal at $\overline{EOD}$	$\overline{EOD}$			3.1	ms	48 kHz/s, 320 kbit/s
$t_{START48-64}$					5.7	ms	48 kHz/s, 64 kbit/s
$t_{START24-320}$					4.2	ms	24 kHz/s, 320 kbit/s
$t_{START24-32}$					9.2	ms	24 kHz/s, 32 kbit/s
$t_{START12-64}$					23.1	ms	12 kHz/s, 64 kbit/s
$t_{START12-16}$					25.6	ms	12 kHz/s, 16 kbit/s
$t_{START8-64}$					34.8	ms	8 kHz/s, 64 kbit/s
$t_{START8-8}$					38.4	ms	8 kHz/s, 8 kbit/s
t_{STOP}	Allowed delay time before stop of serial data transmission after deassertion of signal at $\overline{EOD}$	$\overline{EOD}$			1.3	ms	Clock rate of input data 1 Mbit/s

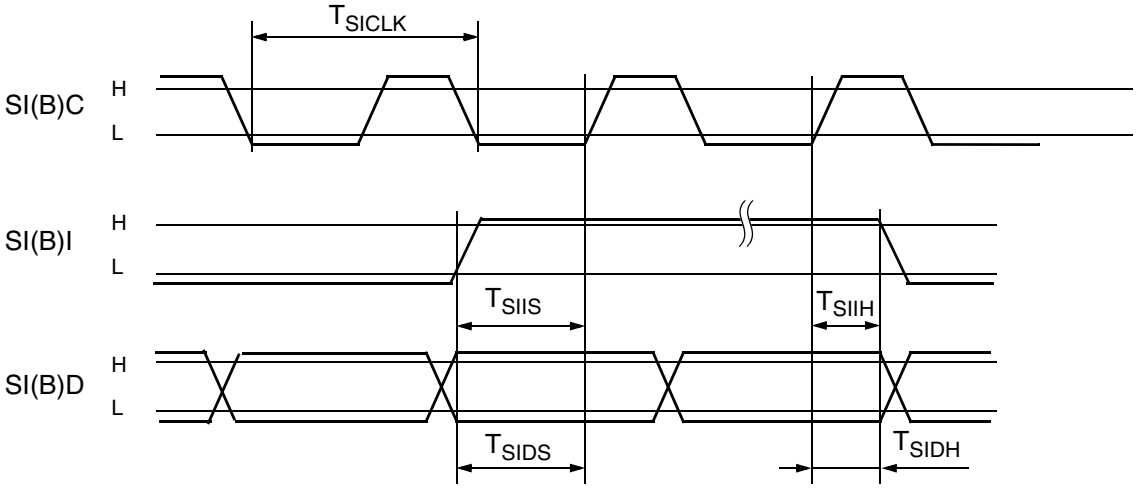


Fig. 4–22: Serial input of I^2S signal

4.6.2.3. Serial Output Interface Characteristics (SDO)

at T = T_A, V_{SUPD}, V_{SUPA} = 2.2 ... 3.6 V, $f_{CRYSTAL}$ = 18.432 MHz, Typ. values for T_A = 25 °C in P(L/M)QFP package

Symbol	Parameter	Pin Name	Limit Values			Unit	Test Conditions
			Min.	Typ.	Max.		
t_{SOCLK}	I^2S clock output frequency	SOC		325		ns	f_S = 48 kHz Stereo 32 bits per sample
t_{SOISS}	I^2S word strobe delay time after falling edge of clock	SOC, SOI	0			ns	
t_{SOODC}	I^2S data delay time after falling edge of clock	SOC, SOD	0			ns	

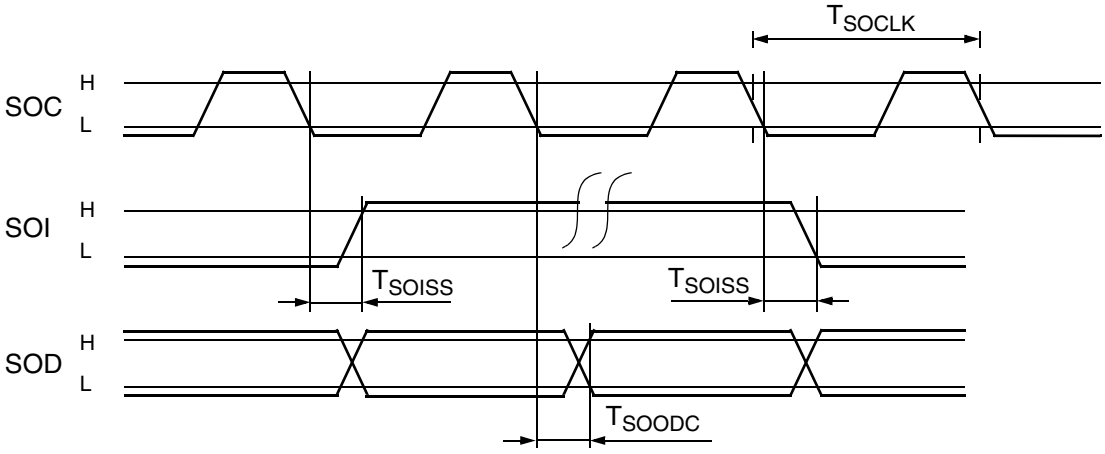


Fig. 4–23: Serial output interface timing

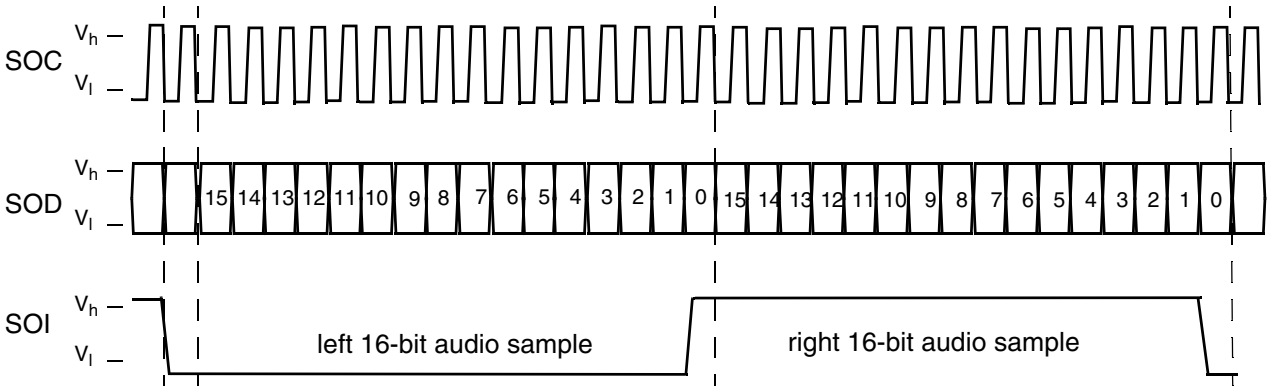


Fig. 4–24: Sample timing of the SDO interface in 16 bit/sample mode
D0:346 settings are
bit[14] = 0 (SOC not inverted)
bit[11] = 1 (SOI delay)
bit[5] = 0 (word strobe not inverted)
bit[4] = 1 (16 bits/sample)

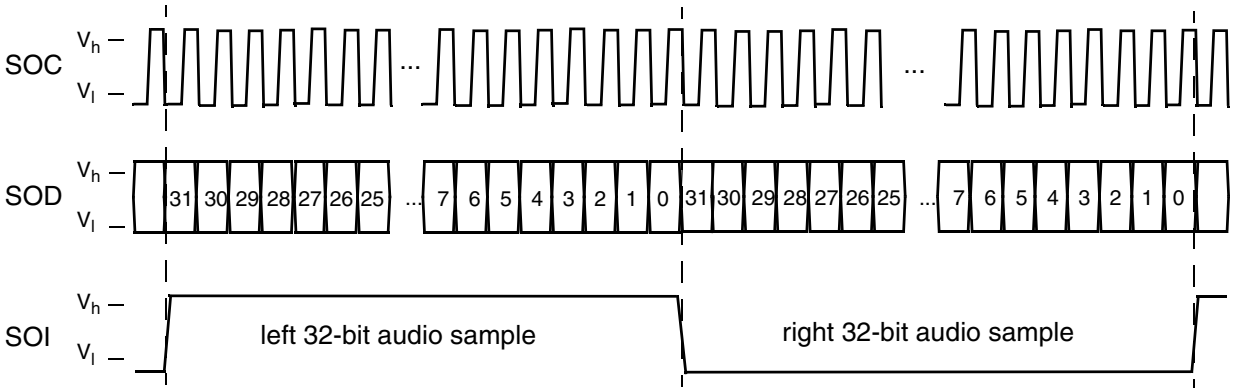


Fig. 4–25: Sample timing of the SDO interface in 32 bit/sample mode
D0:346 settings are
bit[14] = 0 (SOC not inverted)
bit[11] = 0 (no SOI delay)
bit[5] = 1 (word strobe inverted)
bit[4] = 0 (32 bits/sample)

4.6.2.4. S/PDIF Input Characteristics

at T = T_A, V_{SUPD}, V_{SUPA} = 2.2 ... 3.6 V, $f_{Crystal}$ = 18.432 MHz, Typ. values for T_A = 25 °C in P(L/M)QFP package.

Symbol	Parameter	Pin Name	Limit Values			Unit	Test Conditions
			Min.	Typ.	Max.		
V_S	Signal amplitude	SPDI1, SPDI2, SPDIR	200	500	1000	mV_{pp}	
f_{s1}	Bi-phase frequency	SPDI1, SPDI2, SPDIR		2.048		MHz	±1000 ppm, f_s = 48 kHz
f_{s2}	Bi-phase frequency	SPDI1, SPDI2, SPDIR		2.822		MHz	±1000 ppm, f_s = 44.1 kHz
f_{s3}	Bi-phase frequency	SPDI1, SPDI2, SPDIR		3.072		MHz	±1000 ppm, f_s = 32 kHz
t_P	Bi-phase period	SPDI1, SPDI2, SPDIR		326		ns	at f_s = 48 kHz, (highest sampling rate)
t_R	Rise time	SPDI1, SPDI2, SPDIR	0		65	ns	at f_s = 48 kHz, (highest sampling rate)
t_F	Fall time	SPDI1, SPDI2, SPDIR	0		65	ns	at f_s = 48 kHz, (highest sampling rate)
	Duty cycle	SPDI	40	50	60	%	at bit value=1 and f_s = 48 kHz
$t_{H1,L1}$		SPDI	81		163	ns	minimum/maximum pulse duration with a level above 90 % or below 10 % and at f_s = 48 kHz
$t_{H0,L0}$		SPDI	163		244	ns	minimum/maximum pulse duration with a level above 90 % or below 10 % and at f_s = 48 kHz

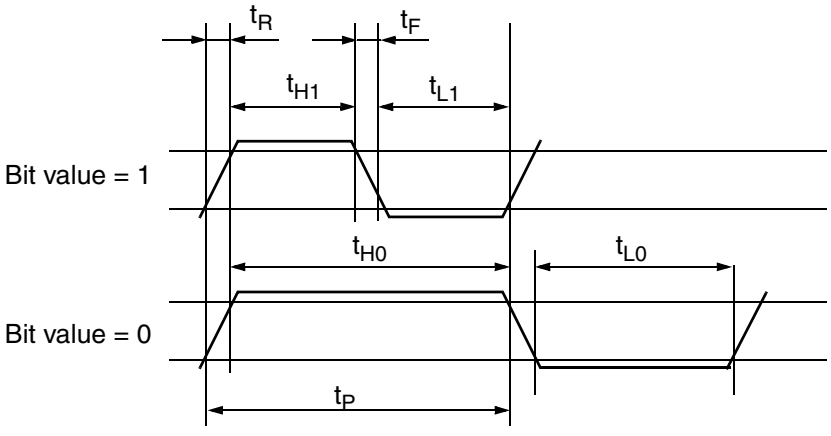


Fig. 4–26: Timing of the S/PDIF input

4.6.2.5. S/PDIF Output Characteristics

at T = T_A, V_{SUPD}, V_{SUPA} = 2.2 ... 3.6 V, $f_{CRYSTAL}$ = 18.432 MHz, Typ. values for T_A = 25 °C in P(L/M)QFP package.

Symbol	Parameter	Pin Name	Limit Values			Unit	Test Conditions
			Min.	Typ.	Max.		
f_{s1}	Bi-phase frequency	SPDO		3.072		MHz	f_s = 48 kHz
f_{s2}	Bi-phase frequency	SPDO		2.822		MHz	f_s = 44.1 kHz
f_{s3}	Bi-phase frequency	SPDO		2.048		MHz	f_s = 32 kHz
t_P	Bi-phase period	SPDO		326		ns	at f_s = 48 kHz, (highest sampling rate)
t_R	Rise time	SPDO	0		2	ns	C_{load} = 10 pF
t_F	Fall time	SPDO	0		2	ns	C_{load} = 10 pF
	Duty cycle	SPDO		50		%	
$t_{H1,L1}$		SPDO		163		ns	minimum/maximum pulse duration with a level above 90% or below 10% and at f_s = 48 kHz
$t_{H0,L0}$		SPDO		326		ns	minimum/maximum pulse duration with a level above 90% or below 10% and at f_s = 48 kHz
V_S	Signal amplitude	SPDO		V_{SUPD}			

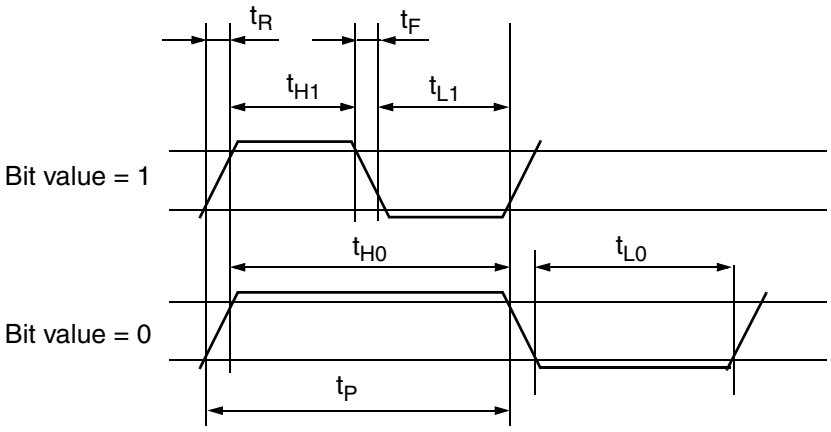


Fig. 4–27: Timing of the S/PDIF output

4.6.2.6. PIO as Parallel Input Interface: DMA Mode

In decoding mode, the data transfer can be started after the $\overline{EOD}$ pin of the MAS 35x9F is set to “high”. After verifying this, the controller signalizes the sending of data by activating the PR line. The MAS 35x9F responds by setting the $\overline{RTR}$ line to the “low” level. The MAS 35x9F reads the data PI[19:12] and sets RTR to low after rising edge of PR. After RTR is set to high, the mC sets PR to low. The next data word write operation will be initialized again by setting the PR line via the controller. Please refer to Figure for the exact timing.

The procedure above will be repeated until the MAS 35x9F sets the $\overline{EOD}$ signal to “0” which indicates that the transfer of one data block has been executed. Subsequently, the controller should set PR to “0”, wait until $\overline{EOD}$ rises again and then repeat the procedure to send the next block of data. The DMA buffer for MPEG decoding is 30 bytes long. The size for G.729 is 10 bytes.

Table 4–8: PIO input DMA mode timing

Symbol	Pin Name	Min.	Max.
t_{st}	PR, $\overline{EOD}$	10 ns	2000 µs
t_r	PR, $\overline{RTR}$		t_clm
t_{set1}	PI[19:12]		2*t_clm-33 ns
t_{set2}	PI[19:12]	dep. on appl.	
t_h	PI[19:12]	5*t_clm	
t_{rtrq}	$\overline{RTR}$	5*t_clm	MP3: 60*t_clm AAC: 140*t_clm
t_{pr}	PR	5*t_clm	
t_{rpr}	PR, $\overline{RTR}$	t_clm	
t_{eod}	PR, $\overline{EOD}$	t_clm	
t_{eodq}	$\overline{EOD}$	150*t_clm[1)]	200 ms[1)]
[1)] See Parallel I/O Application Note, Order no. 6251-590-2-1IC.			

Table 4–9: t_clm in MP3

Sample rate [kHz]	t_clm [ns]	f_clm [MHz]
48 or 32	41	24.5760
44.1	44	22.5792
24 or 16	81	12.2880
22.05	89	11.2896
12 or 8	163	6.1440
11.025	177	5.6448

Table 4–10: t_clm in AAC

Sample rate [kHz]	t_clm [ns]	f_clm [MHz]
48 or 32	33	30.720
44.1	35	28.224
24 or 16	65	15.360
22.05	71	14.112
12 or 8	130	7.680
11.025	142	7.056

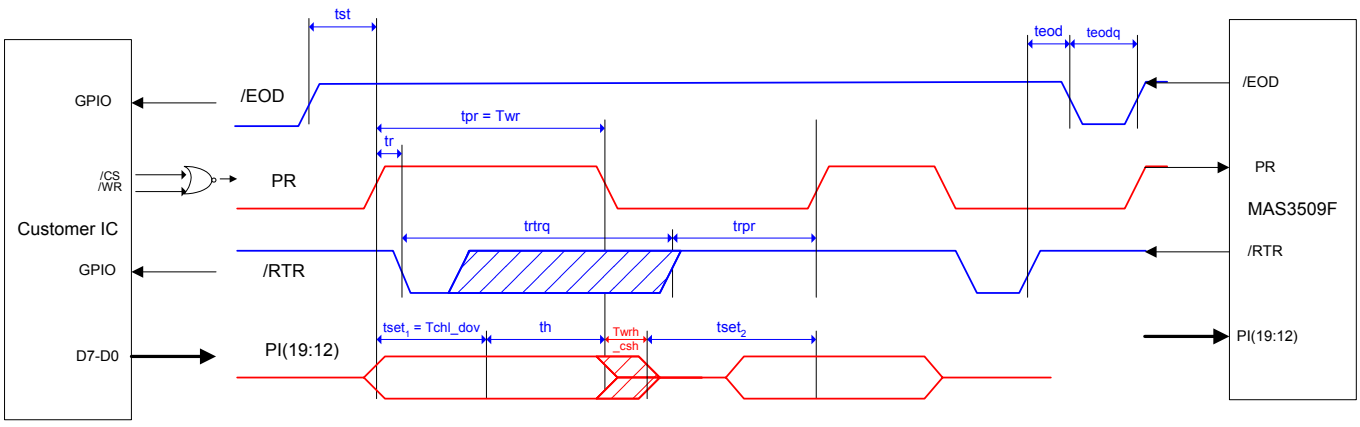


Fig. 4–28: Handshake protocol for writing MPEG data to the PIO-DMA

4.6.2.7. PIO as Parallel Input Interface: Program Download Mode

Handshake for PIO input in Program Download Mode is accomplished through the RTR, PCS, and PI12..PI19 signal lines (see Fig. 4–29). The PR line should be set to low level.

The MAS 35x9F will drive RTR low as soon as it is ready to receive a byte and RTR will stay low until one byte has been written. Writing of a byte is performed with a PCS pulse, driven by the microcontroller. The MAS 35x9F reads data after the falling edge of PCS and will finish the cycle by setting RTR to high level after the rising edge of PCS. The next data transfer is initialized by the MAS 35x9F by driving the RTR line.

Table 4–11: PIO Program Download Mode timing

Symbol	Pin	Min.	Max.	Unit
t_0	$\overline{RTR}$, $\overline{PCS}$	0		µs
t_1	PCS	150		ns
t_2	$\overline{PCS}$, $\overline{RTR}$	0	30	ns
t_3	RTR	0.4	5	µs
t_4	PI	50		ns
t_5	PI	50		ns

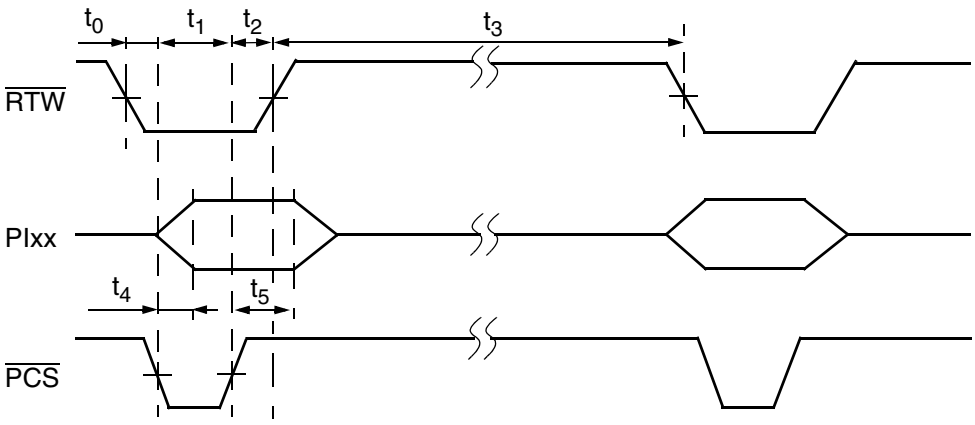


Fig. 4–29: PIO program download mode timing

4.6.2.8. PIO as Parallel Output Interface

Some downloadable software may use the PIO interface (lines PI19...PI12) as output. The data transfer rate and conditions are defines by the software function.

Handshaking for PIO output mode is accomplished through the $\overline{RTW}$, $\overline{PCS}$, and PI12..PI19 signal lines (see Fig. 4–30). The PR line has to be set to high level.

$\overline{RTW}$ will go low as soon as a byte is available in the output buffer and will stay low until a byte has been read. Reading of a byte is performed with a $\overline{PCS}$ pulse. Data is latched out from the MAS on the falling edge of $\overline{PCS}$ and removed from the bus on the rising edge of $\overline{PCS}$.

Table 4–12: PIO output mode timing

Symbol	Pin	Min.	Max.	Unit
t_0	$\overline{RTW}$, $\overline{PCS}$	0.010	1800	µs
t_1	PCS	0.330		µs
t_2	$\overline{PCS}$, $\overline{RTW}$	0.010		µs
t_3	RTW	0.330	10000	µs
t_4	PI	0.330		µs
t_5	PI	0.081		µs

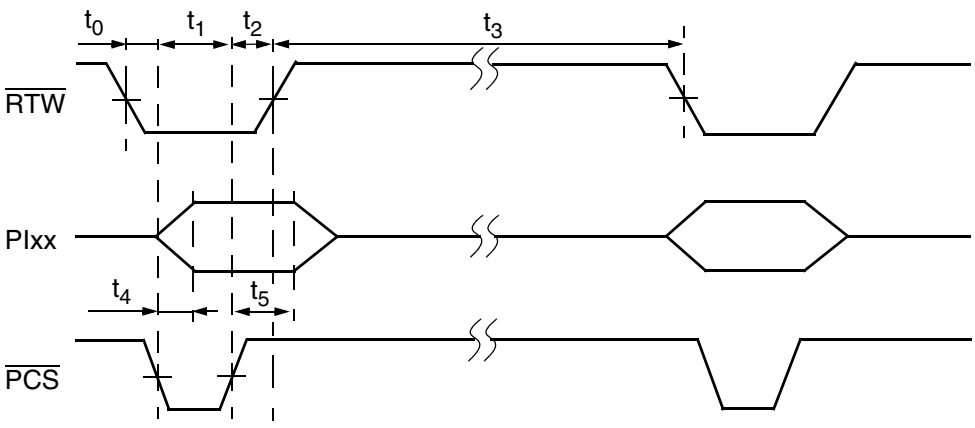


Fig. 4–30: Output timing

4.6.3. Analog Characteristics

at T = T_A, V_{SUPDn}, V_{SUPx} = 2.2 to 3.6 V, V_{SUPA} = 2.2 to 3.6 V, $f_{CRYSTAL}$ = 13 to 20 MHz, typical values at T_A = 25 °C and $f_{CRYSTAL}$ = 18.432 MHz in P(L/M)QFP package

Symbol	Parameter	Pin Name	Limit Values			Unit	Test Conditions
			Min.	Typ.	Max.		
Analog Supply							
I_{AVDD}	Current consumption analog audio	AVDD0/1		5		mA	V_{SUPA} = 2.2 V, Mute
I_{QOSC}	Current consumption crystal oscillator	AVDD0/1		200		µA	Codec = off DSP = off DC/DC = on
$I_{STANDBY}$					10		Codec = off DSP = off DC/DC = off
Crystal Oscillator							
V_{DCCLK}	DC voltage at oscillator pins	XTI, XTO		0.5		V_{SUPA}	
V_{ACLK}	Clock amplitude		0.5		V_{SUPA} −0.5	V_{PP}	if crystal is used
C_{IN}	Input capacitance			3		pF	
R_{OUT}	Output resistance	XTO		220		Ω	V_{SUPA} = 2.2 V
				125			V_{SUPA} = 2.7 V
				94			V_{SUPA} = 3.3 V
Analog Reference							
V_{AGNDC}	Analog Reference Voltage	AGNDC				V	R_L >> 10 MΩ, referred to VREF
							V_{SUPA} bits[15], [14] in register $6A_{hex}$
				1.1			>2.2 V 00
				1.3			>2.4 V 01
				1.6			>3.0 V 10
V_{MICBI}	Bias voltage for microphone	MICBI					V_{SUPA} bits[15], [14] in register $6A_{hex}$
				1.8			>2.2 V 00
				2.13			>2.4 V 01
				2.62			>3.0 V 10
R_{MICBI}	Source resistance	MICBI		180		Ω	
I_{MAX}	Maximum current microphone bias	MICBI				µA	V_{SUPA} bits[15], [14] in register $6A_{hex}$
				300			>2.2 V 00

Symbol	Parameter	Pin Name	Limit Values			Unit	Test Conditions
			Min.	Typ.	Max.		
Analog Audio Input							
V_{AI}	Analog line input clipping level (at minimum analog input gain, i.e. –3 dB)	INL/R				V_{pp}	V_{SUPA} bits[15], [14] in register $6A_{hex}$
				2.2			>2.2 V 00
				2.6			>2.4 V 01
				3.2			>3.0 V 10
V_{MI}	Microphone input clipping level (at minimum analog input gain, i.e. +21 dB)	MICIN				mV_{pp}	V_{SUPA} bits[15], [14] in register $6A_{hex}$
				141			>2.0 V 00
				167			>2.4 V 01
				282			>3.0 V 10
R_{inAI}	Analog line input resistance	INL/R		97		kΩ	at minimum analog input gain, i.e. –3 dB
				20			at maximum analog input gain, i.e. +19.5 dB
				67			not selected
R_{inMI}	Microphone input resistance	MICIN		94		kΩ	at minimum analog input gain, i.e. –21 dB
				8			at maximum analog input gain, i.e. +43.5 dB
				94			not selected
SNR_{AI}	Signal-to-noise ratio of line input	INL/R		74		dB(A)	BW = 20 Hz...20 kHz, analog gain = 0 dB, input 1 kHz at V_{AI}–20 dB
SNR_{MI}	Signal-to-noise ratio of microphone input	MICIN		73		dB(A)	BW = 20 Hz...20 kHz, analog gain = +21 dB, input 1 kHz at V_{MI}–20 dB
THD_{AI}	Total harmonic distortion of analog inputs	INL/R MICIN		0.01	0.02	%	BW = 20 Hz...20 kHz, analog gain = 0 dB, resp. 24 dB, input 1 kHz at –3 dBFS = V_{AI}–6 dB resp. V_{MI}–6 dB
$XTALK_{AI}$	Crosstalk attenuation left/right channel (analog inputs)	INL/R MICIN		80		dB	f = 1 kHz, sine wave, analog gain = 0 dB, input = –3 dBFS
$PSRR_{AI}$	Power supply rejection ratio for analog audio inputs	AVDD0/1, INL/R MICIN		45		dB	1 kHz sine at 100 mV_{rms}
				20		dB	≤100 kHz sine at 100 mV_{rms}

Symbol	Parameter	Pin Name	Limit Values			Unit	Test Conditions
			Min.	Typ.	Max.		
Audio Output							
V_{AO1}	Analog output voltage AC	OUTL/R					$R_L \geq 1\ k\Omega$ input = 0 dBFS digital V_{SUPA} bits[15], [14] in register $6A_{hex}$
	at 0 dB output gain			1.56		V_{pp}	>2.2 V 00
				1.84			>2.4 V 01
				2.27			>3.0 V 10
	at +3 dB output gain			2.20		V_{pp}	>2.2 V 00
				2.60			>2.6 V 01
				3.20			>3.2 V 10
dV_{AO1}	Deviation of DC-level at analog output for AGNDC-Voltage	OUTL/R	−20		20	mV	
V_{AO2}	Analog output voltage AC	OUTL/R					R_L is 16 Ω headphone and 22 Ω series resistor Input = 0 dBFS digital (see Fig. 5–1 on page 89) V_{SUPA} bits[15], [14] in register $6A_{hex}$
	at 0 dB output gain			1.56		V_{pp}	>2.2 V 00
				1.84			>2.4 V 01
				2.27			>3.0 V 10
	at +3 dB output gain			2.00		V_{pp}	>2.2 V 00
				2.40			>2.6 V 01
				3.00			>3.2 V 10
R_{outAO}	Analog output resistance	OUTL/R			6	Ω	analog gain = +3 dB, input = 0 dBFS digital
SNR_{AO}	Signal-to-noise ratio of analog output	OUTL/R		94		dB(A)	$R_L \geq 16\ \Omega$ BW = 20 Hz...20 kHz, analog gain = 0 dB input = −20 dBFS
THD_{AO}	Total harmonic distortion (headphone)	OUTL/R		0.03 0.003	0.05 0.01	%	for $R_L \geq 16\ \Omega$ plus 22 Ω series resistor (see Fig. 5–1 on page 89) for $R_L \geq 1\ k\Omega$
Lev_{MuteAO}	Mute level	OUTL/R		−113		dBV	A-weighted BW = 20 Hz...22 kHz, no digital input signal, analog gain = mute

Symbol	Parameter	Pin Name	Limit Values			Unit	Test Conditions
			Min.	Typ.	Max.		
$XTALK_{AO}$	Crosstalk attenuation left/right channel (headphone)	OUTLR		80		dB	f = 1 kHz, sine wave, OUTL/R: $R_L \geq 16\ \Omega$ (see Fig. 5–1 on page 89) analog gain = 0 dB input = –3 dBFS
$PSRR_{AO}$	Power supply rejection ratio for analog audio outputs	AVDD0/1 OUTL/R		70		dB	1 kHz sine at 100 mV_{rms}
				35		dB	≤100 kHz sine at 100 mV_{rms}

4.6.4. DC/DC Converter Characteristics

at T = T_A, V_{in} = 1.2 V, V_{outn} = 3.0 V, f_{clk} = 18.432 MHz, f_{sw} = 384 kHz, PWM mode, L = 22 µH, in P(L/M)QFP package (unless otherwise noted) Typ. values for T_A = 25 °C

Symbol	Parameter	Pin Name	Limit Values			Unit	Test Conditions
			Min.	Typ.	Max.		
V_{IN}	Minimum start-up input voltage			0.9		V	$I_{LOAD} \leq 1$ mA, DCCF = 5050_{hex} (reset)
V_{IN}	Minimum operating input voltage						1)
	DC1 DC2			0.7 0.8		V	I_{LOAD} = 50 mA, DCCF = 5050_{hex} (reset)
	DC1 DC2			1.1 1.2		V	I_{LOAD} = 200 mA, DCCF = 5050_{hex} (reset)
V_{OUT}	Programmable output voltage range	VSENSn	2.0		3.5	V	Voltage settings in DCCF register (I^2C subaddress 76_{hex})
V_{OTOL}	Output voltage tolerance	VSENSn	–4		4	%	I_{LOAD} = 20 mA T_A = 25 °C 2)
I_{LOAD1}	Output current 1 battery cell	VSENSn			200	mA	V_{IN} = 0.9...1.5 V, 330 µF
I_{LOAD2}	Output current 2 battery cells				600	mA	V_{IN} = 1.8...3.0 V, 330 µF
$dV_{OUT}/dV_{IN}/V_{OUT}$	Line regulation	VSENSn		0.7		%/V	I_{LOAD} = 20 mA
dV_{OUT}/V_{OUT}	Load regulation	VSENSn		–1.8		%	I_{LOAD} = 20...200 mA,
h_{max}	Maximum efficiency				95	%	V_{IN} = 2.4 V, V_{OUT} = 3.5 V
f_{switch}	Switching frequency	DCSOn	297	384	576	kHz	(see Section 2.6.2. on page 12), (see Table 3–3)
$f_{startup}$	Switching frequency during start-up	DCSOn		250		kHz	VSENSn < 1.9 V

1) Since the regulators are bootstrapped, once started they will operate down to 0.7 V input voltage
2) PFM mode regulates approx. 1% higher

Symbol	Parameter	Pin Name	Limit Values			Unit	Test Conditions
			Min.	Typ.	Max.		
$I_{supPFM1}$	Supply current in PFM mode	VSENS1		75		µA	3)
$I_{supPFM2}$		VSENS2		135			
$I_{supPWM1}$	Supply current in PWM mode	VSENS1		265		µA	VSENSn 3) 4)
$I_{supPWM2}$		VSENS2		325			
I_{lnmax}	NMOS switch current limit (low side switch)	DCSOn, DCSGn		1		A	PWM-Mode
				0.4		A	PFM-Mode
I_{lptoff}	PMOS switch turnoff current (rectifier switch)	DCSOn VSENSn		70		mA	
R_{on}	NMOS switch on Resistance (low side switch)	DCSO1, DCSG1		170		mΩ	
		DCSO2, DCSG2		280		mΩ	
I_{LEAK}	Leakage current	DCSOn, DCSGn		0.1		µA	Converter off, no load

3) Current into VSENSn Pin. VIN > VOUT + 0.4V; no DC/DC-Converter switching action present
4) Add. current of oscillator at PIN AVDD0/1, (see Section 4.6.3. on page 81)

4.6.5. Typical Performance Characteristics

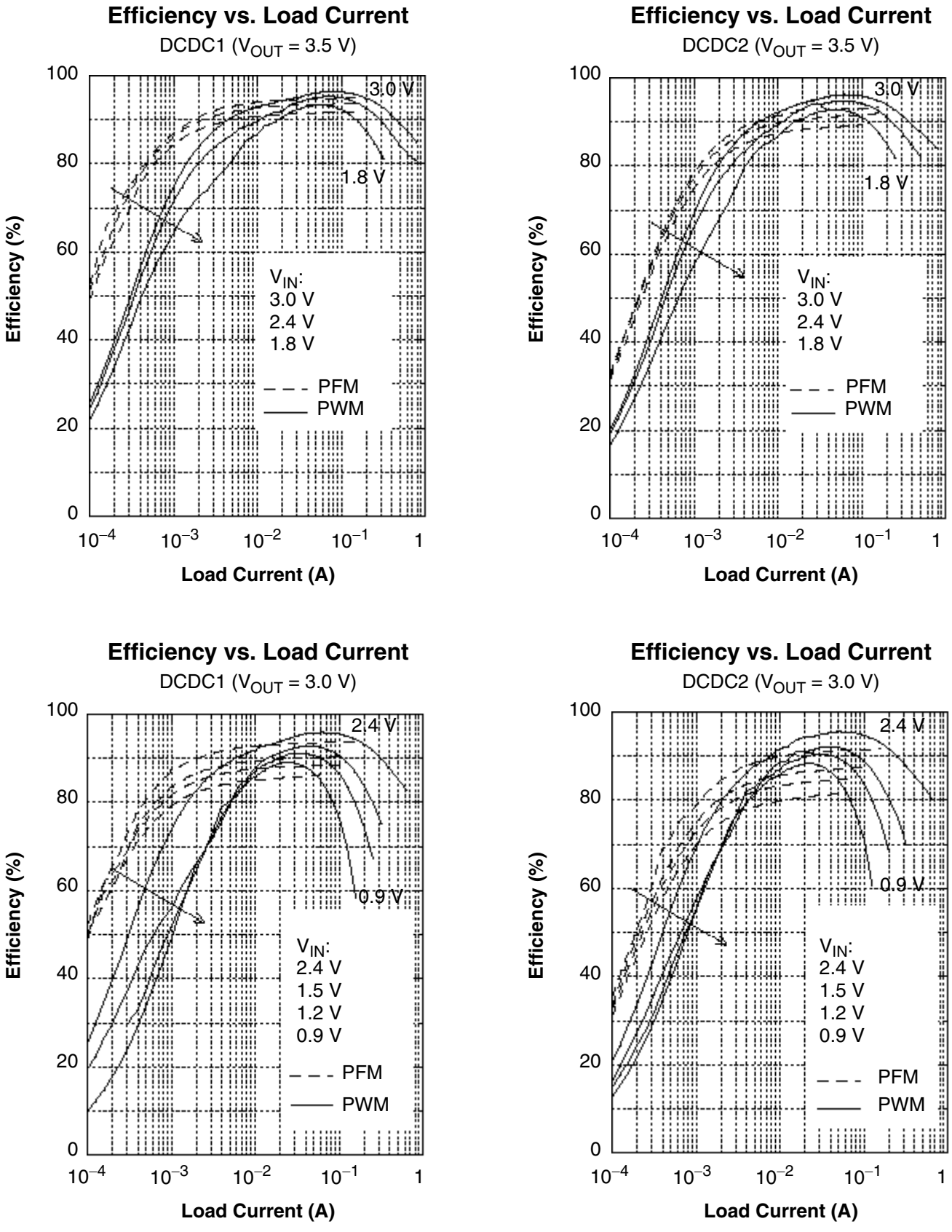


Fig. 4–31: Efficiency vs. Load Current

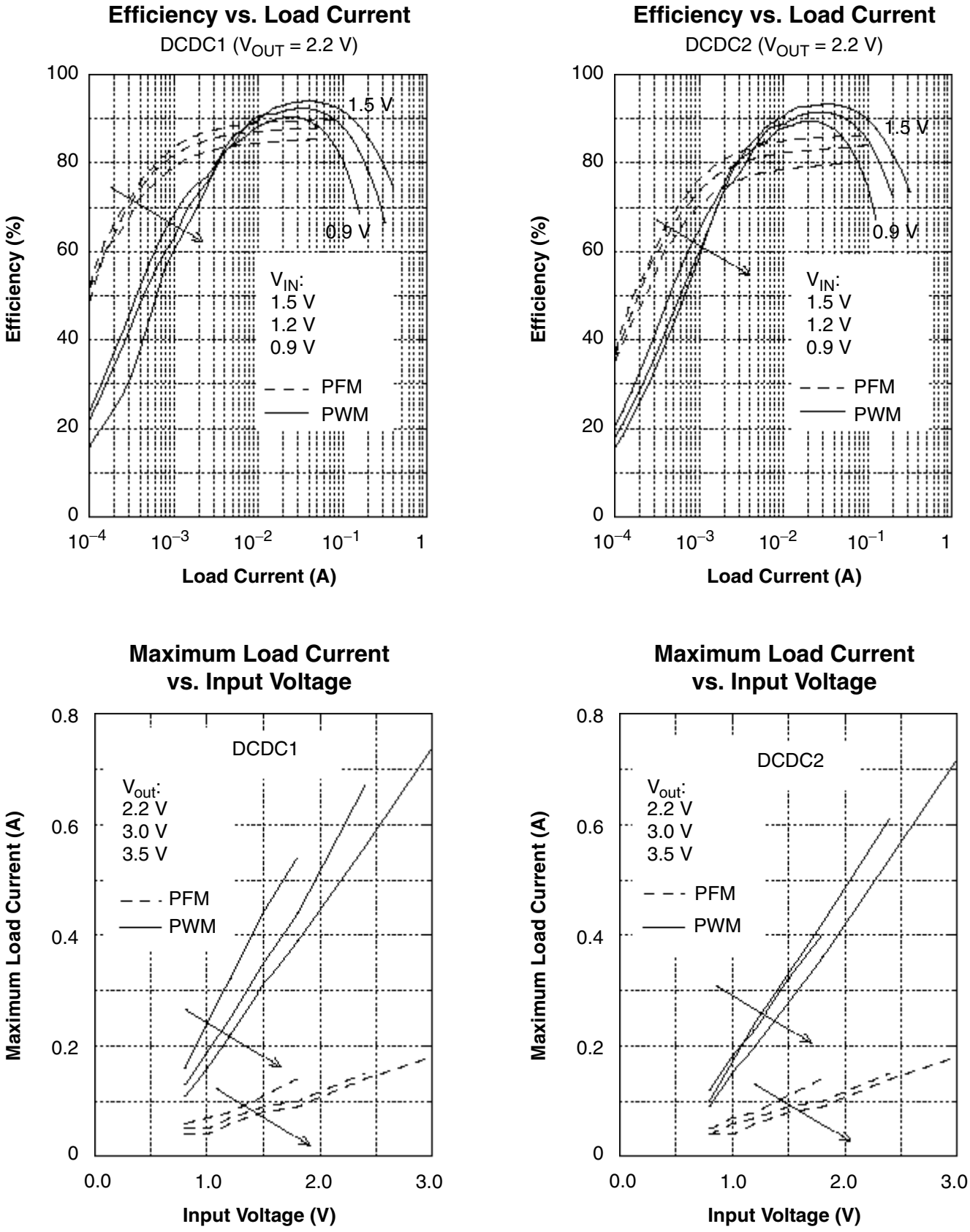
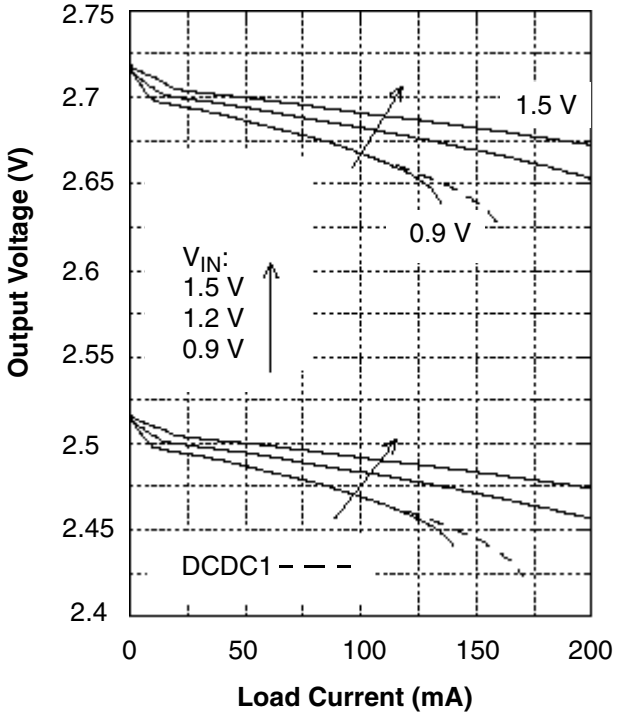


Fig. 4–32: Maximum Load Current vs. Input Voltag

Note: Efficiency is measured as $V_{SENSn} \times I_{LOAD} / (V_{in} \times I_{in})$.
I_{AVDD} is not included (Oscillator current)

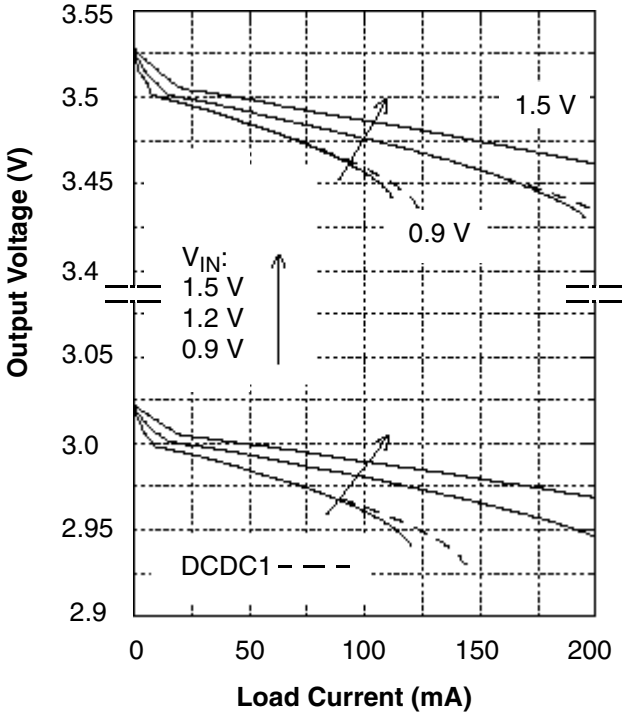
Loadregulation

at V_{OUT} = 2.7 V, 2.5 V



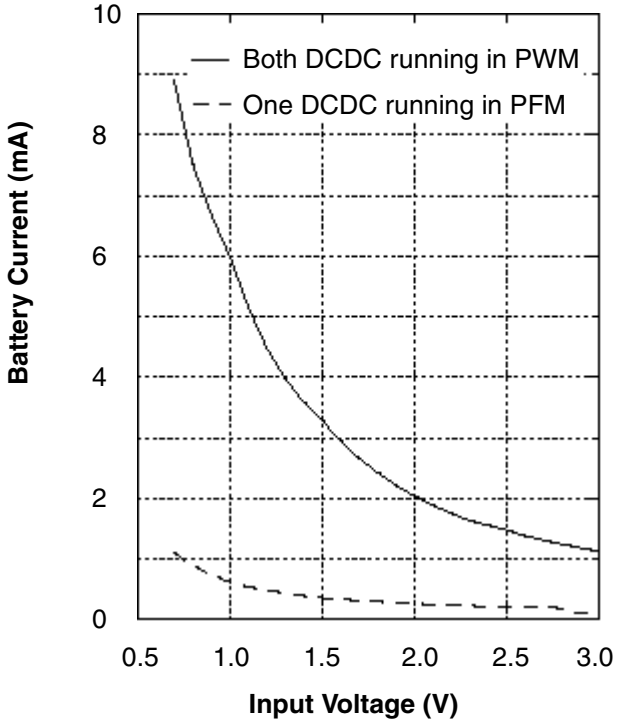
Loadregulation

at V_{OUT} = 3.0 V, 3.5 V



No-Load Battery Current

V_{OUT} = 3.0 V



5. Application

5.1. Typical Application in a Portable Player

– MMC/SDI-Card or SMC/CF2+ used as storage media
– Dashed lines show optional (external) devices

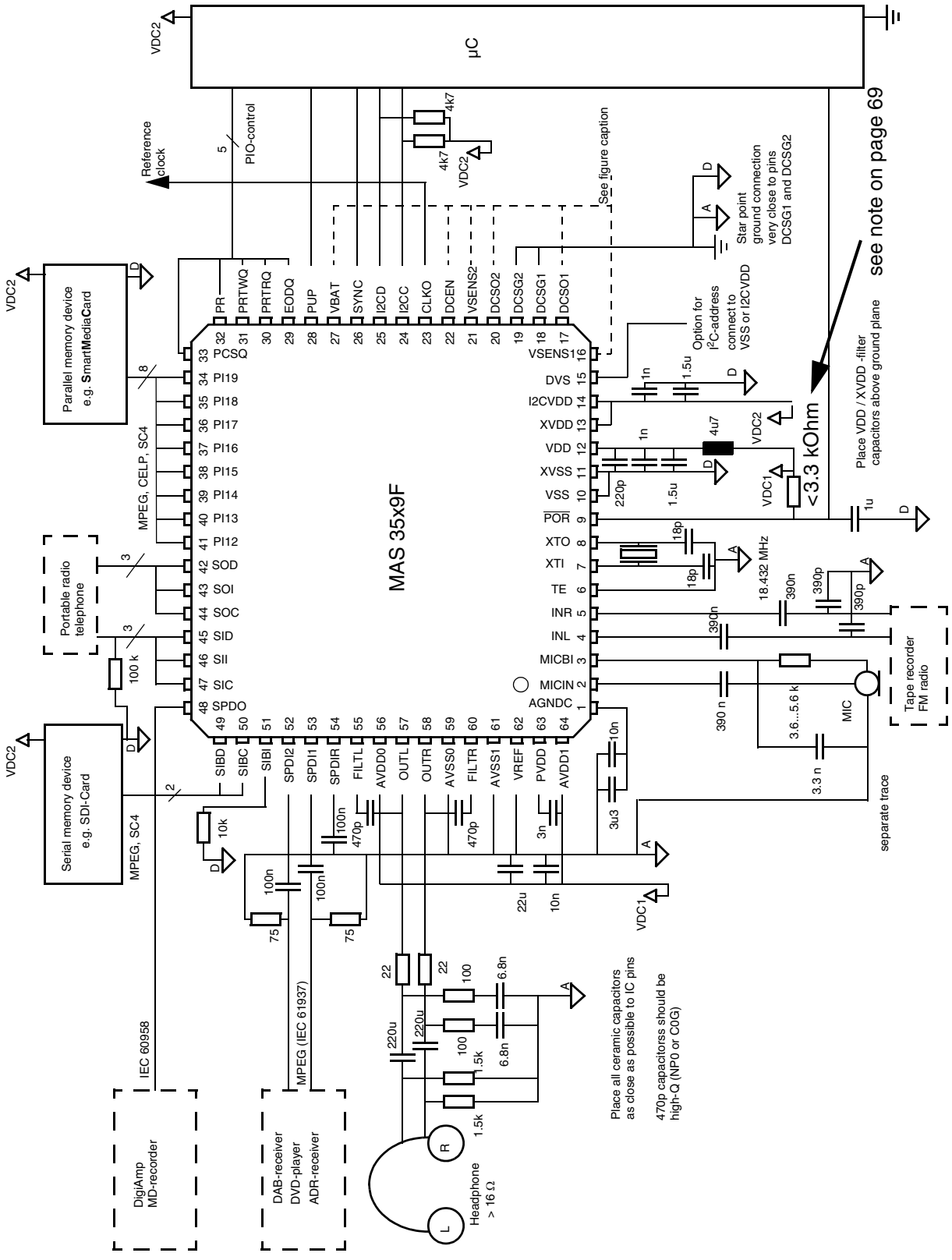


Fig. 5–1: Application circuit of the MAS 35x9F. For connections of the DC/DC converters, please refer to Fig. 5–2.

5.2. Recommended DC/DC Converter Application Circuit

(Power optimized scenario, (see Fig. 2–7 on page 13)).

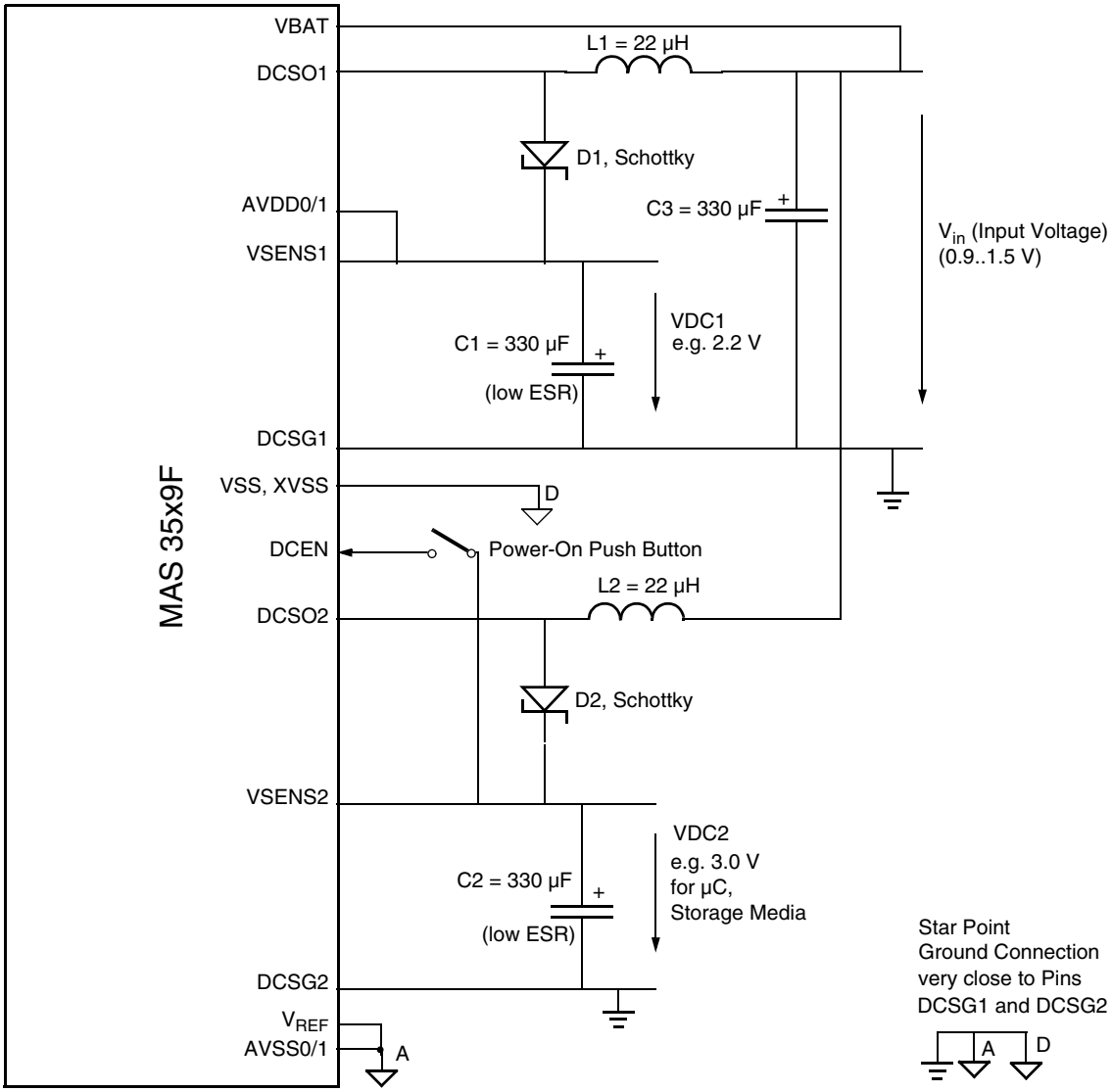


Fig. 5–2: External circuitry for the DC/DC converters

For turn-on voltage of DSP and codec, please refer to Section 2.11.2.1.

6. Data Sheet History

1. Preliminary data sheet: “MAS 35x9F, MPEG Layer 2/3, AAC Audio Decoder, G.729 Annex A Codec”, Aug. 01, 2001, 6251-505-1PD. First release of the preliminary data sheet.
2. Data Sheet: “MAS 35X9F MPEG Layer 2/3, AAC Audio Decoder, G.729 Annex A Codec”, June 30, 2004, 6251-505-1DS. First release of the data sheet.
   Major changes:

– New package diagrams were included for PLQFP64-1, PMQFP64-2, PQFN64-1

– Functional description of the MP3 Block Input Mode now available for improved input timing behavior of the MPEG 1/2/2.5 Layer3 decoder

– Important advice for turn-on and operating voltage

– Changes in configuration registers

– Tables were added: PIO input DMA mode timing; Sample rate in MP3; Sample rate in AAC

– Handshake protocol for writing MPEG data to the PIO-DMA was added.

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