MITSUBISHI BIPOLAR DIGITAL ICs

M54956P

PLL FREQUENCY SYNTHESIZER FOR PERSONAL RADIOS

DESCRIPTION

The M54956P is a single-chip semiconductor integrated circuit consisting of a PLL frequency synthesizer for personal radio.

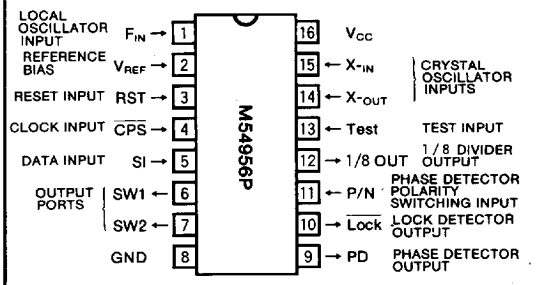
FEATURES

- Built-in 1/256 and 1/258 modulus prescaler (fmax=1.0GHz)
- Low power dissipation (I_{CC}=40mA, at V_{CC}= 5 V)
- Choice of four comparator frequency types (50k, 25k, 12.5k, 6.25k)
- Wide variety of division ratio (32768~262142, binary code)
- 1/8 Clock pulse output for referene oscillator frequency (TTL level)
- Output display for PLL lock/unlock
- Output port status can be set by date transferred from the controller
- Serial data input (three data transfer lines)

APPLICATION

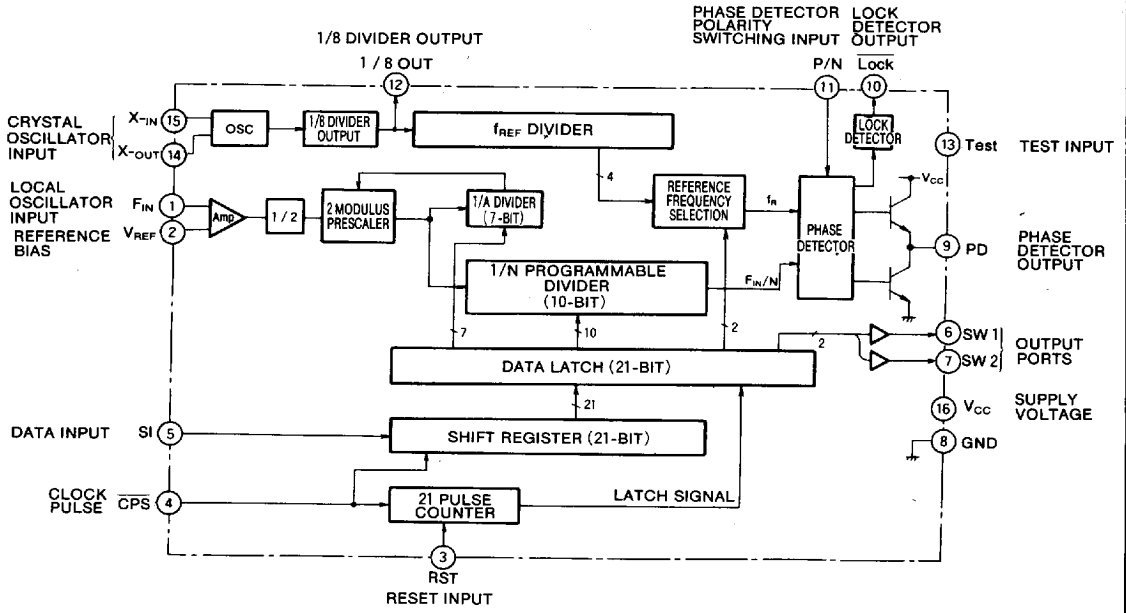
Personal radios, mobile radio telephones, MCA equipment

PIN CONFIGURATION (TOP VIEW)



Outline 16P4

BLOCK DIAGRAM



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PLL FREQUENCY SYNTHESIZER FOR PERSONAL RADIOS

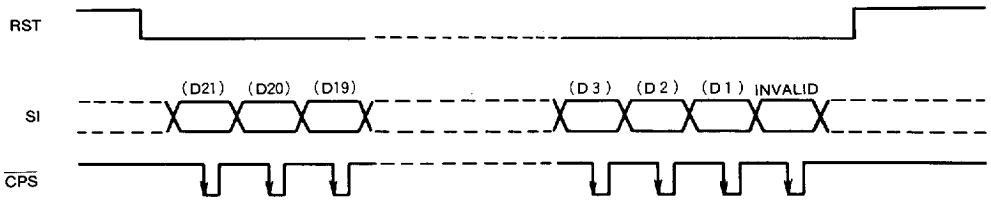
PIN DESCRIPTION

Pin no.	Symbol	Pin name	Description
1	F_{IN}	Local oscillator input	Local oscillator frequency (V.C.O) input. f_{max}=1000MHz
2	V_{REF}	Reference bias	Connbct to ground through a 1000pF capacitor
3	RST	Reset input	Reset input of 21-pulse counter
4	$\overline{CPS}$	Clock input	Clock input for shift register
5	SI	Data input	Data input pin for shift register
6	SW1	Output port	Open-collector output port can be set by data tranferred from the controller.
7	SW2		
8	GND	Ground	0 V
9	PD	Phase detector output	Three-state
10	$\overline{Lock}$	Lock detector output	Low when the PLL is locked, high when unlocked. Open collector.
11	P/N	Phase detector polarity switching	When P/N is high, the output at PD pin becomes high when the phase is advanced and low when the phase is retarded. When P/N is low, the logic states are inverted.
12	1/8OUT	1/8 divider output	TTL level
13	Test	Test input	Normally set low. When set high, f_R (the comparator frequency) is output at SW1 (pin 6) and the f_{IN}/N (programmable divider) is output at SW2 (pin 7).
14	$X\text{-}_{OUT}$	Crystal oscillator input	The output from 12.8MHz reference oscillator is supplied to $X\text{-}_{IN}$. Oscillation is generated by an externally connected crystal oscillator.
15	$X\text{-}_{IN}$		
16	V_{CC}	Supply voltage pin	4.5~5.5V

FUNCTION

1. DATA INPUT

Configuration of input signal



Note 1 : The status of input SI is read by the shift register at the falling edge of the clock signal at $\overline{CPS}$.
2 : All data (N value, port, comparator frequency) are set at the falling edge of the 21st pulse at $\overline{CPS}$.Subsequent clock pulse at $\overline{CPS}$ are ignored.
3 : Pulses are accepted at neither $\overline{CPS}$ nor SI while RST is high.

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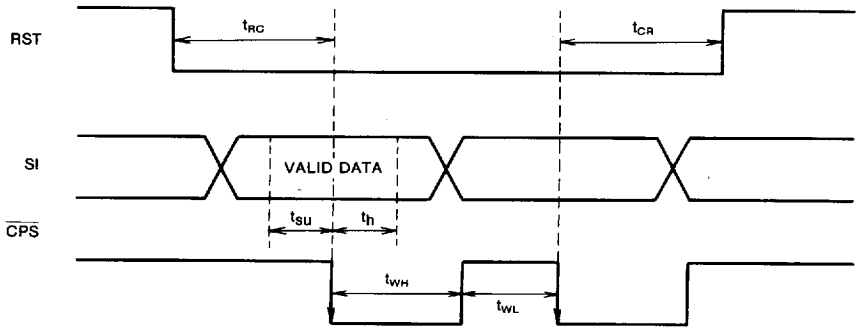
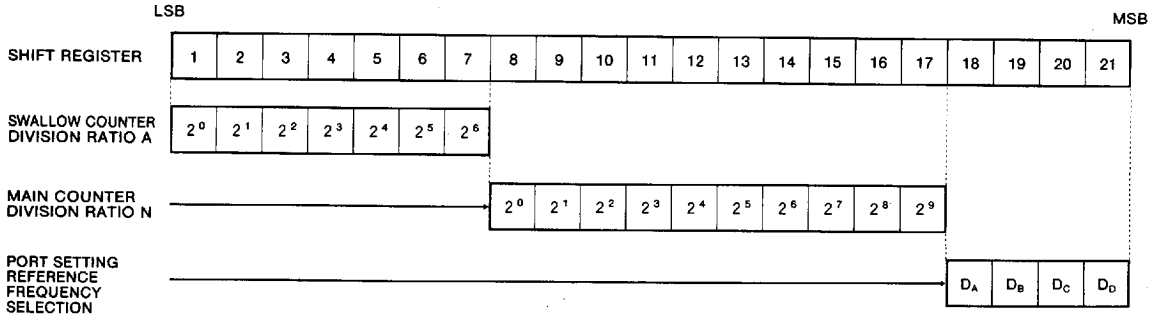
Timing of input signal



$t_{SU}=t_h=t_{WH}=t_{WL}=10\mu S$ min.

$t_{RC}=t_{CR}=20\mu S$ min.

2. BIT CONFIGURATION OF SHIFT REGISTER



Note 4 : Total division ratio M is given by $M=2\times(A+128N)$.
5 : Comparator frequency is selected by D_A and D_B.

Data		Reference frequency
D_A	D_B	
L	L	50k
H	L	25k
L	H	12.5k
H	H	6.25k

Note 6 : Output port is set by D_C and D_D.

Data		Output port	
D_C	D_D	SW1	SW2
L	L	L	L
H	L	H	L
L	H	L	H
H	H	H	H

3. DATA CODING EXAMPLE

When reference freqency is 6.25kHz, M is 153784, SW1 is high and SW2 is low.

	LSB																				MSB
SHIFT REGISTER	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21
DATA	L	L	H	H	H	L	H	L	L	L	H	H	L	H	L	L	H	H	H	H	L

DIVISION RATIO SETTING FOR SWALLOW COUNTER
$A=2^2+2^3+2^4+2^6=92$

DIVISION RATIO SETTING FOR MAIN COUNTER
$N=2^3+2^4+2^6+2^9=600$

REFERENCE FREQUENCY 6.25kHz is selected.

SW1 IS SET HIGH

SW2 IS SET LOW

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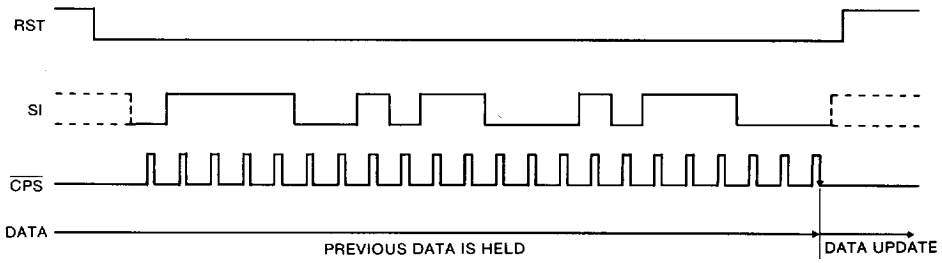
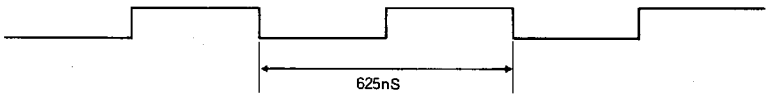


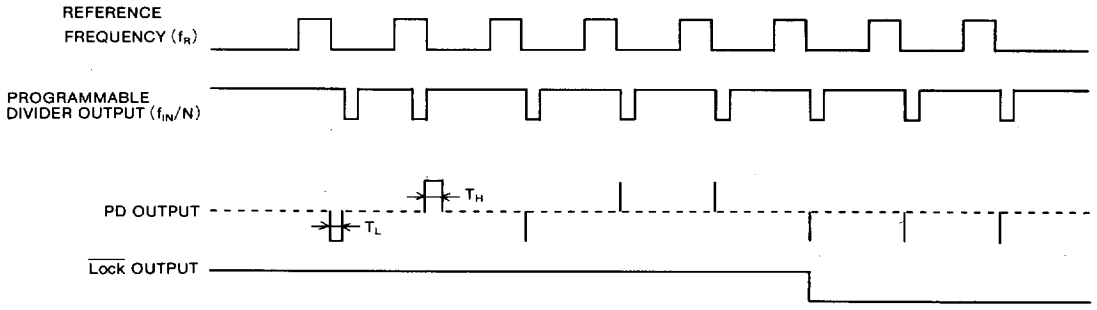
Note 7 : Total division ratio is set by M= 2 ×M(A+128N)= 2 ×(92+128×600)=153784.
8 : When PLL is locked, $f_{V.C.O}$=6.25×153784=961150kHz
=961.15MHz

4. 1/8 OUTPUT SIGNAL WAVEFORM



※Duty cycle is 50%.

5. PD, $\overline{\text{Lock}}$ SIGNAL OUTPUT WAVEFORM

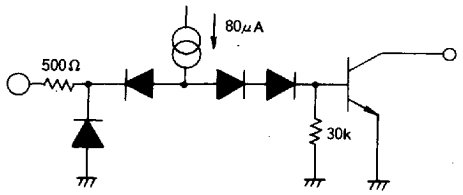


Note 9 : The PD output is low when the phase of the programmable divider output (f_{IN}/N) follows the phase of reference frequency (f_R) and is high when the phase f_{IN}/N leads that of f_R.
10 : Broken lines indicate the high-impedance state.
11 : When phase variance T_L and T_H are less than 625ns for a period of rerence frequency (f_R), the lock output becomes low.

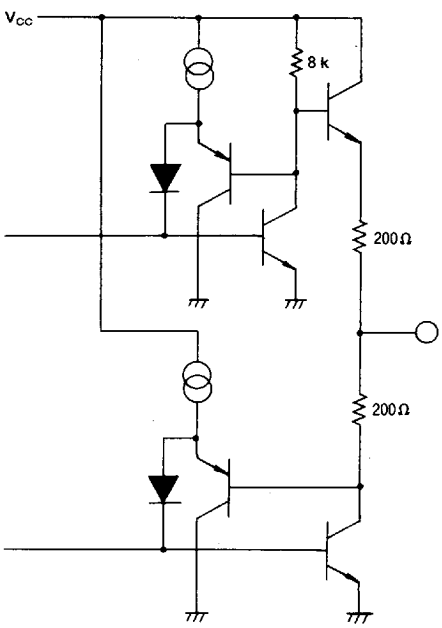
※The above description applies while P/N (pin 11) is high.
While P/N input is low, the logic state of the PD output is inverted.

I/O CIRCUIT DIAGRAM

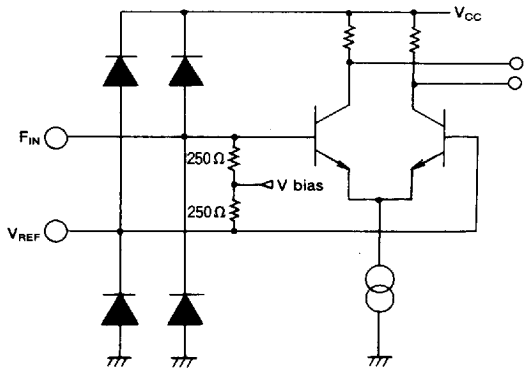
1 RST, $\overline{CPS}$, SI, P/N, Test Inputs



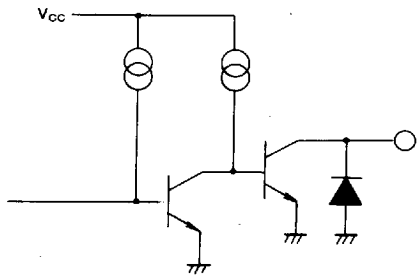
2 PD Output



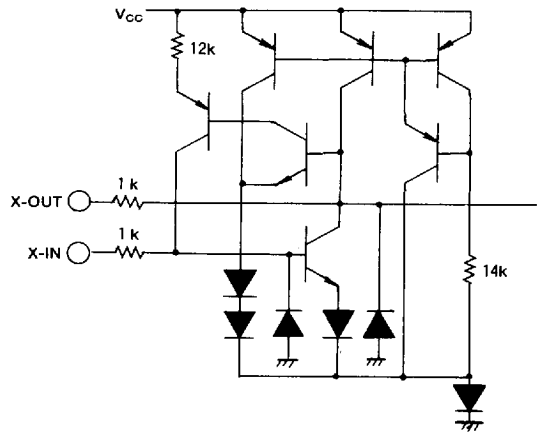
3 F_{IN}, V_{REF} Inputs



4 SW1, SW2, Lock Outputs



5 OSC Circuit



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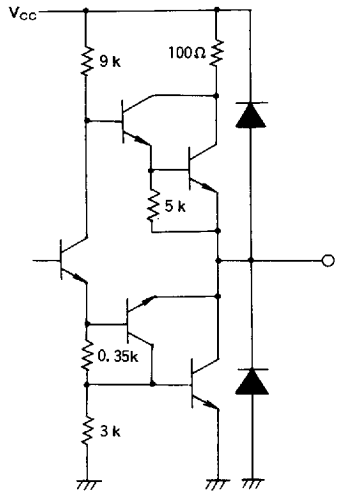
6 1 / 8 OUT Output



Note 12 : Resistance and current are typical values when V_{CC}= 5 V and T_a=−20~+75℃.

ABSOLUTE MAXIMUM RATINGS (T_a = −20~+75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings		Unit
			Min	Max	
V_{CC}	Supply voltage		−0. 5	6. 0	V
V_I	Input voltage	Each input	−0. 5	6. 0	V
V_O	Output voltage	Each input	−0. 5	6. 0	V
Pd	Power dissipation	T_a =75℃		500	mW
Topr	Operating temperature		−20	+75	℃
Tstg	Storage temperature		−40	+125	℃

RECOMMENDED OPERATING CONDITIONS (V_{CC} = 4. 5~5. 5V, T_a = −20~+75℃ unless otherwise noted)

Symbol	Parameter	Conditions	Limits			Unit	Remark
			Min	Typ	Max		
V_{CC}	Supply voltage		4. 5	5	5. 5	V	
V_{IN}	Input amplitude	F_{IN} =100~1000MHz	400		1200	mV_{P-P}	
F_{IN1}	Input frequency	V_{IN} =400mV_{P-P}	100		1000	MHz	
I_{OL}	Low-level output current	SW1, SW2, Lock output			5	mA	
V_{X-IN}	X_{-IN} input amplitude	Note 14	1		2	V_{P-P}	Sine wave
f_{OSC}	Reference oscillation frequency	Note 13, Note 14		12. 8		MHz	

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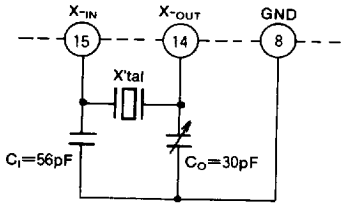
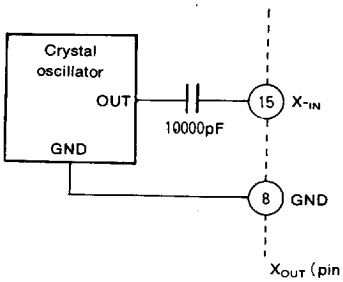
Note 13 : Connection of crystal vibrator



Load capacitance of crystal oscillator

Valid resistance 100Ω or less

Note 14 : Connection of crystal oscillator



X_{OUT} (pin 14) should be left open.

ELECTRICAL CHARACTERISTICS (T_a = −20~+75℃, unless otherwise noted)

Symbol	Parameter	Test pin	Test conditions	Limits			Unit
				Min	Typ	Max	
V_{IH}	High-level input voltage	3, 4, 5, 11, 13	V_{CC}=5.5V	2.0			V
V_{IL}	Low-level input voltage	3, 4, 5, 11, 13	V_{CC}=5.5V			0.6	V
I_{IH}	High-level input current	3, 4, 5, 11, 13	V_{CC}=5.5V, V_{IH}=5.5V			30	μA
I_{IL}	Low-level input current	3, 4, 5, 11, 13	V_{CC}=4.5V, V_{IL}=0V		−80	−160	μA
V_{OL}	Low-level output current	6, 7, 10, 12	V_{CC}=4.5V, I_{OL}=5mA			0.5	V
V_{OHP1}	PD high-level output voltage	9	V_{CC}=4.5V, I_{OH}=−1mA	3.0			V
V_{OHP2}	PD low-level output voltage	9	V_{CC}=5V, I_{OH}=−0.1mA	4.0			V
V_{OLP1}	PD low-level output current	9	V_{CC}=4.5V, I_{OL}=1mA			1.5	V
V_{OLP2}	PD low-level output current	9	V_{CC}=5V, I_{OL}=0.1mA			1.0	V
I_{PD1}	PD leak current	9	V_{CC}=5.5V, V_O=0.8~4.7V			±1.0	μA
I_{PD2}	PD leak current	9	V_{CC}=5V, V_O=2.5V			±100	μA
I_{CC}	Supply voltage	16	V_{CC}=5.5V		40	60	mA
I_{OLK}	Output leak current	6, 7, 10	V_{CC}=5.5V, V_{OH}=5.5V			30	μA
V_{OH}	High-level output voltage	12	V_{CC}=4.5V, I_{OH}=−1V	2.0			V

Note 15 : The GND pin (pin 8) for voltages in this circuit is based on the reference voltage (0)

16 : Whn the currents flowing into the circuit are positive (no sings) and the currents flowing out from the circuit are negative (negative sign) and the minimum and maximum are shown in absolute values.

17 : Typical values are at V_{CC}= 5 V, and T_a=25℃

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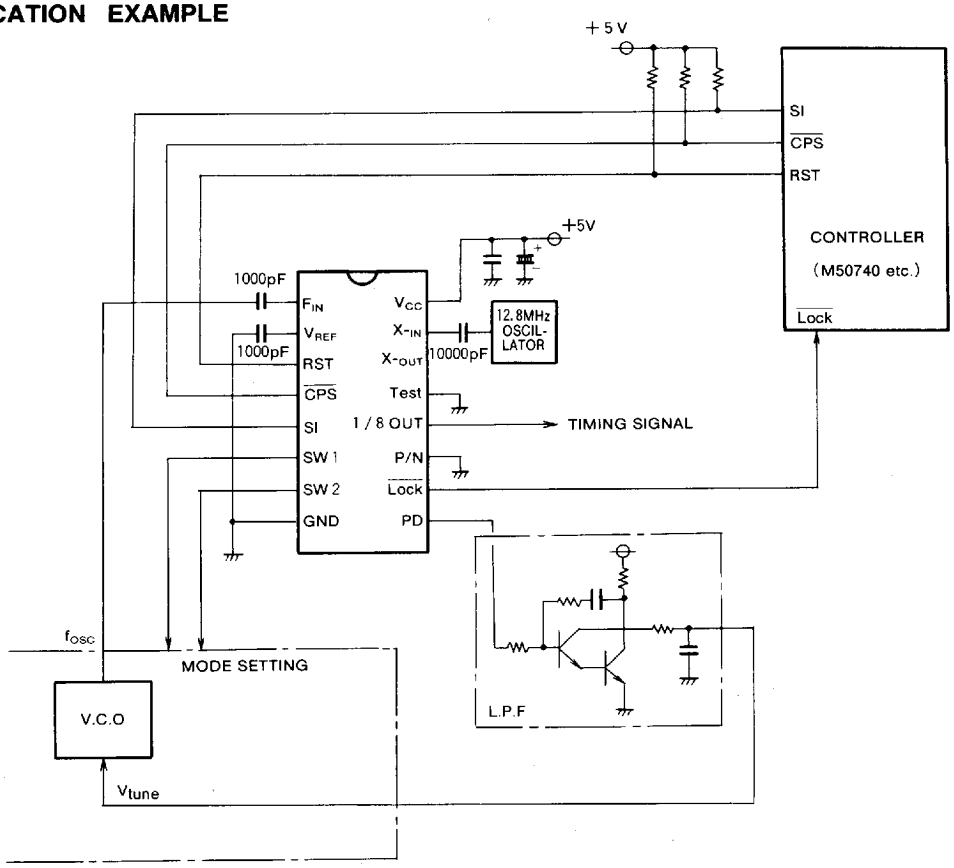
APPLICATION EXAMPLE



TYPICAL CHARACTERISTICS

INPUT AMPLITUDE VS INPUT FREQUENCY