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# HM62256B Series

256k SRAM (32-kword × 8-bit)

# HITACHI

ADE-203-135F (Z)

Rev. 6.0

Nov. 13, 1997

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## Description

The Hitachi HM62256B Series is a CMOS static RAM organized 32,768-word × 8-bit. It realizes higher performance and low power consumption by employing 0.8 μm Hi-CMOS process technology. The device, packaged in 8 × 14 mm TSOP, 8 × 13.4 mm TSOP with thickness of 1.2 mm, 450 mil SOP (foot print pitch width), 600 mil plastic DIP, or 300 mil plastic DIP, is available for high density mounting. It offers low power standby power dissipation; therefore, it is suitable for battery backup systems.

## Features

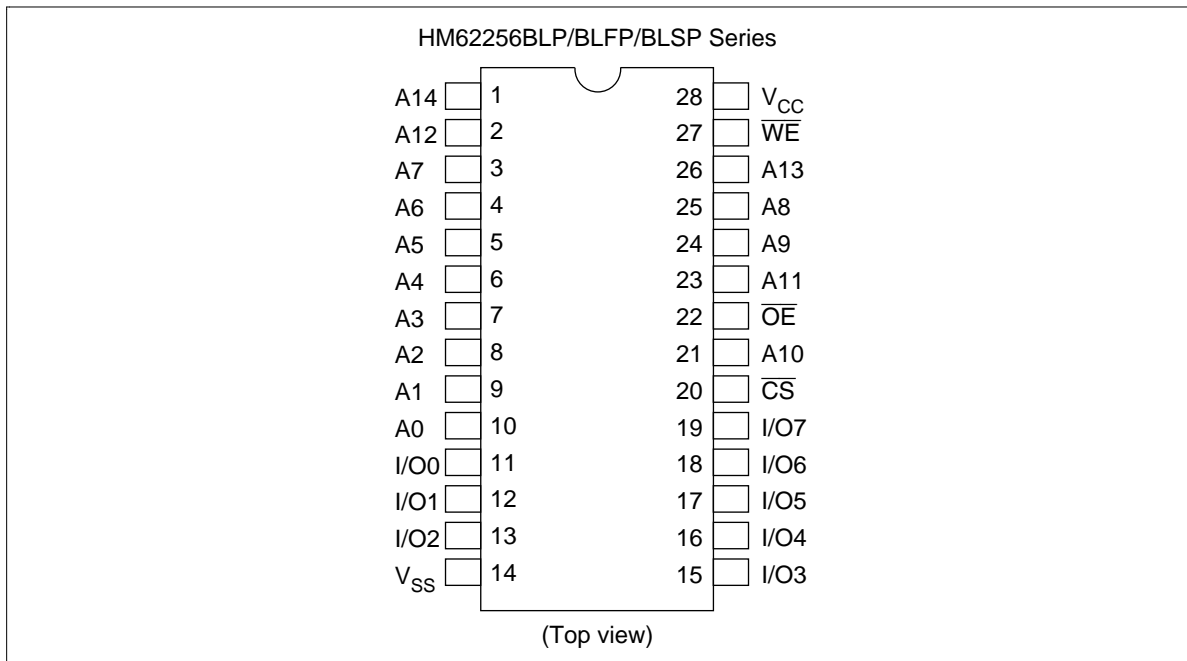
- Single 5.0 V supply: 5.0 V ± 10%
- Access time: 55 ns/70 ns/85 ns (max)
- Power dissipation:
  - Active: 25 mW (typ) (f = 1 MHz)
  - Standby: 1.0 μW (typ)
- Completely static memory
  - No clock or timing strobe required
- Equal access and cycle times
- Common data input and output
  - Three state output
- Directly TTL compatible all inputs and outputs
- Battery backup operation

## HM62256B Series

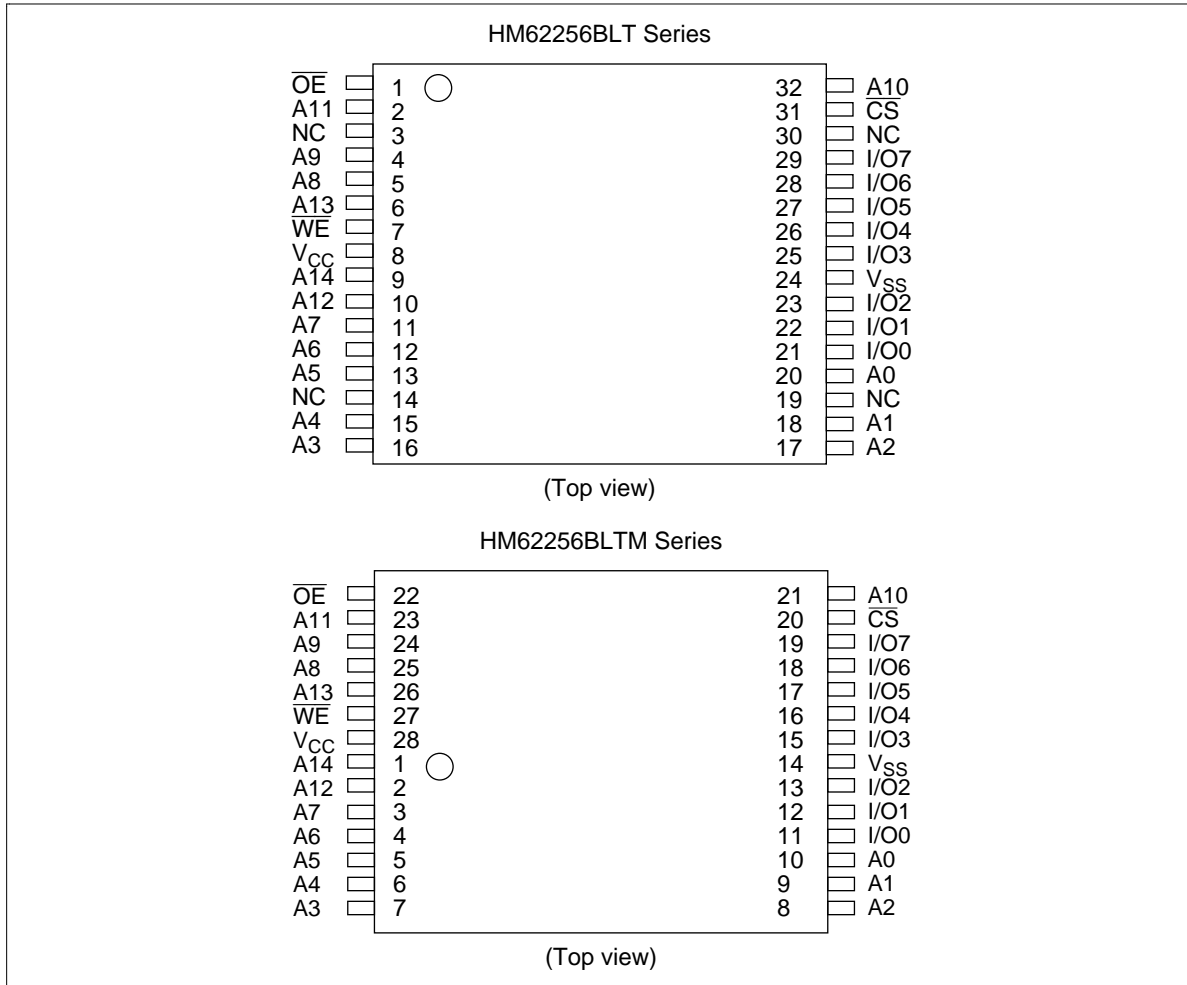
### Ordering Information

Type No.	Access time	Package
HM62256BLP-7	70 ns	600-mil 28-pin plastic DIP (DP-28)
HM62256BLP-7SL	70 ns	
HM62256BLSP-7	70 ns	300-mil 28-pin plastic DIP (DP-28NA)
HM62256BLSP-7SL	70 ns	
HM62256BLFP-7T	70 ns	450-mil 28-pin plastic SOP (FP-28DA)
HM62256BLFP-5SLT	55 ns	
HM62256BLFP-7SLT	70 ns	
HM62256BLFP-7ULT	70 ns	
HM62256BLT-8	85 ns	8 mm × 14 mm 32-pin TSOP (TFP-32DA)
HM62256BLT-7SL	70 ns	
HM62256BLTM-8	85 ns	8 mm × 13.4 mm 28-pin TSOP (TFP-28DA)
HM62256BLTM-5SL	55 ns	
HM62256BLTM-7SL	70 ns	
HM62256BLTM-7UL	70 ns	

### Pin Arrangement



## Pin Arrangement (cont.)

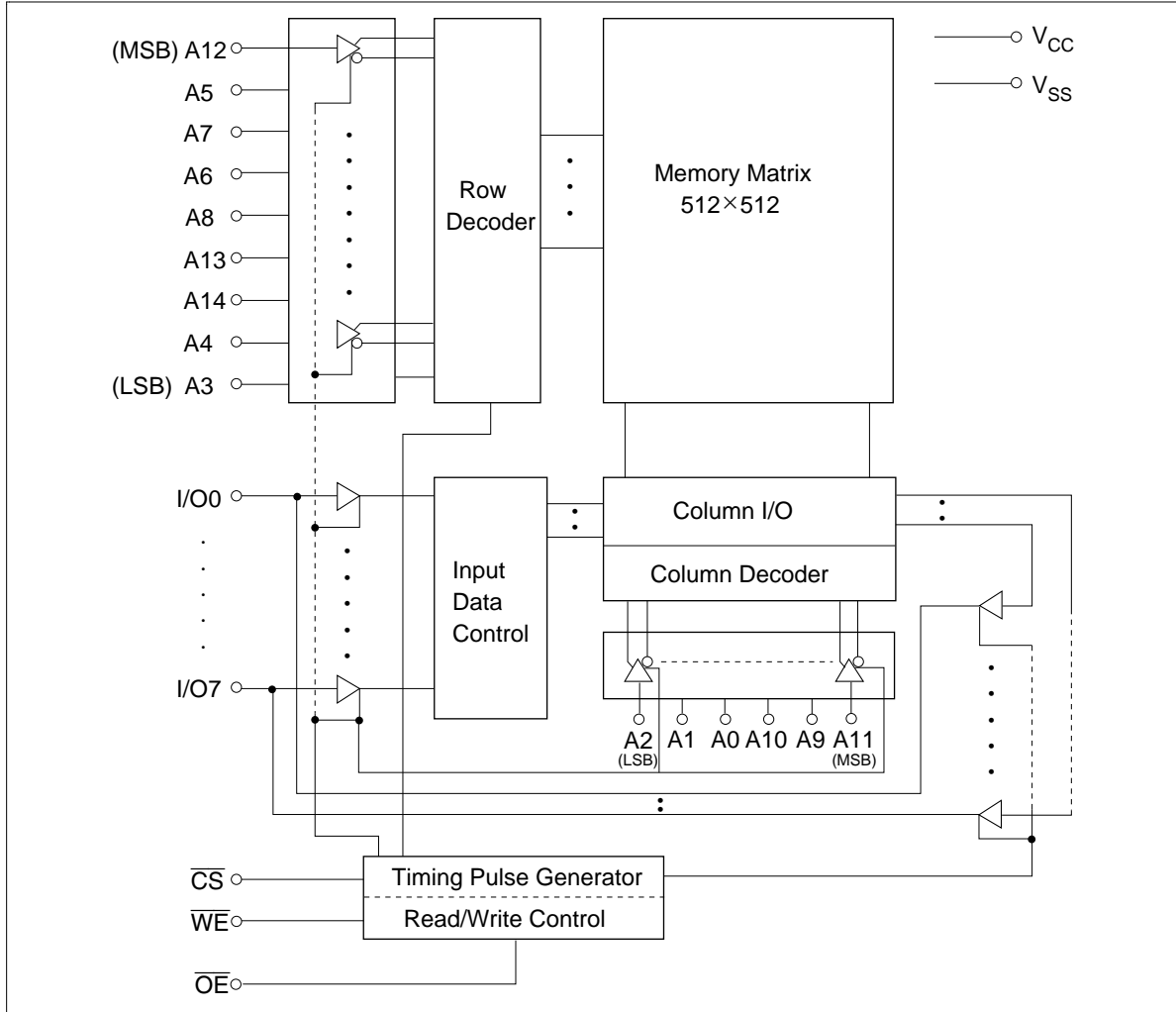


## Pin Description

Pin Name	Function
A0 to A14	Address input
I/O0 to I/O7	Data input/output
$\overline{CS}$	Chip select
$\overline{WE}$	Write enable
$\overline{OE}$	Output enable
V <sub>CC</sub>	Power supply
V <sub>SS</sub>	Ground
NC	No connection

# HM62256B Series

## Block Diagram



**Operation Table**

$\overline{WE}$	$\overline{CS}$	$\overline{OE}$	Mode	$V_{CC}$ current	I/O pin	Ref. cycle
×	H	×	Standby	$I_{SB}, I_{SB1}$	High-Z	—
H	L	H	Output disable	$I_{CC}$	High-Z	—
H	L	L	Read	$I_{CC}$	Dout	Read cycle (1)to (3)
L	L	H	Write	$I_{CC}$	Din	Write cycle (1)
L	L	L	Write	$I_{CC}$	Din	Write cycle (2)

Note: ×: H or L

**Absolute Maximum Ratings**

Parameter	Symbol	Value	Unit
Power supply voltage relative to $V_{SS}$	$V_{CC}$	-0.5 to +7.0	V
Terminal voltage on any pin relative to $V_{SS}$	$V_T$	-0.5* <sup>1</sup> to $V_{CC}+0.3$ * <sup>2</sup>	V
Power dissipation	$P_T$	1.0	W
Operating temperature range	$T_{opr}$	0 to +70	°C
Storage temperature range	$T_{stg}$	-55 to +125	°C
Storage temperature range under bias	$T_{bias}$	-10 to +85	°C

Notes: 1.  $V_T$  min: -3.0 V for pulse half-width ≤ 50 ns  
 2. Maximum voltage is 7.0 V

**DC Operating Conditions ( $T_a = 0$  to +70°C)**

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Supply voltage	$V_{CC}$	4.5	5.0	5.5	V	
	$V_{SS}$	0	0	0	V	
Input high voltage	$V_{IH}$	2.2	—	$V_{CC} + 0.3$	V	
Input low voltage	$V_{IL}$	-0.5* <sup>1</sup>	—	0.8	V	

Note: 1.  $V_{IL}$  min: -3.0 V for pulse half-width ≤ 50 ns

## HM62256B Series

**DC Characteristics** ( $T_a = 0$  to  $+70^\circ\text{C}$ ,  $V_{CC} = 5\text{ V} \pm 10\%$ ,  $V_{SS} = 0\text{ V}$ )

Parameter	Symbol	Min	Typ* <sup>1</sup>	Max	Unit	Test conditions	
Input leakage current	$ I_{LI} $	—	—	1	$\mu\text{A}$	$V_{in} = V_{SS}$ to $V_{CC}$	
Output leakage current	$ I_{LO} $	—	—	1	$\mu\text{A}$	$\overline{CS} = V_{IH}$ or $\overline{OE} = V_{IH}$ or $\overline{WE} = V_{IL}$ , $V_{IO} = V_{SS}$ to $V_{CC}$	
Operating current	$I_{CC}$	—	6	15	mA	$\overline{CS} = V_{IL}$ , Others = $V_{IH}/V_{IL}$ , $I_{IO} = 0\text{ mA}$	
Average operating current	HM62256B-5	$I_{CC1}$	—	—	60	mA	Min cycle, duty = 100%, $I_{IO} = 0\text{ mA}$ , $\overline{CS} = V_{IL}$ , Others = $V_{IH}/V_{IL}$
	HM62256B-7	$I_{CC1}$	—	33	60	mA	
	HM62256B-8	$I_{CC1}$	—	29	50	mA	
		$I_{CC2}$	—	5	15	mA	Cycle time = 1 $\mu\text{s}$ , $I_{IO} = 0\text{ mA}$ , $\overline{CS} = V_{IL}$ , $V_{IH} = V_{CC}$ , $V_{IL} = 0$
Standby current	$I_{SB}$	—	0.3	2	mA	$\overline{CS} = V_{IH}$	
	$I_{SB1}$	—	0.2	100	$\mu\text{A}$	$V_{in} \geq 0\text{ V}$ , $\overline{CS} \geq V_{CC} - 0.2\text{ V}$	
	$I_{SB1}$	—	$0.2^{*2}$	$50^{*2}$	$\mu\text{A}$		
	$I_{SB1}$	—	$0.2^{*3}$	$10^{*3}$	$\mu\text{A}$		
Output low voltage	$V_{OL}$	—	—	0.4	V	$I_{OL} = 2.1\text{ mA}$	
Output high voltage	$V_{OH}$	2.4	—	—	V	$I_{OH} = -1.0\text{ mA}$	

Notes: 1. Typical values are at  $V_{CC} = 5.0\text{ V}$ ,  $T_a = +25^\circ\text{C}$  and not guaranteed.

2. This characteristic is guaranteed only for L-SL version.

3. This characteristic is guaranteed only for L-UL version.

**Capacitance** ( $T_a = 25^\circ\text{C}$ ,  $f = 1.0\text{ MHz}$ )

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input capacitance* <sup>1</sup>	$C_{in}$	—	—	8	pF	$V_{in} = 0\text{ V}$
Input/output capacitance* <sup>1</sup>	$C_{IO}$	—	—	10	pF	$V_{IO} = 0\text{ V}$

Note: 1. This parameter is sampled and not 100% tested.

**AC Characteristics** ( $T_a = 0$  to  $+70^\circ\text{C}$ ,  $V_{CC} = 5.0\text{ V} \pm 10\%$ )

**Test Conditions**

- Input pulse levels: 0.8 V to 2.4 V
- Input rise and fall time: 5 ns
- Input and output timing reference levels: 1.5 V
- Output load: 1 TTL Gate +  $C_L$  (50 pF) (HM62256B-5)  
 1 TTL Gate +  $C_L$  (100 pF) (HM62256B-7/8)  
 (Including scope & jig)

**Read Cycle**

Parameter	Symbol	HM62256B						Unit	Notes
		-5		-7		-8			
		Min	Max	Min	Max	Min	Max		
Read cycle time	$t_{RC}$	55	—	70	—	85	—	ns	
Address access time	$t_{AA}$	—	55	—	70	—	85	ns	
Chip select to access time	$t_{ACS}$	—	55	—	70	—	85	ns	
Output enable to output valid	$t_{OE}$	—	35	—	40	—	45	ns	
Chip select to output in low-Z	$t_{CLZ}$	5	—	10	—	10	—	ns	2
Output enable to output in low-Z	$t_{OLZ}$	5	—	5	—	5	—	ns	2
Chip deselect to output in high-Z	$t_{CHZ}$	0	20	0	25	0	30	ns	1, 2
Output disable to output in high-Z	$t_{OHZ}$	0	20	0	25	0	30	ns	1, 2
Output hold from address change	$t_{OH}$	5	—	5	—	5	—	ns	

## HM62256B Series

### Write Cycle

Parameter	Symbol	HM62256B						Unit	Notes
		-5		-7		-8			
		Min	Max	Min	Max	Min	Max		
Write cycle time	$t_{WC}$	55	—	70	—	85	—	ns	
Chip selection to end of write	$t_{CW}$	40	—	60	—	75	—	ns	5
Address setup time	$t_{AS}$	0	—	0	—	0	—	ns	6
Address valid to end of write	$t_{AW}$	40	—	60	—	75	—	ns	
Write pulse width	$t_{WP}$	35	—	50	—	55	—	ns	4, 13
Write recovery time	$t_{WR}$	0	—	0	—	0	—	ns	7
Write to output in high-Z	$t_{WHZ}$	0	20	0	25	0	30	ns	1, 2, 8
Data to write time overlap	$t_{DW}$	25	—	30	—	35	—	ns	
Data hold from write time	$t_{DH}$	0	—	0	—	0	—	ns	
Output active from end of write	$t_{OW}$	5	—	5	—	5	—	ns	2
Output disable to output in High-Z	$t_{OHZ}$	0	20	0	25	0	30	ns	1, 2, 8

Notes: 1.  $t_{CHZ}$ ,  $t_{OHZ}$  and  $t_{WHZ}$  are defined as the time at which the outputs achieve the open circuit conditions and are not referred to output voltage levels.

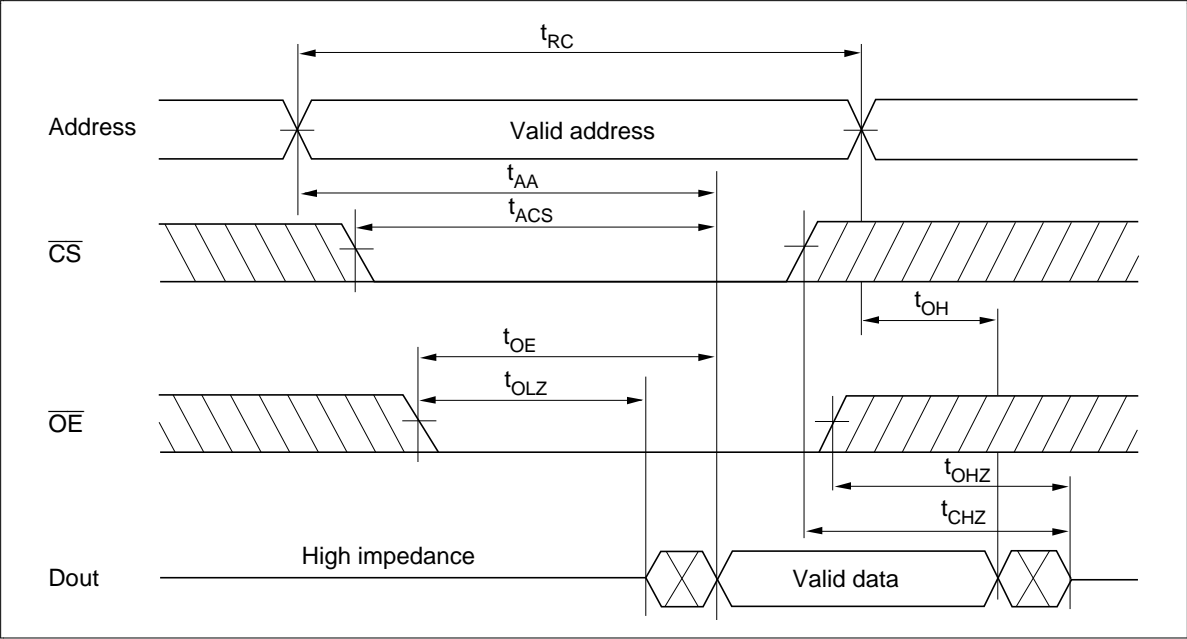
2. This parameter is sampled and not 100% tested.
3. Address must be valid prior to or simultaneously with  $\overline{CS}$  going low.
4. A write occurs during the overlap of a low  $\overline{CS}$  and a low  $\overline{WE}$ . A write begins at the latest transition of  $\overline{CS}$  going low or  $\overline{WE}$  going low. A write ends at the earliest transition of  $\overline{CS}$  going high or  $\overline{WE}$  going high.  $t_{WP}$  is measured from the beginning of write to the end of write.
5.  $t_{CW}$  is measured from  $\overline{CS}$  going low to the end of write.
6.  $t_{AS}$  is measured from the address valid to the beginning of write.
7.  $t_{WR}$  is measured from the earliest of  $\overline{CS}$  or  $\overline{WE}$  going high to the end of write cycle.
8. During this period, I/O pins are in the output state; therefore, the input signals of the opposite phase to the outputs must not be applied.
9. If  $\overline{CS}$  goes low simultaneously with  $\overline{WE}$  going low or after  $\overline{WE}$  going low, the outputs remain in the high impedance state.
10. Dout is the same phase of the latest written data in this write cycle.
11. Dout is the read data of next address.
12. If  $\overline{CS}$  is low during this period, I/O pins are in the output state. Therefore, the input signals of the opposite phase to the outputs must not be applied to them.
13. In the write cycle with  $\overline{OE}$  low fixed,  $t_{WP}$  must satisfy the following equation to avoid a problem of data bus contention.

$$t_{WP} \geq t_{DW} \text{ min} + t_{WHZ} \text{ max}$$

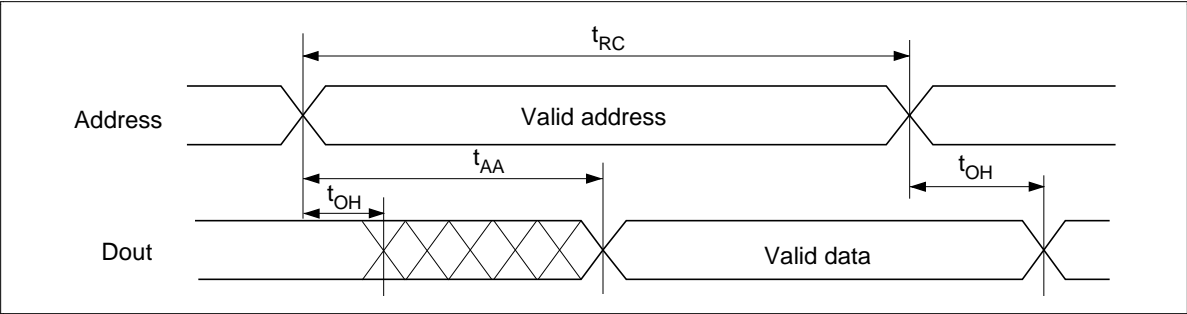


Timing Waveform

Read Timing Waveform (1) ( $\overline{WE} = V_{IH}$ )

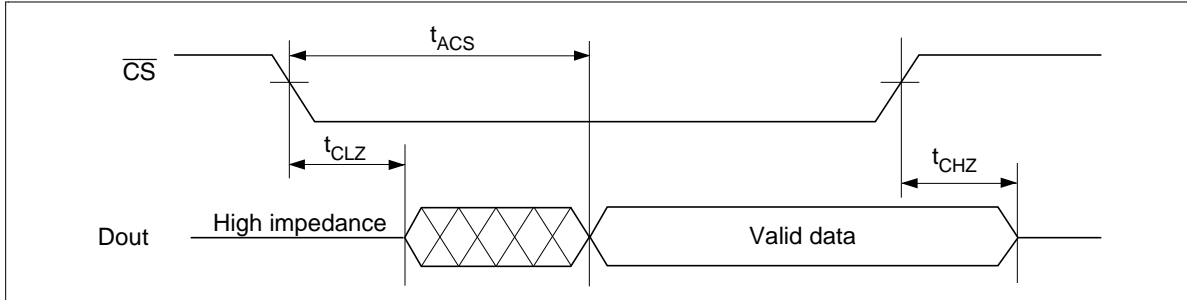


Read Timing Waveform (2) ( $\overline{WE} = V_{IH}, \overline{CS} = V_{IL}, \overline{OE} = V_{IL}$ )

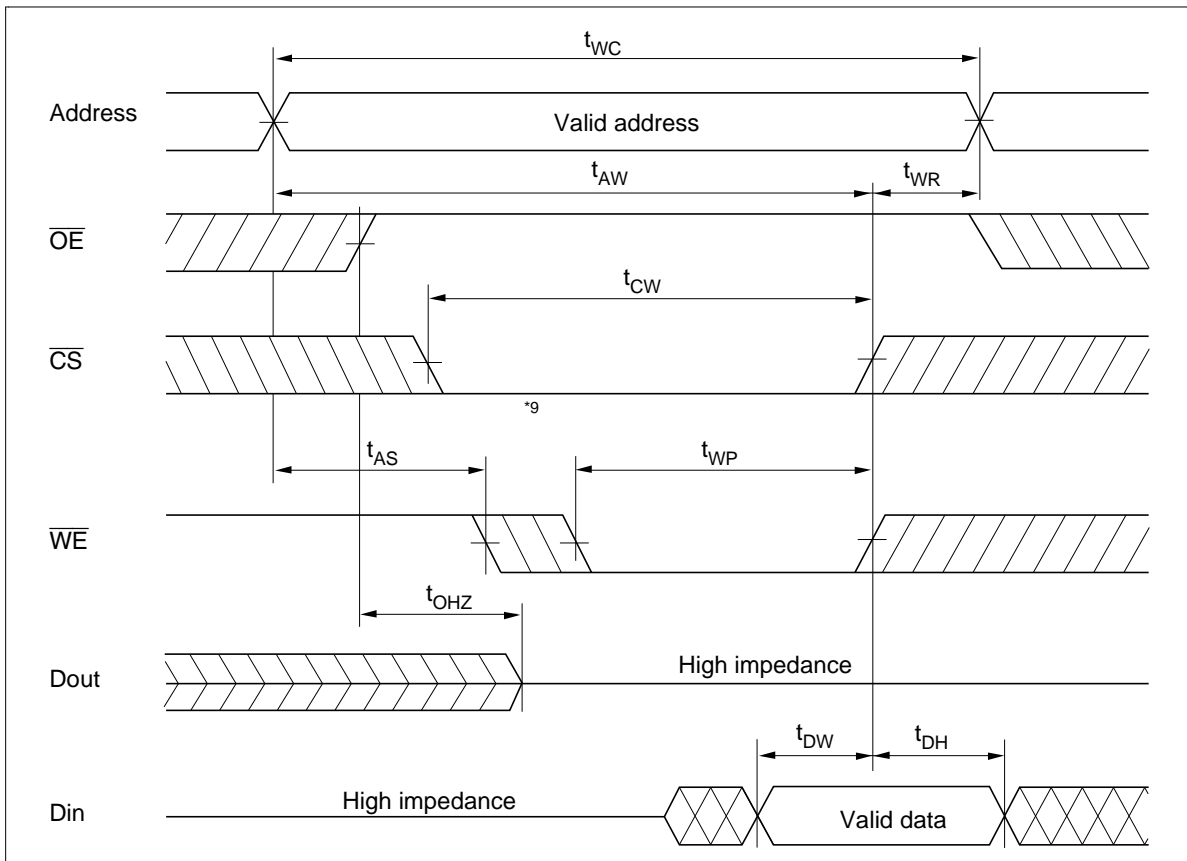


## HM62256B Series

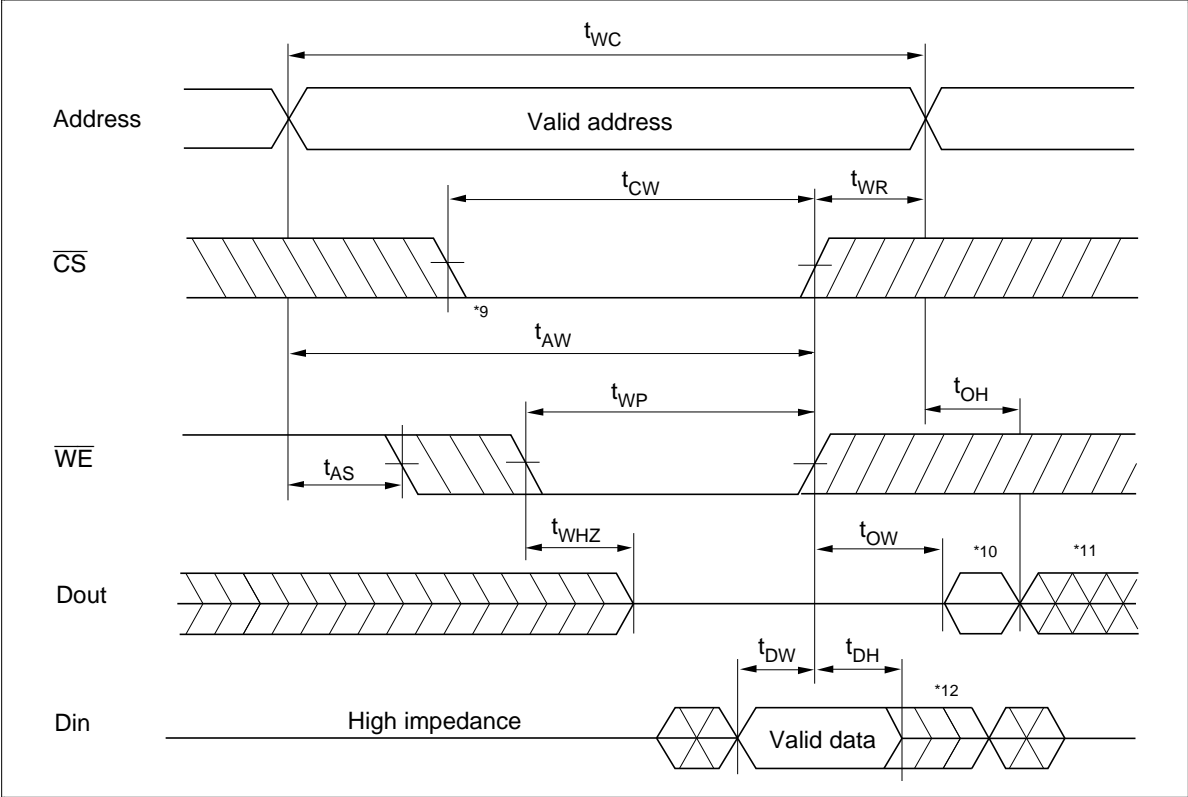
Read Timing Waveform (3) ( $\overline{WE} = V_{IH}, \overline{OE} = V_{IL}$ )\*<sup>3</sup>



Write Timing Waveform (1) ( $\overline{OE}$  Clock)



Write Timing Waveform (2) ( $\overline{OE}$  Low Fixed)



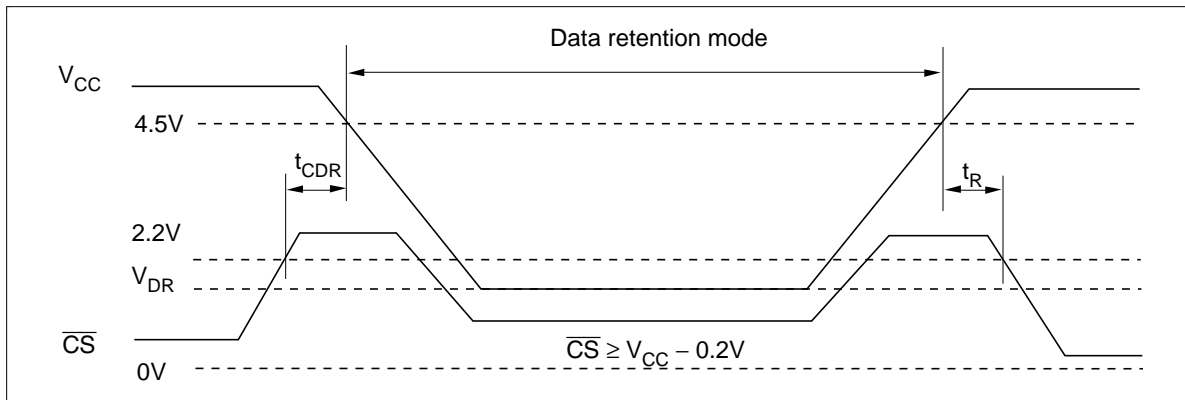
## HM62256B Series

### Low $V_{CC}$ Data Retention Characteristics ( $T_a = 0$ to $70^\circ\text{C}$ )

Parameter	Symbol	Min	Typ <sup>*1</sup>	Max	Unit	Test conditions <sup>*6</sup>
$V_{CC}$ for data retention	$V_{DR}$	2.0	—	5.5	V	$\overline{CS} \geq V_{CC} - 0.2\text{ V}$ , $V_{in} \geq 0\text{ V}$
Data retention current	$I_{CCDR}$	—	0.05	$30^{*2}$	$\mu\text{A}$	$V_{CC} = 3.0\text{ V}$ , $V_{in} \geq 0\text{ V}$ $\overline{CS} \geq V_{CC} - 0.2\text{ V}$
	$I_{CCDR}$	—	0.05	$10^{*3}$	$\mu\text{A}$	
	$I_{CCDR}$	—	0.05	$3^{*4}$	$\mu\text{A}$	
Chip deselect to data retention time	$t_{CDR}$	0	—	—	ns	See retention Waveform
Operation recovery time	$t_R$	$t_{RC}^{*5}$	—	—	ms	

- Notes: 1. Typical values are at  $V_{CC} = 3.0\text{ V}$ ,  $T_a = +25^\circ\text{C}$  and not guaranteed.  
 2.  $10\ \mu\text{A}$  max. at  $T_a = 0$  to  $+40^\circ\text{C}$ .  
 3. This characteristic is guaranteed only for L-SL version,  $3\ \mu\text{A}$  max. at  $T_a = 0$  to  $+40^\circ\text{C}$ .  
 4. This characteristic is guaranteed only for L-UL version,  $0.6\ \mu\text{A}$  max. at  $T_a = 0$  to  $+40^\circ\text{C}$ .  
 5.  $t_{RC}$  = Read cycle time.  
 6.  $\overline{CS}$  controls address buffer,  $\overline{WE}$  buffer,  $\overline{OE}$  buffer, and Din buffer. If  $\overline{CS}$  controls data retention mode,  $V_{in}$  levels (address,  $\overline{WE}$ ,  $\overline{OE}$ , I/O) can be in the high impedance state.

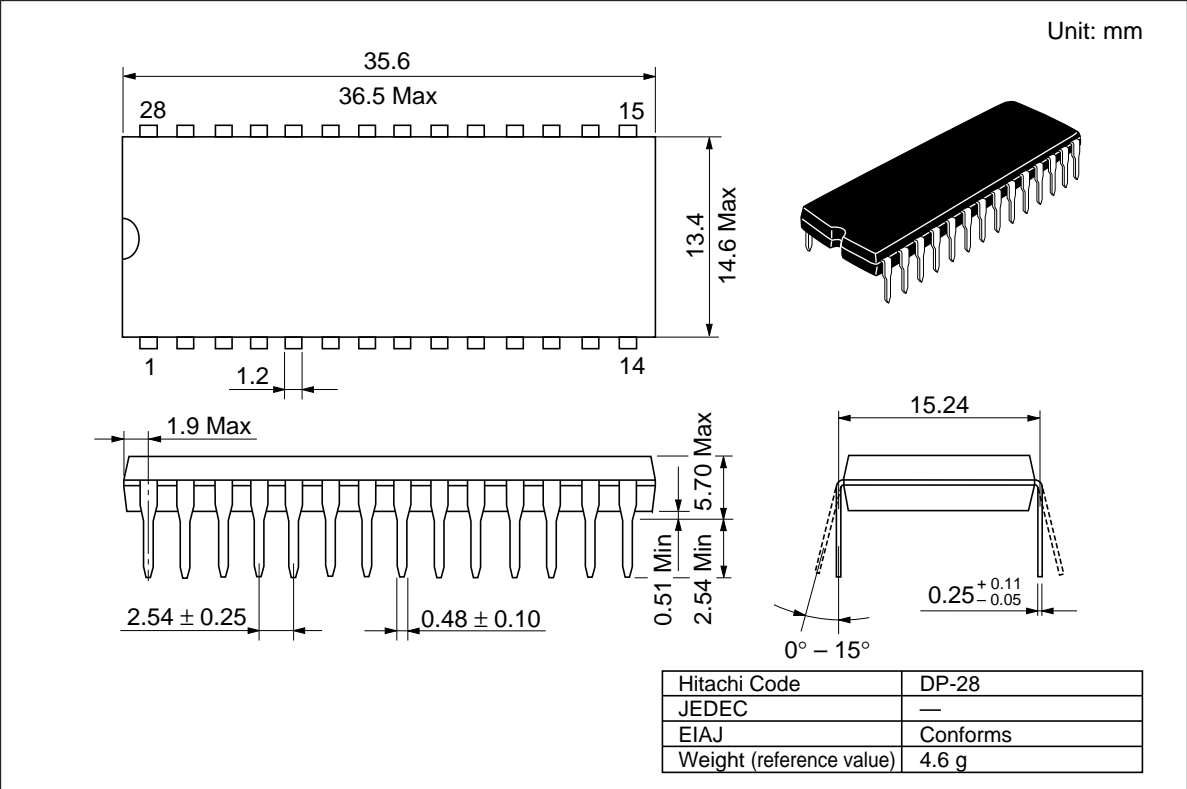
### Low $V_{CC}$ Data Retention Timing Waveform



**HM62256B Series**

**Package Dimensions**

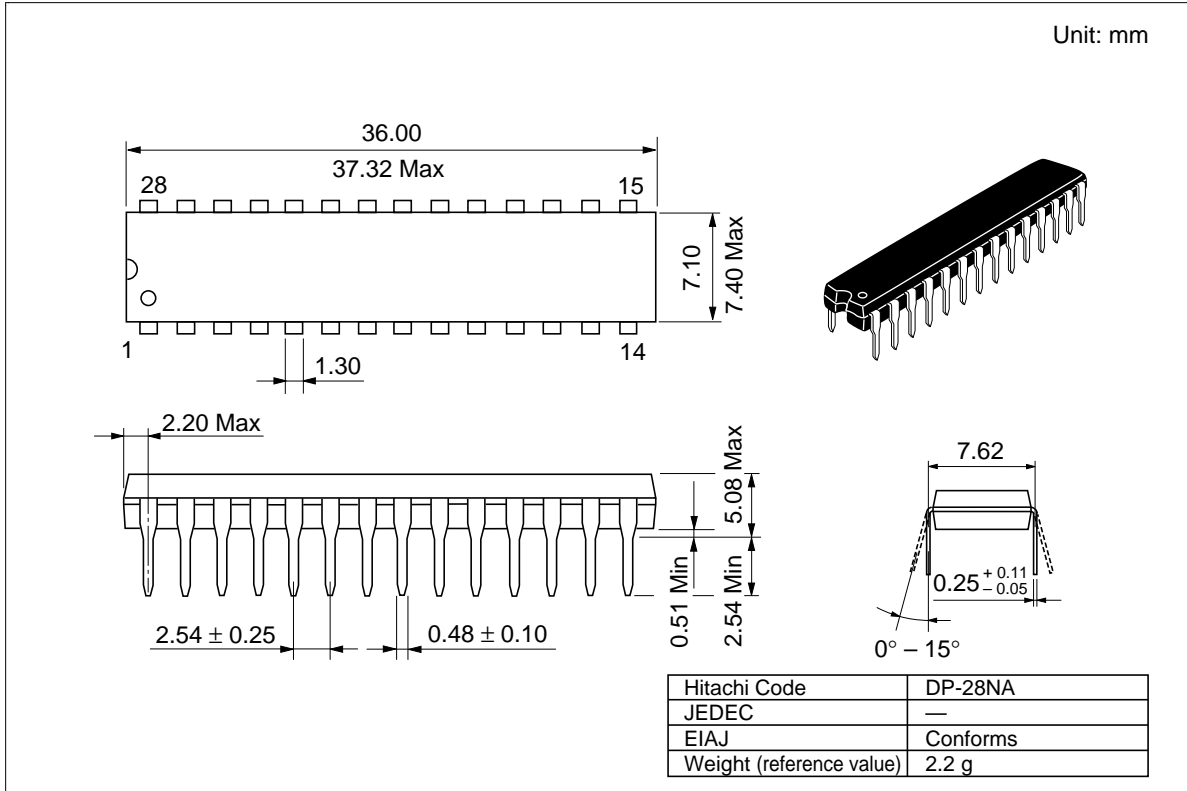
HM62256BLP Series (DP-28)



# HM62256B Series

## Package Dimensions (cont.)

### HM62256BLSP Series (DP-28NA)

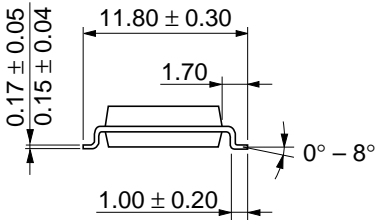
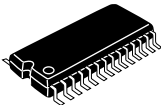
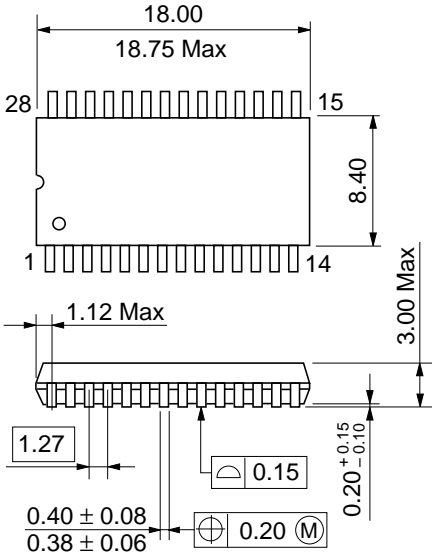


**HM62256B Series**

**Package Dimensions (cont.)**

**HM62256BLFP Series (FP-28DA)**

Unit: mm



Dimension including the plating thickness  
Base material dimension

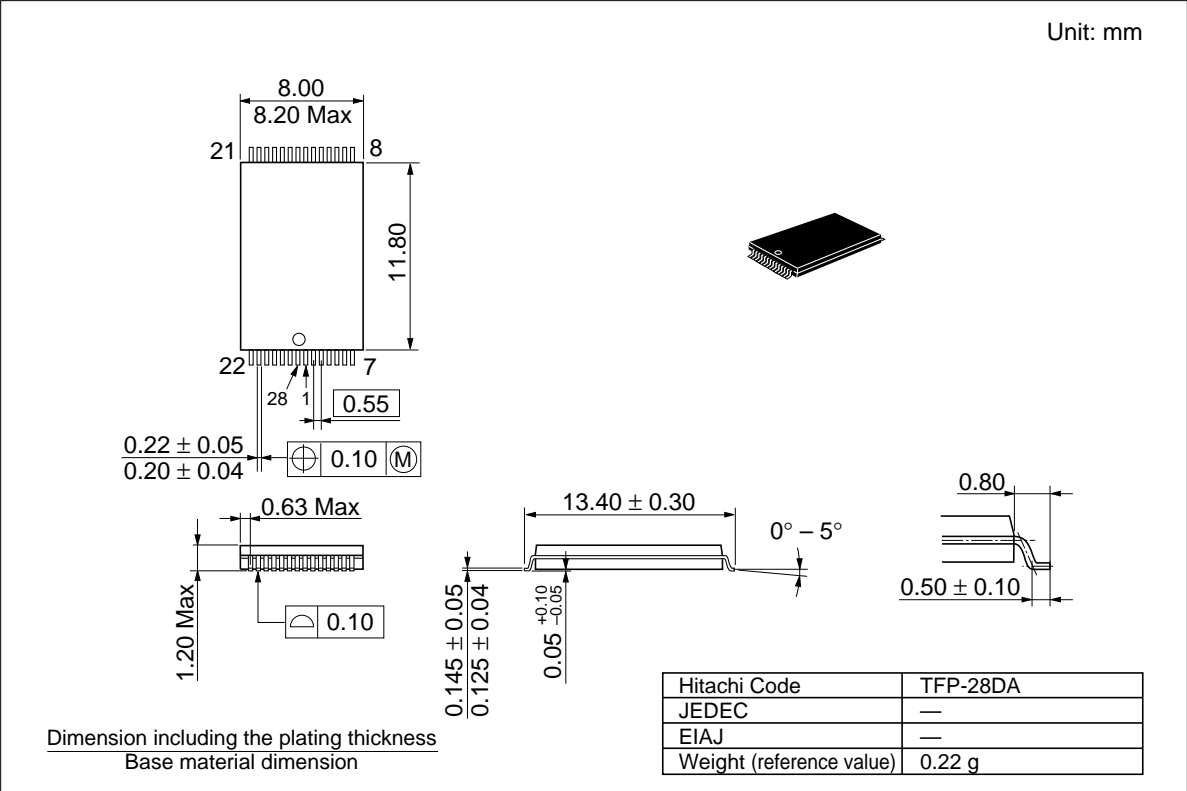
Hitachi Code	FP-28DA
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	0.82 g





Package Dimensions (cont.)

HM62256BLTM Series (TFP-28DA)



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## HM62256B Series

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**Revision Record**

Rev.	Date	Contents of Modification	Drawn by	Approved by
0.0	Sep. 10, 1993	Initial Issue	Y. Saito	K. Yoshizaki
1.0	Mar. 23, 1994	DC Characteristics I <sub>CC1</sub> Typ: —/—/—/— mA to 33/29/26/24 mA	Y. Saito	K. Yoshizaki
2.0	Oct. 31, 1994	Deletion of HM62256BLT-7/10SL/12SL Addition of HM62256BLTM-8/7SL/8SL(TFP-28DA) AC Characteristics Addition of note 12 Low V <sub>CC</sub> data retention characteristics V <sub>DR</sub> max: — to 5.5 V Note 2: 20 μA max at Ta = 0 to +40°C to 10 μA max at Ta = 0 to +40°C Deletion of description; (only for L-version)	Y. Saito	K. Yoshizaki
3.0	Jun. 19, 1995	Change of format Deletion of HM62256BLP-8/10/12/8SL/10SL/12SL Deletion of HM62256BLSP-8/10/12/8SL/10SL/12SL Deletion of HM62256BLFP-8T/10T/12T Deletion of HM62256BLFP-8SLT/10SLT/12SLT Deletion of HM62256BLT-10/12/8SL Deletion of HM62256BLTM-8SL Addition of HM62256BLFP-4SLT/5SLT/7ULT Addition of HM62256BLTM-4SLT/5SLT/7ULT Features Fast access time: 70/85/100/120 ns to 45/55/70/85 ns DC Characteristics I <sub>CC1</sub> typ: 33/29/26/24 mA to —/—/33/29 mA max: 60/50/50/45 mA to 70/60/60/50 mA I <sub>SB1</sub> typ: 0.3/0.3 μA to 0.2/0.2/0.2 μA max: 100/50 μA to 100/50/10 μA Addition of note 3 AC Characteristics Change order of notes. Test Condition Addition of HM62256B-4: 1TTL Gate + C <sub>L</sub> (100pF) (Including scope & jig) t <sub>RC</sub> min: 70/85/100/120 ns to 45/55/70/85 ns t <sub>AA</sub> max: 70/85/100/120 ns to 45/55/70/85 ns t <sub>ACS</sub> max: 70/85/100/120 ns to 45/55/70/85 ns t <sub>OE</sub> max: 40/45/50/60 ns to 30/35/40/45 ns t <sub>CLZ</sub> min: 10/10/10/10 ns to 5/5/10/10 ns t <sub>OHZ</sub> max: 25/30/35/40 ns to 20/20/25/30 ns t <sub>OH</sub> min: 5/5/10/10 ns 5/5/5/5 ns t <sub>WC</sub> min: 70/85/100/120 ns to 45/55/70/85 ns t <sub>CW</sub> min: 60/75/80/85 ns to 35/40/60/75 ns t <sub>AW</sub> min: 60/75/80/85 ns to 35/40/60/75 ns t <sub>WP</sub> min: 50/55/60/70 ns to 30/35/50/55 ns t <sub>WHZ</sub> max: 25/30/35/40 ns to 20/20/25/30 ns	M. Higuchi	K. Yoshizaki

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## HM62256B Series

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### Revision Record (cont.)

Rev.	Date	Contents of Modification	Drawn by	Approved by
3.0	Jun. 19, 1995	AC Characteristics $t_{PW}$ min: 30/35/40/50 ns to 20/25/30/35 ns $t_{OHZ}$ max: 25/30/35/40 ns to 20/20/25/30 ns Low $V_{CC}$ Data Retention Characteristics Addition of note 4. $t_{CCDR}$ typ: 0.2/0.2 $\mu$ A to 0.05/0.05/0.05 $\mu$ A max: 30/10 $\mu$ A to 30/10/3 $\mu$ A	M. Higuchi	K. Yoshizaki
4.0	Nov. 29, 1995	Ordering Information (HM62256BLFP-4 Series) Addition of note (Under development) AC Characteristics Test Conditions HM62256-5/7/8:1TTL Gate + $C_L$ (100pF) to HM62256-5:1TTL Gate + $C_L$ (50pF) and HM62256-7/8:1TTL Gate + $C_L$ (100pF)	M. Higuchi	K. Yoshizaki
5.0	Jul. 9, 1997	Change of format Deletion of HM62256B-4 Series	M. Higuchi	K. Imato
6.0	Nov. 13, 1997	Operation Table Correct Error DC Operating Conditions Correct Error DC Characteristics Correct Error		

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