Reset Circuit with Manual Reset and Watchdog

Description

The EM6323/24 are low power, high precision reset ICs featuring a manual reset and a watchdog inputs. They have different threshold voltages and several timeout reset periods (t_{POR}) and watchdog timeout periods (t_{WD}) for maximum flexibility in the application. EM6323 has a manual reset ($\overline{MR}$ with internal pull-up) and a watchdog input pins. EM6324 has only a watchdog input pin (WDI). The watchdog function can be disabled by driving WDI with a three-state driver or by leaving WDI unconnected. This is useful when the MCU is in sleep mode.
Small SOT23-5L package as well as ultra-low supply current of 3.8µA make the EM6323 and the EM6324 an ideal choice for portable and battery-operated devices.

Features

- Ultra-low supply current of 3.8µA (V_{DD}=3.3V)
- Operating temperature range: -40°C to +125°C
- ±1.5% reset threshold accuracy
- 11 reset threshold voltages V_{TH}: 4.63V, 4.4V, 3.08V, 2.93V, 2.63V, 2.2V, 1.8V, 1.66V, 1.57V, 1.38V, 1.31V
- 200ms reset timeout period (1.6ms, 25ms, 1600ms on request)
- 1.6s watchdog timeout period (6.2ms, 102ms, 25.6s on request)
- 3 reset output options:
  - Active-low $\overline{RESET}$ push-pull
  - Active-low $\overline{RESET}$ open-drain
  - Active-high RESET push-pull
- Detection of microcontroller in sleep mode

Typical Application

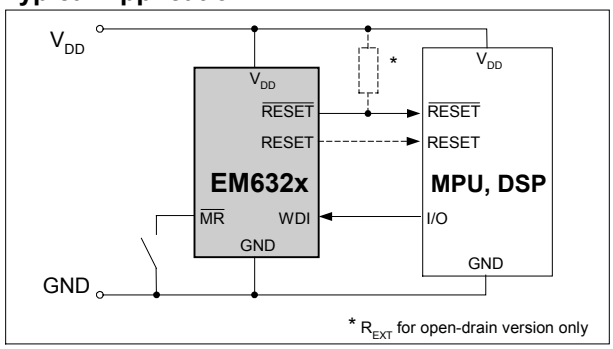


Fig. 1

Applications

- Workstations
- Point of sales (POS)
- Personal computers
- Routers, hubs and switches
- Handheld GPS
- Vending machines and ATM

Block Diagram

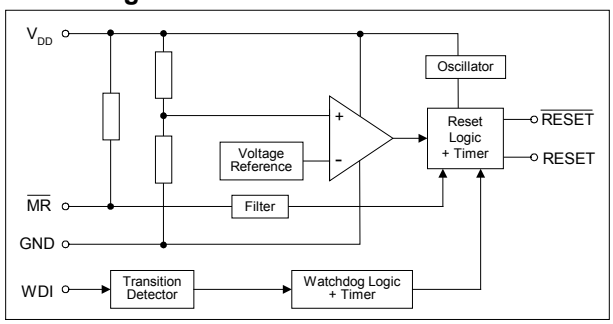


Fig. 2

Pin Configuration

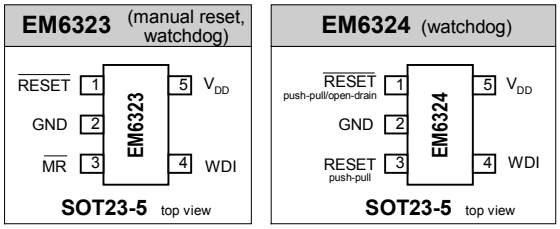


Fig. 3

Pin Description

SOT23-5L		Name	Function
EM6323	EM6324		
1	1	$\overline{RESET}$	Active-low $\overline{RESET}$ output (push-pull or open-drain)
2	2	GND	Ground
3	-	$\overline{MR}$	Manual Reset input with an internal pull-up 30kΩ resistor. Reset remains active as long as $\overline{MR}$ is low and for t_{POR} after returns high. $\overline{MR}$ can be driven with a CMOS output or shorted to ground with a switch
-	3	RESET	Active-high RESET output (push-pull)
4	4	WDI	Watchdog input. WDI must be driven with a CMOS output. If the microcontroller I/O is put in a high impedance condition, the circuit will detect this condition as a microcontroller in sleep mode and prevent its watchdog from timing out
5	5	V_{DD}	Supply Voltage (5.5V max.)

Ordering Information

EM6323 L X SP5B - 2.9

Part Number:
EM6323 = manual reset & watchdog
EM6324 = watchdog

Delays t_{POR} & t_{WD} :

EM6323/24:

t_{WD} [ms] \ t_{POR} [ms]	1.6	25	200	1600
6.2	A	B	C	D
102	E	F	G	H
1600	J	K	L	M
25600	N	P	Q	R

("L" is the standard version)

Reset Threshold Voltage:

1.3 = 1.31V	**1.8** = 1.80V	**3.1** = 3.08V
1.4 = 1.38V	**2.2** = 2.20V	**4.4** = 4.40V
1.6 = 1.57V	**2.6** = 2.63V	**4.6** = 4.63V
1.7 = 1.66V	**2.9** = 2.93V	

Package: *in* ***Tape & Reel, 3000 units***
SP5B = 5-pin SOT23-5

Reset Output Type:
X = Active-low /RESET push-pull
(Active-high RESET push-pull also for EM6324)
Y = Active-low /RESET open-drain
(Active-high RESET push-pull also for EM6324)
Z = Active-high RESET push-pull *(EM6323 only)*

Standard Versions

The versions below are considered standard and should be readily available. For other versions, please contact EM Microelectronic for availability (minimum order quantity can apply). Please make sure to give the complete Part Number when ordering. All parts are offered in tape-and-reel only (3000 units).

Threshold Voltage	Delay (t_{POR})/ Watchdog timer (t_{WD})	Output Type	Package	Part Number	Top Marking
2.63V	200ms/1600ms	Active-low push-pull $\overline{\text{RESET}}$	SOT23-5L	**EM6323**LXSP5B-2.6	APLG
2.93V	200ms/1600ms	Active-low push-pull $\overline{\text{RESET}}$	SOT23-5L	**EM6323**LXSP5B-2.9	APLH
2.93V	200ms/1600ms	Active-low open-drain $\overline{\text{RESET}}$	SOT23-5L	**EM6323**LYSP5B-2.9	APLU
3.08V	200ms/1600ms	Active-low push-pull $\overline{\text{RESET}}$	SOT23-5L	**EM6323**LXSP5B-3.1	APLJ
4.40V	200ms/1600ms	Active-low push-pull $\overline{\text{RESET}}$ Active-high push-pull RESET	SOT23-5L	**EM6324**LXSP5B-4.4	AQLK

Absolute Maximum Ratings

Parameter	Symbol	Conditions
Voltage at V_{DD} to GND	V_{DD}	-0.3V to +6V
Minimum voltage at any signal pin	V_{MIN}	GND - 0.3V
Maximum voltage at any signal pin	V_{MAX}	V_{DD} + 0.3V
Electrostatic discharge maximum to MIL-STD-883C method 3015	V_{ESD}	2000V
Max. soldering conditions	T_{MAX}	250°C x 10s
Storage Temperature Range	T_{STG}	-65°C to +150°C

Stresses above these listed maximum ratings may cause permanent damages to the device. Exposure beyond specified operating conditions may affect device reliability or cause malfunction.

Handling Procedures

This device has built-in protection against high static voltages or electric fields; however, anti-static precautions must be taken as for any other CMOS component. Unless otherwise specified, proper operation can only occur when all terminal voltages are kept within the voltage range. Unused inputs must always be tied to a defined logic voltage level.

Operating Conditions

Parameter	Symbol	Min	Max	Unit
Supply voltage	V_{DD}	0.9	5.5	V
Operating Temperature	T_A	-40	+125	°C
Input transition rise and fall rate on $\overline{MR}$ and WDI	t_R/t_F	-	100	ns/V

Electrical Characteristics

Unless otherwise specified: V_{DD}= 0.9V to 5.5V, T_A=-40°C to +125°C (note 1).

Parameter	Symbol	Conditions		Min	Typ	Max	Unit
Supply current (note 2)	I_{DD}	V_{DD}=1.5V	+25°C	-	2.4	4.4	µA
			-40°C to +125°C	-		6.8	
		V_{DD}=3.3V	+25°C	-	3.86	6.1	
			-40°C to +125°C	-		9.9	
		V_{DD}=5.0V	+25°C	-	5.89	8.6	
			-40°C to +125°C	-		11.6	
Threshold voltage (note 3)	V_{TH}	EM6323/24 – 1.31	+25°C	1.290	1.31	1.330	V
			-40°C to +85°C	1.245		1.382	
			-40°C to +125°C	1.221		1.387	
		EM6323/24 – 1.38	+25°C	1.359	1.38	1.401	
			-40°C to +85°C	1.311		1.456	
			-40°C to +125°C	1.286		1.461	
		EM6323/24 – 1.57	+25°C	1.546	1.57	1.594	
			-40°C to +85°C	1.492		1.656	
			-40°C to +125°C	1.463		1.663	
		EM6323/24 – 1.66	+25°C	1.635	1.66	1.685	
			-40°C to +85°C	1.577		1.751	
			-40°C to +125°C	1.547		1.758	
		EM6323/24 – 1.80	+25°C	1.773	1.80	1.827	
			-40°C to +85°C	1.710		1.899	
			-40°C to +125°C	1.678		1.906	
		EM6323/24 – 2.20	+25°C	2.167	2.20	2.233	
			-40°C to +85°C	2.090		2.321	
			-40°C to +125°C	2.050		2.330	
		EM6323/24 – 2.63	+25°C	2.591	2.63	2.669	
			-40°C to +85°C	2.499		2.775	
			-40°C to +125°C	2.451		2.785	
		EM6323/24 – 2.93	+25°C	2.886	2.93	2.974	
			-40°C to +85°C	2.784		3.091	
			-40°C to +125°C	2.731		3.103	
		EM6323/24 – 3.08	+25°C	3.034	3.08	3.126	
			-40°C to +85°C	2.926		3.249	
			-40°C to +125°C	2.871		3.262	
		EM6323/24 – 4.40	+25°C	4.334	4.40	4.466	
			-40°C to +85°C	4.180		4.642	
			-40°C to +125°C	4.101		4.660	
		EM6323/24 – 4.63	+25°C	4.561	4.63	4.699	
			-40°C to +85°C	4.399		4.885	
			-40°C to +125°C	4.315		4.903	

Note 1: Production tested at +25°C only. Over temperature limits are guaranteed by design, not production tested.
Note 3: Threshold voltage is specified for V_{DD} falling.

Electrical Characteristics (continued)

Unless otherwise specified: V_{DD}= 0.9V to 5.5V, T_A=-40°C to +125° C (note 1).

Parameter	Symbol	Conditions		Min	Typ	Max	Unit
Threshold hysteresis	V_{HYS}	T_A=+25°C		-	2.1%•V_{TH}	-	V
Reset timeout period	t_{POR}	V_{DD} from 0V to $V_{TH\ (typ)}$+15% T_A= +25°C (note 2 and 4)	EM6323/24 C-G-L-Q	160	200	240	ms
			EM6323/24 A-E-J-N	0.7	1.56	3.8	
			EM6323/24 B-F-K-P	20	25	30	
			EM6323/24 D-H-M-R	1280	1600	1920	
Propagation delay time V_{DD} to $\overline{\text{RESET}}$ (RESET) delay	t_P	V_{DD} drops from $V_{TH\ (typ)}$+0.2V to $V_{TH\ (typ)}$-0.2V (note 2). T_A= +25°C		2	70	255	µs
Open-drain $\overline{\text{RESET}}$ output Voltage	V_{OL}	V_{DD}>1V	I_{OL}=100µA	-	-	0.3	V
		V_{DD}>2.5V	I_{OL}=1.5mA	-	-	0.3	
		V_{DD}>5V	I_{OL}=3mA	-	-	0.35	
Push-pull RESET / $\overline{\text{RESET}}$ Output voltage	V_{OL}	V_{DD}>1V	I_{OL}=100µA	-	-	0.3	V
		V_{DD}>2.5V	I_{OL}=1.5mA	-	-	0.3	
		V_{DD}>5V	I_{OL}=3mA	-	-	0.35	
	V_{OH}	V_{DD}>1.1V	I_{OH}=-30µA	0.8	-	-	
		V_{DD}>2.5V	I_{OH}=-1.5mA	2	-	-	
		V_{DD}>5V	I_{OH}=-3mA	4	-	-	
Output leakage current	I_{LEAK}	Only for EM6323/24_Y (open-drain)		-	-	0.5	µA
WATCHDOG INPUT (WDI)							
WDI Input low	V_{WDI} low	T_A= +25°C		-	-	0.3•V_{DD}	V
WDI Input high	V_{WDI} high			0.7•V_{DD}	-	-	V
Pulse width at WDI	t_{WP}			1	-	-	µs
Watchdog timeout period	t_{WD}	(note 6)	EM6323/24 J-K-L-M	1280	1600	1920	ms
			EM6323/24 A-B-C-D	5	6.25	7.5	
			EM6323/24 E-F-G-H	80	100	120	
			EM6323/24 N-P-Q-R	20480	25600	30720	
High-level Input Current	I_{IH}	WDI connected to VDD, T_A= +25°C		-	18	-	µA
Low-level Input Current	I_{IL}	WDI connected to GND, T_A= +25°C		-	8.3	-	µA
MANUAL RESET ($\overline{\text{MR}}$) – *EM6323 only*							
$\overline{\text{MR}}$ Input low	V_{MRT} low	T_A= +25°C		-	-	0.3•V_{DD}	V
$\overline{\text{MR}}$ Input high	V_{MRT} high			0.7•V_{DD}	-	-	V
$\overline{\text{MR}}$ to Reset delay	t_{MD}			-	0.3	-	µs
Pulse width at $\overline{\text{MR}}$ (note 5)	t_{PMD}			1	-	-	µs
$\overline{\text{MR}}$ Internal Pull-up resistor	R_{MR}	T_A=-40°C to +125°C		7	30	74	kΩ

Note 1: Production tested at +25°C only. Over temperature limits are guaranteed by design, not production tested.

Note 2: WDI, $\overline{\text{MR}}$ and $\overline{\text{RESET}}$ (RESET) open.

Note 3: Threshold voltage is specified for V_{DD} falling.

Note 4: Standard version for t_{POR} is 200ms (typ). Other option (1.6ms, 25ms, 1600ms) are available by mask option and upon minimum order quantity. Please contact EM sales.

Note 5: Pulse width must be greater than 1µs to ensure the $\overline{\text{RESET}}$ (RESET) to go active.

Note 6: Standard version for t_{WD} is 1600ms (typ). Other option (6.2ms, 102ms, 25.6s) are available by mask option and upon minimum order quantity. Please contact EM sales.

Timing Waveforms

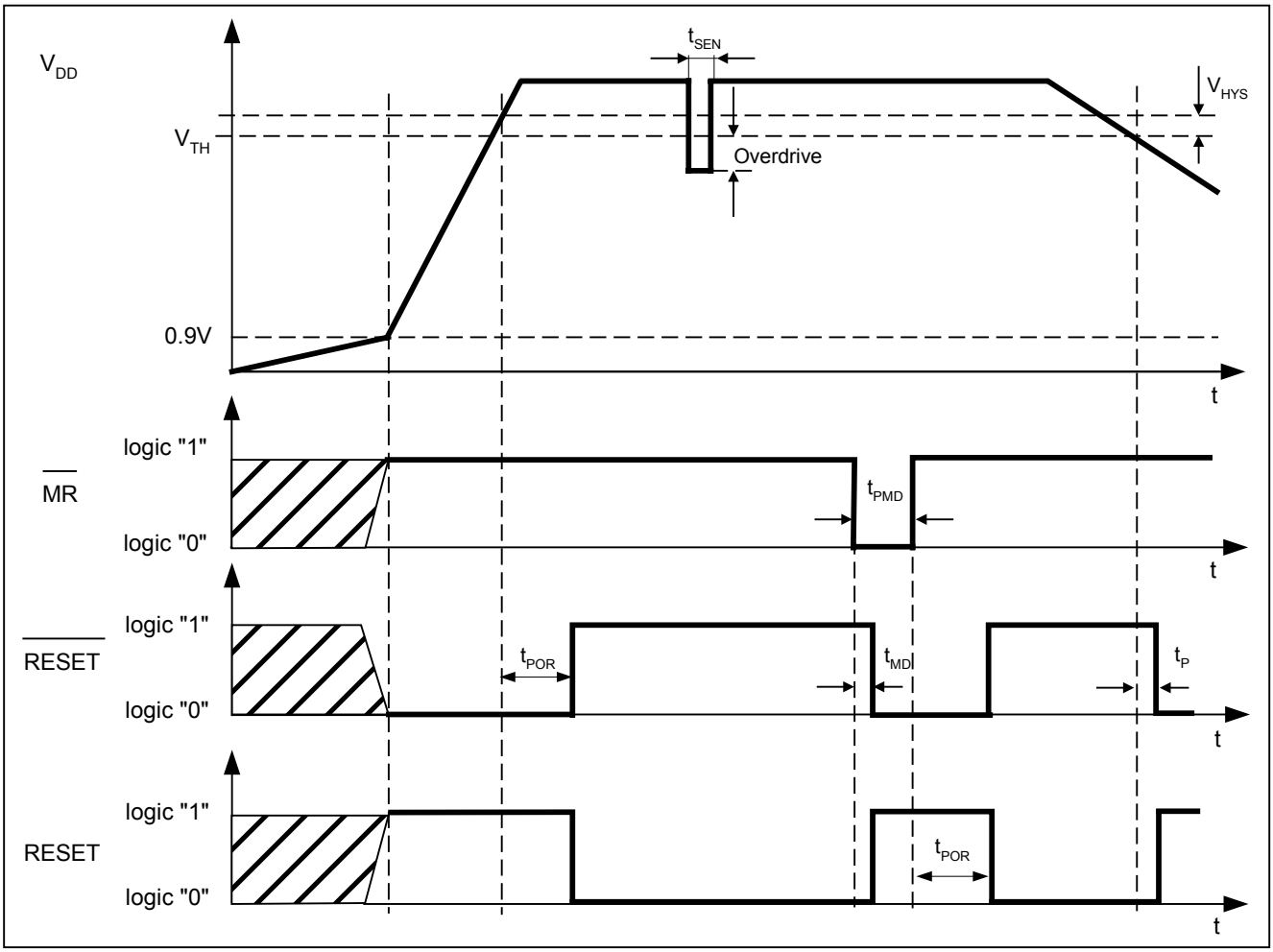


Fig. 4

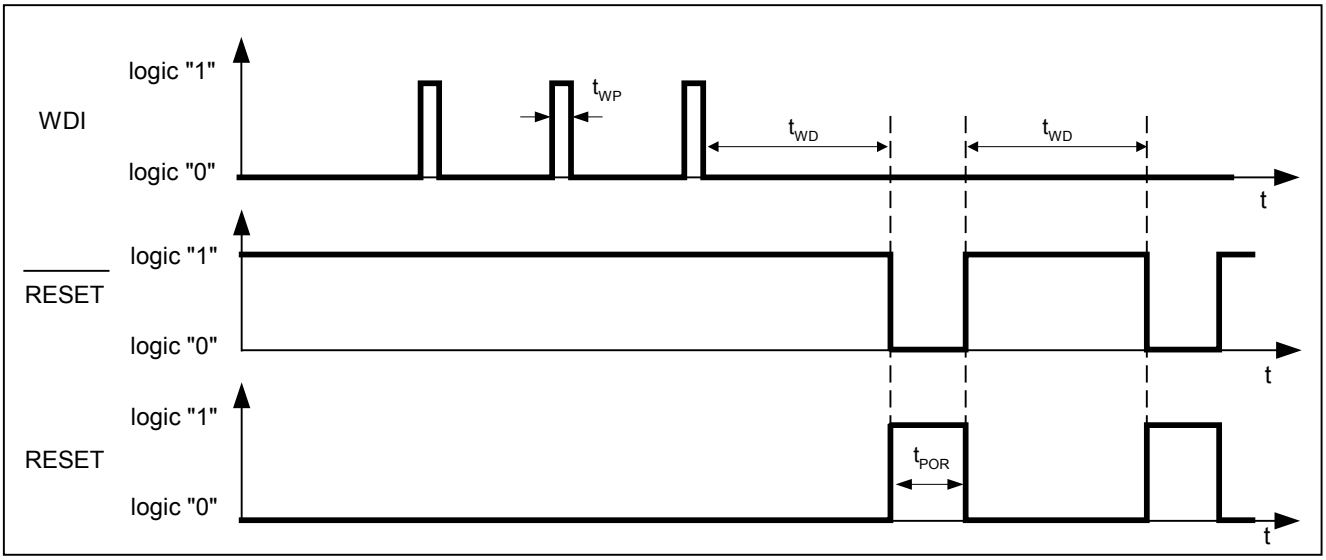


Fig. 5

Note 7: t_{SEN} = Maximum Transient Duration. Please refer to figure on the next page.
Note 8: Overdrive = V_{TH} -V_{DD}. Please refer to figure on the next page.

Typical Operating Characteristics

(Typical values are at T_A=+25°C unless otherwise noted. WDI, $\overline{MR}$, $\overline{RESET}$ and RESET open.)

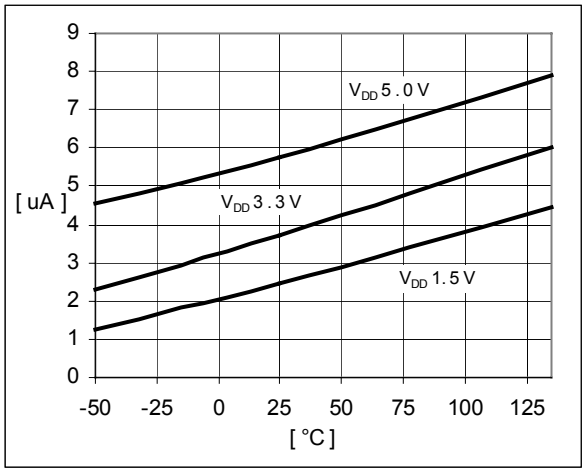


Fig. 6

I_{DD} vs. Temperature

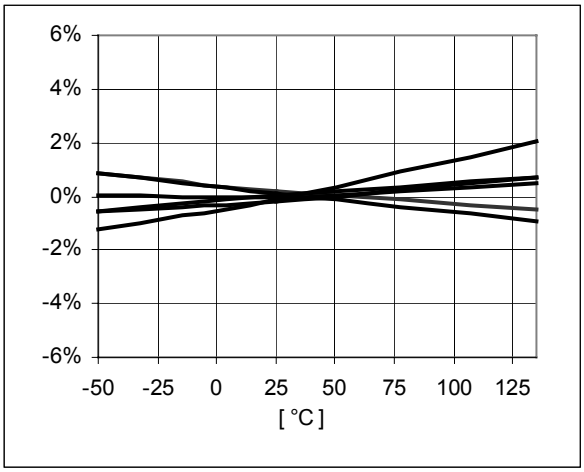


Fig. 7

Threshold Voltage Variation vs. Temperature (normalized)

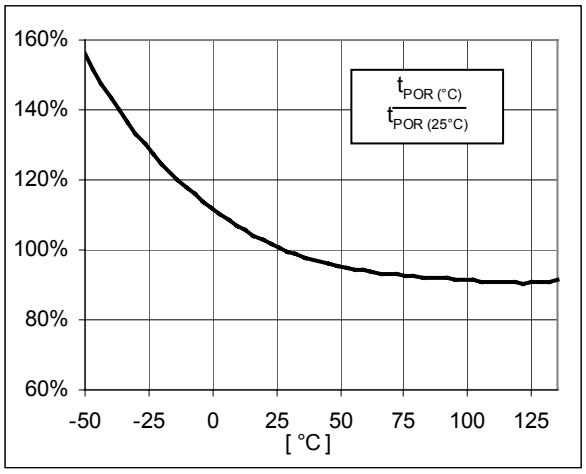


Fig. 8

Reset Timeout Period t_{POR} vs. Temperature (normalized with respect to $t_{POR\ 25°C}$)

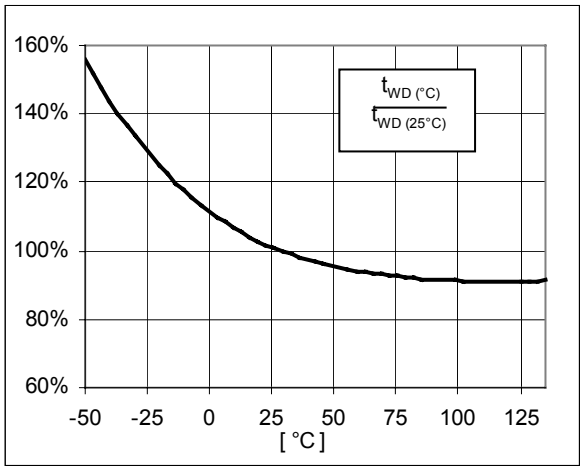


Fig. 9

Watchdog Timeout Period t_{WD} vs. Temperature (normalized with respect to $t_{WD\ 25°C}$)

Typical Operating Characteristics

(Typical values are at T_A=+25°C unless otherwise noted. WDI, $\overline{MR}$, $\overline{RESET}$ and RESET open.)

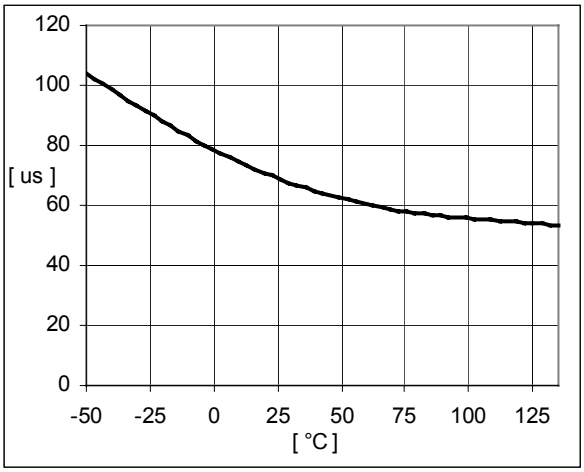


Fig. 10

Propagation Time t_{PHL} vs. Temperature

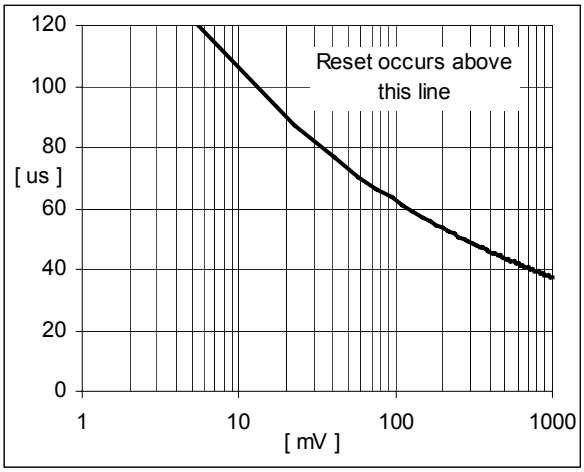


Fig. 11

Maximum Transient Duration t_{SEN} vs. Overdrive V_{TH}-V_D

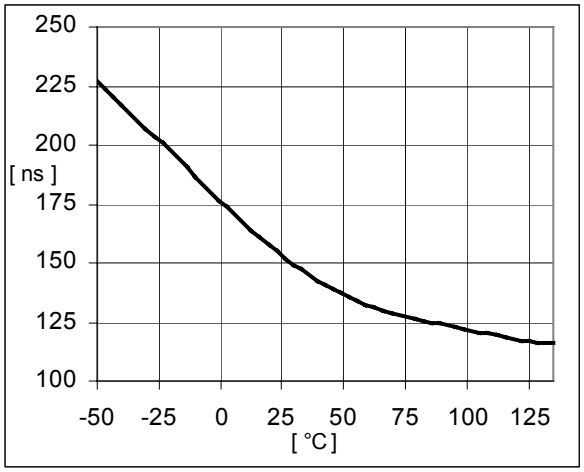


Fig. 12

Watchdog Input Pulse Width t_{WP} vs. Temperature

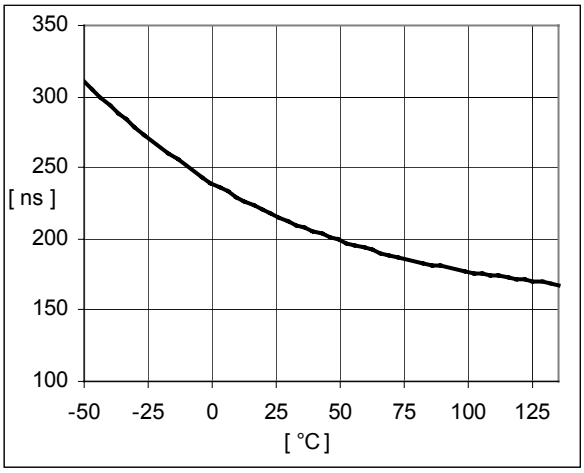


Fig. 13

Manual Reset Pulse Width t_{PMD} vs. Temperature

Functional Description

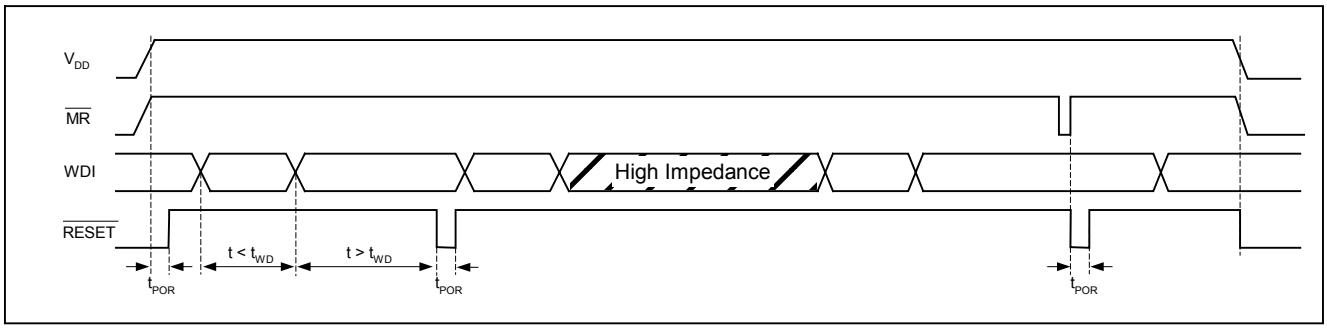


Fig. 14

Reset Outputs

A microprocessor (µP) reset input starts the µP in a known state. The EM6323/24 µP supervisory circuits assert a reset to prevent code-execution errors during power-up, power-down, and brownout conditions. $\overline{RESET}$ is guaranteed to be a logic low for V_{DD} down to 0.9V. Once V_{DD} exceeds the reset threshold, an internal timer keeps $\overline{RESET}$ low for the specified reset timeout period (t_{POR}); after this interval, $\overline{RESET}$ returns high.
If a brownout condition occurs (V_{DD} dips below the reset threshold), $\overline{RESET}$ goes low. Each time $\overline{RESET}$ is asserted it stays low for the reset timeout period. Any time V_{DD} goes below the reset threshold the internal timer restarts. $\overline{RESET}$ is the inverse of RESET.

Manual Reset Input (EM6323 only)

A logic low on $\overline{MR}$ asserts a reset. Reset remains asserted while $\overline{MR}$ is low, and for t_{POR} (200ms nominal for EM6323 C-G-L-Q) after it returns high. $\overline{MR}$ has an internal 30kΩ pull-up resistor, so it can be left open if unused. This input can be driven with CMOS logic levels or with open-drain outputs. Connect a normally open momentary switch from $\overline{MR}$ to V_{SS} to create a manual-reset function; debounce circuitry is integrated. If $\overline{MR}$ is driven from long cable or the device is used in a noisy environment, connect a 0.1µF capacitor from $\overline{MR}$ to V_{SS} to provide additional noise immunity (stronger external additional pull-up resistor can also be added).

Watchdog Input

If the watchdog timer has not been cleared within t_{WD} (1.6s typ.), reset asserts. The internal 1.6s timer is cleared by either a reset pulse or by toggling WDI. While reset is asserted, the timer remains cleared and does not count. As soon as reset is released, the timer starts counting.
If the microcontroller I/O connected to WDI is put in a high impedance condition, the circuit will detect this condition as a microcontroller in sleep mode and prevent its watchdog from timing out. To monitor a high impedance or a three state condition on WDI, the watchdog input is internally driven low during the first 15/16 of the watchdog timeout period and high for the last 1/16 of the watchdog timeout period.

When WDI is left unconnected, this internal driver clears the 1.6s timer every 1.5s. When WDI is three-stated or unconnected, the maximum allowable leakage current is 0.5µA.
To minimized the overall system power consumption and therefore for a minimum watchdog input current leave WDI low for the majority of the watchdog timeout period, pulsing it low-high-low once within the first 15/16 of the watchdog timeout period to reset the watchdog timer. If WDI is externally driven high for the majority of the timeout period, up to 35µA can flow into WDI. Meanwhile when the microcontroller is not in sleep mode, the output of the microcontroller which drives WDI has to be strong enough to fight the 35µA.

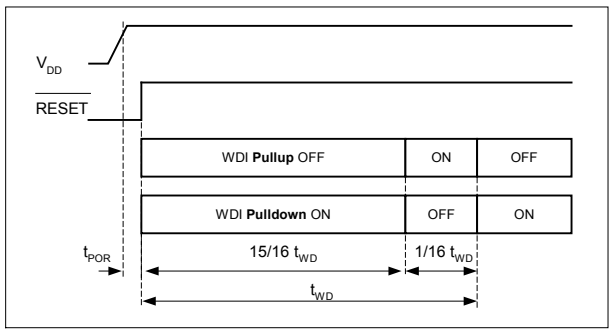


Fig. 15
WDI Input Timing Diagram

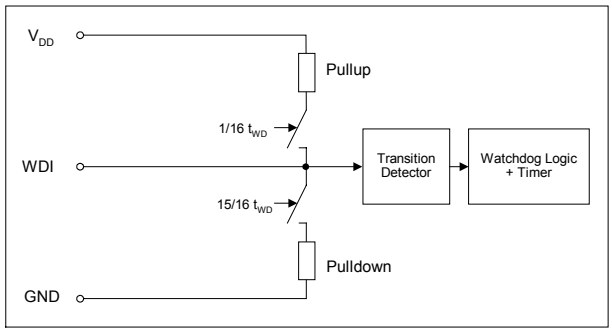


Fig. 16
WDI Input Stage Block Schematic

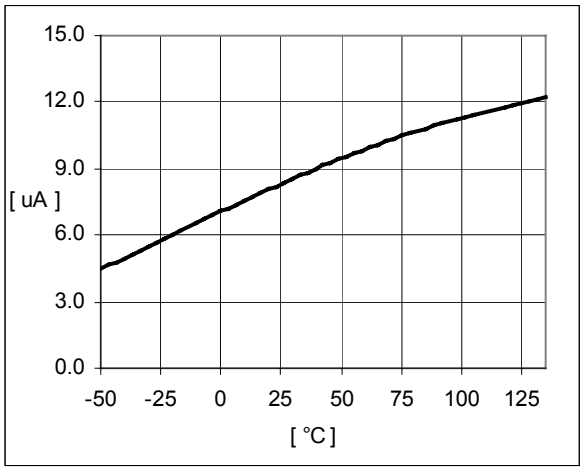


Fig. 17
WDI Input Current Low-level I_{IL} vs. Temperature (V_{DD}=5.5V)

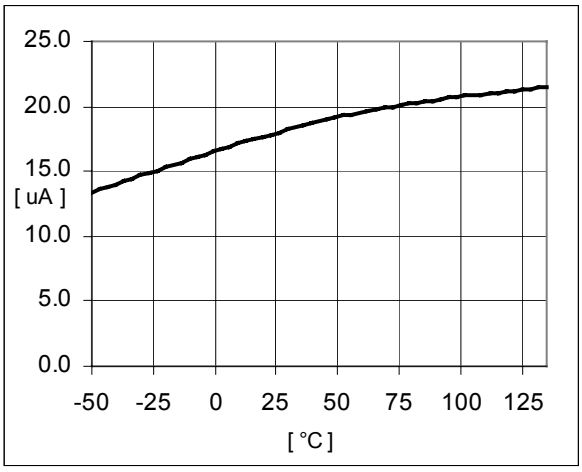
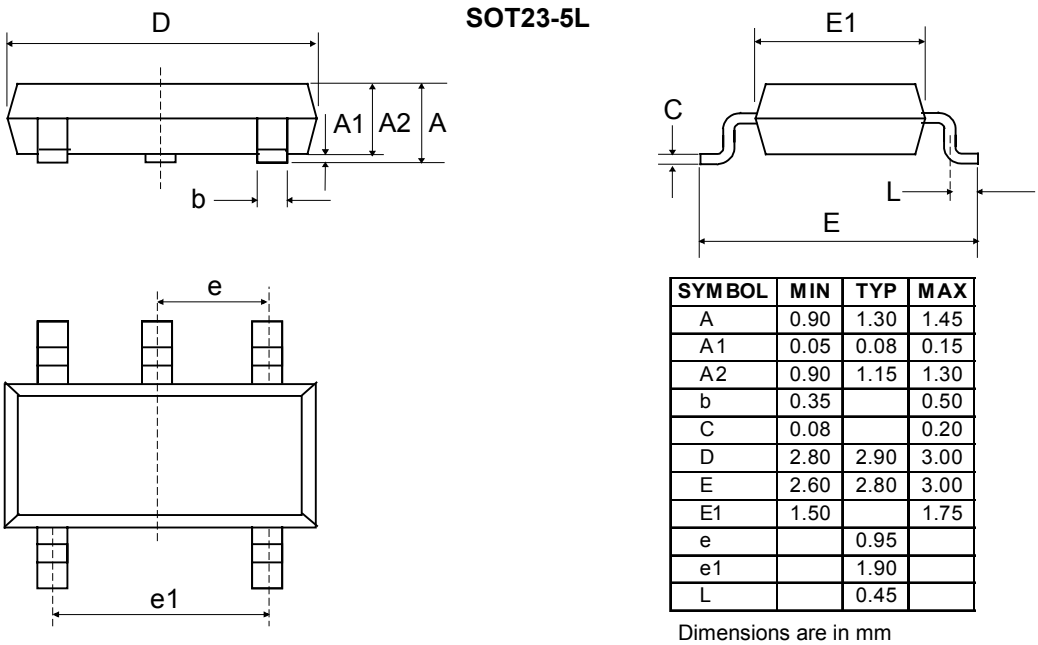


Fig. 18
WDI Input Current High-Level I_{IH} vs. Temperature (V_{DD}=5.5V)

Package Information



SYMBOL	MIN	TYP	MAX
A	0.90	1.30	1.45
A1	0.05	0.08	0.15
A2	0.90	1.15	1.30
b	0.35		0.50
C	0.08		0.20
D	2.80	2.90	3.00
E	2.60	2.80	3.00
E1	1.50		1.75
e		0.95	
e1		1.90	
L		0.45	

Dimensions are in mm

Fig. 19

Traceability for small packages

Due to the limited space on the package surface, the bottom marking contains a limited number of characters that provide only partial information for lot traceability. Full information for complete traceability is however provided on the packing labels of the product at delivery from EM. It is highly recommended that the customer insures full lot traceability of EM product in his final product.