dsPIC30F Enhanced FLASH 16-bit Digital Signal Controllers Sensor and General Purpose Families Product Brief

High Performance Modified RISC CPU:

- Modified Harvard architecture
- C compiler optimized instruction set architecture
- 89 base instructions
- 24-bit wide instructions, 16-bit wide data path
- Linear program memory addressing up to 4M Instruction Words
- Linear data memory addressing up to 64 Kbytes
- Up to 144 Kbytes on-chip FLASH program space
  - Up to 48K Instruction Words
- Up to 8 Kbytes of on-chip data RAM
- Up to 4 Kbytes of non-volatile data EEPROM
- 16 x 16-bit working register array
- Three Address Generation Units that enable:
  - Dual data fetch
  - Accumulator write back for DSP operations
- Flexible Addressing modes supporting:
  - Indirect, Modulo and Bit-Reversed modes
- Two 40-bit wide accumulators with optional saturation logic
- 16-bit x 16-bit single cycle hardware fractional/ integer multiplier
- Single cycle Multiply-Accumulate (MAC) operation
- 40-stage Barrel Shifter
- Up to 30 MIPS operation:
  - DC to 40 MHz external clock input
  - 4 MHz - 10 MHz oscillator input with PLL active (4x, 8x, 16x)
- Up to 45 interrupt sources
  - 8 programmable priority levels
- Vector table with up to 62 vectors
  - 54 interrupt vectors
  - 8 processor exceptions and software traps

Peripheral Features:

- High current sink/source I/O pins: 25 mA/25 mA
- Up to 5 external interrupt sources
- Timer module with programmable prescaler:
  - Up to five 16-bit timers/counters; optionally pair up 16-bit timers into 32-bit timer modules
- 16-bit Capture Input functions
- 16-bit Compare/PWM Output functions
  - Dual Compare mode available
- Data Converter Interface (DCI), supports common audio CODEC protocols, including I^2S and AC'97
- 3-wire SPI™ modules (supports 4 Frame modes)

Peripheral Features (Cont.):

- I^2C™ module supports Multi-Master/Slave mode and 7-bit/10-bit addressing
- Addressable UART modules supporting:
  - Interrupt-on-address bit
  - Wake-up on START bit
  - Four characters deep TX and RX FIFO buffers
- CAN bus modules

Analog Features:

- 12-bit A/D Converter, ±1 LS bit accuracy:
  - 100 Ksps conversion rate
  - Up to 16 input channels
  - Conversion available during SLEEP, IDLE
- Programmable Low Voltage Detection (PLVD)
- Programmable Brown-out Detection and RESET generation

Special Microcontroller Features:

- Enhanced FLASH program memory
  - 100,000 erase/write cycle (typical)
  - Operating temp: Industrial temperature range
- Data EEPROM memory
  - 1,000,000 erase/write cycle (typical)
  - Operating temp: Industrial temperature range
  - Data EEPROM Retention > 20 years
- Self-reprogrammable under software control
- Power-on Reset (POR), Power-up Timer (PWRT) and Oscillator Start-up Timer (OST)
- Flexible Watchdog Timer (WDT) with on-chip Low Power RC Oscillator (512 kHz)
- Fail safe clock monitor operation
  - Detects clock failure and switches to on-chip fast RC 8 MHz oscillator
- Programmable code protection
- In-Circuit Serial Programming™ (ICSP™) via 3 pins and power/ground
- Selectable Power Management modes
  - SLEEP and IDLE modes

CMOS Technology:

- Low power, high speed FLASH technology
- Wide operating voltage range (2.5V to 5.5V)
- Industrial and Extended temperature ranges
- Low Power consumption

TABLE 1: dsPIC30F SENSOR PROCESSOR FAMILY VARIANTS

Device	Pins	Program Memory		SRAM Bytes	EEPROM Bytes	Timer 16-bit	Input Cap	Output Comp/Std PWM	A/D 12-bit 100 Ksps	UART	SPI™	I^2C™
		Bytes	Instructions									
dsPIC30F2011	18	12K	4K	1024	0	3	2	2	8 ch	1	1	1
dsPIC30F3012	18	24K	8K	2048	1024	3	2	2	8 ch	1	1	1
dsPIC30F2012	28	12K	4K	1024	0	3	2	2	10 ch	1	1	1
dsPIC30F3013	28	24K	8K	2048	1024	3	2	2	10 ch	2	1	1

TABLE 2: dsPIC30F GENERAL PURPOSE CONTROLLER FAMILY VARIANTS

Device	Pins	Program Memory		SRAM Bytes	EEPROM Bytes	Timer 16-bit	Input Cap	Output Comp/ Std PWM	CODEC Interface	A/D 12-bit 100 Ksps	UART	SPI™	I^2C™	CAN
		Bytes	Instructions											
dsPIC30F3014*	40/44	24K	8K	2048	1024	3	2	2	-	13 ch	2	1	1	-
dsPIC30F4013*	40/44	48K	16K	2048	1024	5	4	4	AC97, I^2S	13 ch	2	1	1	1
dsPIC30F4014*	64	36K	12K	2048	1024	5	8	8	AC97, I^2S	16 ch	2	2	1	1
dsPIC30F5011	64	66K	22K	4096	1024	5	8	8	-	16 ch	2	2	1	2
dsPIC30F5012	64	96K	32K	4096	2048	5	8	8	AC97, I^2S	16 ch	2	2	1	2
dsPIC30F6011	64	132K	44K	6144	2048	5	8	8	-	16 ch	2	2	1	2
dsPIC30F6012	64	144K	48K	8192	4096	5	8	8	AC97, I^2S	16 ch	2	2	1	2
dsPIC30F4015*	80	36K	12K	2048	1024	5	8	8	AC97, I^2S	16 ch	2	2	1	1
dsPIC30F5013	80	66K	22K	4096	1024	5	8	8	-	16 ch	2	2	1	2
dsPIC30F5014	80	96K	32K	4096	2048	5	8	8	AC97, I^2S	16 ch	2	2	1	2
dsPIC30F6013	80	132K	44K	6144	2048	5	8	8	-	16 ch	2	2	1	2
dsPIC30F6014	80	144K	48K	8192	4096	5	8	8	AC97, I^2S	16 ch	2	2	1	2

*Proposed products (others are committed).

FIGURE 1: PART NUMBER STRUCTURE

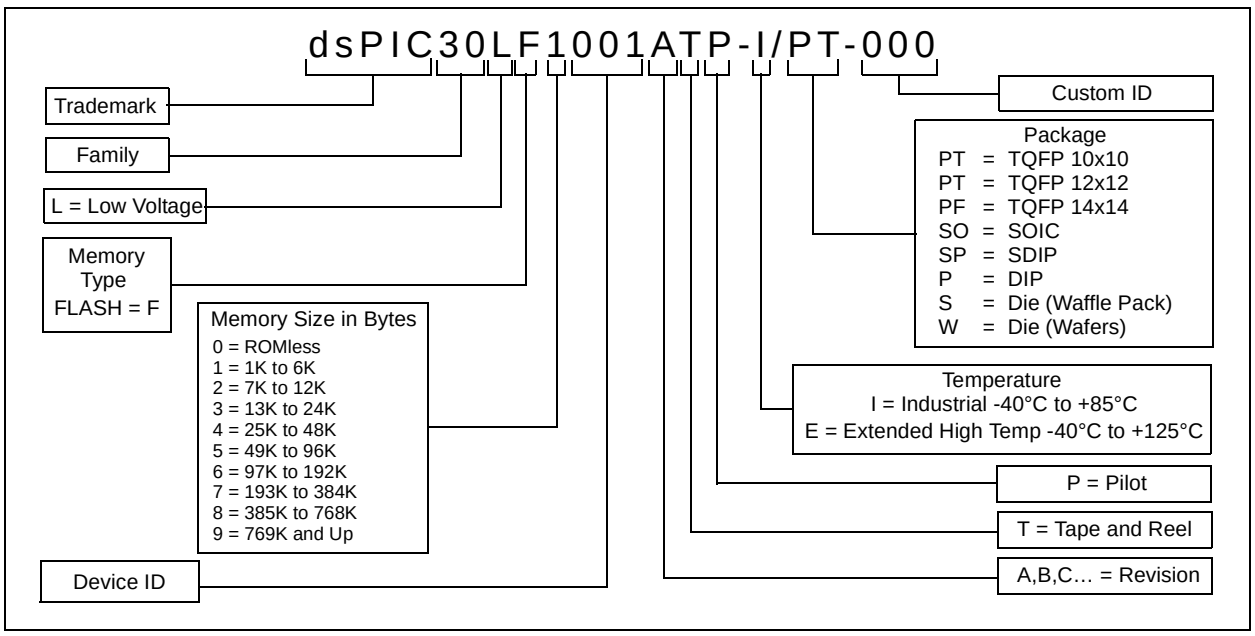
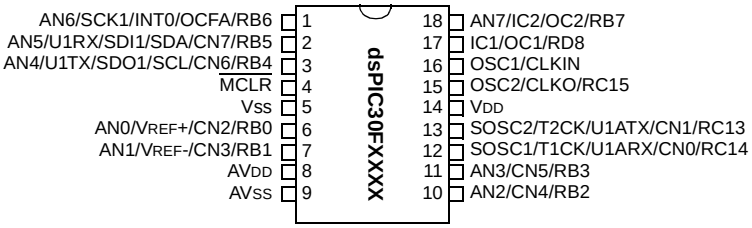


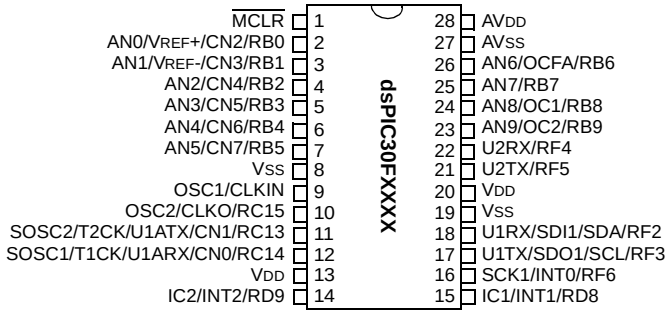
FIGURE 2: PIN DIAGRAMS

18-Pin SOIC and PDIP **Part No.: 30F2011 / 30F3012**



Note: Pinout subject to change.

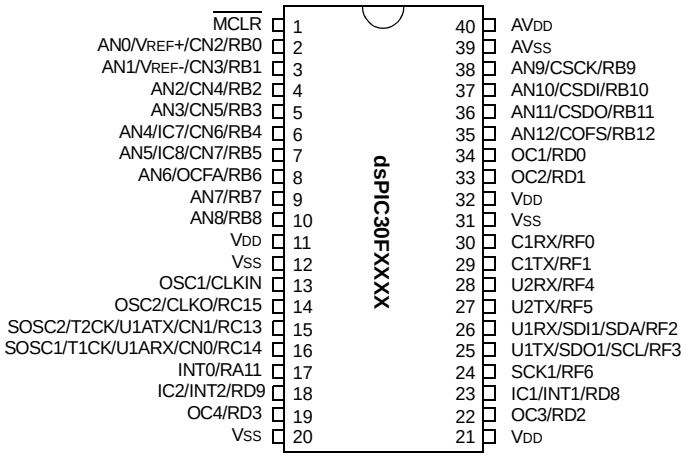
28-Pin SDIP **Part No.: 30F2012 / 30F3013**



Note: Pinout subject to change.

FIGURE 3: PIN DIAGRAMS (CONT.)

40-Pin PDIP **Part No.: 30F3014 / 30F4013**

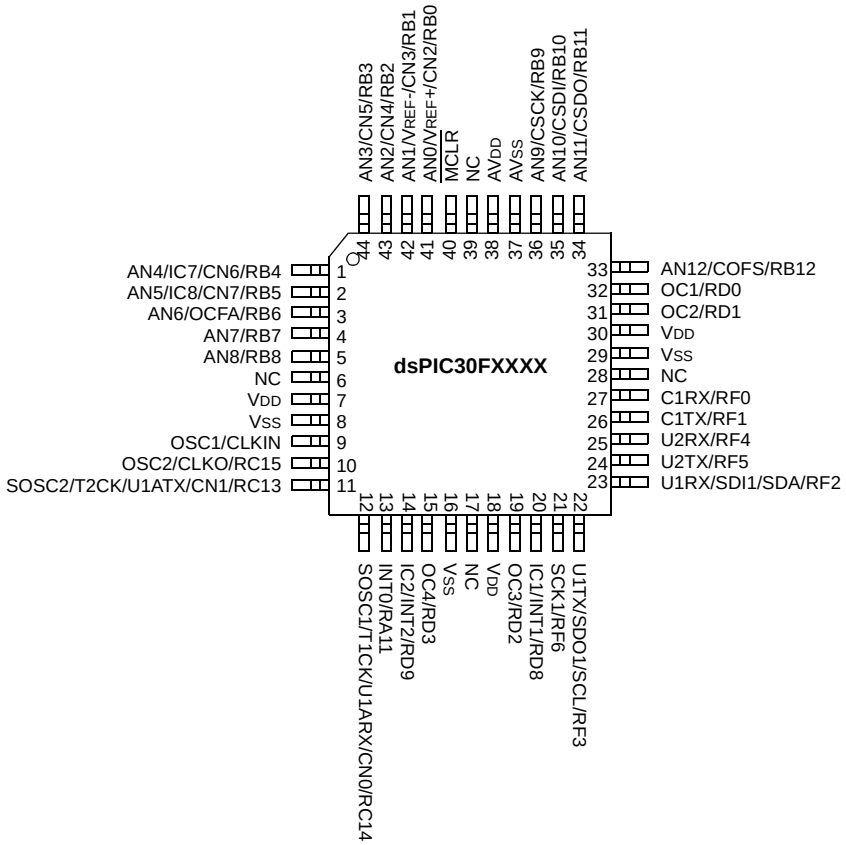


Note: Pinout subject to change.

FIGURE 4: PIN DIAGRAMS (CONT.)

44-Pin TQFP

Part No.: 30F3014 / 30F4013

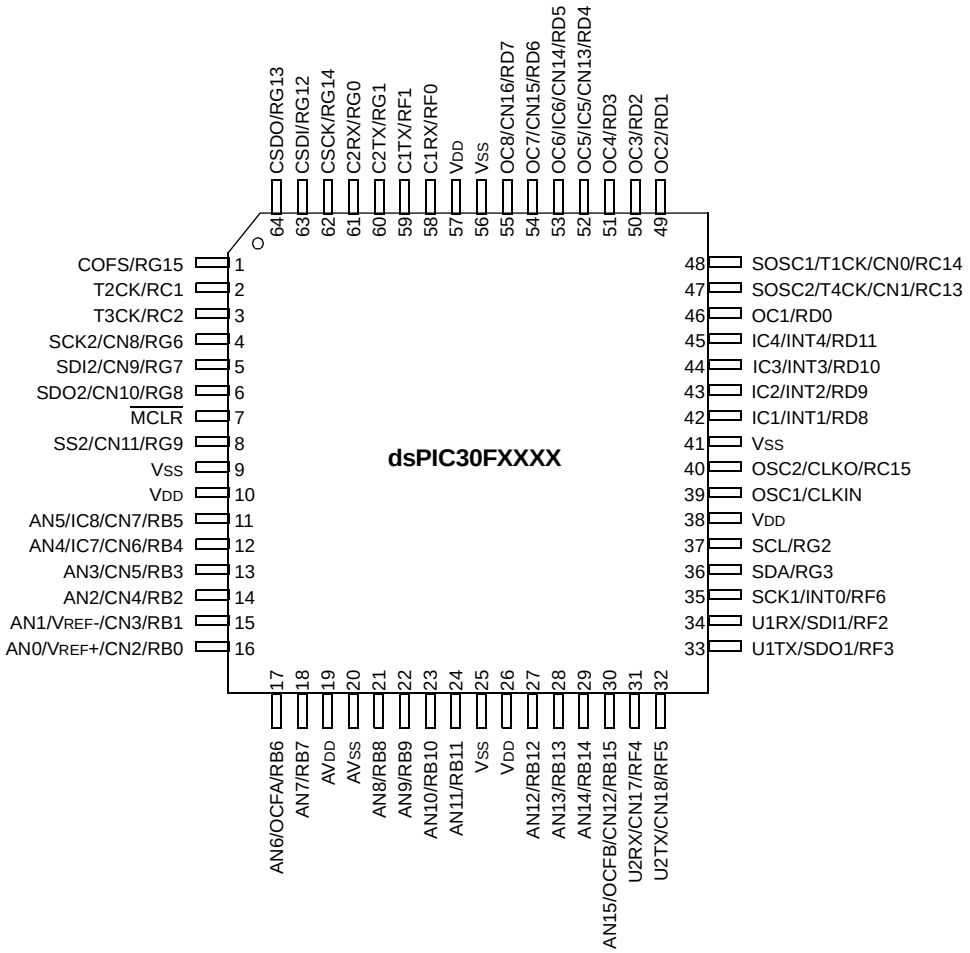


Note: Pinout subject to change.

FIGURE 5: PIN DIAGRAMS (CONT.)

64-Pin TQFP

Part No.: 30F4014 / 30F5011 / 30F5012 / 30F6011 / 30F6012

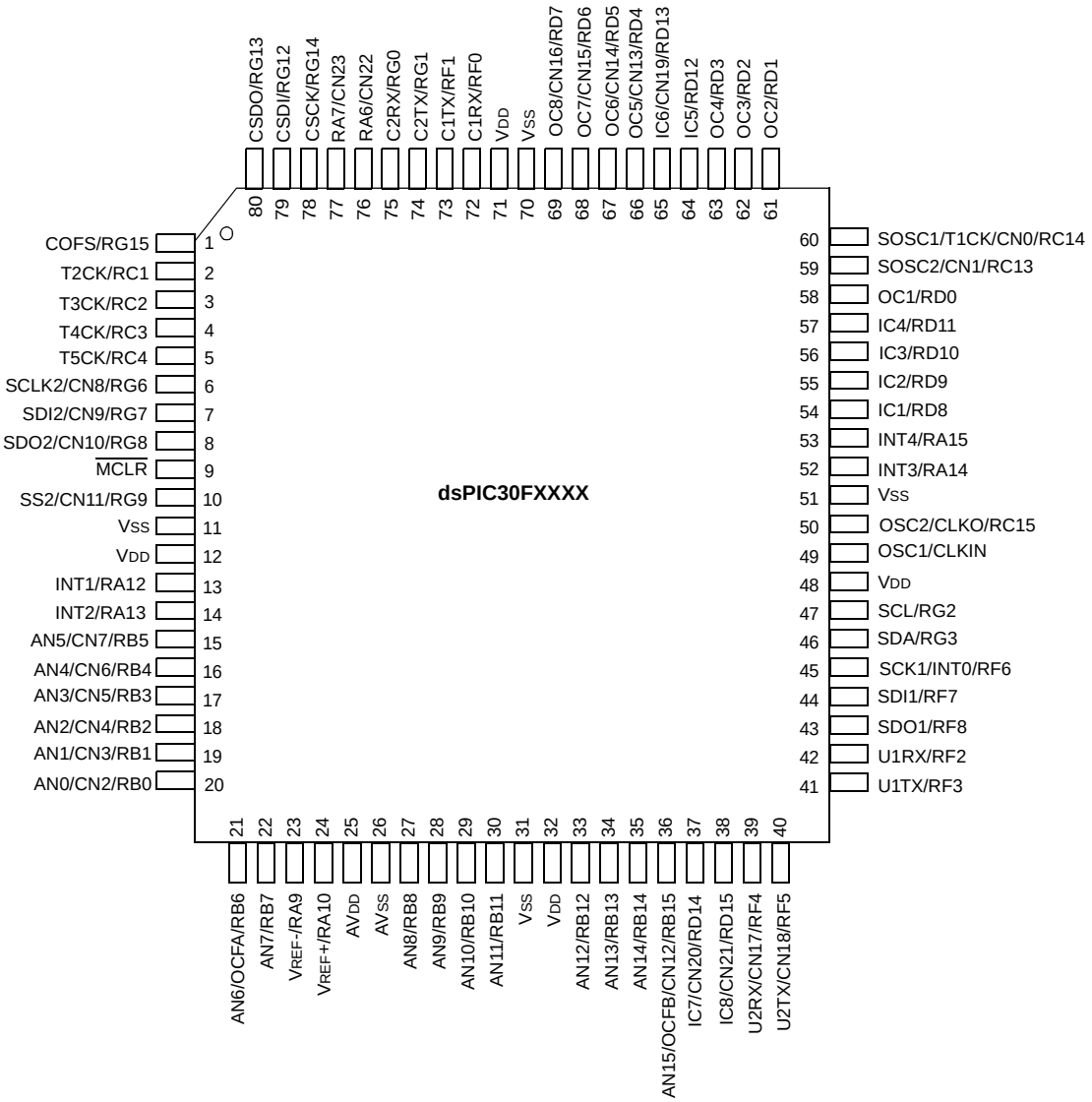


Note: Pinout subject to change.

FIGURE 6: PIN DIAGRAMS (CONT.)

80-Pin TQFP

Part No.: 30F4015 / 30F5013 / 30F5014 / 30F6013 / 30F6014



Note: Pinout subject to change.

NOTES:

Note the following details of the code protection feature on PICmicro® MCUs.

- The PICmicro family meets the specifications contained in the Microchip Data Sheet.
- Microchip believes that its family of PICmicro microcontrollers is one of the most secure products of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the PICmicro microcontroller in a manner outside the operating specifications contained in the data sheet. The person doing so may be engaged in theft of intellectual property.
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