

SANYO

No.2674A

DM2021

20 Characters × 2 Lines

Liquid Crystal
Dot Matrix Display Module**Overview**

The DM2021 is a liquid crystal dot matrix display module that consists of LCD panel LCD-5121, LCD control driver LC7985NA, and driver SED1181 and is capable of providing 20 characters × 2 lines display. It contains a controller, a data RAM, and a character generator ROM required for providing display. Data interfacing is in 4-bit parallel or 8-bit parallel and data can be written in or read from a microprocessor.

General Specifications

1. Display method	1/5 bias 1/16 duty
2. Display content	20 characters × 2 lines
3. Dots organizing 1 character	5 × 8 dots
4. Display data RAM	80 × 8 bits
5. Character generator ROM	160-character JIS font set + 32-character Refer to Table 1.
6. Character generator RAM	64 × 8 bits 5 × 7 dots 8 characters
7. Instruction function	Refer to Table 2.
8. Circuit diagram	Refer to Fig. 3.

Outline

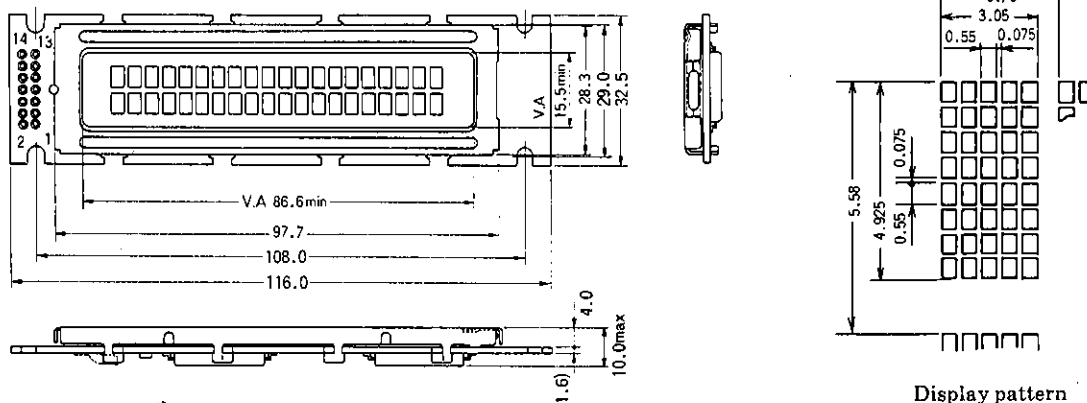
1. Module outline	116.0 (L) × 32.5 (W) × 10 (T) [mm ³]
2. View area	86.0 × 15.5 [mm ²]
3. Dot size	0.55 × 0.55 [mm ²]
4. Dot pitch	0.625 × 0.625 [mm ²]
5. Character size (5 × 8 dots)	3.05 × 4.925 [mm ²]

Absolute Maximum Ratings at Ta = 25°C

			unit
Maximum Supply Voltage	V _{DD} - V _{SS}	-0.3 to +7	V
Input Voltage	V _I	-0.3 to V _{DD} + 0.3	V
LCD Drive Voltage	V _{DD} - V _O	-0.3 to +13.3	V
Operating Temperature	T _{opr}	0 to +50	°C
Storage Temperature	T _{stg}	-20 to +70	°C

Module Dimensions 5008

(unit: mm)



Display pattern

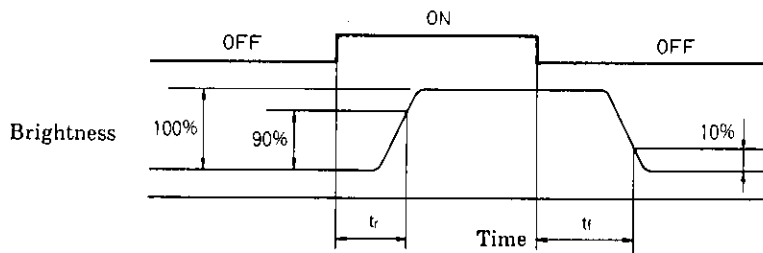
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DM2021

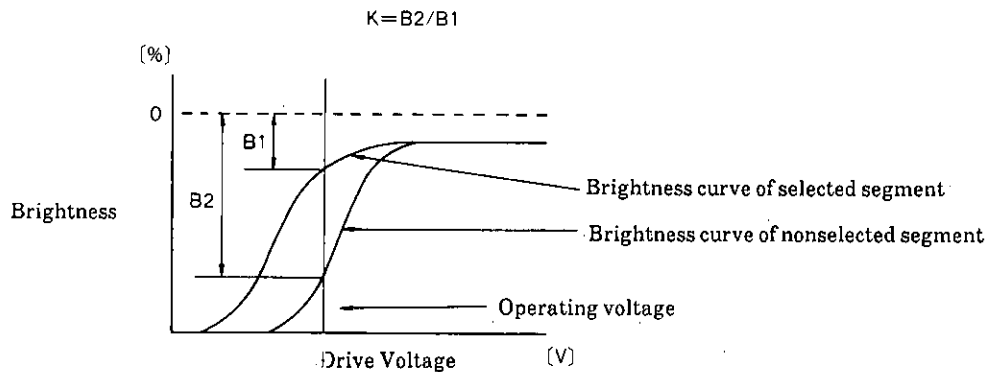
Electro-optical Characteristics at $T_a = 25^\circ\text{C}$, $V_{DD} - V_{SS} = 5\text{V}$ unless otherwise specified

			min	typ	max	unit
Input 'H'-Level Voltage	V_{IH}		2.2		V_{DD}	V
Input 'L'-Level Voltage	V_{IL}		0		0.6	V
Output 'H'-Level Voltage	V_{OH}	DB_0 to DB_7 , $-I_{OH} = 0.2\text{mA}$	2.4		V_{DD}	V
Output 'L'-Level Voltage	V_{OL}	DB_0 to DB_7 , $-I_{OL} = 1.2\text{mA}$	0		0.4	V
Pull-up MOS Current	I_P	DB_0 to DB_7 , RS, R/W	50	125	250	μA
Current Dissipation	I_{DD}	No input/output current included		(1.5)	3.0	mA
Oscillation Frequency	F_{OSC}		190	270	350	kHz
Viewing Angle	$\phi_2 - \phi_1$	$K = 1.4, \theta = 0^\circ$	20	30		deg.
Contrast Ratio	K	$\phi = 20^\circ, \theta = 0^\circ$	3.0			
Rise Time	t_r	$\phi = 20^\circ, \theta = 0^\circ$		200	300	ms
Fall Time	t_f	$\phi = 20^\circ, \theta = 0^\circ$		300	450	ms
LCD Drive Voltage (Recommended Value)	$V_{DD} - V_O$	$T_a = 0^\circ\text{C}, \phi = 20^\circ, \theta = 0^\circ, K \geq 3$	4.4	4.5	4.6	V
		$T_a = 25^\circ\text{C}, \phi = 20^\circ, \theta = 0^\circ, K \geq 3$	4.0	4.1	4.2	V
1/16 Duty		$T_a = 50^\circ\text{C}, \phi = 20^\circ, \theta = 0^\circ, K \geq 3$	3.4	3.5	3.6	V

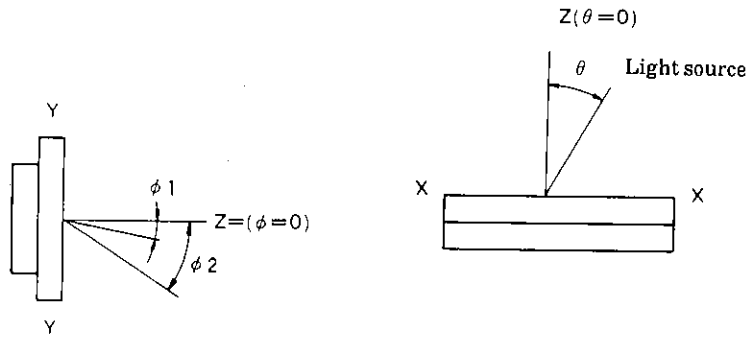
(1) Test Condition for Response Time (t_r, t_f)



(2) Definition of Contrast Ratio [K]



(3) Contrast Ratio Measuring Method



Angles ϕ and θ are defined as shown above.

The light source is placed in the θ direction at an angle of 30° and the sensor is placed in the ϕ direction to measure the contrast.

Pin Description

No.	Pin Name	Function
1	V _{SS}	(-) power supply pin 0V
2	V _{DD}	(+) power supply pin +5V
3	V _O	Pin for applying LCD drive voltage
4	RS	Input pin, HI = Data, LOW = Instruction
5	R/W	Input pin, HI = Read, LOW = Write
6	E	Input pin, Enable signal
7	DB ₀	} Data bus line
8	DB ₁	
9	DB ₂	
10	DB ₃	
11	DB ₄	
12	DB ₅	
13	DB ₆	
14	DB ₇	

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Timing Characteristics		min	typ	max	unit
Enable Cycle Time	t_{cycE}	1000			ns
Enable Pulse Width [High Level]	P_{WEH}	450			ns
Enable Rise/Fall Time	t_{Er}, t_{Ef}			25	ns
Setup Time [RS/RW-E]	t_{As}	140			ns
Address Hold Time	t_{AH}	10			ns
Data Delay Time	t_{DDR}			320	ns
Data Setup Time	t_{DSW}	195			ns
Data Hold Time	$t_H(t_{DHR})$	10(20)			ns

Write Operation

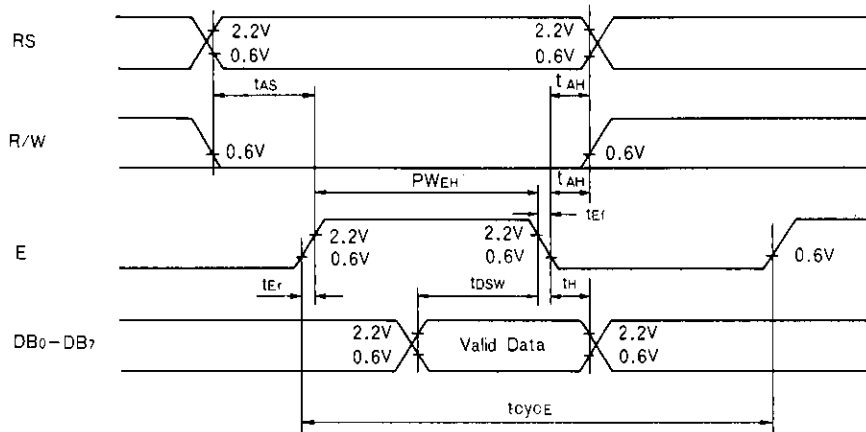


Fig.1 Interface Timing (Data Write)

Read Operation

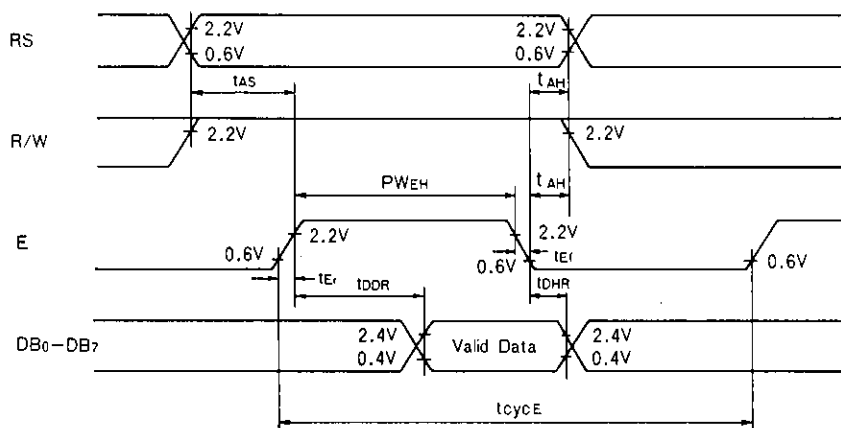


Fig.2 Interface Timing (Data Read)

Table 1 Character Code

Low-order 4bits \ Hi-order 4 bits	0000	0010	0011	0100	0101	0110	0111	1010	1011	1100	1101	1110	1111
xxxx0000	CG RAM (1)		0	a	P	`	P	-	9	E	e	p	
xxxx0001	(2)	!	1	A	Q	a	q	a	7	+	4	a	q
xxxx0010	(3)	"	2	B	b	r	r	4	9	x	p	e	
xxxx0011	(4)	#	3	C	c	s	s	j	7	E	e	e	
xxxx0100	(5)	\$	4	D	d	t	t	\	1	1	P	a	
xxxx0101	(6)	%	5	E	e	u	u	.	*	1	e	o	
xxxx0110	(7)	&	6	F	f	v	v	9	h	2	p	z	
xxxx0111	(8)	'	7	G	g	w	w	7	+	x	9	π	
xxxx1000	(1)	(8	H	h	x	x	4	9	*	U	π	π
xxxx1001	(2))	9	I	i	y	y	e	7	U	U	U	U
xxxx1010	(3)	*	0	J	j	z	z	x	3	n	j	π	
xxxx1011	(4)	+	1	K	k	l	l	4	9	E	0	π	π
xxxx1100	(5)	,	<	L	l	1	1	+	9	7	7	0	π
xxxx1101	(6)	-	=	M	m	n	n	3	x	9	0	π	+
xxxx1110	(7)	.	>	N	n	+	+	a	E	+	'	π	
xxxx1111	(8)	/	?	O	o	+	u	v	7	0	0	0	0

(Note) The CG RAM is a character generator RAM used to store the character patterns that can be program-rewritten, as desired, by the user.

Table 2 Instruction Function

Instruction	Code										Contents	Execution Time ($f_{OSC}=250kHz$)	
	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0			
Display clear	0	0	0	0	0	0	0	0	0	1	Clears all display and returns the cursor to the home position (address 0).	82 μ s to 1.64ms	
Cursor home	0	0	0	0	0	0	0	0	0	1	*	Returns the cursor to the home position address 0). Also returns the display being shifted to the original position. The DD RAM contents remain unaffected.	40 μ s to 1.6ms
Entry mode set	0	0	0	0	0	0	0	1	I/D	S	Settings the cursor move direction and specifies whether or not the shift the display. These operations are performed during data write and read.	40 μ s	
Display ON/OFF control	0	0	0	0	0	0	1	D	C	B	Sets all display ON/OFF (D), cursor ON/OFF (C), cursor position character blink (B).	40 μ s	
Cursor/display shift	0	0	0	0	0	1	S/C	R/L	*	*	Moves the cursor and shifts the display without affecting the DD RAM contents.	40 μ s	
Function set	0	0	0	0	1	DL	N	F	*	*	Sets the interface data length (DL), number of display lines (L), and character font (F).	40 μ s	
CG RAM address set	0	0	0	1	ACG						Sets the CG RAM address. RAM data is sent/received after this setting.	40 μ s	
DD RAM address set	0	0	1	ADD						Sets the DD RAM address. DD RAM data is sent/received after this setting	40 μ s		
Busy flag/address read	0	1	BF	AC						Reads the contents of busy flag (BF) indicating internal operation is in progress and reads the contents of address counter.	1 μ s		
CG RAM/DD RAM data write	1	0	Write data						Writes data into the DD RAM or CG RAM.	40 μ s			
CG RAM/DD RAM data read	1	1	Read data						Reads data from the DD RAM or CG RAM.	40 μ s			
	I/D=1: Increment (+1) I/D=0: Decrement (-1) S=1: Accompanied by display shift S=0: Not accompanied by display shift S/C=1: Display shift S/C=0: Cursor move R/L=1: Right-shift R/L=0: Left-shift DL=1: 8 bits DL=0: 4 bits N=1: 2 lines N=0: 1 line F=1: 5 \times 10 dots F=0: 5 \times 7 dots BF=1: Internally operating BF=0: Possible to accept instruction										DD RAM: Display data RAM CG RAM: Character generator RAM ACG: CG RAM address ADD: DD RAM address Corresponds to cursor address. AC: Address counter used for both DD RAM and CG RAM.	The change in the frequency (f_{OSC}) also causes the execution time to be changed. (Example) When $f_{OSC}=270kHz$, $40\mu s \times \frac{250}{270} = 37\mu s$	

Fig. 3 Circuit Diagram DM2021

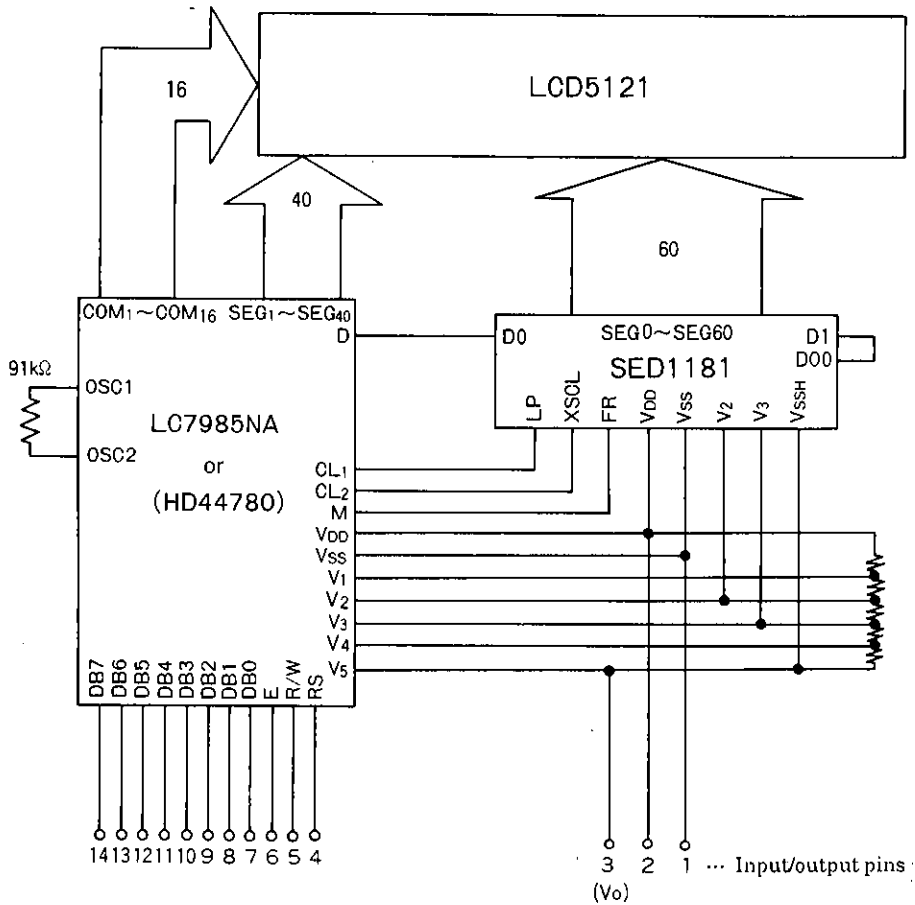
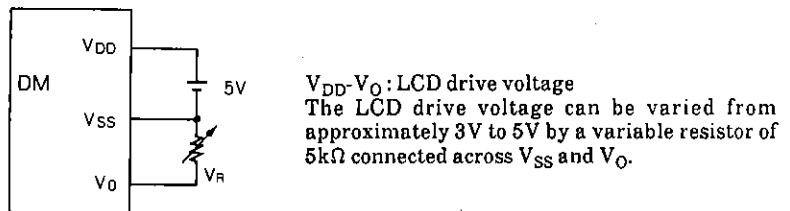


Fig. 4 Sample Power Supply



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