May 2001

8 - Bit Micro-controller

with 32KB flash embedded

Product List

SM8958C25, 25 MHz 32KB internal memory MCU
SM8958C40, 40 MHz 32KB internal memory MCU

Description

The SM8958 series product is an 8 - bit single chip micro-controller with 32KB flash & 1KB RAM embedded. It is a derivative of the 80C51 microcontroller family. With its hardware features and powerful instruction set, it's straight forward to make it a versatile and cost effective controller for those applications which demand up to 32 I/O pins for PDIP package or up to 36 I/O pins for PLCC/QFP package, or applications which need up to 32KB memory either for program or for data or mixed.
To program the on-chip flash memory, a commercial writer is available to do it in parallel programming method.

Ordering Information

SM8958ihhk

i: process identifier {L, C}
hh: working clock in MHz {25, 40}
k: package type postfix {as below table}

Postfix	Package	Pin/Pad Configuration	Dimension
P	40L PDIP	page 2	page 12
J	44L PLCC	page 2	page 14
Q	44L QFP	page 2	page 13

Features

- Working voltage:4.5V through 5.5V
  program voltage:12V
- General 80C51 family compatible
- 12 clocks per machine cycle
- 32K bytes on-chip flash memory
- 1024 bytes on-chip data RAM
- Three 16 bit timers/counters
- Four 8-bit I/O ports for PDIP package
- Four 8-bit I/O ports + one 4-bit I/O ports for PLCC or QFP package
- Full duplex serial channel
- Bit operation instructions
- Page free jumps
- 8-bit unsigned division
- 8-bit unsigned multiply
- BCD arithmetic operations
- Direct addressing
- Indirect addressing
- Nested interrupts
- Two priority level interrupts
- A serial I/O port
- Power save modes:
  Idle mode and power down mode
- Code protection function
- One watch dog timer (WDT)
- Low EMI (inhibit ALE)

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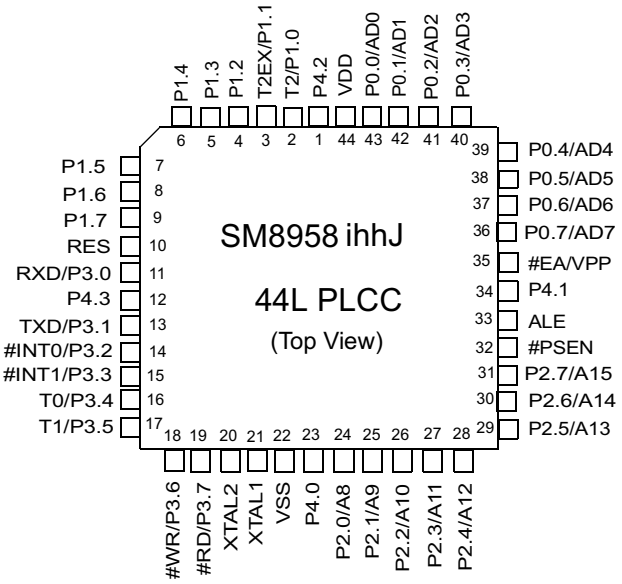
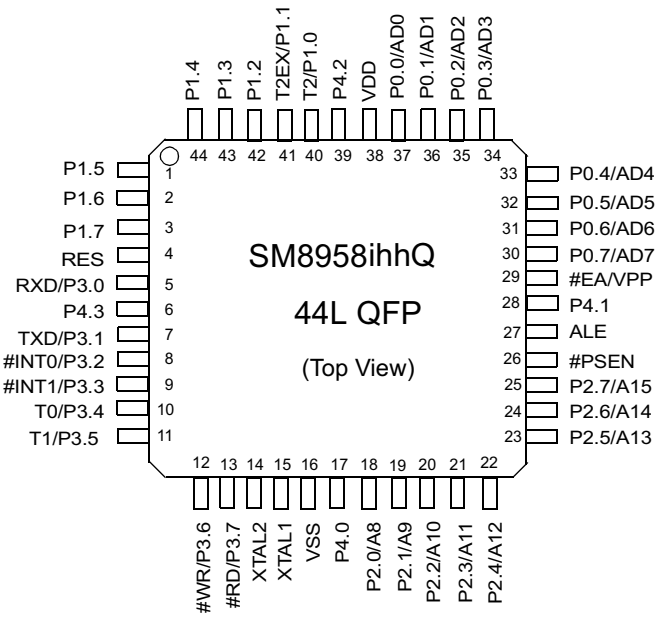
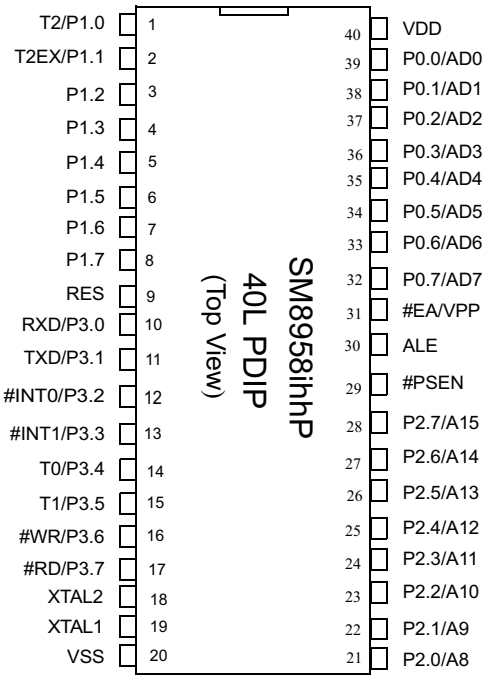
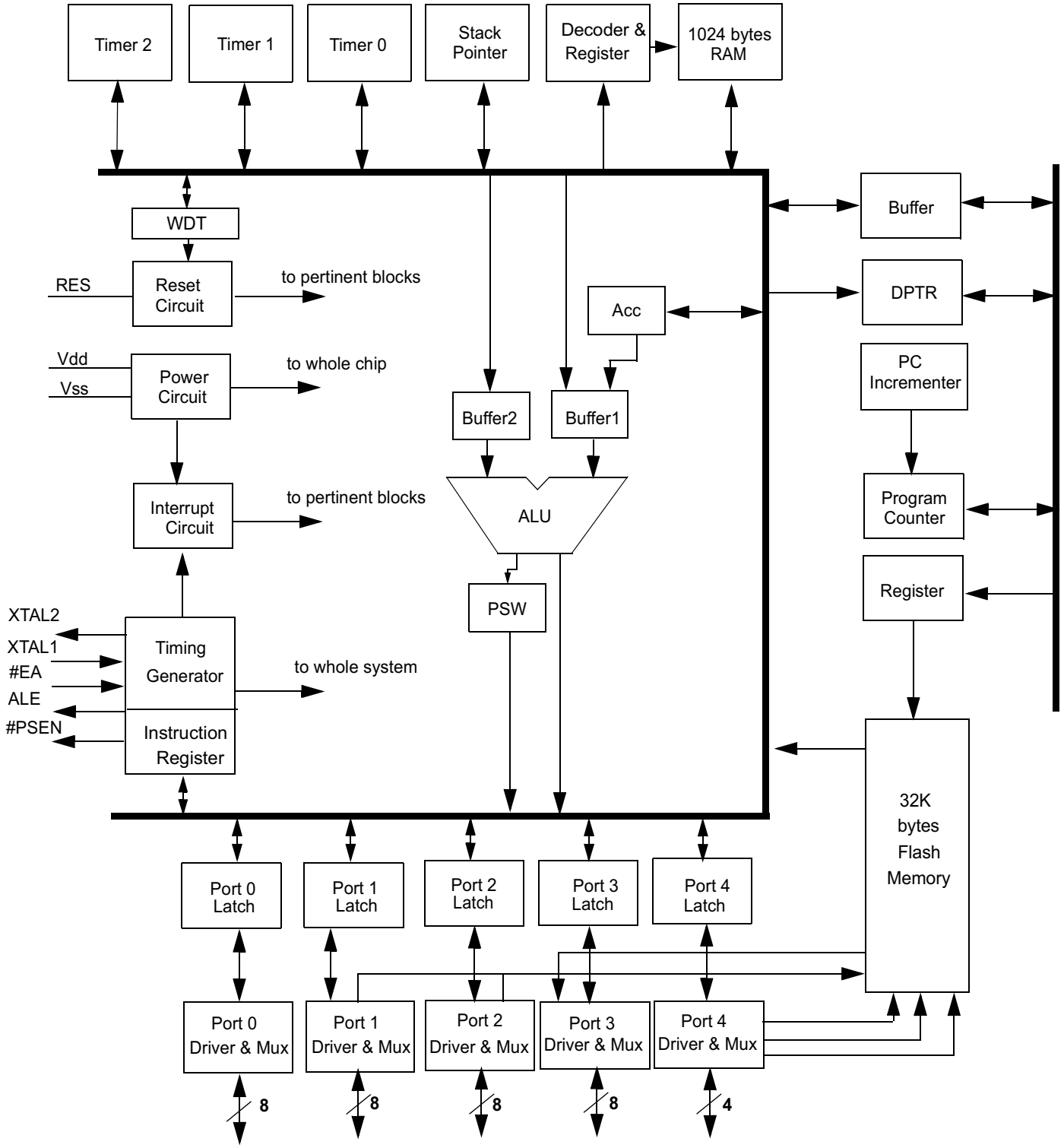
Pin Configurations







Block Diagram



Pin Descriptions

40L PDIP Pin#	44L QFP Pin#	44L PLCC Pin#	Symbol	Active	I/O	Names
1	40	2	T2/P1.0		i/o	bit 0 of port 1 & timer 2
2	41	3	T2EX/P1.1		i/o	bit 1 of port 1 & timer control
3	42	4	P1.2		i/o	bit 2 of port 1
4	43	5	P1.3		i/o	bit 3 of port 1
5	44	6	P1.4		i/o	bit 4 of port 1
6	1	7	P1.5		i/o	bit 5 of port 1
7	2	8	P1.6		i/o	bit 6 of port 1
8	3	9	P1.7		i/o	bit 7 of port 1
9	4	10	RES	H	i	Reset
10	5	11	RXD/P3.0		i/o	bit 0 of port 3 & Receive data
11	7	13	TXD/P3.1		i/o	bit 1 of port 3 & Transmit data
12	8	14	#INT0/P3.2	L/ -	i/o	bit 2 of port 3 & low true interrupt 0
13	9	15	#INT1/P3.3	L/ -	i/o	bit 3 of port 3 & low true interrupt 1
14	10	16	T0/P3.4		i/o	bit 4 of port 3 & Timer 0
15	11	17	T1/P3.5		i/o	bit 5 of port 3 & Timer 1
16	12	18	#WR/P3.6	L/ -	i/o	bit 6 of port 3 & ext. memory write
17	13	19	#RD/P3.7	L/ -	i/o	bit 7 of port 3 & ext. mem. read
18	14	20	XTAL2		o	Crystal out
19	15	21	XTAL1		i	Crystal in
20	16	22	VSS			Sink Voltage, Ground
21	18	24	P2.0/A8		i/o	bit 0 of port 2 & bit 8 of ext. memory address
22	19	25	P2.1/A9		i/o	bit 1 of port 2 & bit 9 of ext. memory address
23	20	26	P2.2/A10		i/o	bit 2 of port 2 & bit 10 of ext. memory address
24	21	27	P2.3/A11		i/o	bit 3 of port 2 & bit 11 of ext. memory address
25	22	28	P2.4/A12		i/o	bit 4 of port 2 & bit 12 of ext. memory address
26	23	29	P2.5/A13		i/o	bit 5 of port 2 & bit 13 of ext. memory address
27	24	30	P2.6/A14		i/o	bit 6 of port 2 & bit 14 of ext. memory address
28	25	31	P2.7/A15		i/o	bit 7 of port 2 & bit 15 of ext. memory address
29	26	32	#PSEN	L	o	program storage enable
30	27	33	ALE	-	o	address latch enable
31	29	35	#EA/VPP	L	i	external access & VPP
32	30	36	P0.7/AD7		i/o	bit 7 of port 0 & data/address bit 7 of ext. memory
33	31	37	P0.6/AD6		i/o	bit 6 of port 0 & data/address bit 6 of ext. memory
34	32	38	P0.5/AD5		i/o	bit 5 of port 0 & data/address bit 5 of ext. memory
35	33	39	P0.4/AD4		i/o	bit 4 of port 0 & data/address bit 4 of ext. memory
36	34	40	P0.3/AD3		i/o	bit 3 of port 0 & data/address bit 3 of ext. memory
37	35	41	P0.2/AD2		i/o	bit 2 of port 0 & data/address bit 2 of ext. memory
38	36	42	P0.1/AD1		i/o	bit 1 of port 0 & data/address bit 1 of ext. memory
39	37	43	P0.0/AD0		i/o	bit 0 of port 0 & data/address bit 0 of ext. memory
40	38	44	VDD			Drive Voltage, +5 Vcc
	17	23	P4.0		i/o	bit 0 of Port 4
	28	34	P4.1		i/o	bit 1 of Port 4
	39	1	P4.2		i/o	bit 2 of Port 4
	6	12	P4.3		i/o	bit 3 of Port 4

Special Function Register (SFR) Memory MAP

$F8								$FF
$F0	B							$F7
$E8								$EF
$E0	ACC							$E7
$D8	**P4**							$DF
$D0	PSW							$D7
$C8	T2CON		RC2H	RC2L	TL2	TH2		$CF
$C0								$C7
$B8	IP						**SCONF**	$BF
$B0	P3							$B7
$A8	IE							$AF
$A0	P2							$A7
$98	SCON	SBUF					**WDTC**	$9F
$90	P1							$97
$88	TCON	TMOD	TL0	TL1	TH0	TH1		$8F
$80	P0	SP	DPL	DPH	(Reserved)		PCON	$87

Note: The text of SFRs with bold type characters are Extension Special Function Registers for SM8958

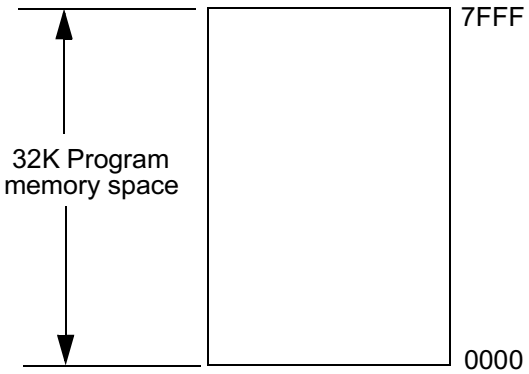
Extension Function Description

Memory Structure

The SM8958 is the general 80C52 hardware core to integrate the expanded 768B data RAM and 32KB flash program memory as a single chip microcontroller. Its memory structure follows genaral 80C52 structure.

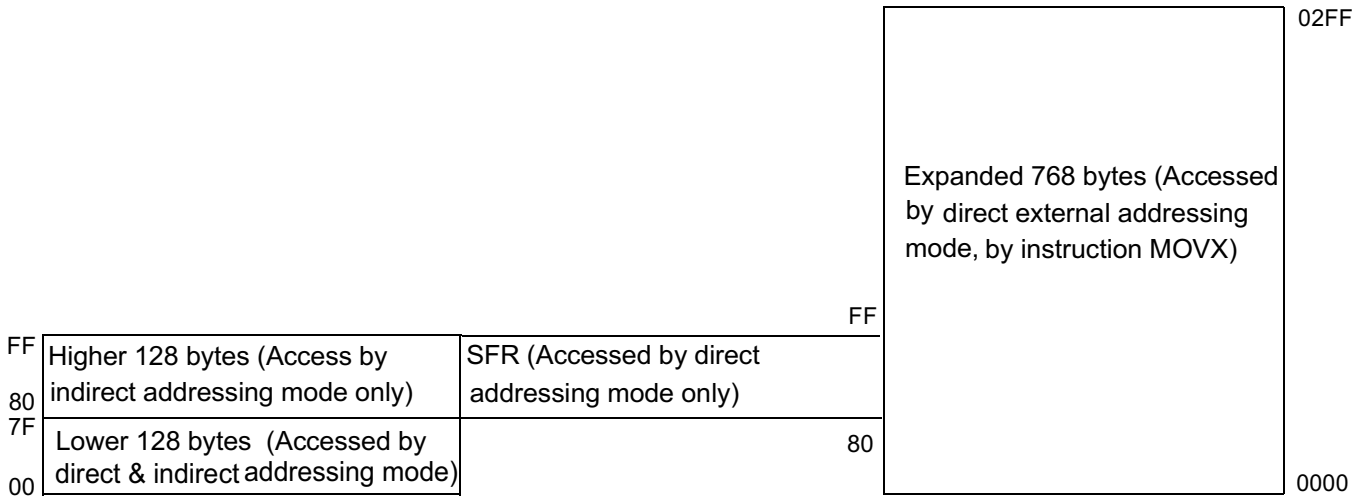
Program Memory

The SM8958 has 32K bytes on-chip flash memory which can be used as general program memory.



Data Memory

The SM8958 has 1K bytes on-chip RAM, 256 bytes of it are the same as general 80C52 internal memory structure while the expanded 768 bytes on-chip RAM can be accessed by external memory addressing method. (by instruction MOVX)



Data Memory - Lower 128 byte

Data memory $00 to $FF is the same as 80C52
The address $00 to $7F can be accessed by direct and indirect addressing modes.
Address $00 to $1F is register area.
Address $20 to $2F is memory bit area.
Address $30 to $7F is for general memory area.

Data memory - Higher 128 byte

The address $80 to $FF can be accessed by indirect addressing mode only.
Addressing $80 to $FF is data area.

Data Memory - Expanded 768 bytes

From external address $0000 to $02FF is the on-chip expanded RAM area, total 768 bytes. This area can be accessed by external direct addressing mode only (by instruction MOVX).

Internal Memory Page Select Register (IMPSR, $85)

	R	R	R	R	R	R	PS1	PS0
Reset value	0	0	0	0	0	0	0	0
	MSB							LSB

Note: “R” means reserved

The address space of instruction MOVX @Rn is determined by bit 1 & bit 0 (PS1, PS0) of IMPSR. The default setting of PS1, PS0 bits is 00 (page 0).

If the address of instruction MOVX @DPTR is larger than $02FF then SM8958 will generate the external memory control signal automatically. The bit 1 (OME) of special function register $BF (SCONF) can enable or disable this expanded 768 byte RAM. The default setting of OME bit is 1 (enable).

The address space of instruction MOVX @Rn is determined by bit 1 & bit 0 (PS1, PS0) of special function register $85 (IMPSR). The default setting of PS1, PS0 bits is 00 (page 0).

One page of data RAM is 256 bytes.

PS1, PS0=00, Rn of instruction MOVX @Rn mapping to expanded RAM address $0000 to $ 00FF (page 0)
PS1, PS0=01, Rn of instruction MOVX @Rn mapping to expanded RAM address $0100 to $ 01FF (page 1)
PS1, PS0=10, Rn of instruction MOVX @Rn mapping to expanded RAM address $0200 to $ 02FF (page 2)
PS1, PS0=11, Rn of instruction MOVX @Rn mapping to expanded RAM address $XY00 to $ XYFF where high byte address specified by port 2. (SM8958 will generate the external memory control signal automatically).

Port 4 for PLCC or QFP package:

The bit addressable port 4 is available with PLCC or QFP package. The port 4 has only 4 pins and its port address is located at 0D8H. The function of port 4 is the same as the function of port 1, port 2 and port 3.

port4 (P4, $D8)

	0	0	0	0	P4.3	P4.2	P4.1	P4.0
Reset value	0	0	0	0	1	1	1	1
	MSB							LSB

The bit 3, bit 2, bit 1, bit 0 output the setting to pin P4.3, P4.2, P4.1, P4.0 respectively.

Extension Function Description

Watch Dog Timer

The Watch Dog Timer (WDT) is a 16-bit free-running counter that generate a reset signal if the counter overflows. The WDT is useful for systems which are susceptible to noise, power glitches, or electronics discharge which causing software dead loop or runaway. The WDT function can help user software recover from abnormal software condition. The WDT is different from Timer0 , Timer1 and Timer2 of general 80C52. WDT reset can be prevented by software periodically clearing the WDT counter.

The SM8958 WDT has selectable divider input for the time base source clock. To select the divider input, the setting of bit2~bit0 (PS2~PS0) of Watch Dog Timer Control Register (WDTC) should be set accordingly.

The WDT is enabled by setting 1 to the bit 7 (WDTE) of WDT. After WDTE set to 1. The 16-bit counter starts to count with the selected time base source clock set by PS2 ~ PS0. It will generate a reset signal when overflow occurs. The WDTE bit will be cleared to 0 automatically when SM8958 been reset, either hardware reset or WDT reset.

The WDT is reset by setting 1 to the bit 5 (CLEAR) of WDT. This will clear the content of the 16-bit counter and force the counter re-start counting from the beginning.

Watch Dog Timer Registers - WDT Control Register (WDTC, $9F)

	WDTE	0	CLEAR	0	0	PS2	PS1	PS0
Reset value	0	0	0	0	0	0	0	0

MSB LSB

WDTE: Watch Dog Timer enable bit
CLEAR: Watch Dog Timer reset bit
PS2 ~ PS0: clock source divider selection bit

PS [2:0]	Divider (OSC in)	Time Period (ms) @40MHz
000	8	13.1
001	16	26.21
010	32	52.42
011	64	104.8
100	128	209.71
101	256	419.43
110	512	838.86
111	1024	1677.72

System Control Register (SCONF,$BF)

	WDR	R	R	R	R	R	OME	ALEI
Reset value	0	0	0	0	0	0	1	0

MSB LSB

WDR : Watch Dog Timer Reset. When system reset by Watch Dog Timer overflow, WDR will be set to 1
OME : 768 bytes on-chip RAM enable bit
ALEI : ALE output inhibit bit, to reduce EMI

The bit 7(WDR) of SCONF is Watch Dog Timer Reset bit. It will be set to 1 when reset signal generated by WDT overflow. User should check WDR bit whenever unpredicted reset happened.

Reduce EMI Function

The SM8958 allows user to reduce the EMI emission by setting 1 to the bit 0 (ALEI) of SCONF register. This function will inhibit the clock signal in Fosc/6Hz output to the ALE pin. This function is available when there is no external program memory or no external data RAM in the system.

Operating Conditions

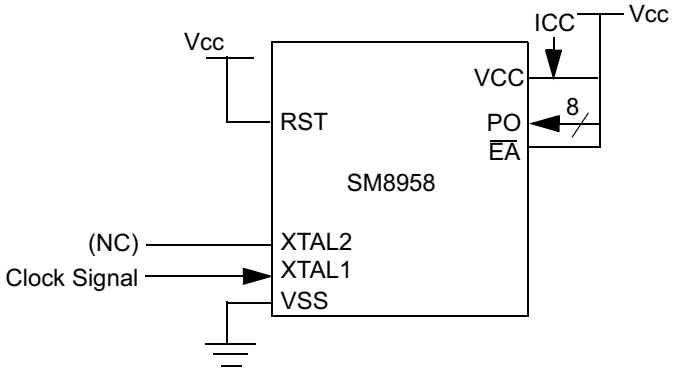
Symbol	Description	Min.	Typ.	Max.	Unit.	Remarks
TA	Ambient temperature under bias	0	25	70	C	
VCC5	Supply voltage	4.5	5.0	5.5	V	SM8958C
Fosc 16	Oscillator Frequency	3.0	16	16	MHz	SM8958C16
Fosc 25		3.0	25	25	MHz	SM8958C25
Fosc 40		3.0	40	40	MHz	SM8958C40

DC Characteristics

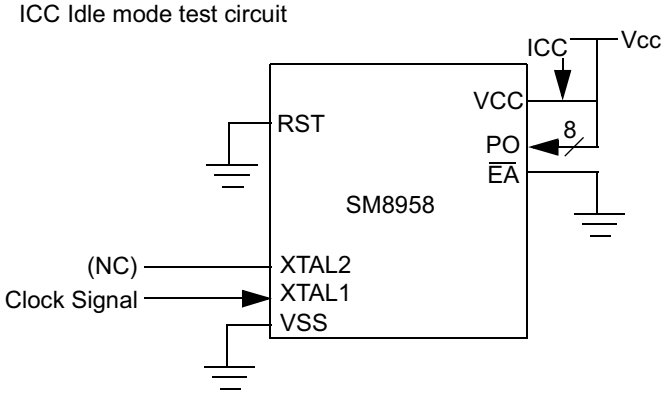
(16/25/40 MHZ , typical operating conditions , vaild for SM8958 series)

Symbol	Parameter	Valid	Min.	Max.	Unit	Test Conditions
VIL1	Input Low Voltage	port 0,1,2,3,4,#EA	-0.5	0.8	V	Vcc=5V
VIL2	Input Low Voltage	RES, XTAL1	0	0.8	V	"
VIH1	Input High Voltage	port 0,1,2,3,4,#EA	2.0	Vcc+0.5	V	"
VIH2	Input High Voltage	RES, XTAL1	70%Vcc	Vcc+0.5	V	"
VOL1	Output Low Voltage	port 0, ALE, #PSEN		0.45	V	IOL=3.2mA
VOL2	Output Low Voltage	port 1,2,3,4		0.45	V	IOL=1.6mA
VOH1	Output High Voltage	port 0	2.4		V	IOH=-800uA
			90%Vcc		V	IOH=-80uA
VOH2	Output High Voltage	port 1,2,3,4,ALE,#PSEN	2.4		V	IOH=-60uA
			90%Vcc		V	IOH=-10uA
IIL	Logical 0 Input Current	port 1,2,3,4		-75	uA	Vin=0.45V
ITL	Logical Transition Current	port 1,2,3,4		-650	uA	Vin=2.0V
ILI	Input Leakage Current	port 0, #EA		± 10	uA	0.45V<Vin<Vcc
R RES	Reset Pulldown Resistance	RES	50	300	Kohm	
C IO	Pin Capacitance			10	pF	Freq=1MHz, Ta=25°C
I CC	Power Supply Current	Vdd		20	mA	Active mode, 40MHz
				15	mA	Active mode, 25MHz
				10	mA	Active mode, 16MHz
				10	mA	Idle mode, 40MHz
				7.5	mA	Idle mode, 25MHz
				6	mA	Idle mode, 16MHz
				150	uA	Power down mode

ICC Active mode test circuit



ICC Idle mode test circuit

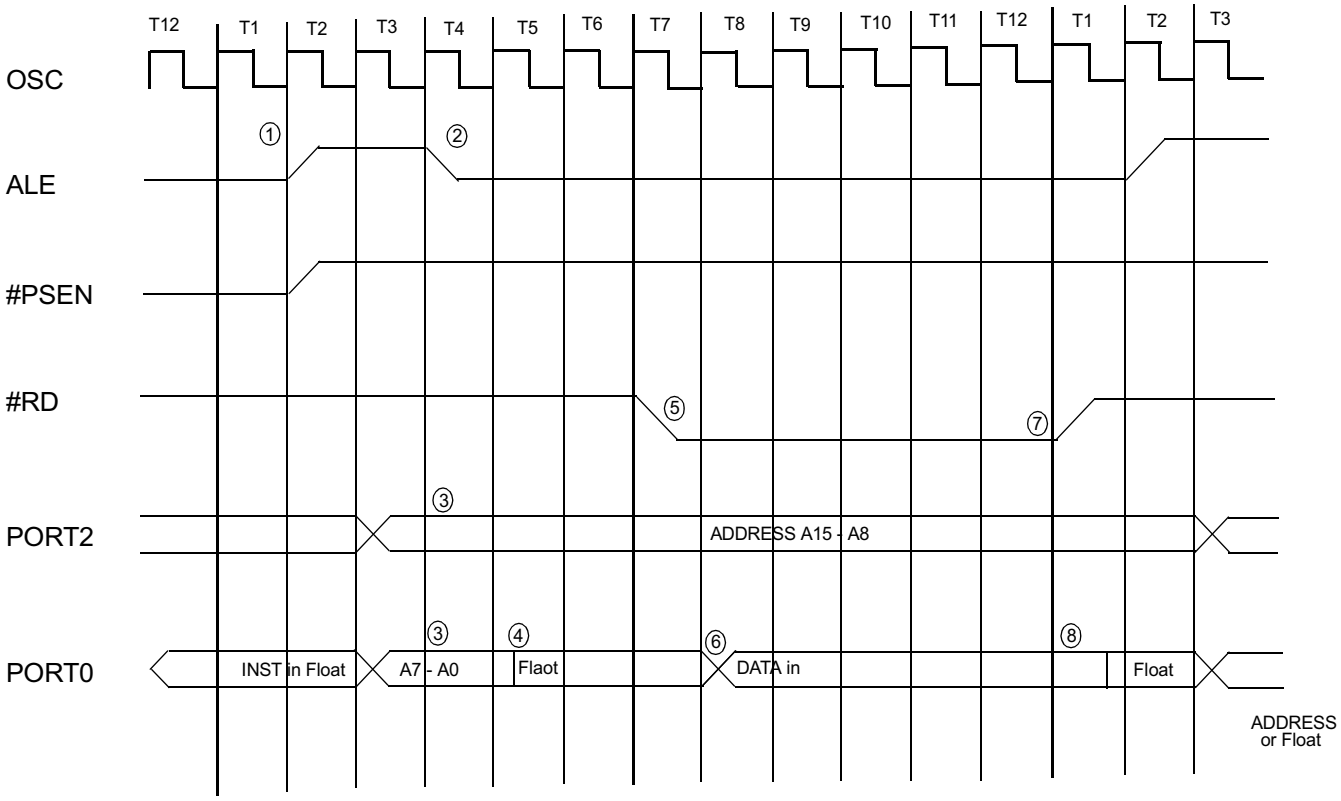


AC Characteristics

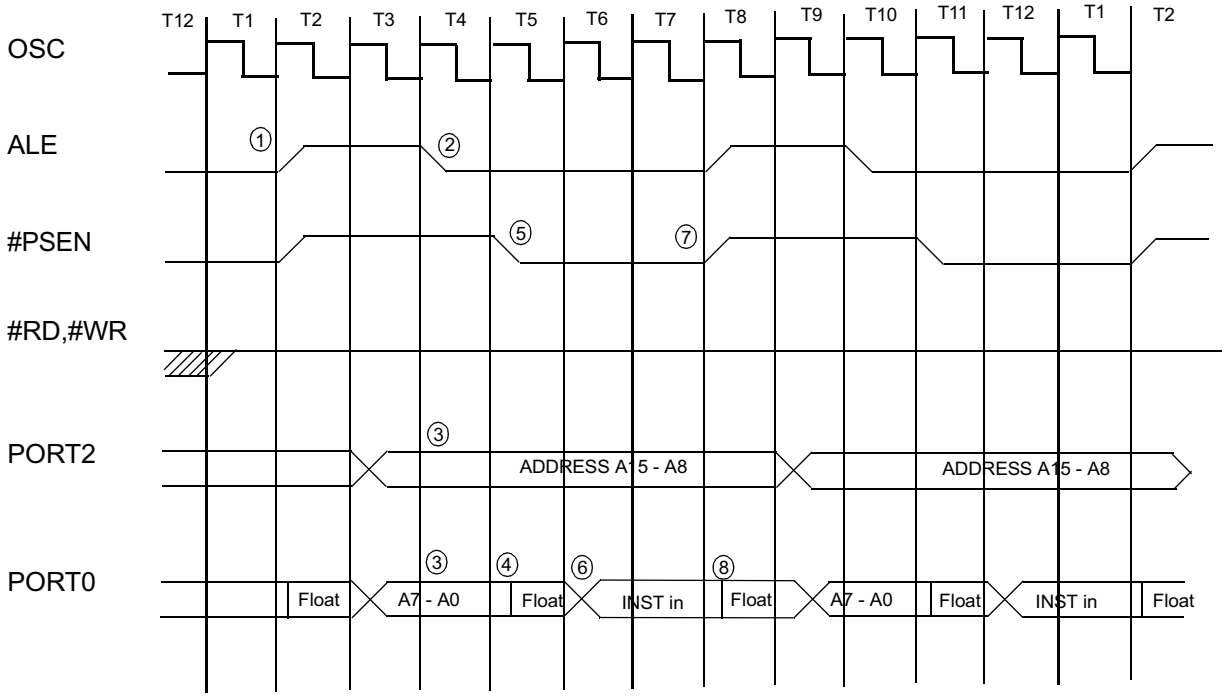
(16/25/40 MHz, operating conditions ; CL for Port 0, ALE and PSEN Outputs=100pF ; CL for all Other Output=80pF)

Symbol	Parameter	Valid Cycle	fosc=16MHz			Variable fosc			Unit	Remarks
			Min.	Typ.	Max	Min.	Typ.	Max		
T LHLL	ALE pulse width	RD/WRT	115			2xT - 10			nS	
T AVLL	Address Valid to ALE low	RD/WRT	43			T - 20			nS	
T LLAX	Address Hold after ALE low	RD/WRT	53			T - 10			nS	
T LLIV	ALE low to Valid Instruction In	RD			240			4xT - 10	nS	
T LLPL	ALE low to #PSEN low	RD	53			T - 10			nS	
T PLPH	#PSEN pulse width	RD	173			3xT - 15			nS	
T PLIV	#PSEN low to Valid Instruction In	RD			177			3xT - 10	nS	
T PXIX	Instruction Hold after #PSEN	RD	0			0			nS	
T PXIZ	Instruction Float after #PSEN	RD			87			T + 25	nS	
T AVIV	Address to Valid Instruction In	RD			292			5xT - 20	nS	
T PLAZ	#PSEN low to Address Float	RD			10			10	nS	
T RLRH	#RD pulse width	RD	365			6xT - 10			nS	
T WLWH	#WR pulse width	WRT	365			6xT - 10			nS	
T RLDV	#RD low to Valid Data In	RD			302			5xT - 10	nS	
T RHDX	Data Hold after #RD	RD	0			0			nS	
T RHDZ	Data Float after #RD	RD			145			2xT + 20	nS	
T LLDV	ALE low to Valid Data In	RD			590			8xT - 10	nS	
T AVDV	Address to Valid Data In	RD			542			9xT - 20	nS	
T LLYL	ALE low to #WR High or #RD low	RD/WRT	178		197	3xT - 10		3xT + 10	nS	
T AVYL	Address Valid to #WR or #RD low	RD/WRT	230			4xT - 20			nS	
T QVWH	Data Valid to #WR High	WRT	403			7xT - 35			nS	
T QVWX	Data Valid to #WR transition	WRT	38			T - 25			nS	
T WHQX	Data hold after #WR	WRT	73			T + 10			nS	
T RLAZ	#RD low to Address Float	RD						5	nS	
T YALH	#WR or #RD high to ALE high	RD/WRT	53		72	T -10		T + 10	nS	
T CHCL	clock fall time								nS	
T CLCX	clock low time								nS	
T CLCH	clock rise time								nS	
T CHCX	clock high time								nS	
T, TCLCL	clock period			63			1/fosc		nS	

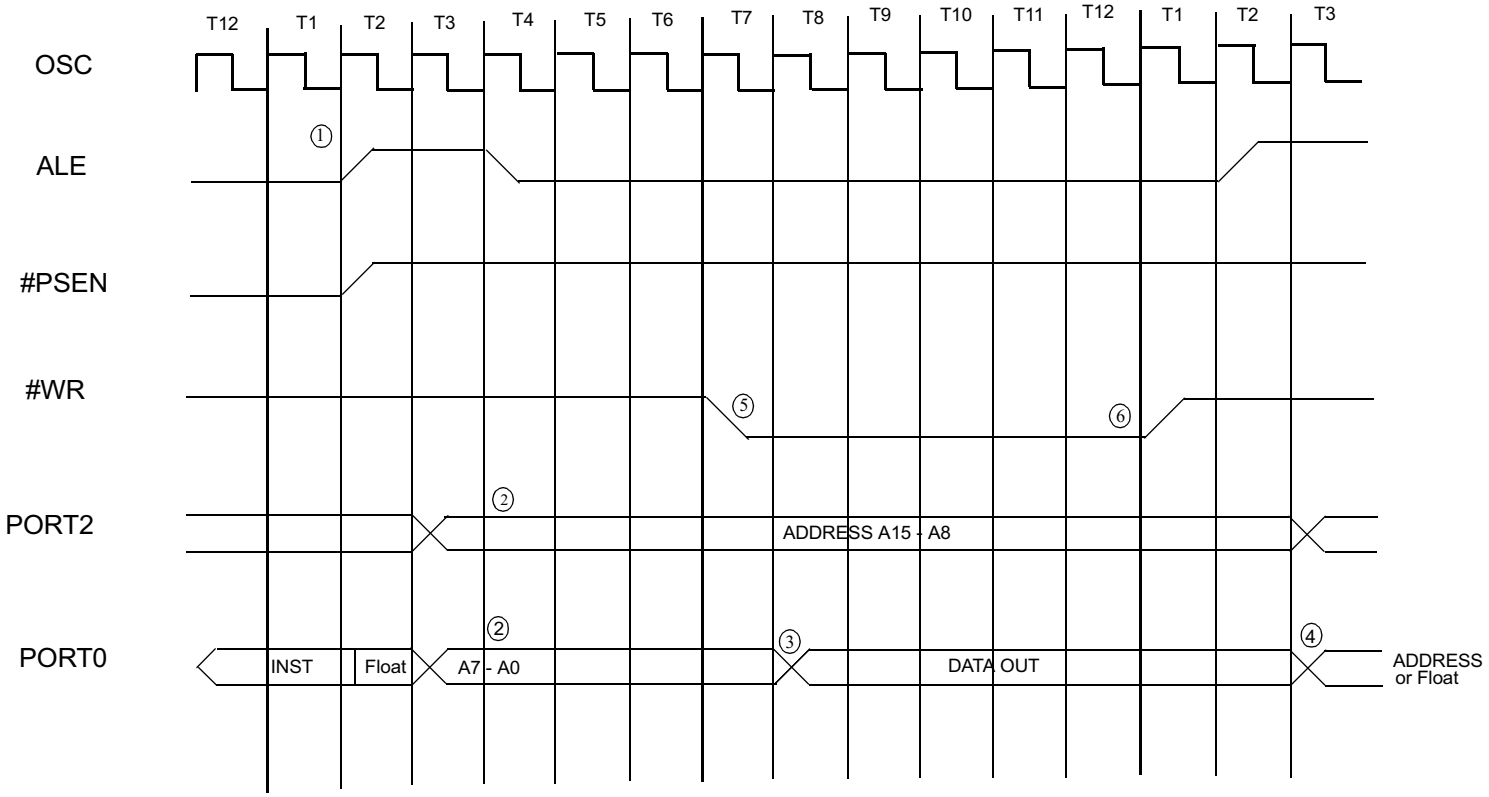
Data Memory Read Cycle Timing



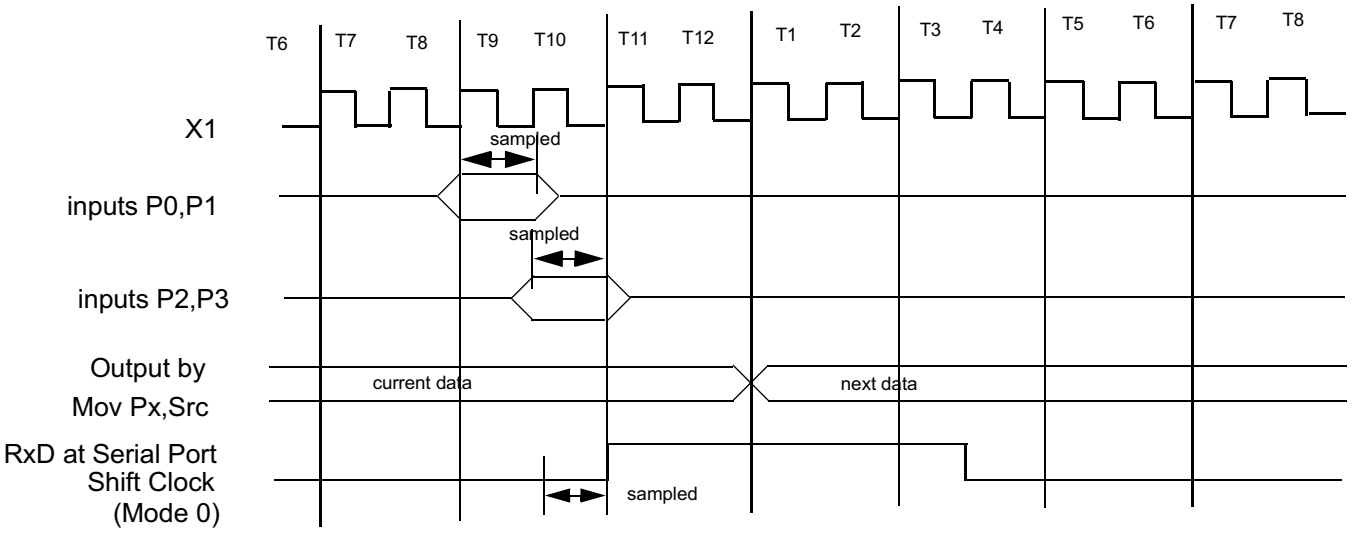
Program Memory Read Cycle Timing



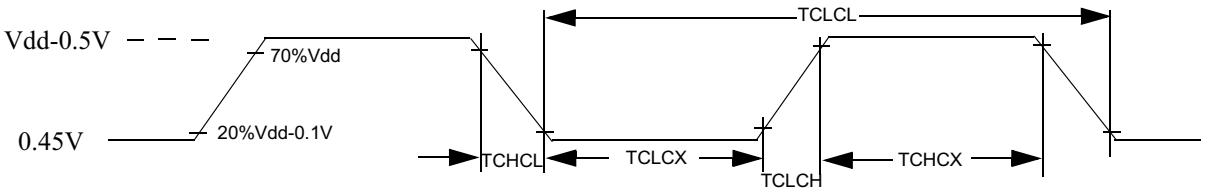
Data Memory Write Cycle Timing



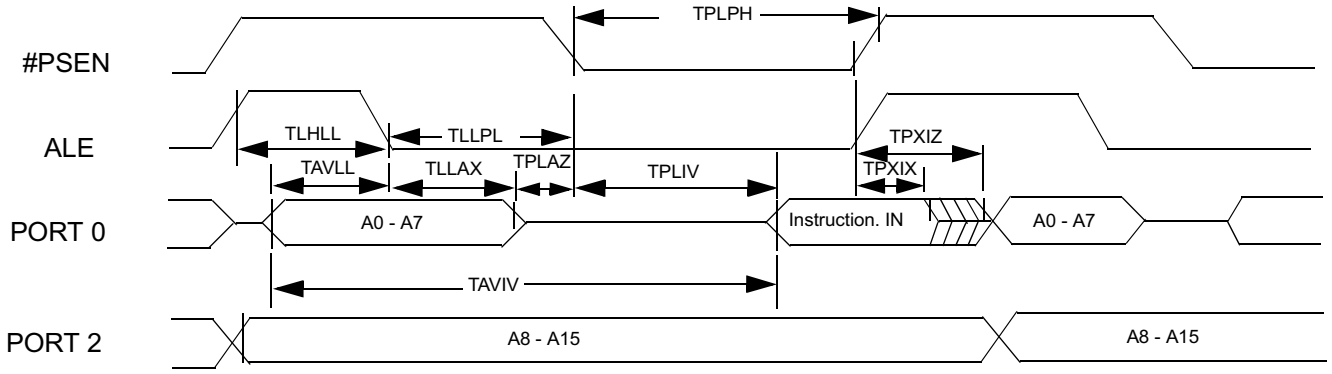
I/O Ports Timing



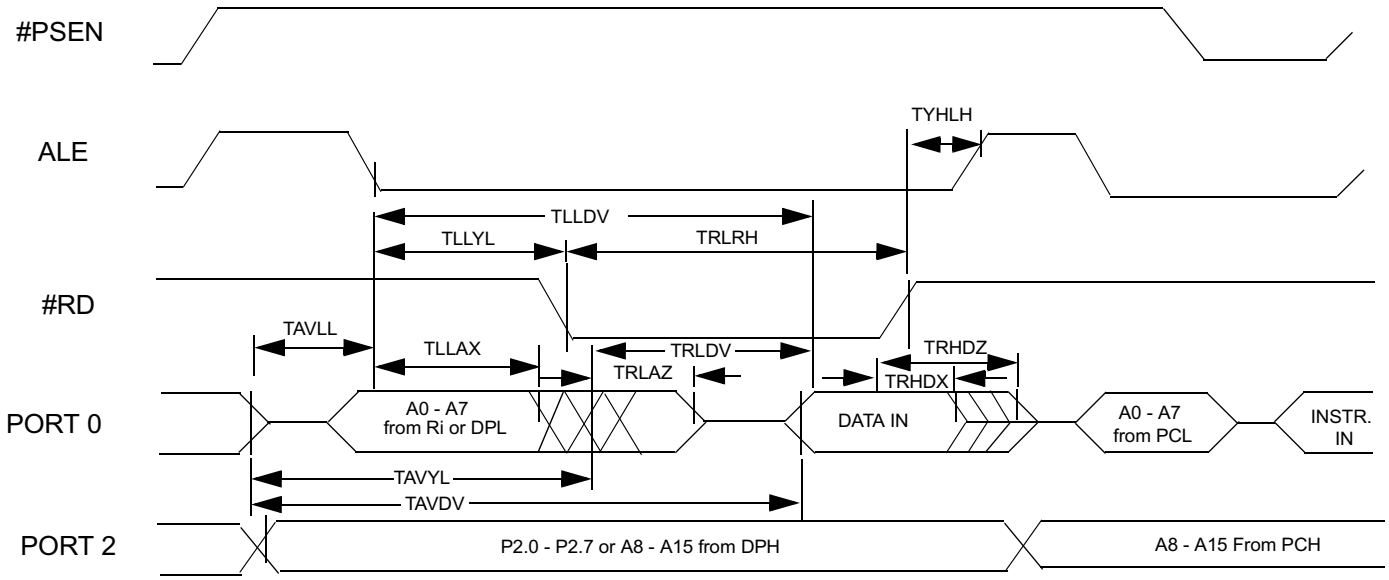
Timing Critical, Requirement of External Clock (Vss=0.0V is assumed)



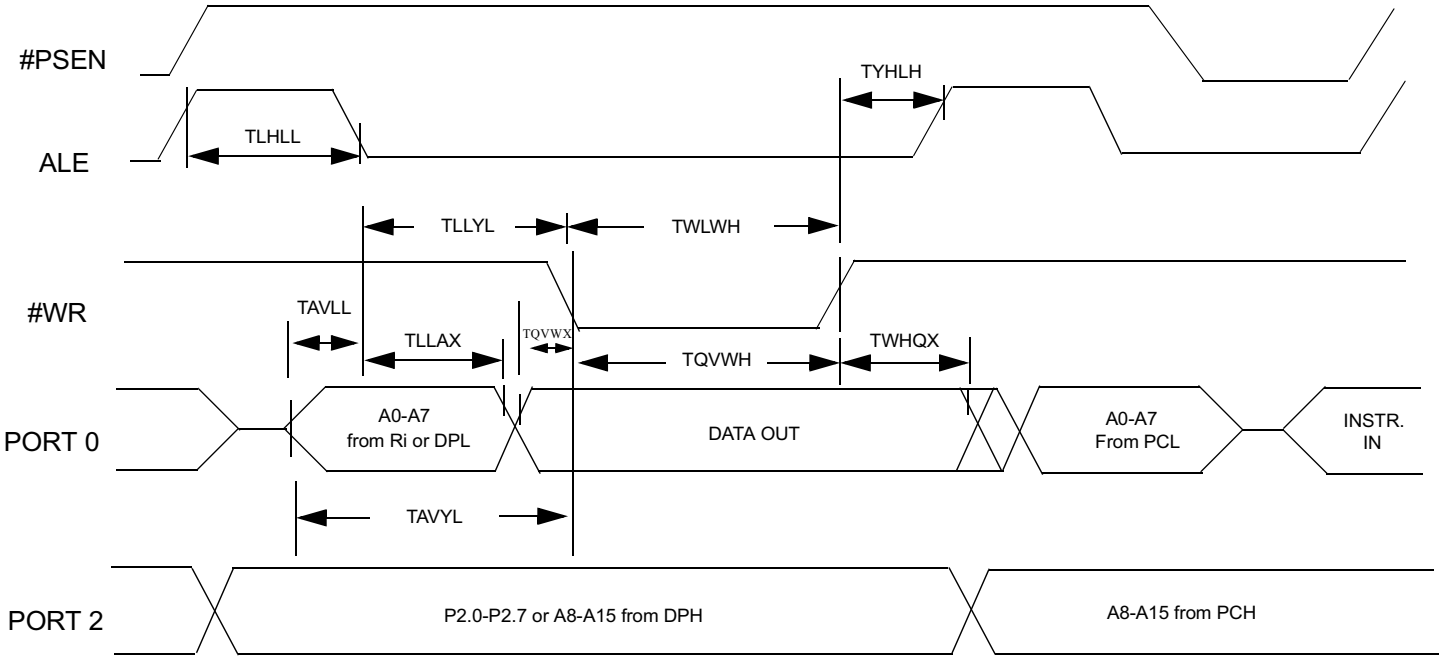
Tm.I External Program Memory Read Cycle



Tm.II External Data Memory Read Cycle

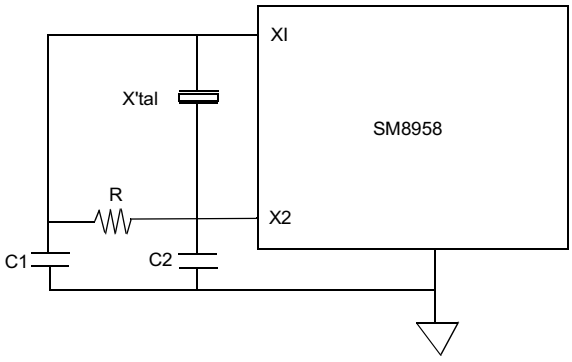


Tm.III External Data Memory Write Cycle



Application Reference

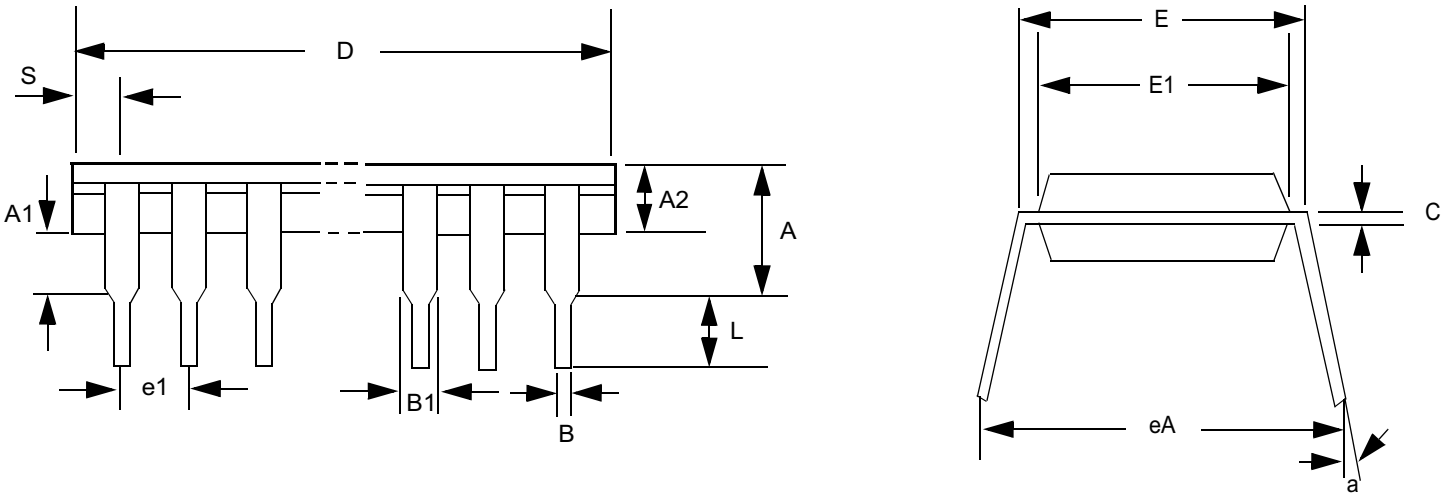
Vaild for SM8958				
X'tal	3MHz	6MHz	9MHz	12MHz
C1	30 pF	30 pF	30 pF	30 pF
C2	30 pF	30 pF	30 pF	30 pF
R	open	open	open	open
X'tal	16MHz	25MHz	33MHz	40MHz
C1	30 pFF	15 pF	10 pF	5 pF
C2	30 pF	15 pF	10 pF	5 pF
R	open	62KΩ	6.8KΩ	4.7KΩ



NOTE: Oscillation circuit may differ with different crystal or ceramic resonator in higher oscillation frequency which is due to each crystal or ceramic resonator has its own characteristics.

User should check with the crystal or ceramic resonator manufacturer for appropriate values of external components.

40L 600mil PDIP Information

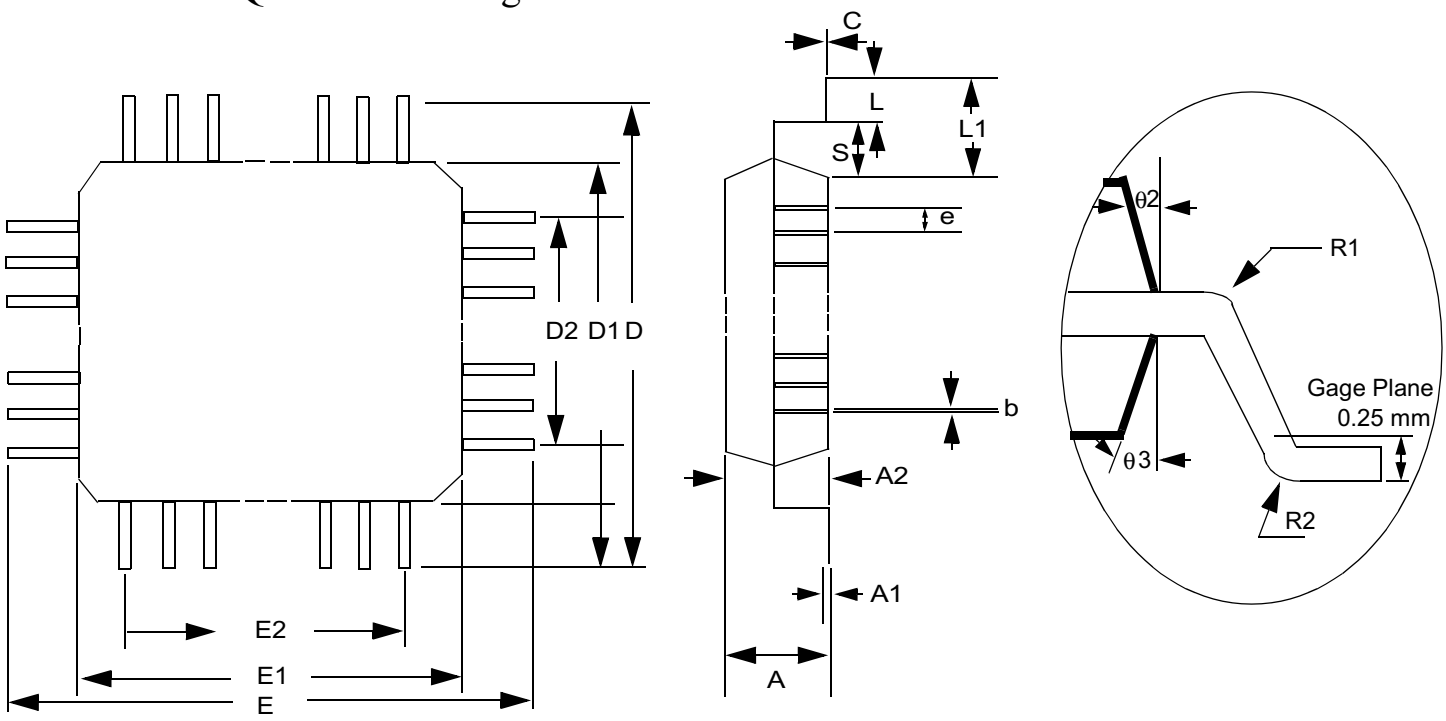


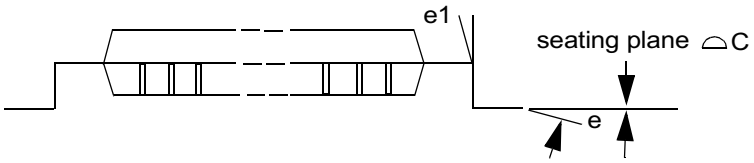
Note:

1. Dimension D Max & include mold flash or tie bar burrs.
2. Dimension E1 does not include interlead flash.
3. Dimension D & E1 include mold mismatch and are determined at the mold parting line.
4. Dimension B1 does not include dambar protrusion/ infrusion.
5. Controlling dimension is inch.
6. General appearance spec. should base on final visual inspection spec.

Symbol	Dimension in inch minimal/maximal	Dimension in mm minimal/maximal
A	- / 0.210	- / 5.33
A1	0.010 / -	0.25 / -
A2	0.150 / 0.160	3.81 / 4.06
B	0.016 / 0.022	0.41 / 0.56
B1	0.048 / 0.054	1.22 / 1.37
C	0.008 / 0.014	0.20 / 0.36
D	- / 2.070	- / 52.58
E	0.590 / 0.610	14.99 / 15.49
E1	0.540 / 0.552	13.72 / 14.02
e1	0.090 / 0.110	2.29 / 2.79
L	0.120 / 0.140	3.05 / 3.56
a	0°/ 15°	0°/ 15°
eA	0.630 / 0.670	16.00 / 17.02
S	- / 0.090	- / 2.29

44L Plastic Quad Flat Package





Note:

Dimension D1 and E1 do not include mold protrusion.

Allowance protrusion is 0.25mm per side.

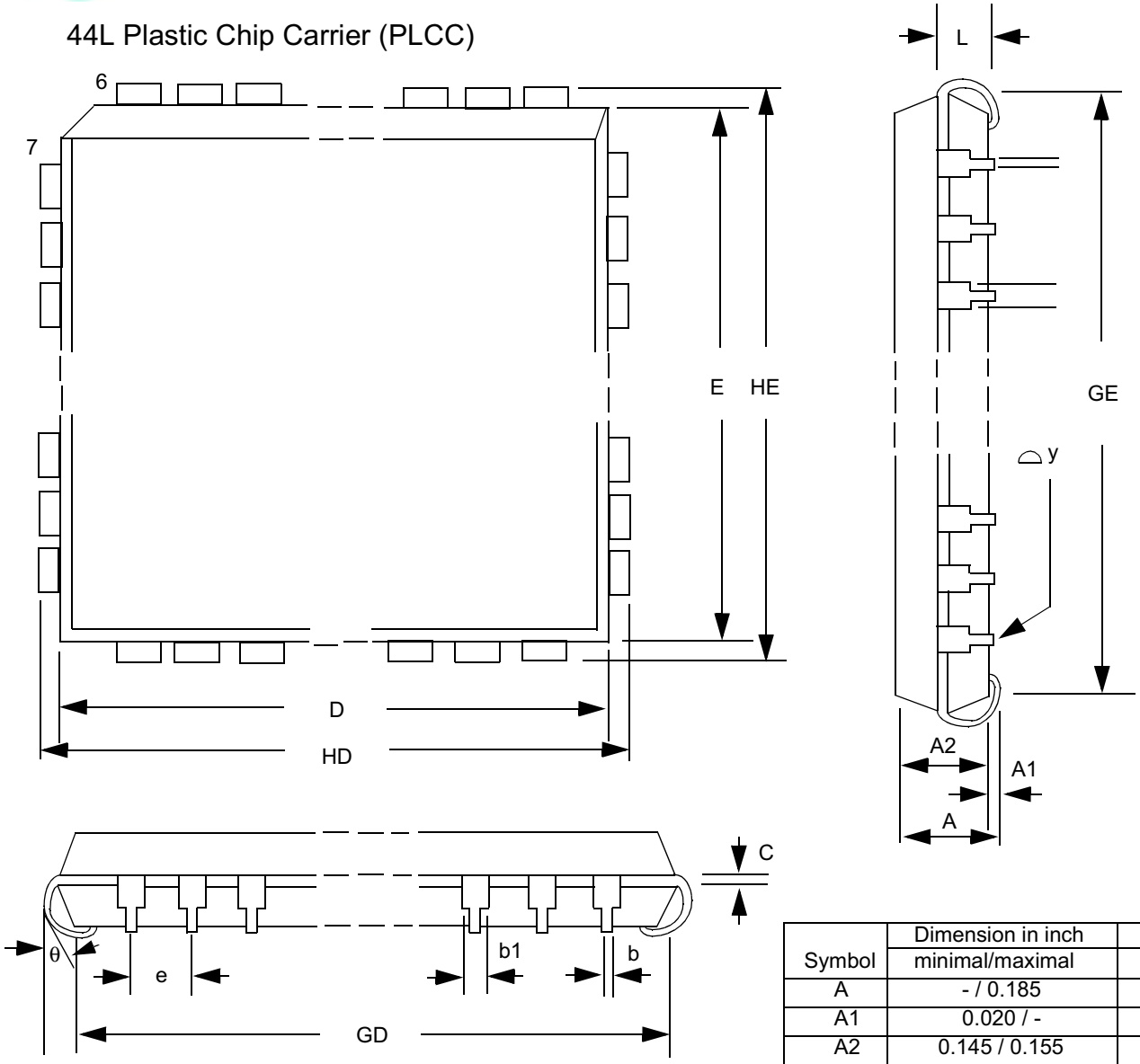
Dimension D1 and E1 do include mold mismatch and are determined datum plane.

Dimension b does not include dambar protrusion.

Allowance dambar protrusion shall be 0.08 mm total in excess of the b dimension at maximum material condition. Dambar cannot be located on the lower radius or the lead foot.

Symbol	Dimension in Inch minimal/maximal	Dimension in mm minimal/maximal
A	- / 0.100	- / 2.55
A1	0.006 / 0.014	0.15 / 0.35
A2	0.071 / 0.087	1.80 / 2.20
b	0.012 / 0.018	0.30 / 0.45
c	0.004 / 0.009	0.09 / 0.20
D	0.520 BSC	13.20 BSC
D1	0.394 BSC	10.00 BSC
D2	0.315	8.00
E	0.520 BSC	13.20 BSC
E1	0.394 BSC	10.00 BSC
E2	0.315	8.00
e	0.031 BSC	0.80 BSC
L	0.029 / 0.041	0.73 / 1.03
L1	0.063	1.60
R1	0.005 / -	0.13 / -
R2	0.005 / 0.012	0.13 / 0.30
S	0.008 / -	0.20 / -
θ	0° / 7°	as left
θ1	0° / -	as left
θ2	10° REF	as left
θ3	7° REF	as left
⌓C	0.004	0.10

44L Plastic Chip Carrier (PLCC)



Symbol	Dimension in inch minimal/maximal	Dimension in mm minimal/maximal
A	- / 0.185	- / 4.70
A1	0.020 / -	0.51 / -
A2	0.145 / 0.155	3.68 / 3.94
b1	0.026 / 0.032	0.66 / 0.81
b	0.016 / 0.022	0.41 / 0.56
C	0.008 / 0.014	0.20 / 0.36
D	0.648 / 0.658	16.46 / 16.71
E	0.648 / 0.658	16.46 / 16.71
e	0.050 BSC	1.27 BSC
GD	0.590 / 0.630	14.99 / 16.00
GE	0.590 / 0.630	14.99 / 16.00
HD	0.680 / 0.700	17.27 / 17.78
HE	0.680 / 0.700	17.27 / 17.78
L	0.090 / 0.110	2.29 / 2.79
θ	- / 0.004	- / 0.10
⌓ y	/	/

Note:

1. Dimension D & E does not include interlead flash.
2. Dimension b1 does not include dambar protrusion/ intrusion.
3. Controlling dimension:Inch
4. General appearance spec. should base on final visual inspection spec.

eMCU writer list		
Company	Contact info	Programmer Model Number
Advantech 7F, No.98, Ming-Chung Rd., Shin-Tien City, Taipei, Taiwan, ROC Website: http://www.aec.com.tw	Tel:02-22182325 Fax:02-22182435 E-mail: aecwebmaster@advantech.com.tw	LabTool - 48 (1 * 1) LabTool - 848 (1*8)
Caprilion P.O. Box 461 KaoHsiung,Taiwan, ROC Website: http://www.market.net.tw/ ~ cap/	Tel:07-3865061 Fax:07-3865421 E-mail: cap@market.net.tw	UNIV2000
Hi-Lo 4F, No. 20, 22, LN, 76, Rui Guang Rd., Nei Hu, Taipei, Taiwan, ROC. Website: http://www.hilosystems.com.tw	Tel:02-87923301 Fax:02-87923285 E-mai: support@hilosystems.com.tw	All - 11 (1*1) Gang - 08 (1*8)
Leap 6th F1-4, Lane 609, Chunghsin Rd., Sec. 5, Sanchung, Taipei Hsien, Taiwan, ROC Website: http://www.leap.com.tw	Tel:02-29991860 Fax:02-29990015 E-mail: service@leap.com.tw	ChipStation (1*1) SU - 2000 (1*8)
System General 5F, No. 9 Alley 6, Lane 45 Bao Shing Rd. Shin - Tien, Taipei, Taiwan, ROC Website: http://www.sg.com.tw	Tel:02-29173005 Fax:02-29111283 E-mail: sales@sg.com.tw	Multi - Apro (1*1)
BP Microsystems 1000 N. Post Oak Road, Suite 225 Houston, Tx, U.S.A 77055-7237 Website: http://www.bpmicro.com	Tel:1-800-225-2102(US only) 713-688-4600 Fax:713-688-0920 E-mail: Tech@BPMicro.com	BP - 1200 (1*1)
Stag Programmers LTD Silver Court, Watchmead, Welwyn Garden, City, Hertfordshire, AL7 1LT. United Kingdom Website: http://www.stag.co.uk	Tel:44(0)1707 332148 Fax:+44(0)1707 371503 E-mail: sales@sg.com.tw	P803 (1*8)
Xeltek Electronic Co., Ltd 338 Hongwu Road, Nanjing, China 210002 Website: http://www.xeltek-cn.com	Tel:+86-25-4408399, 4543153-206 E-mail: xelclw@jlonline.com, xelgbw@jlonline.com	Superpro/2000 (1*1) Superpro/680 (1*1) Superpro/280 (1*1) Superpro/L+(1*1)

Feedback / Inquiry:

To :SyncMOS Technologies, Inc. Attn :MKT / Customer Service Dept. Fax :886-3-5792960 :886-3-5780493 Tel :886-3-5792988 :886-3-5792926	From : _____ Company : _____ Dept, Section : _____ Position Title : _____ Inquiry Date : _____ Ref No : _____

Description: