

# 1.5V Advanced Dual PWM and Dual Linear Power Controller

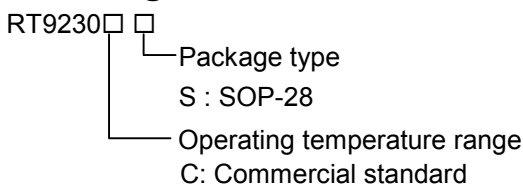
## General Description

The RT9230 is a 4-in-one power controller optimized for high-performance microprocessor and computer applications. The IC integrates two PWM controller, two linear controllers as well as monitoring and protection functions into a 28-pin SOP package. The first PWM controller regulates the microprocessor core voltage with a synchronous buck converter, while the second PWM controller supplies the computer system's AGP 1.5V or 3.3V bus power with a standard buck converter. The first linear regulator provides power for the 1.5V GTL bus and the second linear regulator provides 1.8V power for the North/South Bridge core voltage and/or cache memory circuits.

The RT9230 features an Intel-compatible, TTL 5-bit programmable DAC that adjusts the core voltage from 2.1V to 3.5V in 0.1V increments and from 1.3V to 2.05V in 0.05V steps. The 5-bit DAC has a typical  $\pm 1\%$  tolerance. The second PWM controller is user-selectable for output level of 1.5V and 3.3V with  $\pm 2.5\%$  accuracy. The linear controllers drives external N-MOSFET or NPN bipolar for the pass transistor to provide fixed output voltages of 1.5V  $\pm 3\%$  and 1.8V  $\pm 3\%$ .

The RT9230 monitors all the output voltages. A Power -good signal is issued when the core voltage is within  $\pm 10\%$  of the DAC setting and the other levels are above their under-voltage levels. Additional build-in over-voltage protection for the core output uses the lower MOSFET to prevent output voltage above 115% of the DAC setting. The PWM over-current function monitors the output current using the voltage drop across the MOSFET's  $R_{DS(ON)}$ , which eliminates the need for a current sensing resistor.

## Ordering Information



## Features

- 4-in-one Regulated Voltages for Microprocessor Core, AGP Bus, North/South Bridge and/or Cache Memory, GTL Bus Power
- Compatible with HIP6020
- Power-good Output Voltage Monitor

### Switching section

- 5-bit DAC Programmable from 1.3V to 3.5V
- $\pm 1\%$  DAC Accuracy
- Fast Transient Response
- Full 0% to 100% Duty Cycle Driver
- Fixed 200kHz Switching Frequency
- Adaptive Non-overlapping Gate Driver
- Over-current Monitor Uses MOSFET  $R_{DS(ON)}$
- Over-voltage Protection Uses Lower MOSFET

### Linear Section

- Fixed Linear Regulator Output Voltage
- MOSFET or NPN Driving Capability
- Ultra Fast Response Speed
- Under-voltage Protection
- Internal Thermal Shutdown

## Applications

- Full Motherboard Power Regulation for Computer
- Low-voltage Distributed Power Supplies

## Pin Configurations

Part Number	Pin Configurations
RT9230CS (Plastic SOP-28)	TOP VIEW
	UGATE2 [1]      [28] VCC
	PHASE2 [2]      [27] UGATE1
	VID4 [3]      [26] PHASE1
	VID3 [4]      [25] LGATE1
	VID2 [5]      [24] PGND
	VID1 [6]      [23] OCSET1
	VID0 [7]      [22] VSEN1
	PGOOD [8]      [21] FB1
	OCSET2 [9]      [20] NC
	VSEN2 [10]      [19] VSEN3
	SELECT [11]      [18] DRIVE3
	SS [12]      [17] GND
	FAULT [13]      [16] VAUX
VSEN4 [14]      [15] DRIVE4	

## Absolute Maximum Ratings

- Supply Voltage ..... +15V
- PGOOD, FAULT and GATE Voltage ..... GND-0.3V to V<sub>CC</sub>+0.3V
- Input, Output or I/O Voltage ..... GND-0.3V to 7V
- Ambient Temperature Range ..... 0°C to +70°C
- Junction Temperature Range ..... 0°C to +125°C
- Storage Temperature Range ..... -65°C to +150°C
- Lead Temperature (Soldering, 10 sec.) ..... 300°C
- Package Thermal Resistance  
SOP-28,  $\theta_{JA}$  ..... 60°C/W

## Recommended Operating Conditions

- Supply Voltage ..... +12V ±10%
- Ambient Temperature Range ..... 0°C to 70°C
- Junction Temperature Range ..... 0°C to 125°C

### CAUTION:

Stresses beyond the ratings specified in “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

## Electrical Characteristics

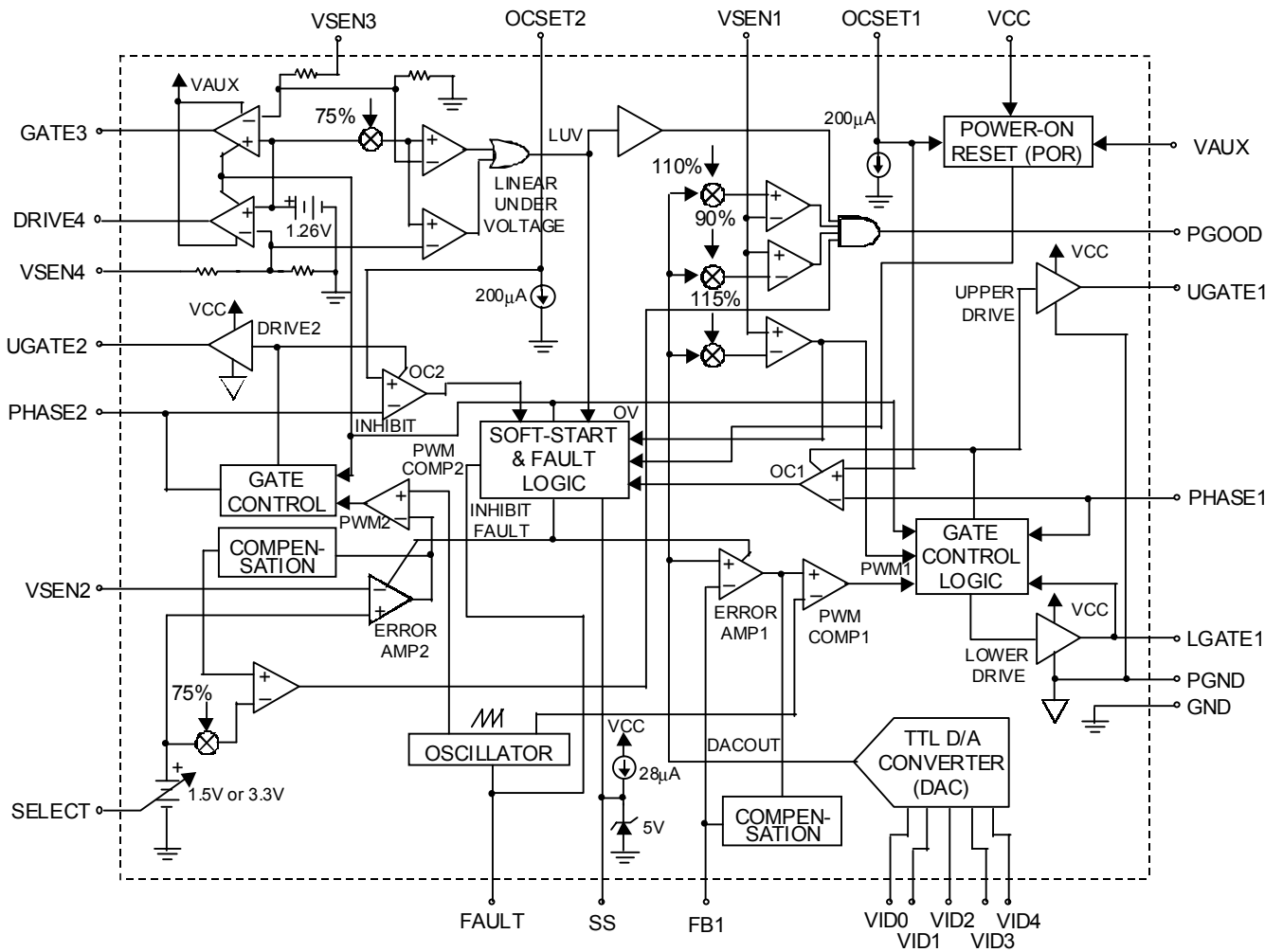
(V<sub>CC</sub> = 12V, PGND = 0V, T<sub>A</sub> = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
<b>VCC Supply Current</b>						
Nominal Supply Current	I <sub>CC</sub>	UGATE1, LGATE1, UGATE2, DRIVE3, and DRIVE4 Open	--	10	--	mA
<b>Power-on Reset</b>						
VCC Rising Threshold		V <sub>OCSET</sub> = 4.5V	7.5	--	9.5	V
VCC Falling Threshold		V <sub>OCSET</sub> = 4.5V	7	--	9	V
Rising VAUX Threshold		V <sub>OCSET</sub> = 4.5V	--	2.8	--	V
VAUX Threshold Hysteresis		V <sub>OCSET</sub> = 4.5V	--	0.5	--	V
Rising V <sub>OCSET1</sub> (and 2) Threshold			--	1.25	--	V
<b>Oscillator</b>						
Free Running Frequency			180	200	225	kHz
Ramp Amplitude	$\Delta V_{OSC}$		--	1.9	--	V <sub>P-P</sub>

*To be continued*

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
<b>DAC and Standard Buck Regulator Reference</b>						
DAC (VID0 ~ VID4) Input Low Voltage			--	--	0.8	V
DAC (VID0 ~ VID4) Input High Voltage			2	--	--	V
DACOUT Voltage Accuracy		DACOUT = 2.05 ~ 3.50V	-1	--	1	%
DACOUT Voltage Accuracy		DACOUT = 1.30 ~ 2.00V	-1%	--	20mV	--
AGP PWM Reference Voltage		SELECT < 0.8V	--	1.5	--	V
AGP PWM Reference Voltage		SELECT > 2.0V	--	3.3	--	V
AGP PWM Reference Voltage Tolerance			-2.5	--	2.5	%
<b>1.5V and 1.8V Linear Regulators (V<sub>OUT3</sub> and V<sub>OUT4</sub>)</b>						
Regulation			-3	--	3	%
VSEN3 Under-voltage Level		VSEN3 Rising	--	1.125	--	V
VSEN3 Under-voltage Hysteresis		VSEN3 Falling	--	100	--	mV
VSEN4 Under-voltage Level		VSEN4 Rising	--	1.350	--	V
VSEN4 Under-voltage Hysteresis		VSEN4 Falling	--	100	--	mV
Output Drive Current		VAUX = 5V	20	40	--	mA
<b>Synchronous PWM Controller Error Amplifier</b>						
DC Gain			--	65	--	dB
<b>PWM Controller Gate Driver</b>						
UGATE 1 (and 2) Source	R <sub>UGATE</sub>	VCC = 12V, VCC-V <sub>UGATE</sub> = 1V	--	4	7	Ω
UGATE 1 (and 2) Sink	R <sub>UGATE</sub>	V <sub>UGATE</sub> = 1V	--	3	7	Ω
LGATE Source	I <sub>LGATE1</sub>	VCC = 12V, V <sub>LGATE1</sub> = 2V	--	1	--	A
LGATE Sink	R <sub>LGATE1</sub>	V <sub>LGATE1</sub> = 1V	--	2	6	Ω
<b>Protection</b>						
VSEN1 Over-voltage (VSEN1/DACOUT)		VSEN1 Rising	112	115	120	%
FAULT Sourcing Current		V <sub>FAULT/RT</sub> = 2.0V	10	14	--	mA
OCSET1, 2 Current Source	I <sub>OCSET</sub>	V <sub>OCSET</sub> = 4.5V	170	200	230	μA
Soft-start Current	I <sub>SS</sub>		--	28	--	μA
<b>Power Good</b>						
V <sub>OUT1</sub> Upper Threshold		VSEN1 Rising	108	--	112	%
V <sub>OUT1</sub> Under Voltage		VSEN1 Rising	87	--	95	%
V <sub>OUT1</sub> Hysteresis (VSEN1/DACOUT)		Upper/Lower Threshold	--	2	--	%
PGOOD Voltage Low	V <sub>PGOOD</sub>	I <sub>PGOOD</sub> = -4mA	--	--	0.5	V

Function Block Diagram



## Functional Pin Description

### UGATE1, UGATE2 (Pins 27 and 1)

Connect UGATE pins to the respective PWM converter's upper MOSFET gate. This pin provides the gate drive for the upper MOSFETs.

### PHASE1, PHASE2 (Pins 26 and 2)

Connect the PHASE pins to the PWM converter's upper MOSFET source. These pins are used to monitor the voltage drop across the upper MOSFETs for over-current protection.

### VID0, VID1, VID2, VID3, VID4 (Pin 7, 6, 5, 4, and 3)

VID0-4 are TTL-compatible the input pins to the 5-bit DAC. The state logic of these five pins program the internal voltage reference, DACOUT. The level of DACOUT sets the microprocessor core converter output voltage, as well as the corresponding PGOOD and OVP thresholds. Table 1 specifies the DACOUT voltage of 32 combinations of VID levels.

### PGOOD (Pin 8)

PGOOD is an open collector output used to indicate the status of the PWM converter output voltage. This pin is pulled low when the synchronous regulator output is not within  $\pm 10\%$  of the DACOUT reference voltage, or when any of the other outputs are below their under-voltage thresholds. The PGOOD output is open for '11111' VID code.

### OCSET1, OCSET2 (Pins 23 and 9)

Connect a resistor ( $R_{OCSET}$ ) from this pin to the drain of the upper MOSFET.  $R_{OCSET}$ , an internal  $200\mu A$  current source ( $I_{OCSET}$ ), and the upper MOSFET on-resistance ( $R_{DS(ON)}$ ) set the converter over-current (OC) trip point according to the following equation:

$$I_{PEAK} = \frac{I_{OCSET} \times R_{OCSET}}{R_{DS(ON)}}$$

An over-current trip cycles the soft-start function.

The voltage at this pin is monitored for power-on reset (POR) purposes and pulling this pin low with an open drain device will shutdown the IC.

### VSEN2 (Pin 10)

Connect this pin to the output of the standard buck PWM regulator. The voltage at this pin is regulated to the level pre-determined by the logic-level status of the SELECT pin. This pin is also monitored by the PGOOD comparator circuit.

### SELECT (Pin 11)

This pin determines the output voltage of the AGP bus switching regulator. A low TTL input sets the output voltage to 1.5V while a high input sets the output voltage to 3.3V.

### SS (Pin 12)

Connect a capacitor from this pin to ground. This capacitor, along with an internal  $28\mu A$  ( $V_{SS} > 1V$ ) current source, sets the soft-start interval of the converter.

### FAULT (Pin 13)

This pin is low during normal operation, but it is pulled to about 8V ( $V_{CC} = 12V$ ) in the event of an over-voltage or over-current condition.

### VSEN4 (Pin 14)

Connect this pin to the output of the 1.8V regulator. This pin is monitored for under-voltage events.

### DRIVE4 (Pin 15)

Connect this pin to the gate of an external MOSEFT. This pin provides the drive for the 1.8V regulator's pass transistor.

### VAUX (Pin 16)

The +3.3V input voltage at this pin is monitored for power-on reset (POR) purpose. Connected to +5V input, this pin provides boost current for the two linear regulator output drives in the event bipolar NPN transistors (instead of N-channel MOSFETs) are employed as pass elements.

**GND (Pin 17)**

Signal ground for the IC. All voltage levels are measured with respect to this pin.

**DRIVE3 (Pin 18)**

Connect this pin to the gate of an external MOSEFT. This pin provides the drive for the 1.5V regulator's pass transistor.

**VSEN3 (Pin 19)**

Connect this pin to the output of the 1.5V linear regulator. This pin is monitored for under-voltage events.

**FB1 (Pin 21)**

The FB1 pin is the inverting input of the error amplifier.

**VSEN1 (Pin 22)**

This pin is connected to the PWM converter's output voltage. The PGOOD and OVP comparator circuits use the signal to report output voltage status and for over-voltage protection.

**PGND (Pin 24)**

This is the power ground of UGATE1, LGATE1, and UGATE2 connection. Tie the synchronous PWM converter's lower MOSFET source to this pin.

**LGATE1 (Pin 25)**

Connect LGATE to the PWM converter's lower MOSFET gate. This pin provides the gate drive for the lower MOSFET.

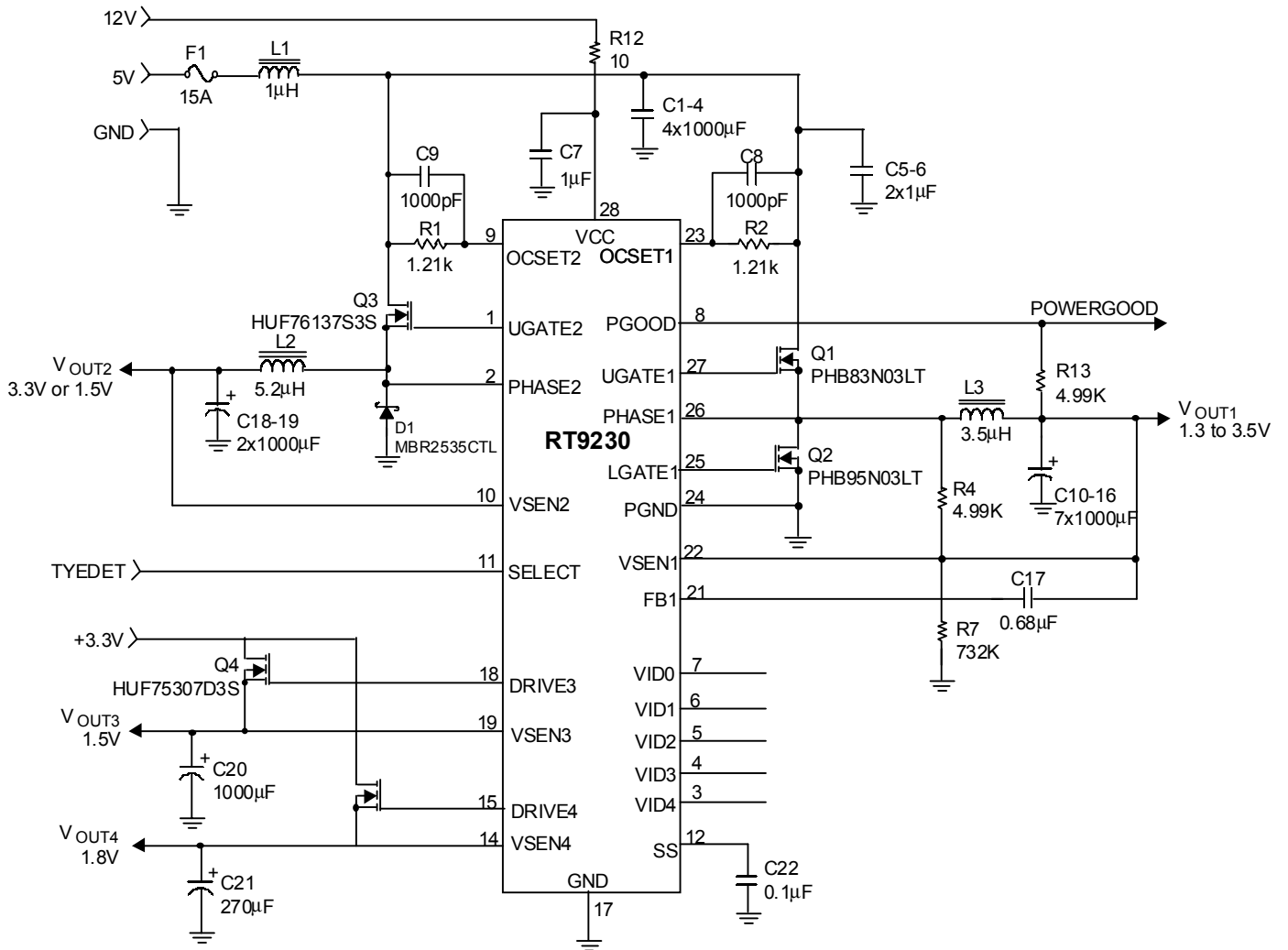
**VCC (Pin 28)**

Provide a 12V bias supply for the IC to this pin. This pin also provides the gate bias charge for all the MOSFETs controlled by the IC. The voltage at this pin monitored for power-on reset (POR) purpose.

**Table 1. VOUT1 Voltage Program**

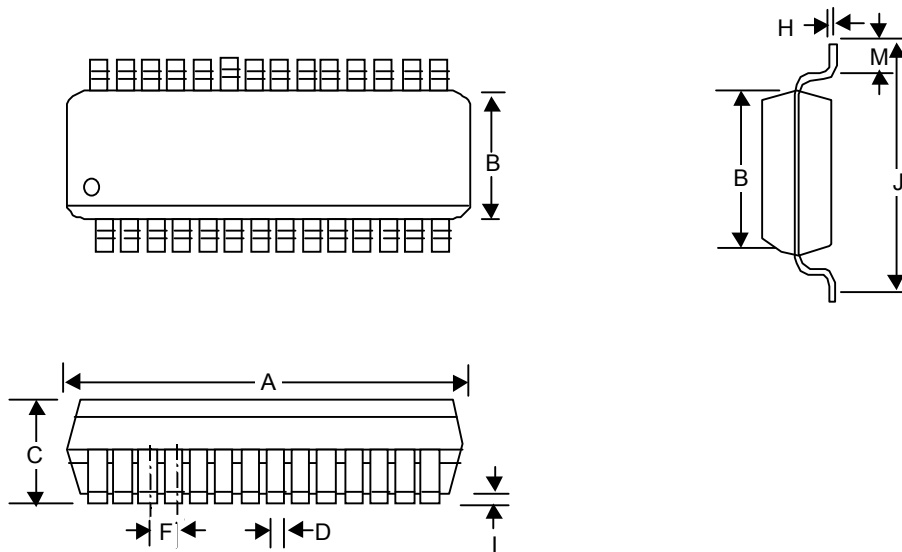
Pin Name					Normal OUT1 Voltage DACOUT
VID4	VID3	VID2	VID1	VID0	
0	1	1	1	1	1.30
0	1	1	1	0	1.35
0	1	1	0	1	1.40
0	1	1	0	0	1.45
0	1	0	1	1	1.50
0	1	0	1	0	1.55
0	1	0	0	1	1.60
0	1	0	0	0	1.65
0	0	1	1	1	1.70
0	0	1	1	0	1.75
0	0	1	0	1	1.80
0	0	1	0	0	1.85
0	0	0	1	1	1.90
0	0	0	1	0	1.95
0	0	0	0	1	2.00
0	0	0	0	0	2.05
1	1	1	1	1	INHIBIT
1	1	1	1	0	2.10
1	1	1	0	1	2.20
1	1	1	0	0	2.30
1	1	0	1	1	2.40
1	1	0	1	0	2.50
1	1	0	0	1	2.60
1	1	0	0	0	2.70
1	0	1	1	1	2.80
1	0	1	1	0	2.90
1	0	1	0	1	3.00
1	0	1	0	0	3.10
1	0	0	1	1	3.30
1	0	0	1	0	3.30
1	0	0	0	1	3.40
1	0	0	0	0	3.50

## Typical Application Circuit





**Package Information**



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	17.704	18.110	0.697	0.713
B	7.391	7.595	0.291	0.299
C	2.362	2.642	0.093	0.104
D	0.330	0.508	0.013	0.020
F	1.194	1.346	0.047	0.053
H	0.229	0.330	0.009	0.013
I	0.102	0.305	0.004	0.012
J	10.008	10.643	0.394	0.419
M	0.381	1.270	0.015	0.050

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