COMPUTER & PERIPHERAL COMPONENTS

IMP16C550A

Universal Asynchronous Receiver/Transmitter with FIFOs

General Description

The IMP16C550A UART (Universal Asynchronous Receiver/Transmitter) provides data communications capabilities for microprocessor-based systems including polled and interrupt driven environments. It converts data characters for transfer between a parallel CPU and a serial peripheral device (MODEM). The IMP16C550A provides this traditional 16450 UART functionality with two significant enhancements; it is updated to support complete compatibility with current state-of-the-art CPUs including the 80386, and it is improved to minimize software overhead requirements.

In addition to the IMP16450 mode (CHARACTER mode) which emulates the 16450 on powerup, the IMP16C550A supports a FIFO mode which provides access to 16 bytes of data storage in internal FIFOs for both receiver and transmitter functions. This built-in buffering capability minimizes the risk of receiver overrun and reduces system overhead in interrupt-driven applications. In addition, the RCVR FIFO provides 3 bits of error data storage per data byte. All control logic needed to fully utilize the added FIFO capabilities is integrated on the chip.

Built-in status reporting capabilities provide the CPU with a current status reading of the UART at any time during its operation. Accessible status information includes the type of transfer function in progress, operating conditions and error conditions (parity, overrun, framing or break interrupt). A processor-interrupt system allows for programmable interrupts, thus maximizing computing efficiency in the communications link. Plus, the MODEM control capability provides a complete range of control functions to address the serial devices.

The IMP16C550A has a 16× internal clock to synchronize transmitter logic and the receiver logic. The clock is generated by an on-chip programmable baud rate generator which can divide input from the timing reference clock by divisors ranging from 1 to (2^{16}–1).

The UART is fabricated using IMP's advanced MxCMOS 1.2 high density CMOS process to provide high performance with low power requirements. The IMP16C550A is available in either a 44-pin PLCC or a 40-pin DIP.

Features

- 100% 16450 software compatibility.
- Near pin-for-pin 16450 hardware compatibility. (CSOUT [24] and NC [29] have been changed to TXRDY and RXRDY, respectively, to allow the signalling of DMA transfers for FIFO mode operations.)
- Register set identical to the 16450 set upon power up or reset.
- 16-byte FIFO transmitter and receiver buffers.
- Holding and shift registers handle CPU to serial data synchronization (in IMP16C550A mode).
- Extensive MODEM control function set (CTS, RTS, DSR, DTR, RI and DCD).
- Independent controls for transmit, receive, line status and data set interrupts.
- TRI-STATE TTL drive for data and control buses.
- Asynchronous communication bits (start, stop and parity) programmable in serial data.
- Programmable serial-interface:
  - — variable character length (5, 6, 7 or 8 bits)
  - — Even, odd or no parity bit selection
  - — 1, 1.5 or 2 stop bit generation
  - — DC to 256K baud generation
- On-chip 16× clock.
- Internal programmable baud generator with a 1 to (2^{16}–1) divisor range.
- Independent receiver clock input.
- Line break generation and detection.
- Status reporting functions.
- False start bit detection.
- Internal diagnostics:
  - — Communications link fault isolation through loopback controls
  - — Error simulation (break, parity overrun and framing)
- System interrupt controls with prioritization.

Operation

The operation of the IMP16C550A consists of five major function areas: data bus buffering, operational control, interrupt control, timing generation and the communications link.

The Data Bus Buffer links the internal and external data buses. It is controlled by the UART's Select and Control Logic to enable data transfers between the device and the CPU.

The Select and Control Logic provides overall control of the UART operation. This logic block sends signals to various sections of the UART based on operating commands received from the CPU. Internal address decoding and read/write circuits enable communications with the microprocessor, and internal registers store configuration commands and device status.

The Interrupt Control System regulates interrupt output signal generation and is comprised of the Interrupt Control Logic, the Interrupt Enable Register and the Interrupt ID Register. An interrupt output signal may be sent to the CPU on the occurrence of any combination

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or subset of the following conditions: the transmit data holding register is empty, the received data holding register is full, the start or end of a received break is encountered, or the counter timeout is reached. The Interrupt ID Register tracks the current state of all the potential interrupt conditions, and the Interrupt Enable Register identifies the conditions selected to assert interrupt output; only conditions that have been enabled are recognized in determining interrupt signal output.

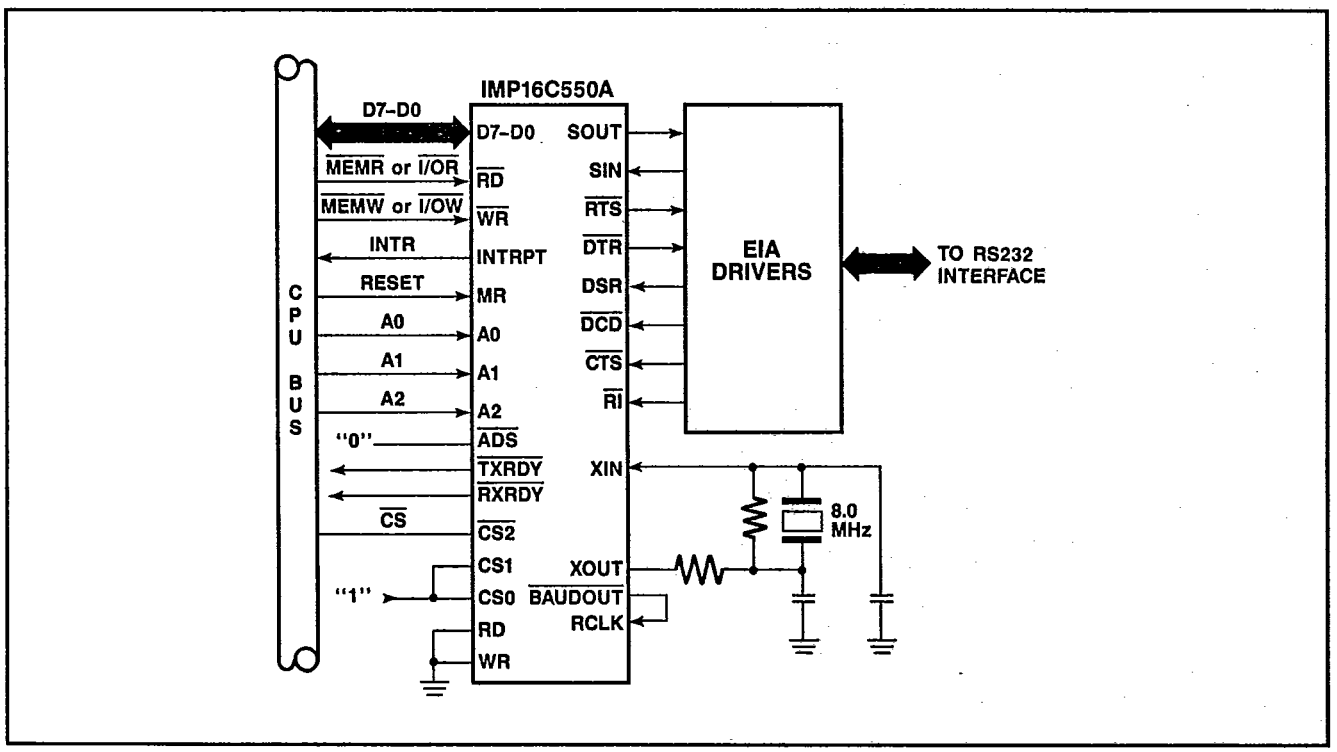
The UART system timing scheme utilizes an internal Programmable Baud Generator with variable divisor capability, and two 8-bit Divisor Latches to produce the on-chip 16× clock. This clock provides timing control for the transmitter. The receiver section of the UART accepts input from the external Receiver Clock pin.

Additionally, External Clock Input and Output pins allow a crystal oscillator or signal clock to be connected to the Control Logic block of the UART as the main timing reference.

The serial channel consists of an asynchronous transmitter and receiver providing the communication link between the CPU and the MODEM device, the serial data set or any serial peripheral emulating the MODEM.

The transmitter converts parallel data from the CPU into a serial bit stream. During this process, start, stop and optional parity bits are added to the data character as dictated by the asynchronous protocol. These same bits are verified by the receiver when it accepts serial data, before converting and reassembling the character for transmission to the CPU.

Basic Configuration



Absolute Maximum Ratings

Temperature Under Bias ..... 0°C to +70°C

Storage Temperature ..... -65°C to +150°C

All Input or Output Voltages with Respect to V_{SS} ..... -0.5V to +7.0V

Power Dissipation 1W

Note: *Maximum ratings indicate limits beyond which permanent damage may occur. Continuous operation at these limits is not intended and should be limited to those conditions specified under DC electrical characteristics.*

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DC Electrical Characteristics:

TA = 0°C to +70°C, V_{CC} = +5V ±5%, V_{SS} = 0V, unless otherwise specified.

Symbol	Parameter	Min.	Max.	Units	Conditions
V_{ILX}	Clock Input Low Voltage	-0.5	0.8	V	
V_{IHX}	Clock Input High Voltage	2.0	V_{CC}	V	
V_{IL}	Input Low Voltage	-0.5	0.8	V	
V_{IH}	Input High Voltage	2.0	V_{CC}	V	
V_{OL}	Output Low Voltage		0.4	V	I_{OL} = 1.6 mA on all (Note 1)
V_{OH}	Output High Voltage	2.4		V	I_{OH} = -1.0 mA (Note 1)
$I_{CC}(AV)$	Avg. Power Supply Current (V_{CC})		160 (Note 2)	mA	V_{CC} = 5.25V No loads on output SIN, DSR, DCD, CTS, RI = 2.0V All other inputs = 0.8V
			140 (Note 3)	mA	
I_{IL}	Input Leakage		±10	μA	V_{CC} = 5.25V, V_{SS} = 0V
I_{CL}	Clock Leakage		±10	μA	All other pins floating. V_{IN} = 0V, 5.25V
I_{OZ}	TRI-STATE Leakage		±20	μA	V_{CC} = 5.25V, V_{SS} = 0V V_{OUT} = 0V, 5.25V 1) Chip deselected 2) WRITE mode, chip selected
V_{ILMR}	MR Schmitt V_{IL}		0.8	V	
V_{IHMR}	MR Schmitt V_{IH}	2.0		V	

Notes:

1 Does not apply to XOUT
2 T_A = 25°C
3 T_A = 70°C

Capacitance: T_A = 25°C, V_{CC} = V_{SS} = 0V

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
C_{XIN}	Clock Input Capacitance		15	20	pF	f_c = 1 MHz Unmeasured pins returned to V_{SS}
C_{XOUT}	Clock Output Capacitance		20	30	pF	
C_{IN}	Input Capacitance		6	10	pF	
C_{OUT}	Output Capacitance		10	20	pF	

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AC Electrical Characteristics: T_A = 0°C to +70°C, V_{CC} = +5V ±5%

Symbol	Parameter	Min.	Max.	Units	Conditions
t_{ADS}	Address Strobe Width	60		ns	
t_{AH}	Address Hold Time	0		ns	
t_{AR}	$\overline{RD}$, RD Delay from Address	30		ns	(Note 1)
t_{AS}	Address Setup Time	60		ns	
t_{AW}	$\overline{WR}$, WR Delay from Address	30		ns	(Note 1)
t_{CH}	Chip Select Hold Time	0		ns	
t_{CS}	Chip Select Setup Time	60		ns	
t_{CSR}	$\overline{RD}$, RD Delay from Chip Select	30		ns	(Note 1)
t_{CSW}	$\overline{WR}$, WR Delay from Select	30		ns	(Note 1)
t_{DH}	Data Hold Time	30		ns	
t_{DS}	Data Setup Time	30		ns	
t_{HZ}	$\overline{RD}$, RD to Floating Data Delay	0	100	ns	@ 100 pF loading (Note 3)
t_{MR}	Master Reset Pulse Width	5		μs	
t_{RA}	Address Hold Time from $\overline{RD}$, RD	20		ns	(Note 1)
t_{RC}	Read Cycle Delay	125		ns	
t_{RCS}	Chip Select Hold Time from $\overline{RD}$, RD	20		ns	(Note 1)
t_{RD}	$\overline{RD}$, RD Strobe Width	125		ns	
t_{RDD}	$\overline{RD}$, RD to Driver Enable/Disable		60	ns	@ 100 pF loading (Note 3)
t_{RVD}	Delay from $\overline{RD}$, RD to Data		125	ns	@ 100 pF loading
t_{WA}	Address Hold Time from $\overline{WR}$, WR	20		ns	(Note 1)
t_{WC}	Write Cycle Delay	150		ns	
t_{WCS}	Chip Select Hold Time from $\overline{WR}$, WR	20		ns	(Note 1)
t_{WR}	$\overline{WR}$, WR Strobe Width	100		ns	
t_{XH}	Duration of Clock High Pulse	55		ns	External Clock (8.0 MHz Max.)
t_{XL}	Duration of Clock Low Pulse	55		ns	External Clock (8.0 MHz Max.)
RC	Read Cycle = $t_{AR} + t_{RD} + t_{RC}$	280		ns	(Note 4)
WC	Write Cycle = $t_{AW} + t_{WR} + t_{WC}$	280		ns	
Baud Generator					
N	Baud Divisor	1	$2^{16}-1$		
t_{BHD}	Baud Output Positive Edge Delay		175	ns	100 pF Load
t_{BLD}	Baud Output Negative Edge Delay		175	ns	100 pF Load
t_{HW}	Baud Output Up Time	75		ns	f_X = 8.0 MHz, ÷ 2, 100 pF Load
t_{LW}	Baud Output Down Time	100		ns	f_X = 8.0 MHz, ÷ 2, 100 pF Load

Notes:

1 Applicable only when $\overline{ADS}$ is tied low.

2 In the FIFO mode (FCR0 = 1) the trigger level interrupts, the receiver data available indication, the active RXRDY indication and the overrun error indication will be delayed 3 RCLKs. Status indicators (PE, FE, BI) will be delayed 3 RCLKs after the first byte has been received. For subsequently received bytes these indicators will be updated immediately after RDRBR goes inactive. Timeout interrupt is delayed 8 RCLKs.

3 Charge and discharge time is determined by V_{OL}, V_{OH} and the external loading.

4 in FIFO mode RC = 425 ns (minimum) between reads of the receiver FIFO and the status registers (interrupt identification register or line status register).

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AC Electrical Characteristics (continued)

Symbol	Parameter	Min.	Max.	Units	Conditions
Receiver					
t_{RINT}	Delay from $\overline{RD}$, RD (RD RBR/or RD LSR) to Reset Interrupt		1	µs	100 pF Load
t_{SCD}	Delay from RCLK to Sample Time		2	µs	
t_{SINT}	Delay from Stop to Set Interrupt		1	RCLK Cycles	(Note 2)
Transmitter					
t_{HR}	Delay from $\overline{WR}$, WR (WR THR) to Reset Interrupt		175	ns	100 pF Load
t_{IR}	Delay from $\overline{RD}$, RD (RD IIR) to Reset Interrupt (THRE)		250	ns	100 pF Load
t_{IRS}	Delay from Initial INTR Reset to Transmit Start	8	24	BAUDOUT Cycles	
t_{SI}	Delay from Initial Write to Interrupt	16	24	BAUDOUT Cycles	(Note 5)
t_{STI}	Delay from Stop to Interrupt (THRE)	8	8	BAUDOUT Cycles	(Note 5)
t_{SXA}	Delay from Start to TXRDY active		8	BAUDOUT Cycles	100 pF Load
t_{WXI}	Delay from Write TXRDY inactive		195	ns	100 pF Load
Modem Control					
t_{MDO}	Delay from $\overline{WR}$, WR (WR MCR) to Output		200	ns	100 pF Load
t_{RIM}	Delay to Reset Interrupt from $\overline{RD}$, RD (RD MSR)		250	ns	100 pF Load
t_{SIM}	Delay to Set Interrupt from MODEM Input		250	ns	100 pF Load

Notes:

1 Applicable only when $\overline{ADS}$ is tied low.

2 In the FIFO mode (FCR0 = 1) the trigger level interrupts, the receiver data available indication, the active RXRDY indication and the overrun error indication will be delayed 3 RCLKs. Status indicators (PE, FE, BI) will be delayed 3 RCLKs after the first byte has been received. For subsequently received bytes these indicators will be updated immediately after RDRBR goes inactive. Timeout interrupt is delayed 8 RCLKs.

3 Charge and discharge time is determined by V_{OL}, V_{OH} and the external loading.

4 in FIFO mode RC = 425 ns (minimum) between reads of the receiver FIFO and the status registers (interrupt identification register or line status register).

5 This delay will be lengthened by 1 character time, minus the last stop bit time if the transmitter interrupt delay circuit is active. (See FIFO Interrupt Mode Operation).

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Timing Waveforms (All timings are referenced to valid 0 and valid 1)

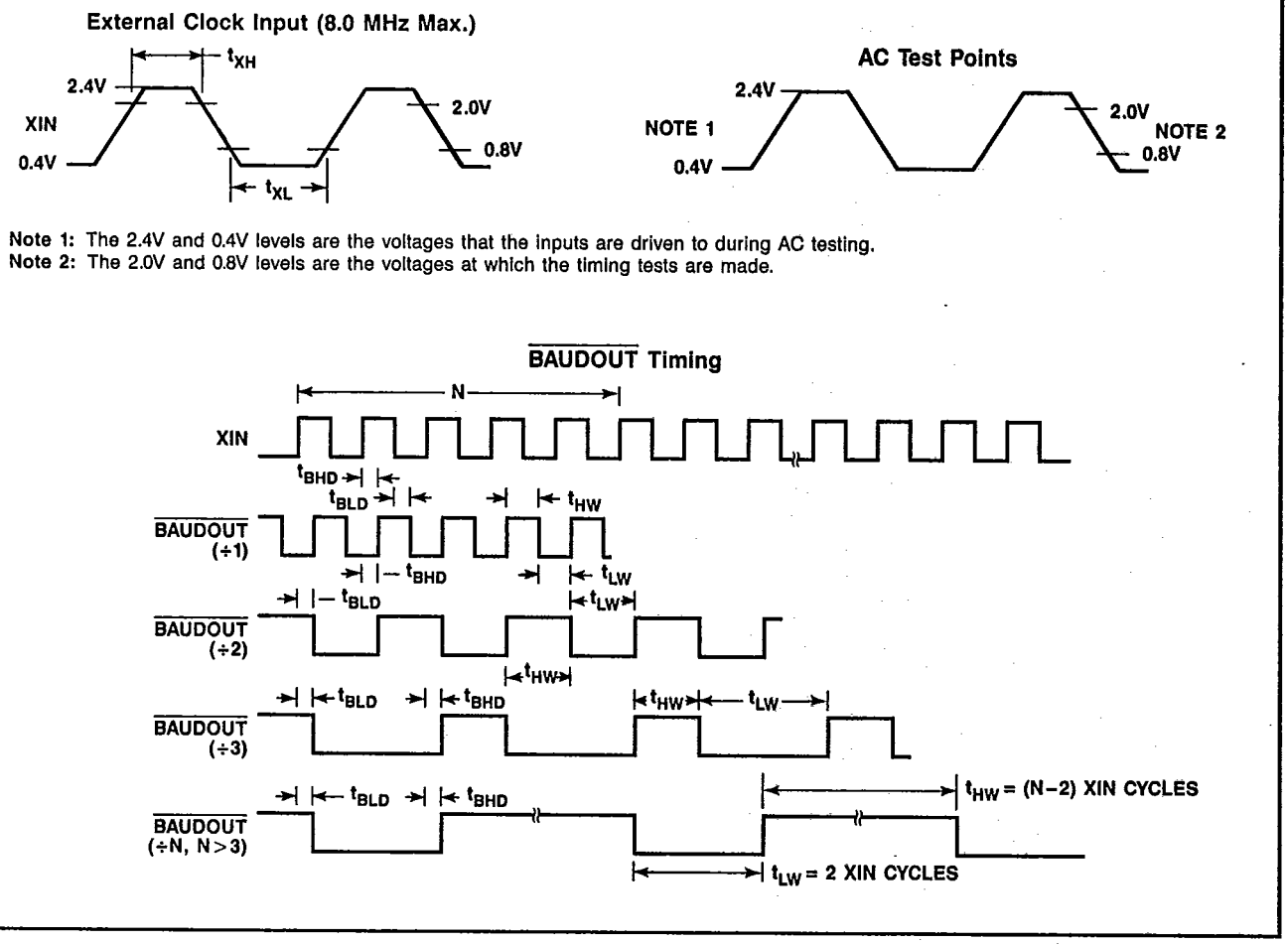

Figure 2. Timing Waveforms

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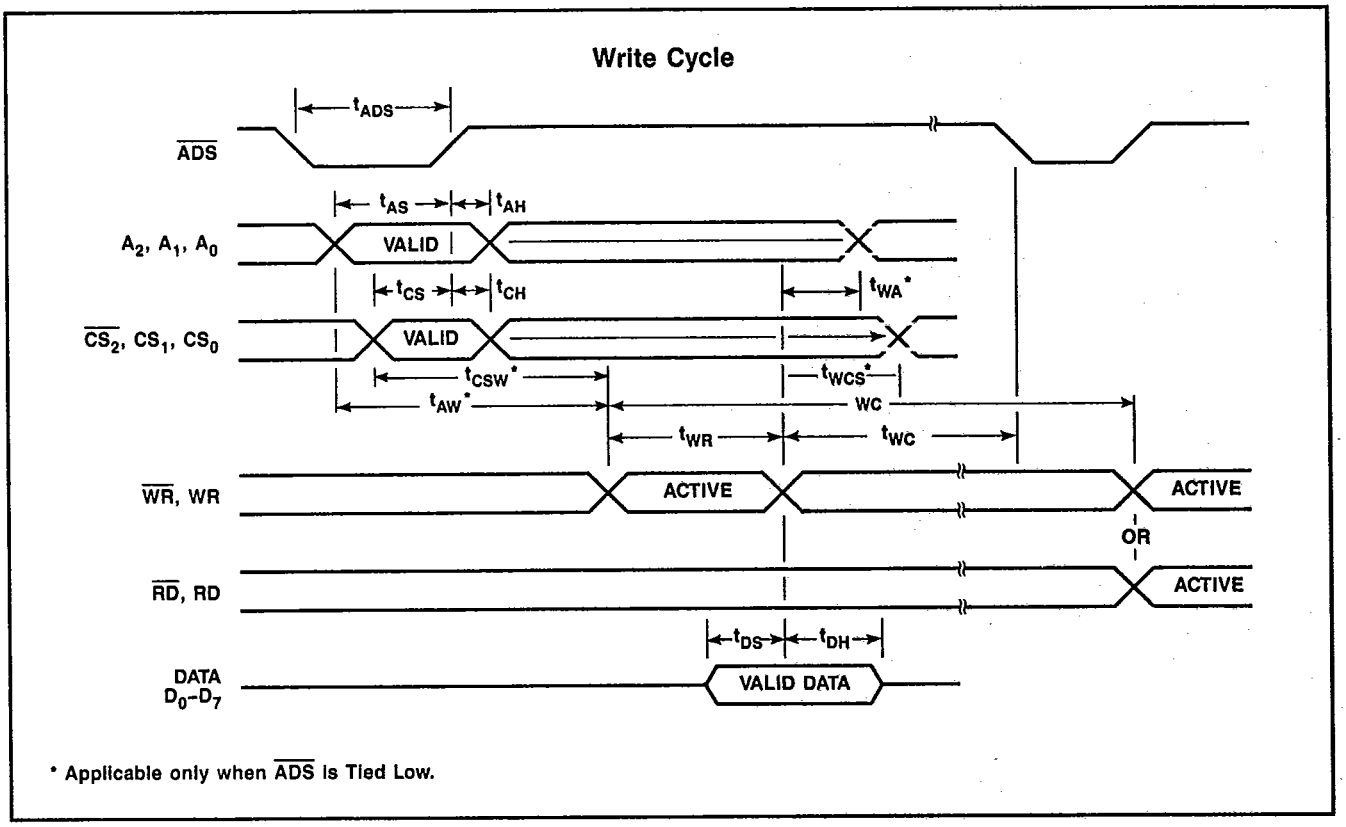

Figure 2. Timing Waveforms (continued)

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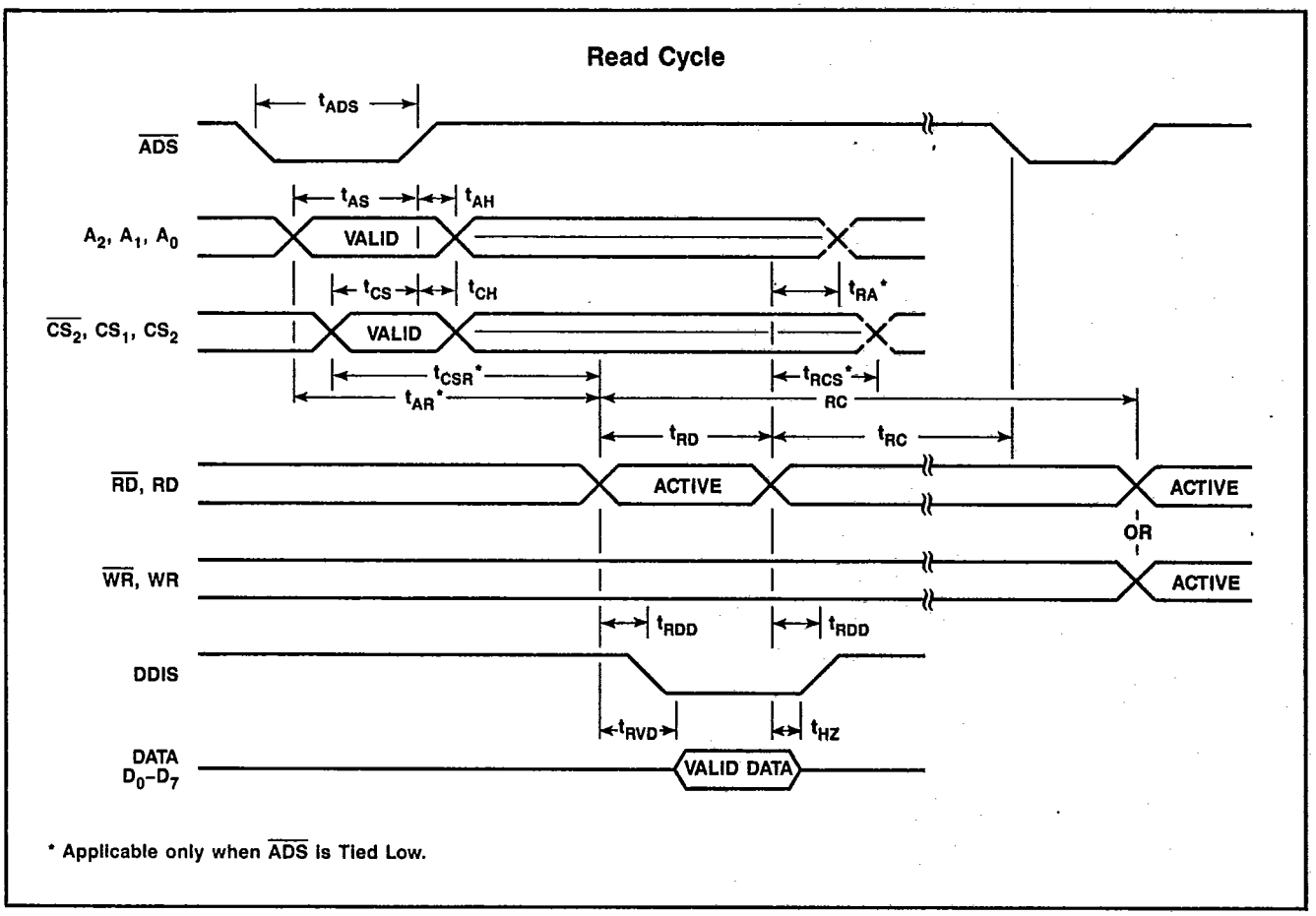

Figure 2. Timing Waveforms (continued)

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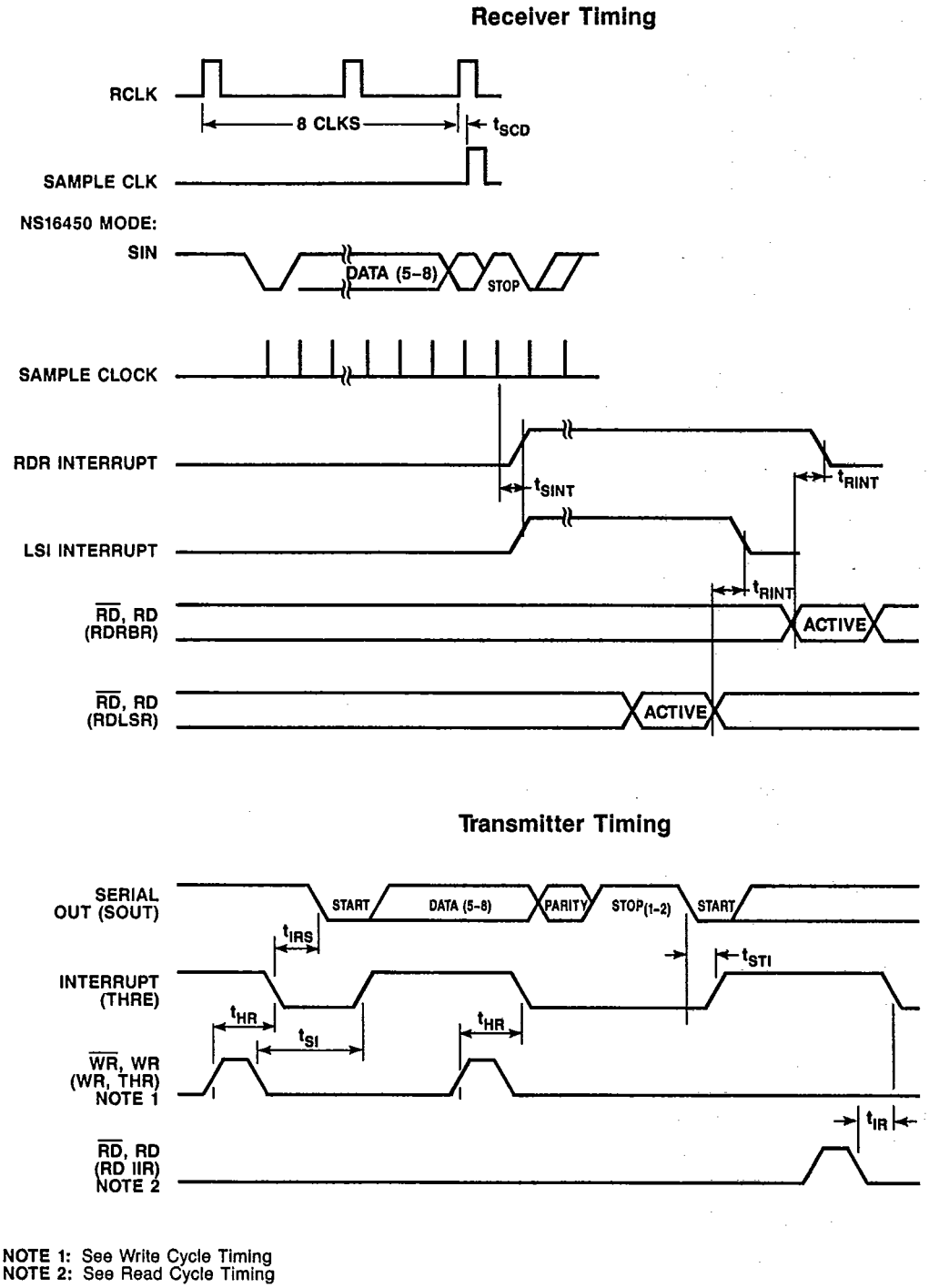

NOTE 1: See Write Cycle Timing
NOTE 2: See Read Cycle Timing

Figure 2. Timing Waveforms (continued)

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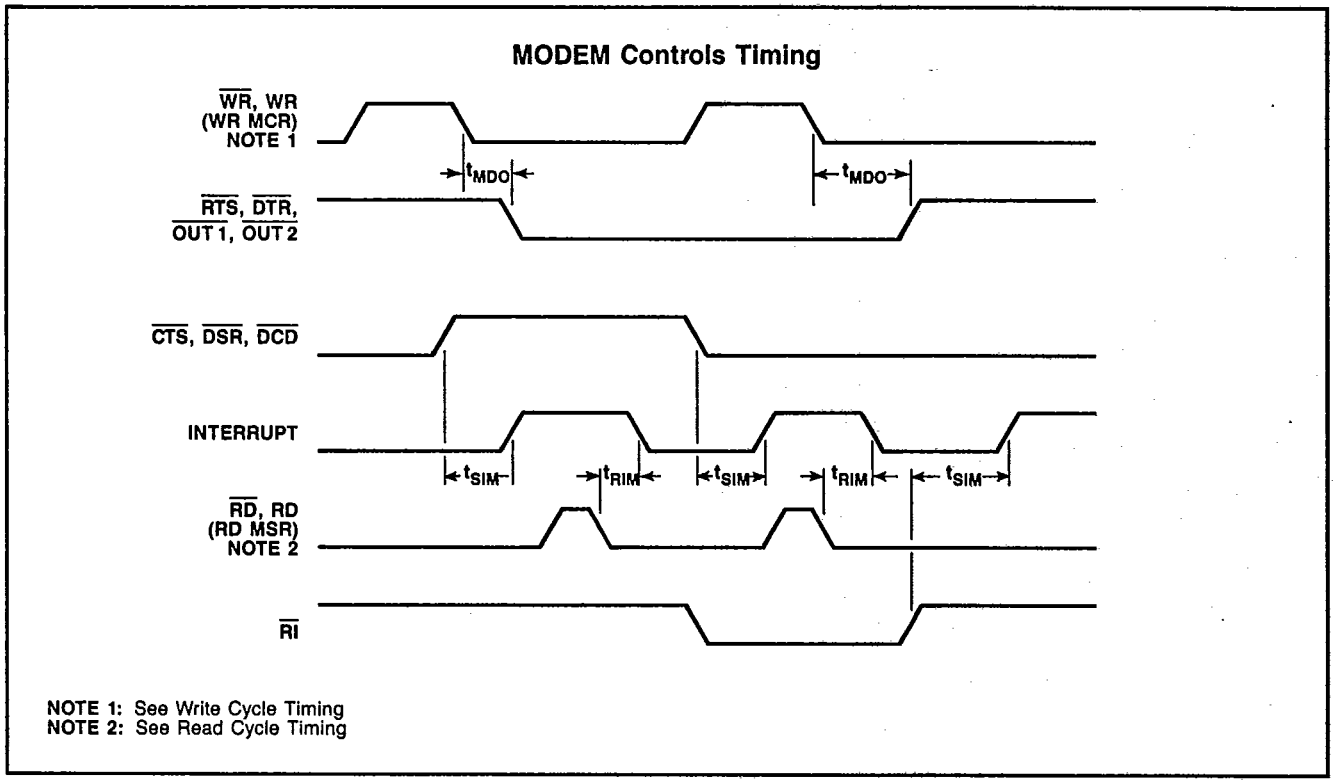

Figure 2. Timing Waveforms (continued)

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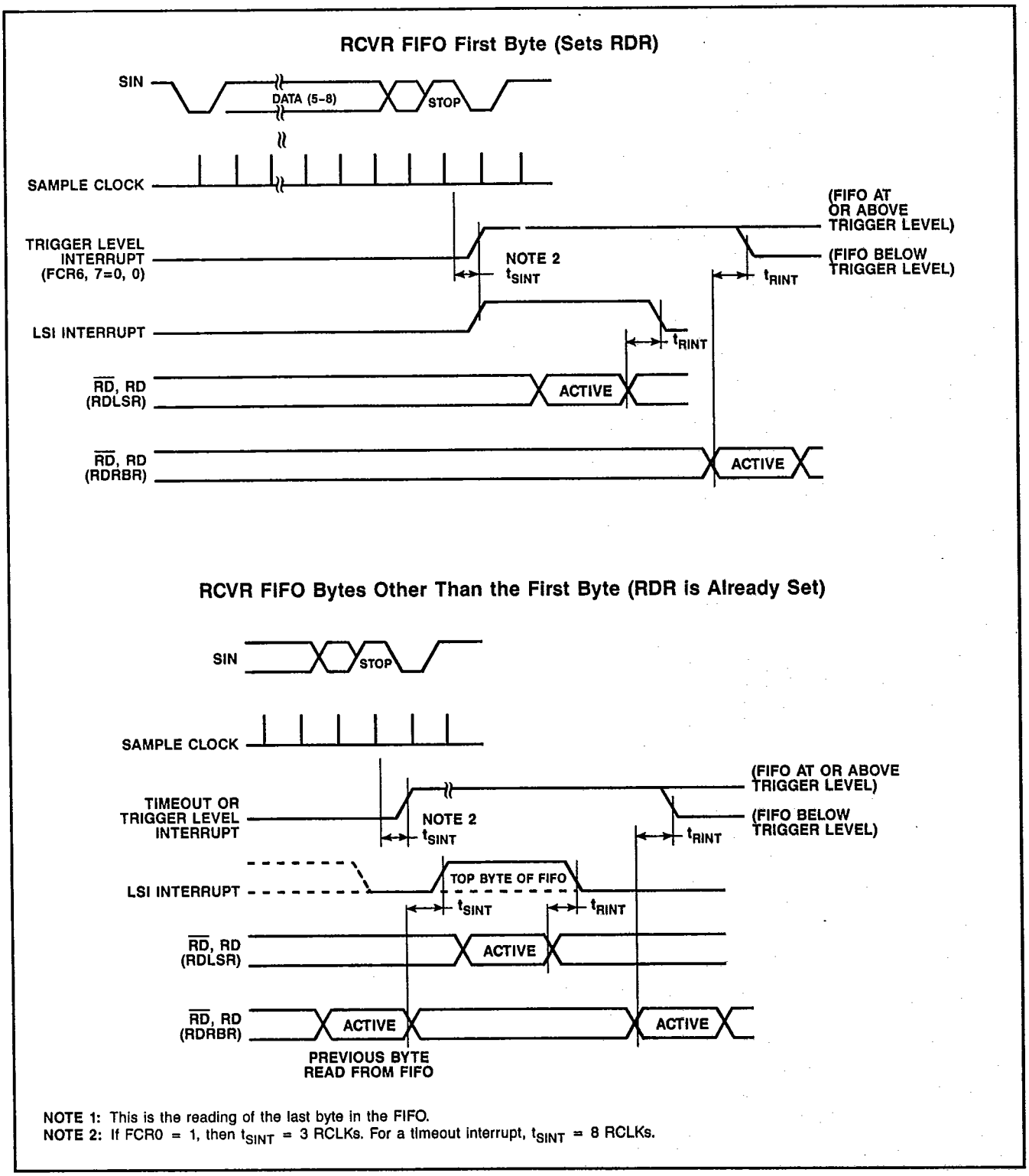

NOTE 1: This is the reading of the last byte in the FIFO.
NOTE 2: If FCR0 = 1, then t_{SINT} = 3 RCLKs. For a timeout interrupt, t_{SINT} = 8 RCLKs.

Figure 2. Timing Waveforms (continued)

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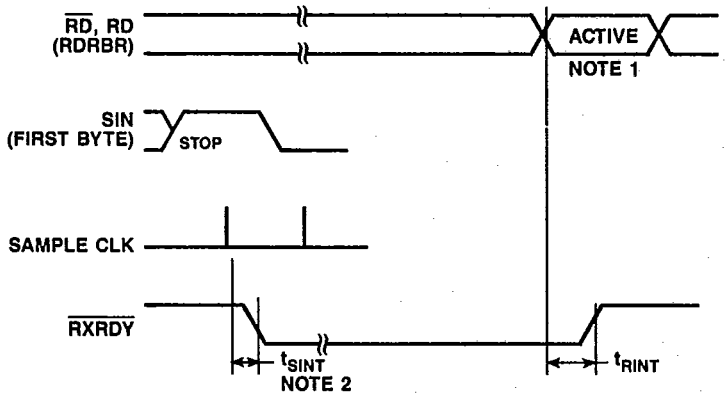
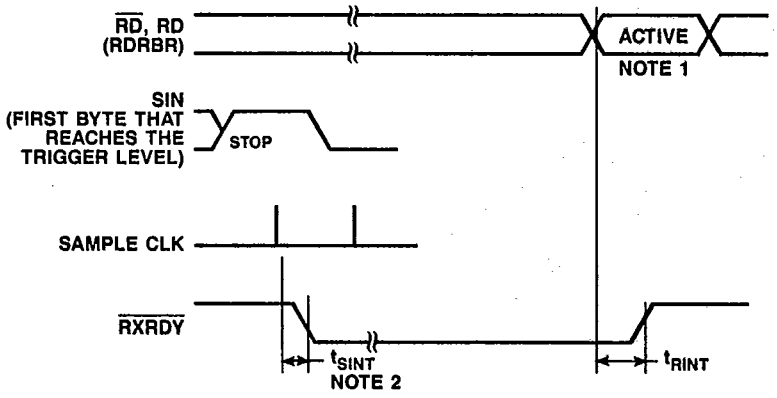
Receiver Ready (Pin 29) FCR0=0 or FCR0=1 and FCR3=0 (Mode 0)



Receiver Read (Pin 29) FCR0=1 and FCR3=1 (Mode 1)



NOTE 1: This is the reading of the last byte in the FIFO.
NOTE 2: If FCR0=1, then t_{SINT}=3 RCLKs. For a timeout interrupt, t_{SINT}=8 RCLKs.

Figure 2. Timing Waveforms (continued)

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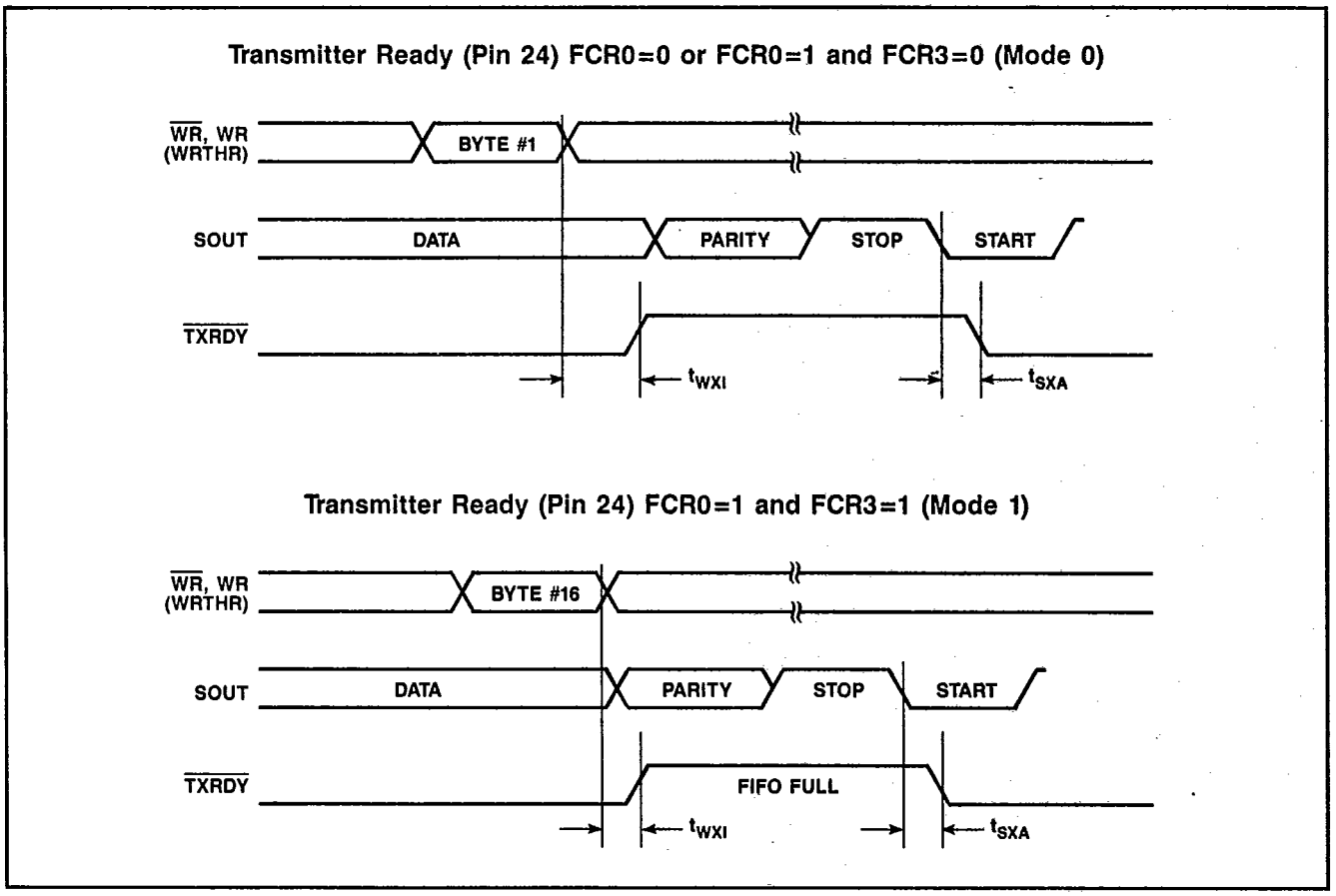

Figure 2. Timing Waveforms (continued)

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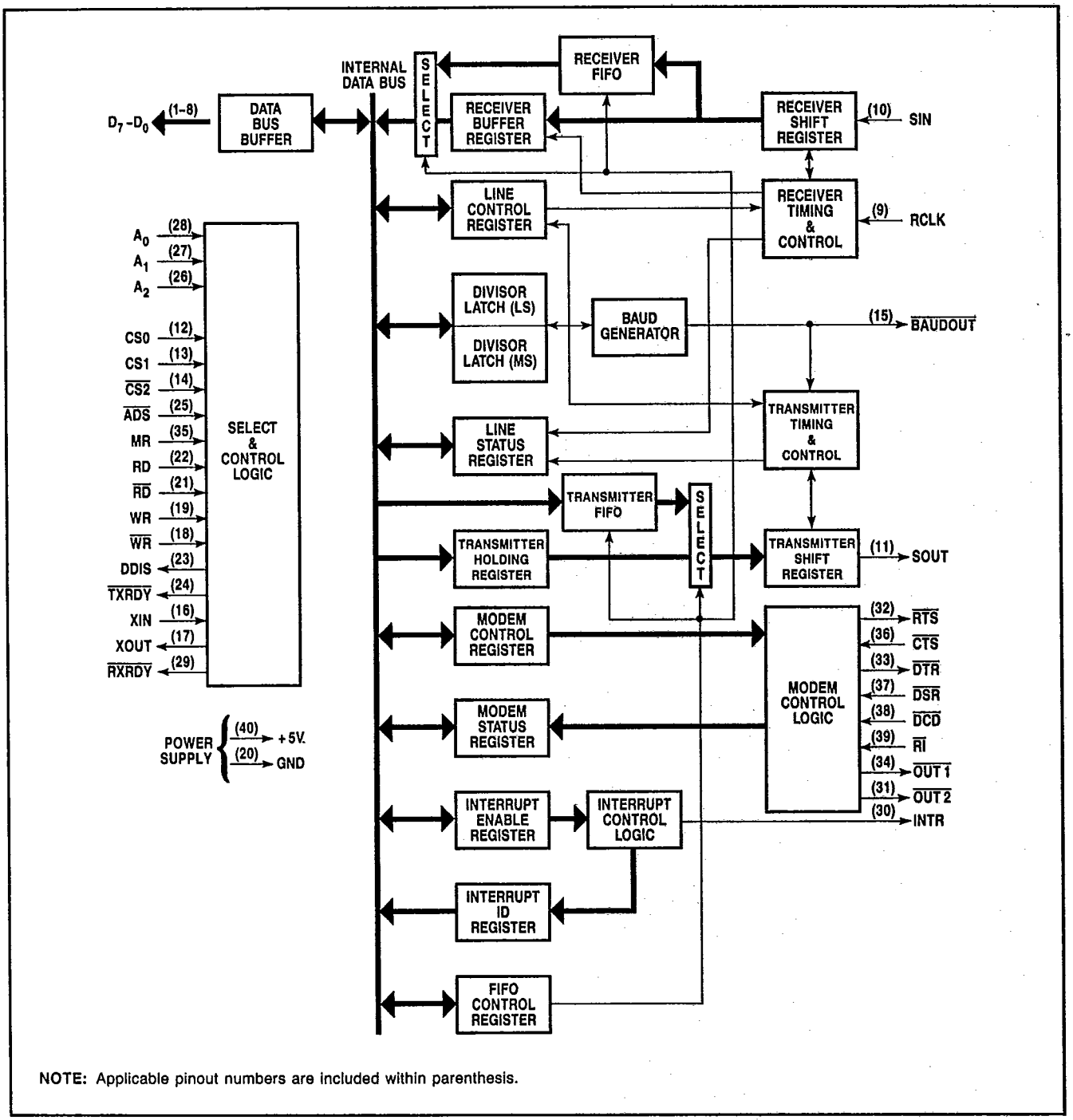
Block Diagram



NOTE: Applicable pinout numbers are included within parenthesis.

Figure 3. Block Diagram

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Pin Descriptions

All UART pins are discussed in the following descriptions with low referring to a logic 0 (0V nominal) and high referring to a logic 1 (+2.4V nominal). Also included in the descriptions are some references to internal circuits.

Input/Output Signals

Data Bus (D_7–D_0), Pins 1–8: Provides bi-directional communications between the CPU and UART. Eight TRI-STATE input-output lines carry data, control words and status information.

External Clock Input/Output (XIN, XOUT), Pins 16, 17: Connects the UART and the main timing reference (crystal or signal clock).

Input Signals

Chip Select (CS0, CS1, $\overline{CS2}$), Pins 12–14: Enables communication between the UART and the CPU. The chip is selected when CS0 and CS1 are high and $\overline{CS2}$ is low, with the chip selection completed when the positive edge of an active Address Strobe Signal ($\overline{ADS}$) latches the decoded chip select signals. For constantly low $\overline{ADS}$, the t_{CW} parameter dictates the stabilization of valid chip selects.

Read (RD, $\overline{RD}$), Pins 22, 21: Allows the transfer of status information or data from the selected UART register to the CPU. Transfer occurs when the chip is selected and when either RD is high or $\overline{RD}$ is low.

Note: When not in use, tie the RD input permanently low or the $\overline{RD}$ input permanently high. During a read, only an active RD or $\overline{RD}$ input enables data transfer from the UART.

Write (WR, $\overline{WR}$), Pins 19, 18: Allows the transfer of control words or data from the CPU to the selected UART register. Transfer occurs when the chip is selected and when either WR is high or $\overline{WR}$ is low.

Note: When not in use, tie the WR input permanently low or the $\overline{WR}$ input permanently high. During a write, only an active WR or $\overline{WR}$ input enables data transfer to the UART.

Address Strobe ($\overline{ADS}$), Pin 25: The positive edge of an active $\overline{ADS}$ signal provides a timing latch for the Register Select (A0, A1, A2) and Chip Select (CS0, CS1, CS2) signals.

Note: When not needed tie the $\overline{ADS}$ input permanently low. During a read or write operation, an active $\overline{ADS}$ input is required only if the Register Select (A0, A1, A2) signals are not stable.

Table 1. UART Reset Configuration

Register/Signal	Reset Control	Reset State
Interrupt Enable Register	Master Reset	**0000** 0000 (Note 1)
Interrupt Identification Register	Master Reset	**0000** 0001
FIFO Control	Master Reset	**0000** 0000
Line Control Register	Master Reset	0000 0000
MODEM Control Register	Master Reset	**0000** 0000
Line Status Register	Master Reset	0110 0000
MODEM Status Register	Master Reset	XXXX 0000 (Note 2)
SOUT	Master Reset	High
INTR (RCVR Errs)	Read LSR/MR	Low
INTR (RCVR Data Ready)	Read RBR/MR	Low
INTR (THRE)	Read IIR/Write THR/MR	Low
INTR (Modem Status Changes)	Read MSR/MR	Low
$\overline{OUT\ 2}$	Master Reset	High
$\overline{RTS}$	Master Reset	High
$\overline{DTR}$	Master Reset	High
$\overline{OUT\ 1}$	Master Reset	High
RCVR FIFO	MR/FCR1•FCR0/ΔFCR0	All Bits Low
XMIT FIFO	MR/FCR1•FCR0/ΔFCR0	All Bits Low

Notes:
1 Boldface bits are permanently low.
2 Bits 7–4 are driven by the input signals.

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Register Select (A0, A1, A2), Pins 26–28: Identifies a source or target UART register during data transfer. CPU read and write operations are directed to a select UART register by address signals connected to these inputs. The most significant bit of the Line Control Register is the Divisor Latch Access Bit (DLAB). The DLAB must be set high to enable the access of the Baud Generator Latches, and the state of the DLAB also affects the selection of certain other UART registers.

Register Addresses

DLAB	A_2	A_1	A_0	Register
0	0	0	0	Receiver Buffer (read), Transmitter Holding Register (write)
0	0	0	1	Interrupt Enable
X	0	1	0	Interrupt Identification (read)
X	0	1	0	FIFO Control (write)
X	0	1	1	Line Control
X	1	0	0	MODEM Control
X	1	0	1	Line Status
X	1	1	0	MODEM Status
X	1	1	1	Scratch
1	0	0	0	Divisor Latch (least significant byte)
1	0	0	1	Divisor Latch (most significant byte)

Master Reset (MR), Pin 35: Clears UART registers and control logic. Except for the Receiver Buffer Register, Transmitter Holding Register and two Divisor Latches, all UART registers and control logic are cleared when MR input is high. The input is buffered by a TTL-compatible Schmitt Trigger with 0.5V typical hysteresis.

Note: An active MR input affects the states of various output signals (SOUT, INTR, $\overline{OUT1}$, $\overline{OUT2}$, $\overline{RTS}$, $\overline{DTR}$). See Table 1.

Receiver Clock (RCLKC), Pin 9: Accepts input for the UART receiver section from the 16× baud rate clock.

Serial Input (SIN), Pin 10: Accepts serial data from the communications link (MODEM, peripheral device, or data set).

Clear to Send ($\overline{CTS}$), Pin 36: Signals MODEM or data set readiness for data exchange. $\overline{CTS}$ low indicates a ready state for data exchange. The $\overline{CTS}$ state reflects the condition of the MODEM status input which can be tested via bit 4 (CTS) of the MODEM Status Register (MSR). Bit 0 (DCTS) of the MSR tracks any change in the $\overline{CTS}$ input state since the last MSR reading. The $\overline{CTS}$ signal has no effect on the transmitter.

Note: Since it is the complement of the $\overline{CTS}$ signal, whenever CTS changes state, an interrupt is generated if the MODEM Status Interrupt is enabled.

Data Set Ready ($\overline{DSR}$), Pin 37: Signals MODEM or data set readiness for communications link. $\overline{DSR}$ low indicates a ready state for communications. The $\overline{DSR}$ state reflects the condition of the MODEM status input which can be tested via bit 5 (DSR) of the MODEM Status Register (MSR). Bit 1 (DDSR) of the MSR tracks any change in the $\overline{DSR}$ input state since the last MSR reading.

Note: Since it is the complement of the $\overline{DSR}$ signal, whenever DSR changes state, an interrupt is generated if the MODEM Status Interrupt is enabled.

Data Carrier Detect ($\overline{DCD}$), Pin 38: Signals data carrier acknowledgment. $\overline{DCD}$ low indicates detection of the data carrier by the MODEM or data set. The $\overline{DCD}$ state reflects the condition of the MODEM status input which can be tested via bit 7 (DCD) of the MODEM Status Register (MSR). Bit 3 (DDCD) of the MSR tracks any change in the $\overline{DSR}$ input state since the last MSR reading. The $\overline{DCD}$ signal has no effect on the Receiver.

Note: Since it is the complement of the $\overline{DCD}$ signal, whenever DCD changes state, an interrupt is generated if the MODEM Status Interrupt is enabled.

Ring Indicator ($\overline{RI}$), Pin 39: Signals telephone signal detection. $\overline{RI}$ low indicates that the MODEM or data set has received the telephone ringing signal. The $\overline{RI}$ state reflects the condition of the MODEM status input which can be tested via bit 6 (RI) of the MODEM Status Register (MSR). Bit 2 (TERI) of the MSR tracks any low to high state change in the $\overline{RI}$ input state since the last MSR reading.

Note: Since it is the complement of the $\overline{RI}$ signal, whenever RI changes state, an interrupt is generated if the MODEM Status Interrupt is enabled.

V_{CC}, Pin 40: +5V supply.

V_{SS}, Pin 20: Ground (0V) reference.

Output Signals

Data Terminal Ready ($\overline{DTR}$), Pin 33: Signals UART readiness for communications link. $\overline{DTR}$ can be set to active low indicating a ready state for communications with the MODEM or data set by programming bit 0 (DTR) of the MODEM Control Register to high.

Note: To set and hold $\overline{DTR}$ inactive, use Master Reset to reset the signal high and a Loop Mode operation to hold the state constant.

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Request to Send ($\overline{RTS}$), Pin 32: Signals UART readiness for data exchange. $\overline{RTS}$ can be set to active low indicating a ready state for data exchange with the MODEM or data set by programming bit 1 (RTS) of the MODEM Control Register to high.

Note: To set and hold $\overline{RTS}$ inactive, use Master Reset to reset the signal high and a Loop Mode operation to hold the state constant.

Output 1 ($\overline{OUT1}$), Pin 34: Use designated output. $\overline{OUT1}$ is set active low by programming bit 2 (OUT1) of the MODEM Control Register to high. In XMOS parts this achieves TTL levels.

Note: To set and hold $\overline{OUT1}$ inactive, use Master Reset to reset the signal high and a Loop Mode operation to hold the state constant.

Output 2 ($\overline{OUT2}$), Pin 31: User designated output. $\overline{OUT2}$ is set active low by programming bit 3 (OUT2) of the MODEM Control Register to high. In XMOS parts this achieves TTL levels.

Note: To set and hold $\overline{OUT2}$ inactive, use Master Reset to reset the signal high and a Loop Mode operation to hold the state constant.

Transmitter/Receiver DMA (TXRDY, RXRDY), Pins 24, 29: DMA mode 0, available in both IMP16C550A mode and FIFO mode, provides single transfer DMA with execution between CPU bus cycles. DMA mode 1, available only in FIFO mode, offers multitransfer DMA with continuous execution until either RCVR FIFO is empty or XMIT FIFO is filled.

RXRDY Mode 0: Accessible in IMP16C550A mode (FCR[0] = 0) or in FIFO mode (FCR[0] = 1, FSR[3] = 0). Whenever at least 1 character resides in the RCVR holding register or the RCVR FIFO, RXRDY (Pin 29) goes active with signal low. Once there is no data left in the FIFO or holding register, it goes inactive.

RXRDY Mode 1: Accessible only in FIFO mode (FCR[0] = 1). Whenever FCR[3] = 1 and the timeout or trigger level has been reached, RXRDY (Pin 29) goes active with signal low. Once there is no data left in the FIFO, it goes inactive.

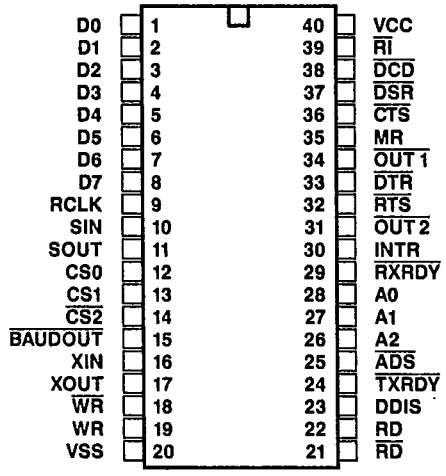
TXRDY Mode 0: Accessible in IMP16C550A mode (FCR[0] = 0) or in FIFO mode (FCR[0] = 1, FSR[3] = 0). Whenever there are no characters residing in the XMIT holding register or the XMIT FIFO, TXRDY (Pin 24) goes active with signal low. Once the first character is loaded into the in the FIFO or holding register, it goes inactive.

TXRDY Mode 1: Accessible only in FIFO mode (FCR[0] = 1). Whenever FCR[3] = 1 and there remains any unfilled position in XMIT FIFO, RXRDY (Pin 24) goes active with signal low. Once the FIFO becomes completely full, it goes inactive.

Driver Disable (DDIS), Pin 23: Controls or disables the direction of the data bus transceiver. While the CPU is reading data from the UART, DDIS goes active low.

Connection Diagrams

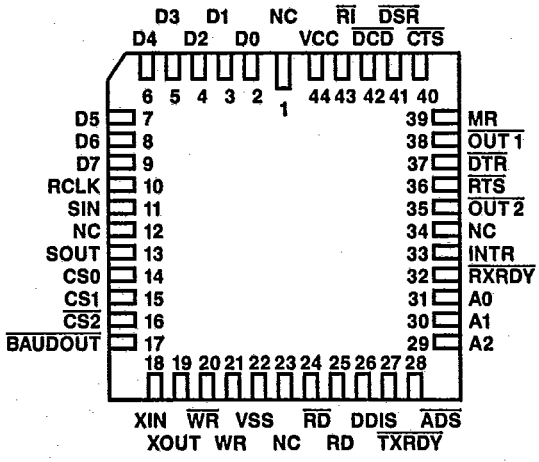
Dual-In-Line Package



Top View

Order Number IMP16550AD
See IMP Package Number N40A

Chip Carrier Package



Top View

Order Number IMP16550AP
See IMP Package Number V44A

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Baud Out (BAUDOUT), Pin 15: 16× clock signal. This clock rate is determined by the main reference oscillator frequency divided by the divisor specified in the Baud Generator Divisor Latches. Generated from the transmitter section of the UART, the BAUDOUT output may also be tied to the receiver section through the RCLK input.

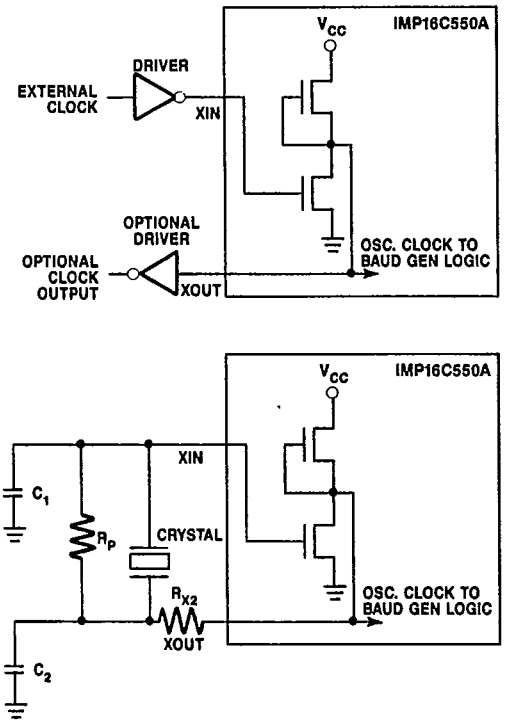
Interrupt (INTR), Pin 30: Signals interrupt conditions. INTR goes high in response to any of the following interrupt types activated via the Interrupt Enable Register: Receiver Error Flag, Received Data Available, Transmitter Holding Register Empty, MODEM Status and timeout (FIFO mode only). INTR is reset low by the appropriate interrupt service or by Master Reset.

Serial Output (SOUT), Pin 11: Composite serial output to the communication link (MODEM, peripheral or data set). SOUT is reset to the logic 1 Marking state by Master Reset.

Programming

The IMP16C550A supports two modes of operation in addition to the default 16450 Mode, all regulated and monitored through registers of the various UART timing, logic and control blocks. The functions enabling data transmission, data reception, and general UART operations are programmed by setting control sequences in the appropriate registers, and operational feedback is obtained by reading the status registers via the CPU.

Typical Clock Circuits



Programmable Baud Generator

The internal programmable Baud Generator drives the UART's internal 16× clock. It can divide any DC clock input up to 8MHz by a selected divisor between 1 and (2^{16}–1), resulting an output frequency of 16× the Baud.

The divisor value equals the frequency input divided by 16× the baud rate, and is stored in a 16-bit binary format in the two 8-bit Divisor Latches. During initialization, the Divisor Latches must be loaded for proper Baud Generator access and to activate the 16-bit Baud counter. When the divisor is 1, the maximum recommended input frequency is 4MHz. Setting the divisor to 0 is not recommended.

Tables 2, 3 and 4 provide decimal divisors to use with 1.8432 MHz, 3.072 MHz and 8 MHz crystal input frequencies. Minimal error is achieved when baud rates are kept under 38400.

Typical Crystal Oscillator Network

CRYSTAL	R_p	R_{X2}	C_1	C_2
3.1 MHz	1 MΩ	1.5k	10–30 pF	40–60 pF
1.8 MHz	1 MΩ	1.5k	10–30 pF	40–60 pF

Table 2. Baud Rates Using 1.8432 MHz Crystal

Desired Baud Rate	Decimal Divisor Used to Generate 16 × Clock	Percent Error Difference Between Desired and Actual
50	2304	—
75	1536	—
110	1047	0.026
134.5	857	0.058
150	768	—
300	384	—
600	192	—
1200	96	—
1800	64	—
2000	58	0.69
2400	48	—
3600	32	—
4800	24	—
7200	16	—
9600	12	—
19200	6	—
38400	3	—
56000	2	2.86

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Table 3. Baud Rates Using 3.072 MHz Crystal

Desired Baud Rate	Decimal Divisor Used to Generate 16 × Clock	Percent Error Difference Between Desired and Actual
50	3840	—
75	2560	—
110	1745	0.026
134.5	1428	0.034
150	1280	—
300	640	—
600	320	—
1200	160	—
1800	107	0.312
2000	96	—
2400	80	—
3600	53	0.628
4800	40	—
7200	27	1.23
9600	20	—
19200	10	—
38400	5	—

Table 4. Baud Rates Using 8 MHz Crystal

Desired Baud Rate	Decimal Divisor Used to Generate 16 × Clock	Percent Error Difference Between Desired and Actual
50	10000	—
75	6667	0.005
110	4545	0.010
134.5	3717	0.013
150	3333	0.010
300	1667	0.020
600	833	0.040
1200	417	0.080
1800	277	0.080
2000	250	—
2400	208	0.160
3600	139	0.080
4800	104	0.160
7200	69	0.644
9600	52	0.160
19200	26	0.160
38400	13	0.160
56000	9	0.790
128000	4	2.344
256000	2	2.344

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Table 5. Summary Registers

Bit No.	Register Address										
	0 DLAB=0	0 DLAB=0	1 DLAB=0	2	3	4	5	6	7	0 DLAB=1	1 DLAB=1
	Receiver Buffer Register (Read Only)	Transmitter Holding Register (Write Only)	Interrupt Enable Register	Interrupt Ident. Register (Read Only)	Line Control Register	MODEM Control Register	Line Status Register	MODEM Status Register	Scratch Register Register	Divisor Latch (LS)	Divisor Latch (MS)
	RBR	THR	IER	IIR	LCR	MCR	LSR	MSR	SCR	DLL	DLM
0	Data Bit 0 (Note 1)	Data Bit 0	Enable Received Data Available Interrupt (ERBFI)	"0" if Interrupt Pending	Word Length Select Bit 0 (WSL0)	Data Terminal Ready (DTR)	Data Ready (DR)	Delta Clear to Send (DCTS)	Bit 0	Bit 0	Bit 8
1	Data Bit 1	Data Bit 1	Enable Transmitter Holding Register Empty Interrupt (ETBEI)	Interrupt ID Bit (0)	Word Length Select Bit 1 (WLS1)	Request to Send (RTS)	Overrun Error (OE)	Delta Data Set Ready (DDSR)	Bit 1	Bite 1	Bit 9
2	Data Bit 2	Data Bit 2	Enable Receiver Line Status Interrupt (ELSI)	Interrupt ID Bit (1)	Number of Stop Bits (STB)	Out 1	Parity Error (PE)	Trailing Edge Ring Indicator (TERI)	Bit 2	Bit 2	Bit 10
3	Data Bit 3	Data Bit 3	Enable MODEM Status Interrupt (EDSSI)	Interrupt ID Bit (2) (Note 2)	Parity Enable (PEN)	Out 2	Framing Error (FE)	Delta Data Carrier Detect (DDCD)	Bit 3	Bit 3	Bit 11
4	Data Bit 4	Data Bit 4	0	0	Even Parity Select (EPS)	Loop	Break Interrupt (BI)	Clear to Send (CTS)	Bit 4	Bit 4	Bit 12
5	Data Bit 5	Data Bit 5	0	0	Stick Parity	0	Transmitter Holding Register (THRE)	Data Set Ready (DSR)	Bit 5	Bit 5	Bit 13
6	Data Bit 6	Data Bit 6	0	FIFOs Enabled (Note 2)	Set Break	0	Transmitter Empty (TEMT)	Ring Indicator (RI)	Bit 6	Bit 6	Bit 14
7	Data Bit 7	Data Bit 7	0	FIFOs Enabled (Note 2)	Divisor Latch Access Bit (DLAB)	0	Error in RCVR FIFO (Note 2)	Data Carrier Detect (DCD)	Bit 7	Bit 7	Bit 15
					RCVR Trigger (LSB)						
					RCVR Trigger (MSB)						
					Reserved						
					Reserved						
					XMIT FIFO Reset						
					RCVR FIFO Reset						
					FIFO Enable						

Note 1: Bit 0 is the least significant bit. It is the first bit serially transmitted or received.

Note 2: These bits are always 0 in the IMP16450 Mode.

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Registers

The UART registers are summarized in Table 5. More detailed discussion on the user-programmable registers is offered below. In the following descriptions, a low state refers to a logic 0 and a high state to a logic 1.

Line Control Register

The Line Control Register (LCR) allows direct system reading of its register contents, eliminating the need for separate system memory allocations for storing line characteristics. The LCR also provides direct programming access for setting the Divisor Latch Access bit and for specifying the format of the asynchronous data communications exchange.

Word Length Select Bits (WSL0, WSL1), Bits 0, 1: Indicate number of bits in each serial character transmitted or received. Bits 0 and 1 are encoded as follows:

Bit 1	Bit 0	Character Length
0	0	5 Bits
0	1	6 Bits
1	0	7 Bits
1	1	8 Bits

Number of Stop Bits (STB), Bit 2: Indicates number of stop bits transmitted and received in each serial character. Stop bits are generated as follows:

Bit 2	Character Length	Stop Bits Generated
0	any	1
1	5	1.5
1	6, 7 or 8	2

Note: The receiver only checks the first stop bit regardless of the number of stop bits selected.

Parity Enable (PEN), Bit 3: Controls parity bit generation and checking. The parity bit resides between the last data word bit and the stop bit of the serial data, and is summed with the data word bits to produce an even or odd number of 1s. When PEN is high, a parity bit is either generated during data transmission or checked during data receiving.

Even Parity Select (EPS), Bit 4: Controls parity bit and data word transmission and checking. EPS is active only when Parity Enable (LCR[3]) is high. When EPS is set low an odd number of 1s is transmitted and checked, and when set high an even number of 1s is transmitted and checked in the data word and parity bit.

Stick Parity, Bit 5: Controls the Parity bit value. Stick Parity is enabled only when both this bit and Parity Enable (LCR[3]) are high. Then, if Even Parity Select (LCR[4]) is low the parity bit is transmitted and checked as a logic 1, and if EPS is high the parity bit is transmitted and checked as a logic 0.

Break Control, Bit 6: Activates break condition transmission. Break Control is disabled when set to low. When it is set high, the Serial Output (SOUT) is forced to the spacing state (logic 0), and the break condition is transmitted to the receiving UART.

Note: The Break Control only affects SOUT and does not act on transmitter logic, so that during any break, the transmitter can be used to time the duration of that break.

Divisor Latch Access (DLAB), Bit 7: Selects latch and buffer access. During a read or write operation, DLAB allows access to the Divisor Latches of the Baud Generator if set high. If set low, access is available to the Receiver Buffer, Transmitter Holding Register or Interrupt Enable Register.

Line Status Register

The Line Status Register (LSR) displays status conditions for the CPU to monitor data transfer operations. This register is intended for read access only. Writing to the Line Status Register is not recommended outside of factory testing applications.

Data Ready (DR), Bit 0: Signals the completion of an incoming character transfer. DR is set high when an entire character is received and transferred to the Receiver Buffer Register or the FIFO. Reading all of the data in the Receiver Buffer Register or FIFO resets DR to low.

Overrun Error (OE), Bit 1: Signals a data transfer failure due to premature overwriting of received data by the next character. OE is set high when a character is transferred into the Receiver Buffer Register, eradicating the previous data before it was successfully read by the CPU. OE is reset to low after the CPU reads the entire contents of the LSR.

In FIFO mode the FIFO can be filled above the trigger level, but an Overrun Error is indicated to the CPU only if the FIFO is completely full and the shift register has received an entire character. The data in the shift register is then overwritten without being transferred to the FIFO.

Parity Error (PE), Bit 2: Signals a parity mismatch in the incoming character. PE set high indicates a discrepancy between the parity of received data and the parity selected by the Even Parity Select bit. It is reset to low after the CPU reads the entire contents of the LSR.

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In FIFO mode, a Parity Error identifies a selected character which resides at the top of the FIFO at the time that the error is signalled to the CPU.

Framing Error (FE), Bit 3: Signals an invalid stop bit in the incoming character. FE is set high if the final bit following the last data or parity bit is low (spacing level). In resynchronizing after a Framing Error, the UART attributes the framing error to the subsequent start bit and resamples the newly assigned start bit twice before reading the associated data bits. FE is reset to low after the CPU reads the entire contents of the LSR.

In FIFO mode, a Framing Error identifies a selected character which resides at the top of the FIFO at the time that the error is signalled to the CPU.

Break Interrupt (BI), Bit 4: Signals a prolonged spacing state condition. BI is set to high if the received data produces a spacing state (logic 0) which outlasts the full-word transmission time (the total transmission time of the Start bit + data bits + Parity + Stop bits). It is reset to low after the CPU reads the entire contents of the LSR.

In FIFO mode, a Break Interrupt identifies a selected character which resides at the top of the FIFO at the time that the error is signalled to the CPU. At the time of the break, one 0 character is written to the FIFO with character transfer resuming only after the serial input pin (SIN) returns to marking state and verifies the next start bit.

Note: If the Receiver Status Line Interrupt is enabled, error conditions signalled by LSR bits 1 through 4 activate an interrupt whenever the associated conditions occur.

Transmitter Holding Register Empty (THRE), Bit 5: Indicates UART readiness for new data transmission. THRE is set high when a character is read to the Transmitter Shift Register from the Transmitter Holding Register. When the Transmit Holding Register Empty Interrupt enable is also set high, the UART issues an interrupt to the CPU. THRE is reset to low when the CPU reads the contents of the Transmitter Holding Register.

In FIFO mode, THRE is set high when XMIT FIFO is empty, and reset to low after the first byte is written to the XMIT FIFO.

Transmitter Empty (TEMT), Bit 6: Indicates that transmitter registers contain no data. TEMT is set high when both the Transmitter Holding Register and the Transmitter Shift Register are empty, and is reset to low when a character has been written to either register.

In FIFO mode, TEMT is set high when both the transmitter FIFO and the shift register are empty.

Error in RCVR FIFO, Bit 7: In FIFO mode only, indicates unresolved parity error, framing error or break indication. This bit is set high if any one of these conditions is present, and is reset to low when all error conditions in the FIFO are cleared and when the CPU reads the entire contents of the LSR.

This bit remains at a constant low in IMP16450 mode.

FIFO Control Register

The FIFO Control Register (FCR) controls FIFO conditions and operations. It is a write-only register at the same location as the read-only Interrupt Identification Register.

FIFO Enable, Bit 0: Controls the XMIT FIFO and the RCVR FIFO. This enables both FIFOs when set high and clears the contents of both FIFOs when reset to low. All bytes from the FIFOs are also cleared when switching between IMP16450 mode and FIFO mode. In addition, when setting any other FIFO Control Register bits, this bit must be high.

RCVR FIFO Reset, Bit 1: Clears the RCVR FIFO. When set high, this bit clears all data from the RCVR FIFO, resets its counter logic to 0, and self clears the 1 written to this bit position. However, it leaves the shift register unchanged.

XMIT FIFO Reset, Bit 2: Clears the XMIT FIFO. When set high, this bit clears all data from the XMIT FIFO, resets its counter logic to 0, and self clears the 1 written to this bit position. However, it leaves the shift register unchanged.

DMA Mode Select, Bit 3: Activates RXRDY and TXRDY pins. If both this bit and FIFO Enable (FCR[0]) are set high, the RXRDY and TXRDY pins are toggled from mode 0 to mode 1.

Bits 4, 5: Reserved for future use.

RCVR Trigger (LSB, MSB), Bits 6, 7: Selects trigger levels for the RCVR FIFO interrupt as follows:

7	6	RCVR FIFO Trigger Level (Bytes)
0	0	01
0	1	04
1	0	08
1	1	14

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Interrupt Identification Register

The Interrupt Identification Register (IIR) prioritizes interrupts into four levels in order to minimize system software overhead. The IIR records these interrupt conditions which are prioritized in the order of: Receiver Line Status, Received Data Ready, Transmitter Holding Register Ready, and MODEM Status.

During CPU access to the IIR, all UART interrupts are frozen and queued according to priority. For the duration of the CPU access, the UART continues to record new interrupts but maintains its current status indication to the CPU until access is completed.

Interrupt Pending, Bit 0: Signals a pending interrupt in the prioritized interrupt environment. This bit set low indicates a pending interrupt for which the remaining data in IIR dictates the appropriate service routine. When this bit is high there is no pending interrupt.

Interrupt ID Bits 0 and 1, Bits 1, 2: Establish the highest priority interrupt pending in accordance with Table 6.

Interrupt ID Bit 2, Bit 3: In FIFO mode only, signals a pending timeout interrupt if both this bit and IIR Bit 2 are set high.

This bit 3 remains at a constant low in IMP16450 mode.

Bits 4, 5: These bits always remain at constant low.

FIFOs Enabled, Bit 6 and 7: These bits are always set to the same value as IIR Bit 0.

Interrupt Enable Register

The Interrupt Enable Register (IER) regulates five types of UART interrupts. Each interrupt has independent access to the interrupt output signal (INTR), and the entire UART interrupt system can be completely enabled

Table 6. Interrupt Control Functions

FIFO Mode Only	Interrupt Identification Register			Interrupt Set and Reset Functions			
Bit 3	Bit 2	Bit 1	Bit 0	Priority Level	Interrupt Type	Interrupt Source	Interrupt Reset Control
0	0	0	1	—	None	None	—
0	1	1	0	Highest	Receiver Line Status	Overrun Error or Parity Error or Framing Error or Break Interrupt	Reading the Line Status Register
0	1	0	0	Second	Received Data Available	Receiver Data Available or Trigger Level Reached	Reading the Receiver Buffer Register or the FIFO drops below the Trigger Level
1	1	0	0	Second	Character Timeout Indication	No characters have been removed from or input to the RCVR FIFO during the last 4 Char. times and there is at least 1 Char. in it during this time	Reading the Receiver Buffer Register
0	0	1	0	Third	Transmitter Holding Register Empty	Transmitter Holding Register Empty	Reading the IIR Register (if source of interrupt) or Writing into the Transmitter Holding Register
0	0	0	0	Fourth	MODEM Status	Clear to Send or Data Set Ready or Ring Indicator or Data Carrier Detect	Reading the MODEM Status Register

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or disabled by setting IER Bits 0 through 3 high or low, respectively. Disabled interrupts cannot be identified as active in the IIR or activate the INTR output signal. However, functions involving the Line Status and MODEM Status Registers, and all other system operations, are not affected by the condition of IER.

Enabled Received Data Available Interrupt (ERBFI), Bit 0: Enables the Received Data Available interrupt when set high.

In FIFO mode, when set high, ERBFI enables the timeout interrupts.

Enable Transmitter Holding Register Interrupt (ETBEI), Bit 1: Enables the Transmitter Holding Register interrupt when set high.

Enable Receiver Line Status Interrupt (ELSI), Bit 2: Enables the Receiver Status Line interrupt when set high.

Enable MODEM Status Interrupt (EMSI), Bit 3: Enables the MODEM Status interrupt when set high.

Bits 4–7: These bits always remain at constant low.

MODEM Control Register

The MODEM Control Register (MCR) regulates UART interface with the MODEM, a peripheral device emulating the MODEM, or the data set.

Data Terminal Ready (DTR), Bit 0: Controls the Data Terminal Ready ($\overline{DTR}$) output. Setting DTR high forces the $\overline{DTR}$ output to low, and resetting it to low forces the $\overline{DTR}$ output high.

Note: The polarity of the input at the MODEM or data set can be induced by applying the previous $\overline{DTR}$ output to an EIA inverting line driver (for example, the DS1488).

Request to Send (RTS), Bit 1: Controls the Request to Send ($\overline{RTS}$) output. Setting RTS high forces the $\overline{RTS}$ output low, and resetting it to low forces the $\overline{RTS}$ output high.

Out 1 (OUT1), Bit 2: Controls the user-defined Output 1 ($\overline{OUT1}$) signal. Setting OUT1 high forces the $\overline{OUT1}$ output low, and resetting it to low forces the $\overline{OUT1}$ output high.

Out 2 (OUT2), Bit 3: Controls the user-defined Output 1 ($\overline{OUT2}$) signal. Setting OUT2 high forces the $\overline{OUT2}$ output low, and resetting it to low forces the $\overline{OUT2}$ output high.

Loop, Bit 4: Enables diagnostic testing through a local loopback operation. Setting this bit high initiates a set of functions which provide the CPU with verification of the UART transmit and received data paths.

First, the transmitter Serial Output (SOUT) is set to the marking state (logic 1) and the receiver Serial Input (SIN) is disconnected. The data from the Transmitter Shift Register output is then looped back into the Receiver Shift Register input. The four MODEM Control inputs ($\overline{CTS}$, $\overline{DSR}$, $\overline{RI}$ and $\overline{DCD}$) are also disconnected and the four MODEM Control outputs ($\overline{DTR}$, $\overline{RTS}$, $\overline{OUT1}$ and $\overline{OUT2}$) are connected internally to the respective MODEM Control inputs. Finally, the MODEM Control output pins are forced into their inactive state (logic 1). In this mode, the data is immediately transmitted and received, allowing data path checking.

In this diagnostic mode, the interrupts are still controlled by the Interrupt Enable Register. The receiver and transmitter interrupt sources lie outside of this operation, so that those interrupts are normally functional. The MODEM Control Interrupts are also operational, but the interrupt sources reside in the lower four bits of the MODEM Control Register instead of in the MODEM Control Inputs for the duration of the diagnostic.

Bits 5–7: These bits always remain at constant low.

MODEM Status Register

The MODEM Status Register (MSR) monitors the current condition and record status changes in the control lines from the MODEM (or peripheral device) to the CPU.

The first four bits of this register indicate change information and are set high if the associated input from the MODEM changes state, and are reset to low when the CPU performs a read of the MODEM Status Register. In addition, a MODEM Status interrupt is generated whenever any of these bits are set high.

Delta Clear to Send (DCTS), Bit 0: Signals any status change in the $\overline{CTS}$ input to the UART since the last CPU read operation.

Delta Data Set Ready (DDSR), Bit 1: Signals any status change in the $\overline{DSR}$ input to the UART since the last CPU read operation.

Trailing Edge of Ring (TERI), Bit 2: Signals any status change from high to low in the $\overline{RI}$ input to the UART since the last CPU read operation.

Delta Data Carrier Detect (DDCD), Bit 3: Signals any status change in the $\overline{DCD}$ input to the UART since the last CPU read operation.

Clear to Send (CTS), Bit 4: Denotes the complement of the Clear to Send input ($\overline{CTS}$). When the MSR Loop bit (bit 4) is set high, this bit takes on the value of the RTS in the MCR.

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Data Set Ready (DSR), Bit 5: Denotes the complement of the Data Set Ready input ($\overline{DSR}$). When the MSR Loop bit (bit 4) is set high, this bit takes on the value of the DTR in the MCR.

Ring Indicator (RI), Bit 6: Denotes the complement of the Ring Indicator input ($\overline{RI}$). When the MSR Loop bit (bit 4) is set high, this bit takes on the value of the OUT1 in the MCR.

Data Carrier Detect (DCD), Bit 7: Denotes the complement of the Data Carrier Detect input ($\overline{DCD}$). When the MSR Loop bit (bit 4) is set high, this bit takes on the value of the OUT2 in the MCR.

Scratchpad Register

The Scratchpad Register (SCR) provides an 8-bit read/write register of temporary data storage for programming use. It does not control the UART operations in any way.

Interrupt and Poll Mode Operations

FIFO Interrupt Mode Operation is activated in FIFO mode by setting both FIFO Enable (FCR[0]) and Enable Received Data Available Interrupt (IER[1]) high. RCVR FIFO and receiver interrupts are also enabled. In this mode, RCVR interrupts will be generated under the following conditions.

Both the Receive Data Available interrupt and the IIR Receive Data Available indicator are issued when the FIFO reaches its programmed trigger level, and cleared when the FIFO drops below its programmed trigger level.

The Data Ready Bit (LSR[0]) is activated immediately when a character is written from the shift register to the RCVR FIFO, and reset when the FIFO is empty. And as in IMP16450 mode, the Receiver Line Status interrupt (IIR[6]) holds higher priority than the Received Data Available interrupt (IIR[4]).

With enabled RCVR FIFO and receiver interrupts in FIFO mode, RCVR FIFO timeout generation will comply with the following conditions.

First FIFO timeout will occur only in conjunction with three conditions: the FIFO contains at least one character, the most current serial character received is longer than 4 continuous character times ago (with the second stop bit included in this time delay if 2 stop bits are detected), and the most current CPU read of the FIFO is longer than 4 continuous character times ago. This induces a delay of 160 ms at 300 BAUD to be issued by the maximum character received using a 12-bit character.

Also, to make delay proportional to the baud rate, the RCLK input must be used for a clock signal in calculating character times.

Following a timeout interrupt, the timeout timer is reset and the interrupt is cleared after the CPU reads the first character from the RCVR FIFO. Similarly, in the absence of a timeout interrupt the timeout timer is reset after a new character is received or after the CPU reads the entire RCVR FIFO.

In FIFO mode, the XMIT FIFO and transmitter interrupts are enabled. Also in this mode, XMIT interrupts will be generated under the following conditions.

The transmit holding interrupt (02) is issued when the XMIT FIFO is empty. While servicing this interrupt, 1 to 16 characters may be written to the XMIT FIFO. The interrupt is cleared when the CPU writes to the transmitter holding register or reads the IIR.

If the current state of THRE is high and there have not been at least two bytes at the same time in the transmit FIFO since the last time THRE was high, the transmitter FIFO empty indications will be delayed 1 character time minus the last stop bit time. And when enabled, the first transmitter interrupt after changing FCR0 will be immediate.

Priority classifications for Character Timeout and RCVR FIFO trigger-level interrupts are the same as those for the current Received Data Available interrupt. When empty, XMIT FIFO holds the same priority level as the current THRE interrupt.

FIFO Polled Mode Operation is implemented when FIFO Enable (FCR[1]) is high and all IER bits are reset to 0. Because the receiver and transmitter are independently controlled, either, both or neither the receiver and transmitter can be in the polled mode operation at any time.

In Polled Mode Operation, the LSR enables software checking of the receiver and transmitter. Specifically, LSR[0] remains set as long as RCVR FIFO contains a full byte of data, LSR[1] through LSR[4] provide error signalling, LSR[6] indicates when both the XMIT FIFO and shift register are empty, and LSR[7] signals any errors in RCVR FIFO. Character error servicing is the same as in the interrupt mode and the IIR is not affected since the Enable Transmitter Holding Register Empty interrupt (IER[2]) is low.

RCVR and XMIT FIFOs are completely able to store characters although FIFO Polled Mode does not support trigger level reached or timeout condition indicators.

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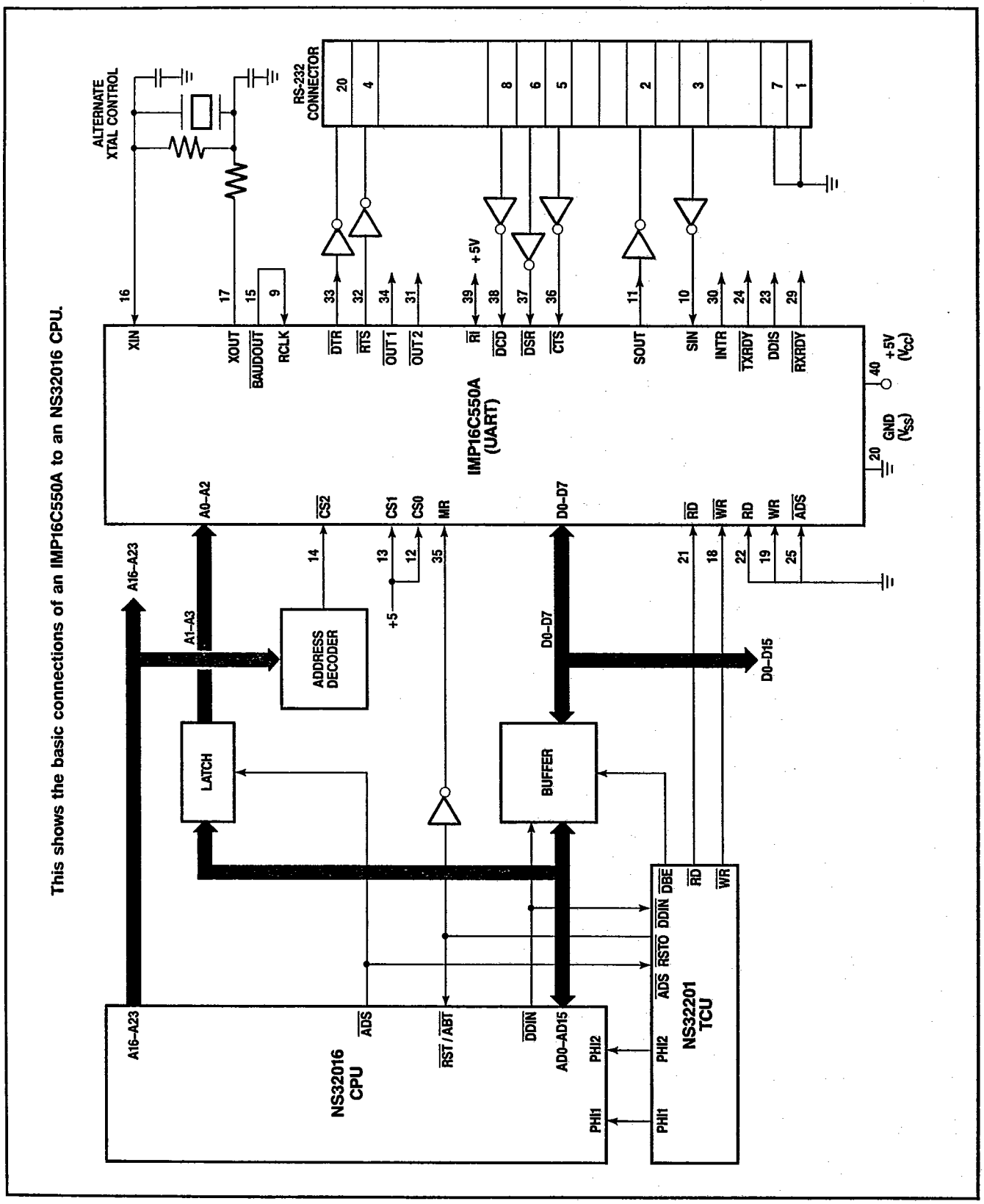

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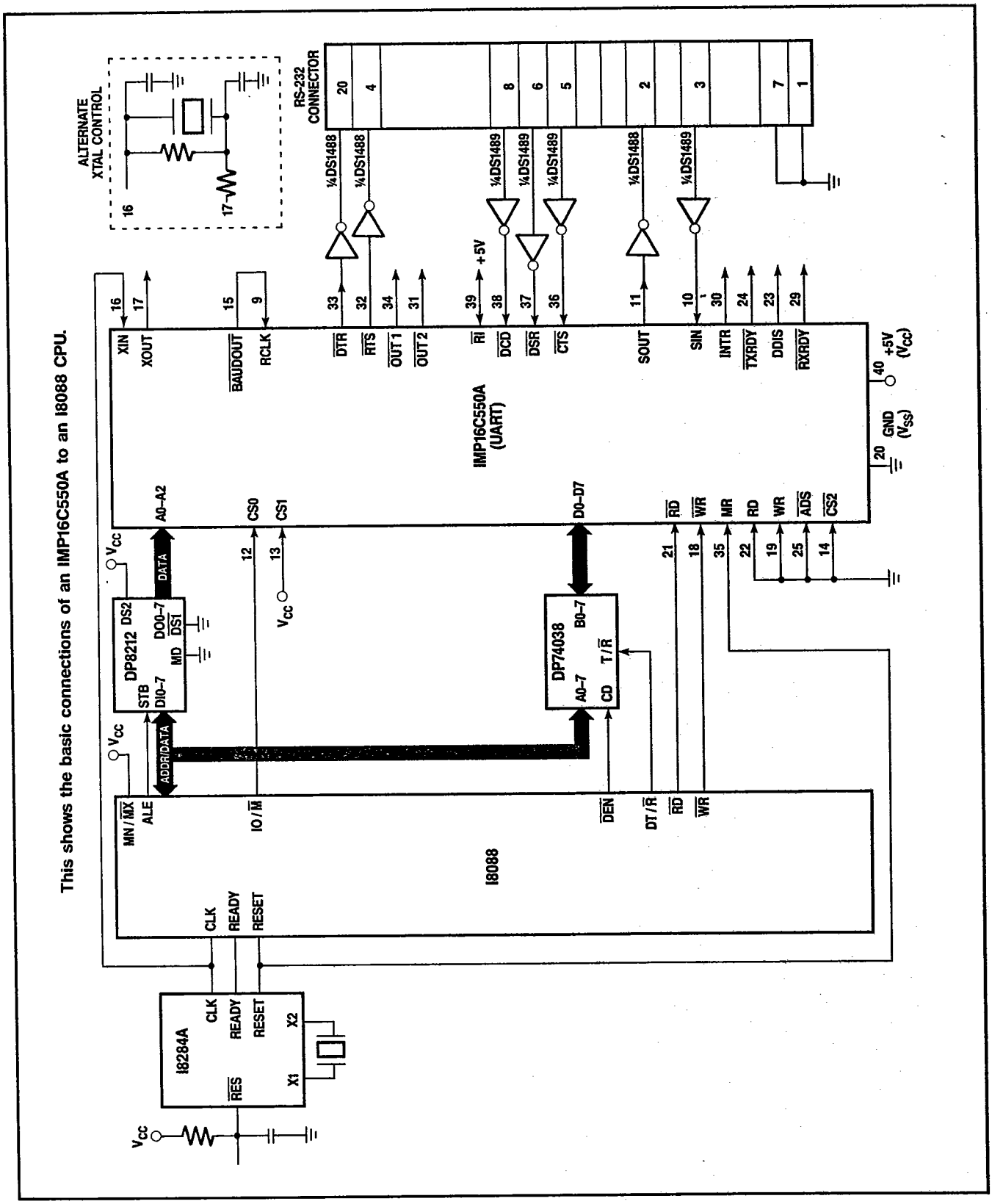

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