500 MHz, Linear-in-dB VGA with AGC Detector

AD8367

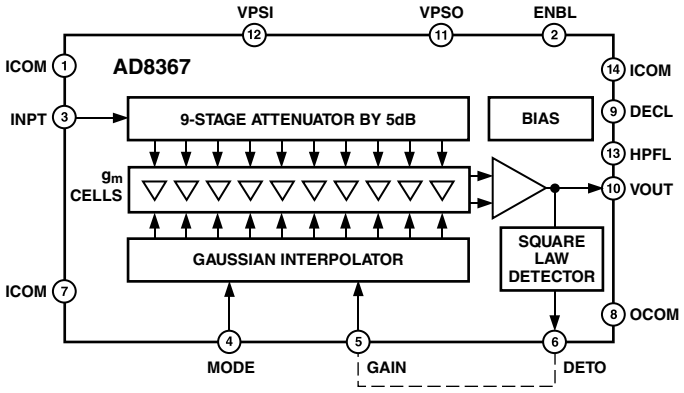
FEATURES

Broad Range Analog Variable Gain
–2.5 dB to +42.5 dB
3 dB Cutoff Frequency of 500 MHz
Gain Up and Gain Down Modes
Linear-in-dB, Scaled 20 mV/dB
Resistive Ground Referenced Input
Nominal Z_{IN} = 200 Ω
On-Chip Square-Law Detector
Single-Supply Operation: 2.7 V to 5.5 V

APPLICATIONS

Cellular Base Station
Broadband Access
Power Amplifier Control Loops
Complete, Linear IF AGC Amplifiers
High-Speed Data I/O

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD8367 is a high-performance 45 dB variable gain amplifier with linear-in-dB gain control for use from low frequencies up to several hundred megahertz. The range, flatness, and accuracy of the gain response are achieved using Analog Devices' X-AMP® architecture, the most recent in a series of powerful proprietary concepts for variable gain applications, which far surpasses what can be achieved using competing techniques.

The input is applied to a 200 Ω resistive ladder network, having nine sections each of 5 dB loss, for a total attenuation of 45 dB. At maximum gain, the first tap is selected; at progressively lower gains, the tap moves smoothly and continuously toward higher attenuation values. The attenuator is followed by a 42.5 dB fixed gain feedback amplifier—essentially an operational amplifier with a gain bandwidth product of 100 GHz—and is very linear, even at high frequencies. The output third order intercept is +20 dBV at 100 MHz (+27 dBm re 200 Ω), measured at an output level of 1 V p-p with V_S = 5 V.

The analog gain-control interface is very simple to use. It is scaled at 20 mV/dB, and the control voltage, V_{GAIN}, runs from 50 mV at –2.5 dB to 950 mV at +42.5 dB. In the inverse-gain mode of operation, selected by a simple pin-strap, the gain decreases from +42.5 dB at V_{GAIN} = 50 mV to –2.5 dB at V_{GAIN} = 950 mV. This inverse mode is needed in AGC applications, which are supported by the integrated square-law detector, whose set point is chosen to level the output to 354 mV rms, regardless of the waveshape. A single external capacitor sets up the loop averaging time.

The AD8367 may be powered on or off by a voltage applied to the ENBL pin. When this voltage is at a logic LO, the total power dissipation drops to the milliwatt range. For a logic HI, the chip powers-up rapidly to its normal quiescent current of 26 mA at 25°C. The AD8367 is available in a 14-lead TSSOP package for the industrial temperature range of –40°C to +85°C.

REV. 0

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AD8367—SPECIFICATIONS

(V_S = 5 V, T_A = 25°C, System Impedance Z_O = 200 Ω, V_{MODE} = 5 V, f = 10 MHz, unless otherwise noted.)

Parameter	Conditions	Min	Typ	Max	Unit
OVERALL FUNCTION					
Frequency Range		LF		500	MHz
GAIN Range			45		dB
INPUT STAGE	Pins INPT and ICOM				
Maximum Input	To Avoid Input Overload		700		mV p-p
Input Resistance	From INPT to ICOM	175	200	225	Ω
GAIN CONTROL INTERFACE	Pin GAIN				
Scaling Factor	V_{MODE} = 5 V, 50 mV ≤ V_{GAIN} ≤ 950 mV		+20		mV/dB
	V_{MODE} = 0 V, 50 mV ≤ V_{GAIN} ≤ 950 mV		–20		mV/dB
Gain Law Conformance	100 mV ≤ V_{GAIN} ≤ 900 mV		±0.2		dB
Maximum Gain	V_{GAIN} = 0.95 V		+42.5		dB
Minimum Gain	V_{GAIN} = 0.05 V		–2.5		dB
V_{GAIN} Step Response	From 0 dB to 30 dB		300		ns
	From 30 dB to 0 dB		300		ns
Small Signal Bandwidth	V_{GAIN} = 0.5 V		5		MHz
OUTPUT STAGE	Pin VOUT				
Max Output Voltage Swing	R_L = 1 kΩ		4.3		V p-p
	R_L = 200 Ω		3.5		V p-p
Output Source Resistance	Series Resistance of Output Buffer		50		Ω
Output Centering Voltage[1]			V_S/2		V
SQUARE LAW DETECTOR	Pin DETO				
Output Set Point			354		mV rms
AGC Small Signal Response Time	C_{AGC} = 100 pF, 6 dB Gain Step		1		µs
POWER INTERFACE	Pins VPSI, VPSO, ICOM, and OCOM				
Supply Voltage		2.7		5.5	V
Total Supply Current	ENBL High, Maximum Gain, R_L = 200 Ω (Includes Load Current)		26	30	mA
Disable Current vs. Temperature	ENBL Low		1.3	1.6	mA
	–40°C ≤ T_A ≤ +85°C			1.8	mA
MODE CONTROL INTERFACE	Pin MODE				
Mode LO Threshold	Device in Negative Slope Mode of Operation		1.2		V
Mode HI Threshold	Device in Positive Slope Mode of Operation		1.4		V
ENABLE INTERFACE	Pin ENBL				
Enable Threshold			2.5		V
Enable Response Time	Time Delay Following LO to HI Transition until Device Meets Full Specifications.		1.5		µs
Enable Input Bias Current	ENBL at 5 V		27		µA
	ENBL at 0 V		32		nA

Parameter	Conditions	Min	Typ	Max	Unit
f = 70 MHz					
Gain	Maximum Gain		+42.5		dB
	Minimum Gain		–3.7		dB
Gain Scaling Factor			19.9		mV/dB
Gain Intercept			–5.6		dB
Noise Figure	Maximum Gain		6.2		dB
Output IP3	f1 = 70 MHz, f2 = 71 MHz, V_{GAIN} = 0.5 V		27.5		dBm
			20.5		dBV rms
Output 1 dB Compression Point	V_{GAIN} = 0.5 V		8.5		dBm
			1.5		dBV rms
f = 140 MHz					
Gain	Maximum Gain		+43.5		dB
	Minimum Gain		–3.6		dB
Gain Scaling Factor			19.7		mV/dB
Gain Intercept			–5.3		dB
Noise Figure	Maximum Gain		7.4		dB
Output IP3	f1 = 140 MHz, f2 = 141 MHz, V_{GAIN} = 0.5 V		24.5		dBm
			17.5		dBV rms
Output 1 dB Compression Point	V_{GAIN} = 0.5 V		8.4		dBm
			1.4		dBV rms
f = 190 MHz					
Gain	Maximum Gain		+43.5		dB
	Minimum Gain		–3.8		dB
Gain Scaling Factor			19.6		mV/dB
Gain Intercept			–5.3		dB
Noise Figure	Maximum Gain		7.5		dB
Output IP3	f1 = 190 MHz, f2 = 191 MHz, V_{GAIN} = 0.5 V		23.9		dBm
			16.9		dBV rms
Output 1 dB Compression Point	V_{GAIN} = 0.5 V		8.4		dBm
			1.4		dBV rms
f = 240 MHz					
Gain	Maximum Gain		+43		dB
	Minimum Gain		–4.1		dB
Gain Scaling Factor			19.7		mV/dB
Gain Intercept			–5.2		dB
Noise Figure	Maximum Gain		7.6		dB
Output IP3	f1 = 240 MHz, f2 = 241 MHz, V_{GAIN} = 0.5 V		24.6		dBm
			17.6		dBV rms
Output 1 dB Compression Point	V_{GAIN} = 0.5 V		8.1		dBm
			1.1		dBV rms

NOTES

[1]The output dc centering voltage is normally set at $V_S/2$ and can be adjusted by applying a voltage to DECL.

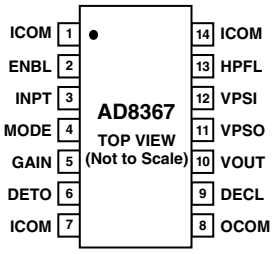
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

Supply Voltage VPSO, VPSI . . . . . 5.5 V
ENBL Voltage . . . . . V_S + 200 mV
MODE Select Voltage . . . . . V_S + 200 mV
V_{GAIN} Control Voltage . . . . . 1.2 V
Input Voltage . . . . . ±600 mV
Internal Power Dissipation . . . . . 250 mW
θ_{JA} . . . . . 150°C/W
Maximum Junction Temperature . . . . . 125°C
Operating Temperature Range . . . . . –40°C to +85°C
Storage Temperature Range . . . . . –65°C to +150°C
Lead Temperature Range (Soldering 60 sec) . . . . . 300°C

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PIN CONFIGURATION



PIN FUNCTION DESCRIPTIONS

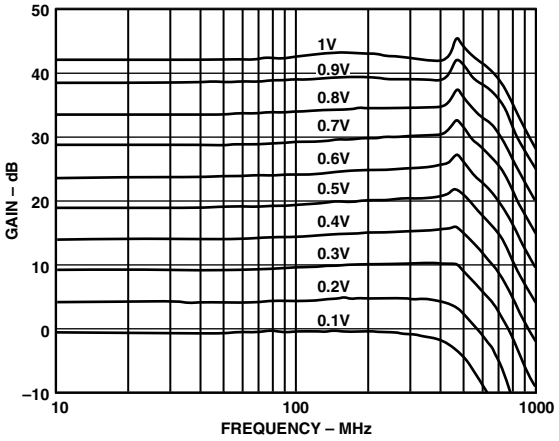
Pin	Mnemonic	Description
1, 7, 14	ICOM	Signal Common. Connect to low impedance ground.
2	ENBL	A HI activates the device.
3	INPT	Signal Input. 200 Ω to ground.
4	MODE	Gain Direction Control. HI for Positive Slope; LO for Negative Slope.
5	GAIN	Gain-Control Voltage Input
6	DETO	Detector Output. Provides output current for RSSI function and AGC control.
8	OCOM	Power Common. Connect to low impedance ground.
9	DECL	Decoupling Pin. Can Be Used to Modify the Output Reference Level.
10	VOUT	Signal Output. Generally will be ac-coupled.
11	VPSO	Positive Supply Voltage. 2.7 V to 5.5 V. VPSI and VPSO are tied together internally with back-to-back PN junctions. They should be tied together externally and properly bypassed.
12	VPSI	Positive Supply Voltage. 2.7 V to 5.5 V.
13	HPFL	High-Pass Filter Connection. A capacitor to ground sets the corner frequency of the output offset control loop.

ORDERING GUIDE

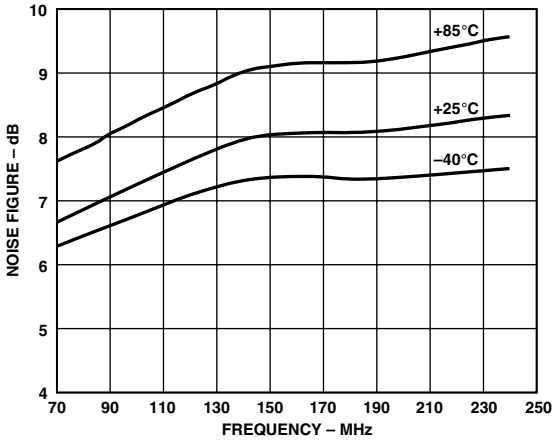
Model	Temperature Range	Package Description	Package Option
AD8367ARU	–40°C to +85°C	Tube, 14-Lead	RU-14
AD8367ARU-REEL-7	–40°C to +85°C	7" Tape and Reel	
AD8367-EVAL	–40°C to +85°C	Evaluation Board	
AD8367ARU-REEL	–40°C to +85°C	13" Tape and Reel	

CAUTION

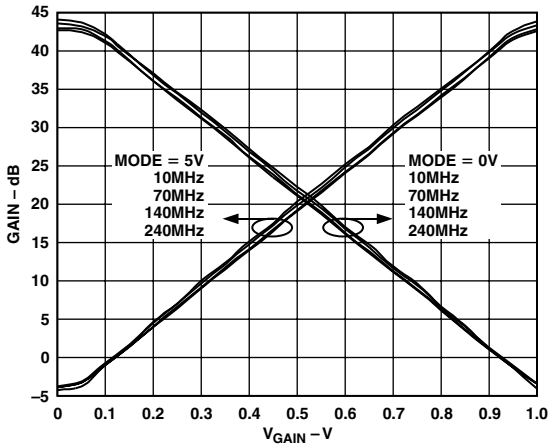
ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD8367 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



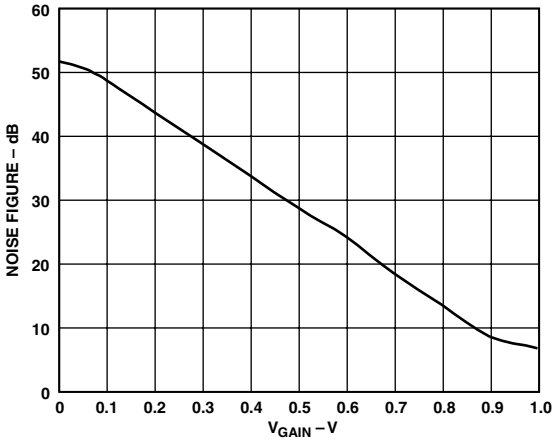
TPC 1. Gain vs. Frequency for Values of V_{GAIN}



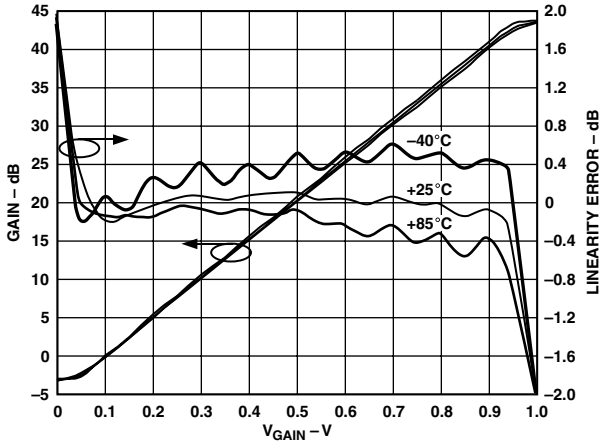
TPC 4. NF (re 200 Ω) vs. Frequency at Maximum Gain



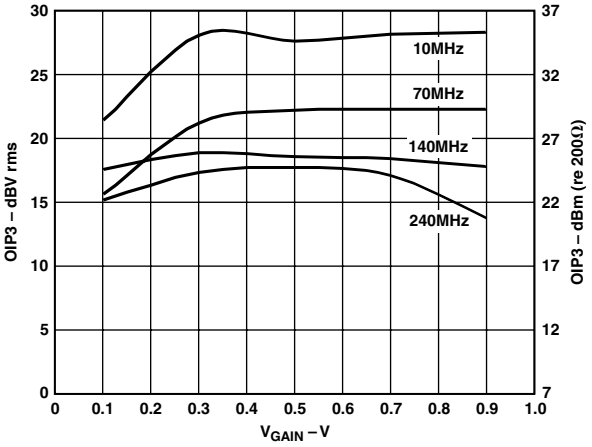
TPC 2. Gain vs. V_{GAIN} (Mode LO and Mode HI)



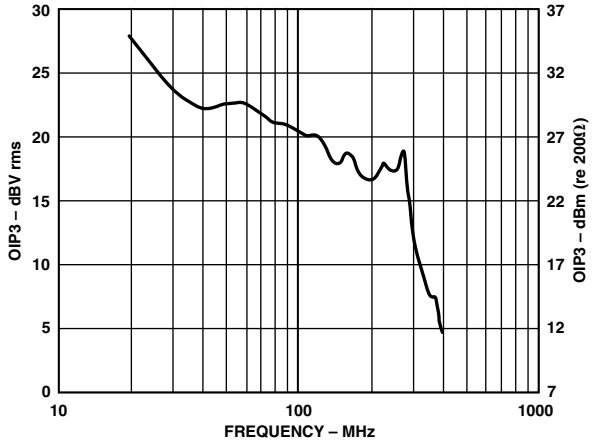
TPC 5. NF (re 200 Ω) vs. V_{GAIN} at 70 MHz



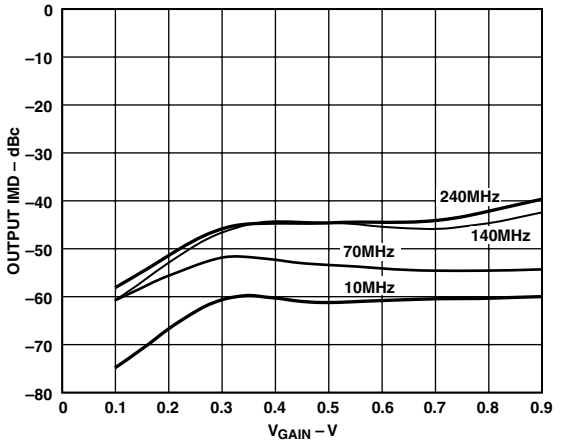
TPC 3. Gain Conformance at 70 MHz for T = –40°C, +25°C, and +85°C.



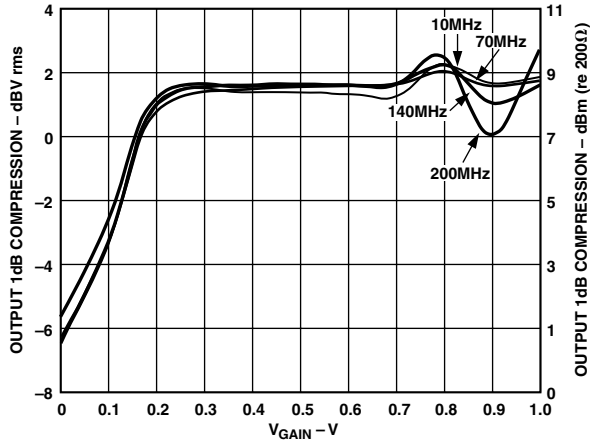
TPC 6. OIP3 vs. V_{GAIN}



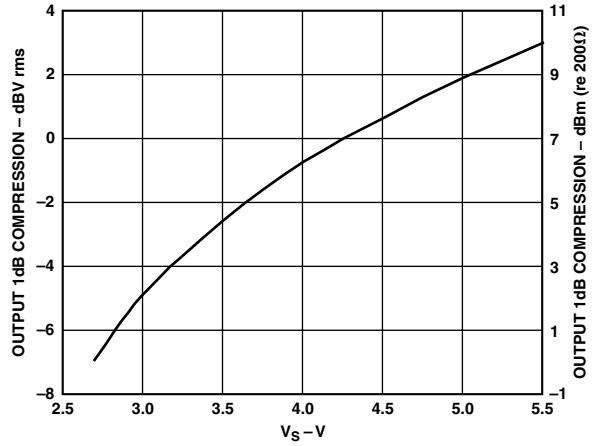
TPC 7. OIP3 vs. Frequency for V_{GAIN} = 500 mV



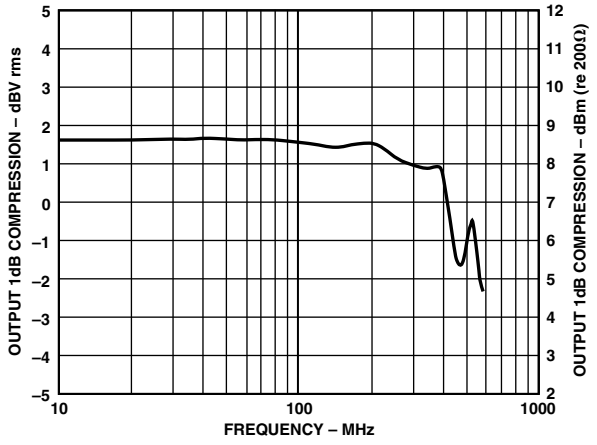
TPC 10. IMD3 vs. Gain (V_{OUT} = 1 V p-p Composite)



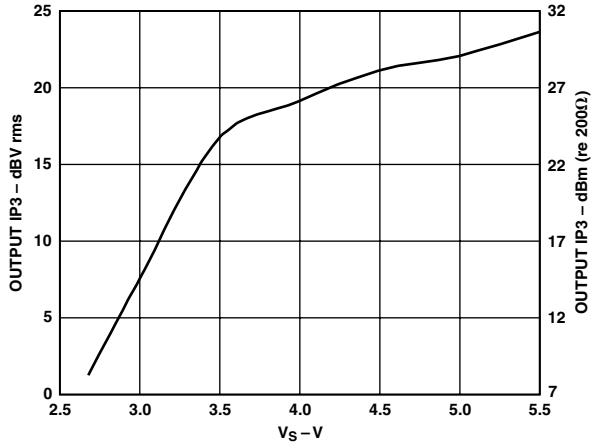
TPC 8. Output P1dB vs. V_{GAIN}



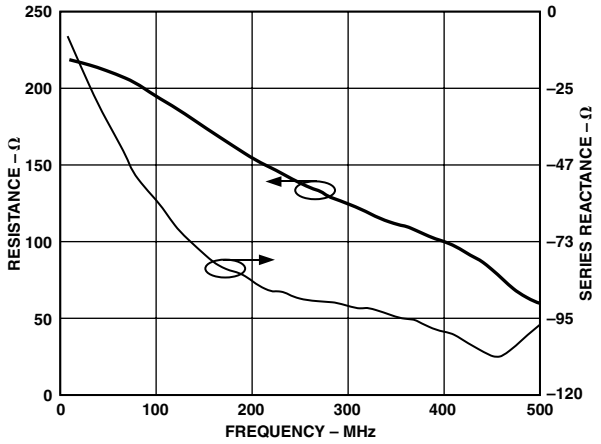
TPC 11. Output Compression Point vs. Supply Voltage at 70 MHz, V_{GAIN} = 500 mV



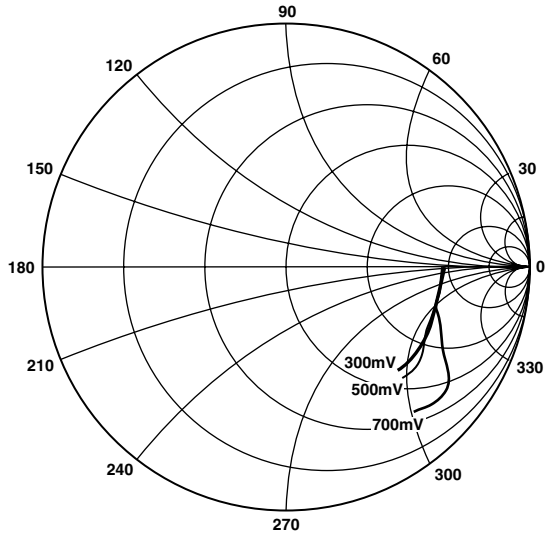
TPC 9. Output P1dB vs. Frequency at V_{GAIN} = 500 mV



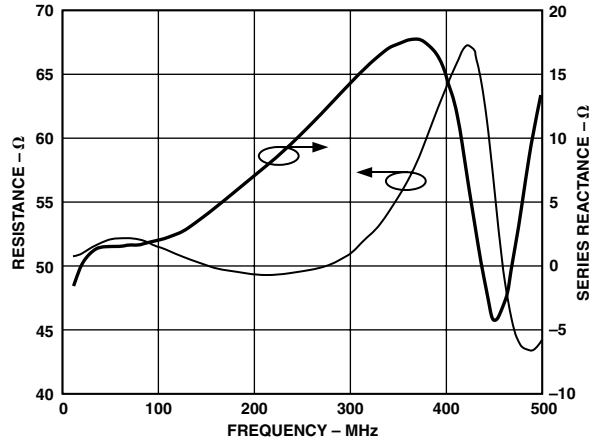
TPC 12. Output Third Order Intercept vs. Supply Voltage at 70 MHz, V_{GAIN} = 500 mV



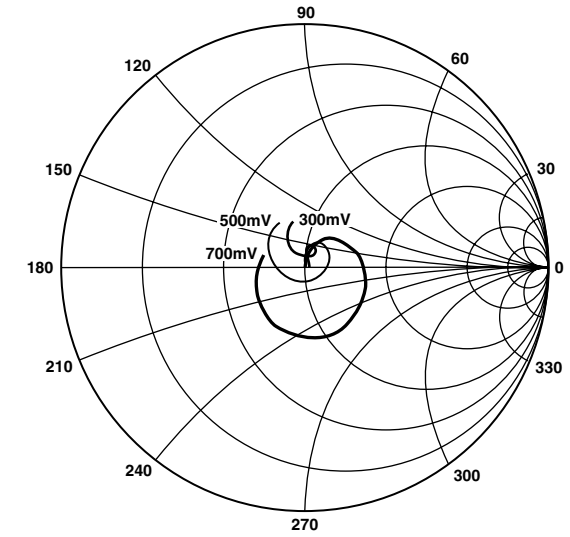
TPC 13. Input Resistance and Series Reactance vs. Frequency at V_{GAIN} = 500 mV



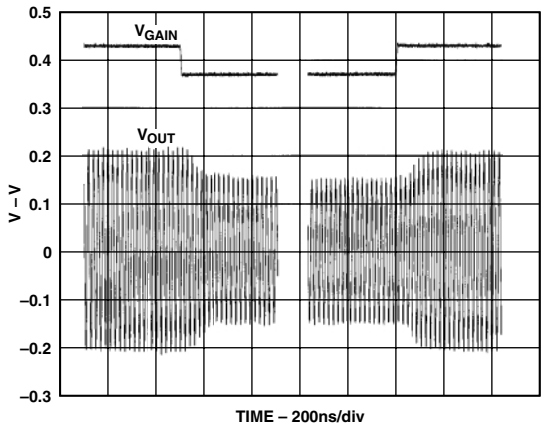
TPC 14. Input Reflection Coefficient vs. Frequency from 10 MHz to 500 MHz for Multiple Values of V_{GAIN}



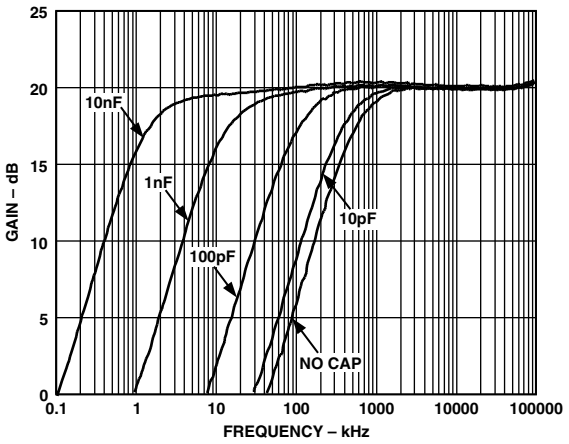
TPC 15. Output Resistance and Series Reactance vs. Frequency at V_{GAIN} = 500 mV



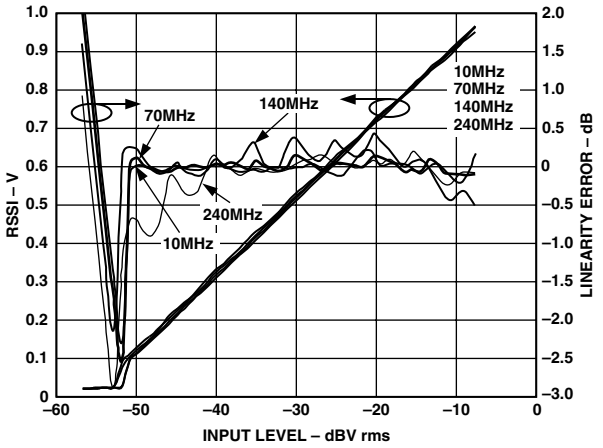
TPC 16. Output Reflection Coefficient vs. Frequency from 10 MHz to 500 MHz for Multiple Values of V_{GAIN}



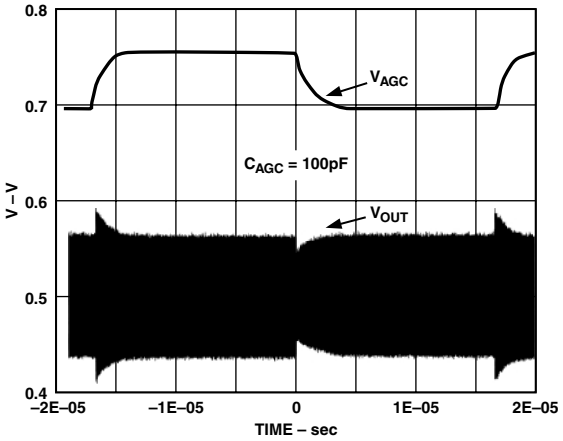
TPC 17. VGA Time Domain Response (3 dB Step)



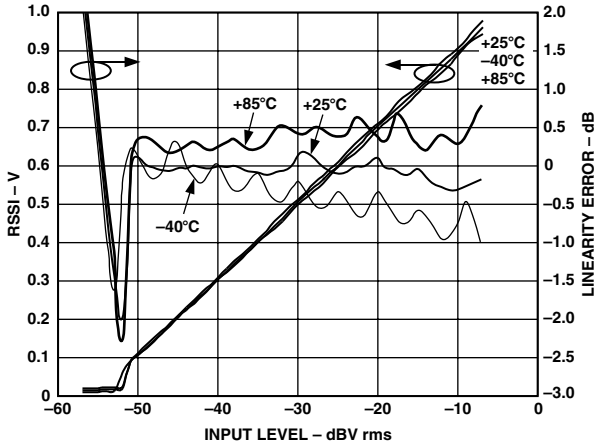
TPC 18. Gain vs. Frequency for Multiple Values of HPFL Capacitor at V_{GAIN} = 500 mV



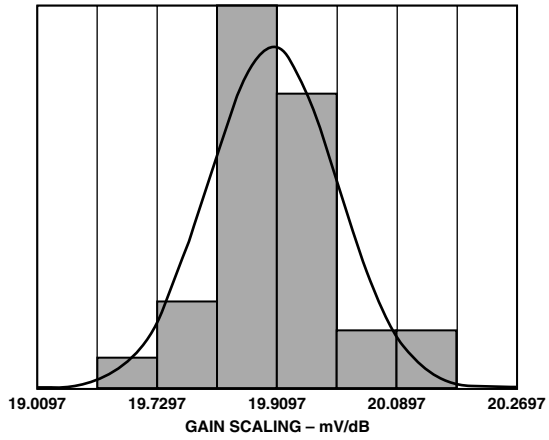
TPC 19. AGC RSSI (Voltage on DETO Pin) vs. Input Power at 10 MHz, 70 MHz, 140 MHz, and 240 MHz



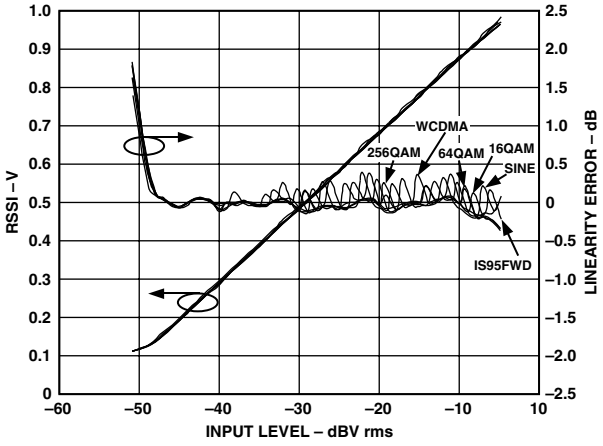
TPC 22. AGC Time Domain Response (3 dB Step)



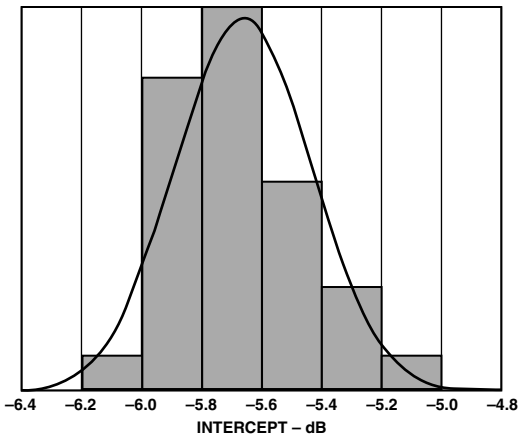
TPC 20. AGC RSSI (Voltage on DETO Pin) vs. Input Power over Temperature at 70 MHz



TPC 23. Gain Scaling Distribution at 70 MHz



TPC 21. AGC RSSI (Voltage on DETO Pin) vs. Input Power for Various Modulation Schemes



TPC 24. Gain Intercept Distribution at 70 MHz

THEORY OF OPERATION

The AD8367 is a variable gain single-ended IF amplifier based on Analog Devices' patented X-AMP architecture. It offers accurate gain control with a 45 dB span and a 3 dB bandwidth of 500 MHz. It can be configured as a traditional VGA with 50 dB/V gain scaling or as an AGC amplifier by using the built-in rms detector. Figure 1 is a simplified block diagram of the amplifier. The main signal path consists of a voltage-controlled 0 dB to 45 dB variable attenuator followed by a 42.5 dB fixed gain amplifier. The AD8367 is designed to operate optimally in a 200 Ω impedance system.

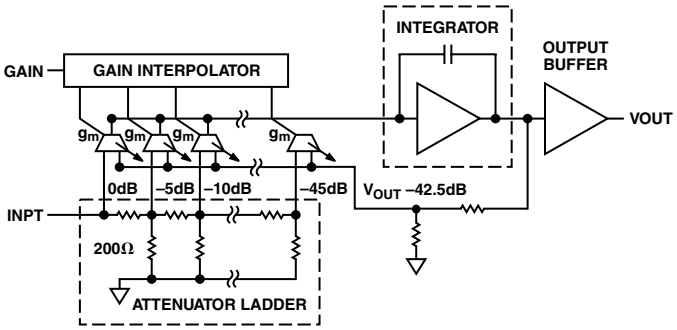


Figure 1. The Simplified Architecture

Input Attenuator and Gain Control

The variable attenuator consists of a 200 Ω single-ended resistive ladder comprising nine 5 dB sections and an interpolator that selects the attenuation factor. Each tap point down the ladder network further attenuates the input signal by a fixed decibel factor. Gain control is achieved by sensing different tap points with variable transconductance stages. Based on the gain control voltage, an interpolator selects which stage(s) are active. For example, if only the first stage is active, the 0 dB tap point is sensed; if the last stage is active, the 45 dB tap point is sensed. Attenuation levels that fall between tap points are achieved by having neighboring g_m stages active simultaneously, creating a weighted average of the discrete tap point attenuations. In this way, a smooth, monotonic attenuation function is synthesized that is linear-in-dB with a very precise scaling.

The gain of the AD8367 can be an increasing or decreasing function of the control voltage, V_{GAIN}, depending on whether the MODE pin is pulled up to the positive supply or down to ground. When the MODE pin is high, the gain increases with V_{GAIN} as shown in Figure 2. The ideal linear-in-dB scaled transfer function is given by,

$$Gain\ (dB) = 50 \times V_{GAIN} - 5 \quad (1)$$

where V_{GAIN} is expressed in volts. Equation 1 contains the gain scaling factor of 50 dB/V (20 mV/dB) and the gain intercept of –5 dB which represents the extrapolated gain for V_{GAIN} = 0 V. The gain ranges from –2.5 dB to 42.5 dB for V_{GAIN} ranging from 50 mV to 950 mV. The deviation from (1), that is, the gain conformance error, is also illustrated in Figure 2. The ripples in the error are a result of the interpolation action between tap points. The AD8367 provides better than ±0.5 dB of conformance error over >40 dB gain range at 200 MHz and ±1 dB at 400 MHz.

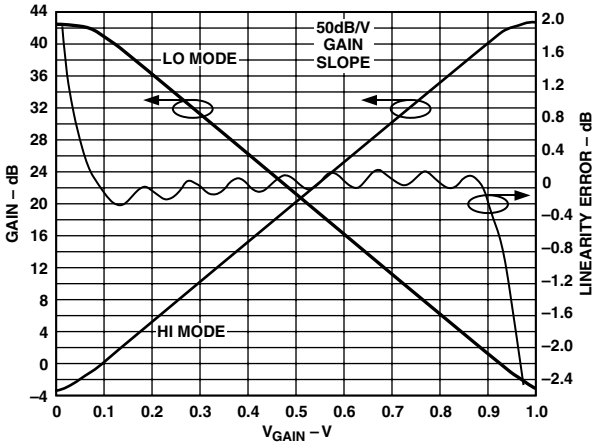


Figure 2. The gain function can be either an increasing or decreasing function of V_{GAIN} depending on the MODE pin.

The gain is a decreasing function of V_{GAIN} when the MODE pin is low. Figure 2 also illustrates this mode which is described by

$$Gain\ (dB) = 45 - 50 \times V_{GAIN} \quad (2)$$

This gain mode is required in AGC applications using the built-in square-law level detector.

Input and Output Interfaces

The AD8367 was designed to operate best in a 200 Ω impedance system. Its gain range, conformance law, noise and distortion assume that 200 Ω source and load impedances are used. Interfacing the AD8367 to other common impedances (from 50 Ω used at radio frequencies to 1 kΩ presented by data-converters) can be accomplished using resistive or reactive passive networks, whose design depends on specific system requirements such as bandwidth, return loss, noise figure and absolute gain range.

The input impedance of the AD8367 is nominally 200 Ω, determined by the resistive ladder network. This presents a 200 Ω dc resistance to ground, and in cases where an elevated signal potential is used, ac coupling is necessary. The input signal level must not exceed 700 mV p-p to avoid overloading the input stage. The output impedance is determined by an internal 50 Ω damping resistor, as shown in the simplified schematic in Figure 3.

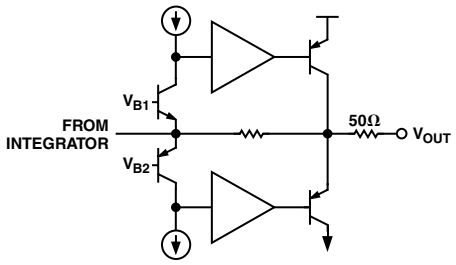


Figure 3. A 50 Ω Resistor is Added to the Output to Prevent Package Resonance

Power and Voltage Metrics

Although power is the traditional metric used in the analysis of cascaded systems, most active circuit blocks fundamentally respond to voltage. The relationship between power and voltage is defined by the impedance level. When input and output impedance levels are the same, power gain and voltage gain are identical. However, when impedance levels change between input and output, they differ. Thus, one must be very careful to use the appropriate gain for system chain analyses. Quantities such as OIP3 are quoted in dBV rms as well as dBm referenced to 200 Ω. The dBV rms unit is defined as decibels relative to 1 V rms. In a 200 Ω environment, the conversion from dBV rms to dBm requires the addition of 7 dB to the dBV rms value. For example, a +2 dBV rms level corresponds to +9 dBm.

Noise and Distortion

Since the AD8367 consists of a passive variable attenuator followed by a fixed gain amplifier, the noise and distortion characteristics as a function of the gain voltage are easily predicted. The input-referred noise increases in proportion to the attenuation level. Figure 4 shows noise figure, NF, as a function of V_{GAIN} for the MODE pin pulled high. The minimum NF of 7.5 dB occurs at maximum gain and increases 1 dB for every 1 dB reduction in gain. In receiver applications, the minimum NF should occur at the maximum gain where the received signal presumably is weak. At higher levels, a lower gain is needed, and the increased NF becomes less important.

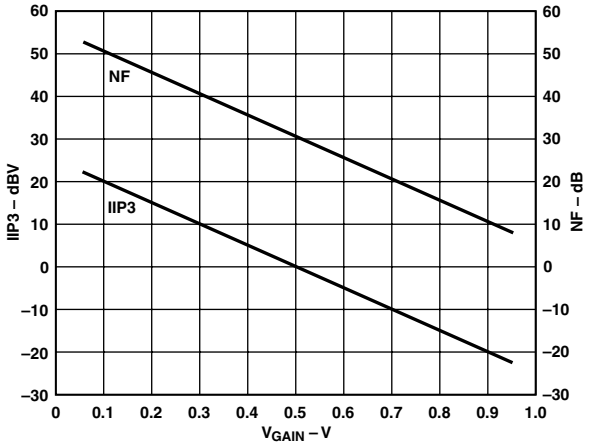


Figure 4. Noise Figure and Input Third Order Intercept vs. Gain (R_{SOURCE} = 200 Ω)

The input-referred distortion varies in a similar manner to the noise. Figure 4 illustrates how the third-order intercept point at the input, IIP3, behaves as a function of V_{GAIN}. The highest IIP3 of 20 dBV rms (27 dBm re 200 Ω) occurs at minimum gain. The IIP3 then decreases 1 dB for every 1 dB increase in gain. At lower levels, a degraded IIP3 is acceptable. Overall, the dynamic range, represented by the difference between IIP3 and NF, remains reasonably constant as a function of gain. The output distortion and compression are essentially independent of the gain. At low gains, when the input level is high, input overload may occur, causing premature distortion.

Output Centering

The output level is centered midway between ground and the supply if the DECL pin is left floating. Alternatively, the output level may be set by driving the DECL pin with the desired reference level. As shown in Figure 5, the loop acts to suppress deviations from the reference at outputs below its corner frequency while not affecting signals above it. The maximum corner frequency with no external capacitor is 500 kHz. The corner frequency can be lowered arbitrarily by adding an external capacitor, C_{HP}:

$$f_{HP}(kHz) = \frac{10}{C_{HP}(nF) + 0.02} \quad (3)$$

A capacitor at pin DECL is recommended to decouple the reference level to which the output is centered.

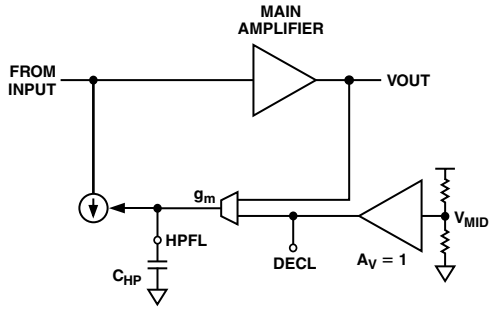


Figure 5. The dc output level is centered to mid supply by a control loop whose corner frequency is determined by C_{HP}.

RMS Detection

The AD8367 contains a square-law detector that senses the output signal and compares it to a calibrated set-point of 354 mV rms which corresponds to a 1 V p-p sine wave. Any difference between the output and set-point generates a current which is integrated by an external capacitor, C_{AGC}, connected from the DETO pin to ground, to provide an AGC control voltage. There is also an internal 5 pF capacitor on the DETO pin.

The resulting voltage is used as an AGC bias. For this application, the MODE pin is pulled low and the DETO pin is tied to the GAIN pin. The output signal level is then regulated to 354 mV rms. The AGC bias represents a calibrated rms measure of the received signal strength (RSSI). Since in the AGC mode the output signal is forced to the 354 mV rms set-point (–9.02 dBV rms), Equation 2 can be recast to express the strength of the received signal, $V_{IN\text{-}RMS}$, in terms of the AGC bias V_{DETO},

$$V_{IN-RMS}\ (dBV\ rms) = -54.02 + 50 \times V_{DETO} \quad (4)$$

where –54.02 *dBV rms* = –45 *dB* − 9.02 *dBV rms*.

For small changes in input signal level, V_{DETO} responds with a characteristic single-pole time constant, τ_{AGC}, which is proportional to C_{AGC},

$$\tau_{AGC}\ (\mu s) = 10 \times C_{AGC}\ (nF) \quad (5)$$

where the internal 5 pF capacitor has been lumped with the external capacitor to give C_{AGC}.

APPLICATIONS

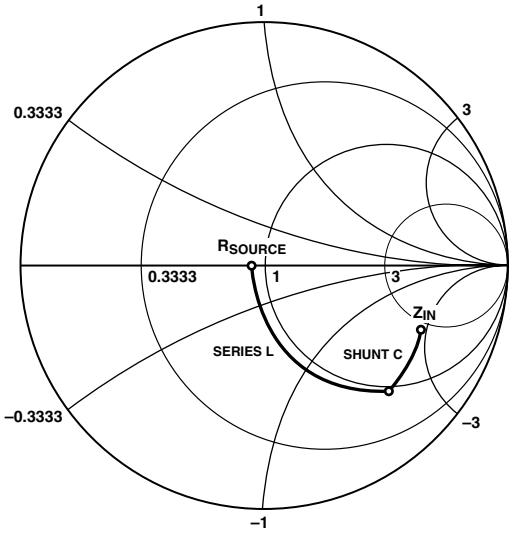
The AD8367 can be configured either as a variable-gain amplifier whose gain is controlled externally through the GAIN pin or as an AGC amplifier, using a supply voltage of 2.7 V to 5.5 V. The supply to the VPSO and VPSI pins should be decoupled using a low-inductance 0.1 μF surface-mount ceramic capacitor, as close to the device as possible. Additional supply decoupling may be provided by a small series resistor. A 10 nF capacitor from pin DECL to OCOM is recommended to decouple the output reference voltage.

Input and Output Matching

The AD8367 is designed to operate in a 200 Ω impedance system. The output amplifier is a low output impedance voltage buffer with a 50 Ω damping resistor to desensitize it from load reactance and parasitics. The quoted performance includes the voltage division between the 50 Ω resistor and the 200 Ω load. The AD8367 can be reactively matched to an impedance other than 200 Ω using traditional step-up and step down matching networks or high quality transformers. Table I lists the 50 Ω S-parameters for the AD8367 at a V_{GAIN} = 750 mV.

Figure 6 illustrates an example where the AD8367 is matched to 50 Ω at 140 MHz. As shown in the Smith Chart, the input matching network shifts the input impedance from Z_{IN} to 50 Ω with an insertion loss of less than 2 dB over a 5 MHz bandwidth. For the output network, the 50 Ω load is made to present 200 Ω to the AD8367 output. Table II provides the component values required for 50 Ω matching at several frequencies of interest.

In situations where added loss and noise can be tolerated, a resistive pad can be used to provide broad-band near-matched impedances at the device terminals and the terminations. Minimum-loss L-pad networks are used on the evaluation board (see Figure 19) to allow easy interfacing to standard 50 Ω test equipment. Each pad introduces an 11.5 dB power loss (5.5 dB voltage loss).



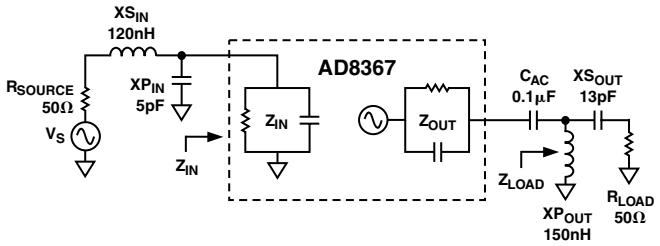


Figure 6. Reactive Matching Example for f = 140 MHz

Table I. S-Parameters for 50 Ω System for V_S = 5 V, and V_{GAIN} = 0.75 V

Frequency (MHz)	S11	S21	S12	S22
10	0.64∠0°	8.5∠177°	2×10^{-3}∠153°	0.02∠11°
70	0.64∠–1.5°	9.0∠168°	5×10^{-4}∠106°	0.02∠54°
140	0.63∠–3.0°	10.0∠152°	9×10^{-4}∠80°	0.06∠88°
190	0.63∠–3.7°	10.4∠138°	9×10^{-4}∠147°	0.09∠83°
240	0.62∠–4.9°	10.8∠125°	1×10^{-3}∠148°	0.1∠76°

Table II. Reactive Matching Components for a 50 Ω System, R_S = 50 Ω, R_{LOAD} = 50 Ω

Frequency (MHz)	XS_{IN}	XP_{IN} (pF)	XS_{OUT} (pF)	XP_{OUT}
10	1.5 μH	120	180	1.8 μH
70	220 nH	15	27	270 nH
140	120 nH	7	13	150 nH
190	82 nH	4	10	100 nH
240	68 nH	3	7	82 nH

VGA Operation

The AD8367 is a general-purpose VGA suitable for use in a wide variety of applications where voltage-control of gain is needed. While having a 500 MHz bandwidth, its use is not limited to high frequency signal processing. Its accurate, temperature- and supply-stable linear-in-dB scaling will be valuable wherever it is important to have a more dependable response to the control voltage than is usually offered by VGAs of this sort. For example, there is no preclusion to its use in speech-bandwidth systems.

Figure 7 shows the basic connections. The capacitor C_{HP} at Pin HPFL may be used to alter the high-pass corner frequency of the signal path, and is associated with the offset control loop that eliminates the inherent variation in the internal dc balance of the signal path as the gain is varied ("offset ripple"). This frequency should be chosen to be about a decade below the lowest frequency component of the signal. If made much lower than necessary, the offset loop will not be able to track the variations that occur when there are rapid changes in V_{GAIN}. The control of offset is important even when the output is ac-coupled because of the potential reduction of the upper and lower voltage range at this pin.

However, in many applications these components will be unnecessary, since an internal network provides a default high-pass corner of about 500 kHz. For C_{HP} = 1 nF, the modified corner is at ~10 kHz; it scales downward with increasing capacitance. TPC 18 shows representative response curves for the indicated component values.

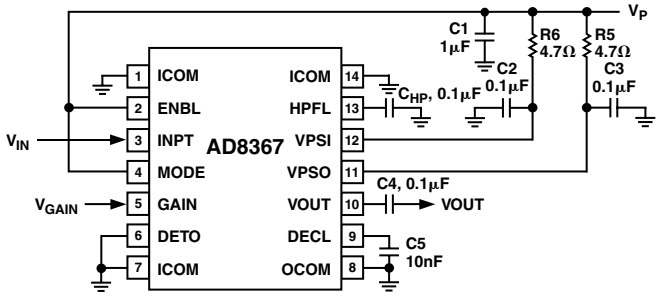


Figure 7. Basic Connections for Voltage-Controlled Gain Mode

Modulated Gain Mode

The AD8367 may be used as a means of modulating the signal level. It should be kept in mind, however, that the gain is a nonlinear (exponential) function of V_{GAIN}; thus it is not suitable for normal amplitude-modulation functions. The small-signal bandwidth of the gain interface is ~5 MHz and the slew-rate is of the order of ±500 dB/µs. During gain slewing from close to minimum to maximum gain (or vice versa) the internal interpolation processes in an X-AMP-based VGA rapidly scan the full range of gain values. The gain and offset ripple associated with this process may cause transient disturbances in the output. Therefore, it is inadvisable to use high-amplitude pulse drives with rise and fall times below 200 ns.

AGC Operation

The AD8367 may be used as an AGC amplifier as shown in Figure 8. For this application, the accurate internal square-law detector is employed. The output of this detector is a current that varies in polarity depending on whether the rms value of the output is greater or less than its internally-determined "set-point" of 354 mV rms. This is 1 V p-p for sine-wave signals, but the peak amplitude for other signals, such as Gaussian noise, or those carrying complex modulation, will invariably be somewhat greater. However, for all waveforms having a crest factor of less than 5, and when using a supply voltage of 4.5 V to 5.5 V, the rms value will be correctly measured and delivered at V_{OUT}. When using lower supplies, the rms value of V_{OUT} is unaffected (the set-point is determined by a band-gap reference) but the peak crest factor capacity is reduced.

The output of the detector is delivered to Pin DETO. The detector can source up to 60 µA and can sink up to 11 µA. For a sine-wave output signal, and under conditions where the AGC loop is settled, the detector output also takes the form of a sine-wave, but at twice the frequency and having a mean value of zero. If the input to the amplifier increases the mean of this current also increases, and charges the external loop filter capacitor C_{AGC} toward more positive voltages. Conversely, a reduction in V_{OUT} below the set-point of 354 mV rms causes this voltage to fall toward ground. The capacitor voltage is the AGC bias; this may be used as an RSSI (Received Signal Strength Indicator) output, and is scaled exactly as V_{GAIN}, that is, 20 mV/dB.

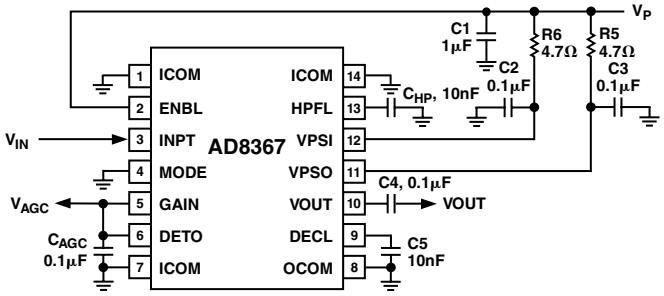


Figure 8. Basic Connections for AGC Operation

A valuable feature of using a square law detector is that the RSSI voltage is a true reflection of signal power, and may be converted to an absolute power measurement for any given source impedance. The AD8367 may thus be employed as a true-power meter, or decibel-reading ac voltmeter, as distinct from its basic amplifier function.

The AGC mode of operation requires that the correct gain direction is chosen. Specifically, the gain must fall as V_{AGC} increases to restore the needed balance against the set-point. Therefore, the MODE pin must be pulled low. This accurate leveling function is shown in Figure 9, where the rms output is held to within 0.1 dB of the set point for >35 dB range of input levels.

The dynamics of this loop are controlled by C_{AGC} acting in conjunction with an on-chip equivalent resistance R_{AGC} of 10 kΩ which form an effective time-constant $T_{AGC} = R_{AGC} C_{AGC}$. The loop thus operates as a single-pole system with a loop bandwidth of $1/(2\pi T_{AGC})$. Because the gain control function is linear in decibels, this bandwidth is independent of absolute signal level. Figure 10 illustrates the loop dynamics for a 30 dB change in input signal level with C_{AGC} = 100 pF.

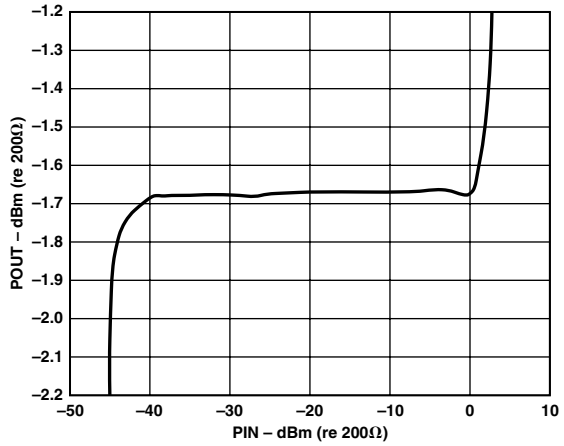


Figure 9. Leveling Accuracy of the AGC Function

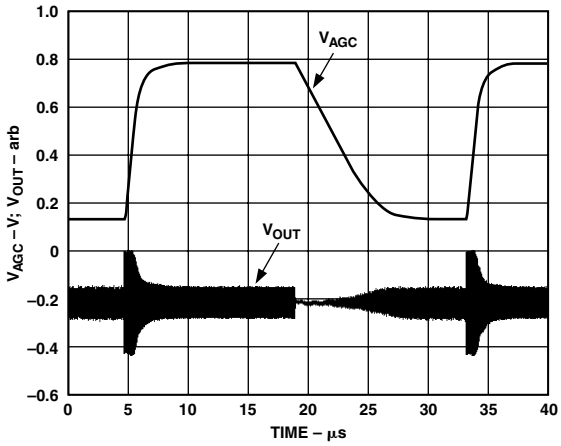


Figure 10. AGC Response to a 32 dB Step in Input Level (f = 50 MHz)

It is important to understand that R_{AGC} does not act as if in shunt with C_{AGC}. Rather, the error-correction process is that of a true integrator, to guarantee an output that is exactly equal in rms amplitude to the specified set-point. For large changes in input level, the integrating action of this loop will be most apparent. The slew rate of V_{AGC} is determined by the peak output current from the detector and the capacitor. Thus, for a representative value of C_{AGC} = 3 nF, this rate is about 20 V rms or 10 dB/µs, while the small-signal bandwidth is 1 kHz.

Most AGC loops incorporating a true error-integrating technique have a common weakness. When driven from an increasingly larger signal, the AGC bias increases to reduce the gain. But eventually, the gain will fall to its minimum value, for which further increase in this bias will have no effect on the gain. That is, the voltage on the loop capacitor will be forced progressively higher because the detector output is a current, and the AGC bias is its integral. Consequently there will always be a precipitous increase in this bias voltage when the input to the AD8367 exceeds that value which overdrives the detector, and because the minimum gain is –2.5 dB, that will happen for all inputs +2.5 dB greater than the set-point of ~350 mV rms. If possible, the user should ensure that this limitation is preserved, preferably with a guard-band of 5 dB to 10 dB below overload.

In some cases, it may be found that, if driven into AGC overload, the AD8367 will require unusually long times to recover; that is, the voltage at DETO will remain at an abnormally high value and the gain will be at its lowest value. To avoid this situation, it is recommended that a clamp be placed on the DETO pin as shown in Figure 11.

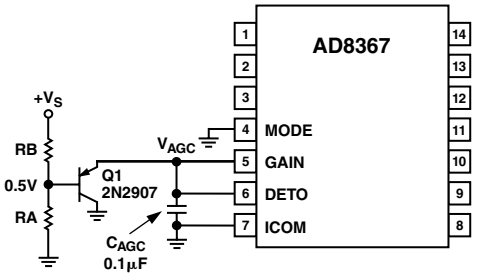


Figure 11. External Clamp to Prevent AGC Overload. The resistive divider network, RA and RB, should be designed such that the base of Q1 is driven to 0.5 V.

Modifying the AGC Set Point

If an AGC set point other than the internal one is desired, an external detector may be used. Figure 12 depicts a method that uses an external true-rms detector and error integrator to operate the AD8367 as a closed-loop AGC system with a user-settable operating level.

The AD8361 (U2) produces a dc output level which is proportional to the rms value of its input, taken as a sample of the AD8367 (U1) output. This dc voltage is compared to an externally-supplied set-point voltage, and the difference is integrated by the AD820 (U3) to form the gain control voltage which is applied to the GAIN input of the AD8367 through the divider composed of R4 and R5. This divider is included in order to minimize overload recovery time of the loop by having the integrator saturate at a point that only slightly overdrives the gain control input of the AD8367. The scale factor at V_{AGC} is influenced by the values of R4 and R5; for the values shown, the factor is 86 mV/dB. Note that in this circuit the AD8367's MODE pin must be pulled high to obtain correct feedback polarity because the integrator inverts the polarity of the feedback signal.

The relationship between set-point voltage and the rms output voltage of the AD8367 is as follows:

$$V_{OUT-RMS} = V_{SET} \times \frac{(R1+225)}{225 \times 7.5} \quad (6)$$

where *225* is the input resistance of the AD8361 and *7.5* is its conversion gain. For R1 = 200 Ω, this reduces to $V_{OUT-RMS} = V_{SET} \times 0.25$.

Capacitor C2 sets the averaging time for the rms detector. This should be made long enough to provide sufficient smoothing of the detector's output in the presence of the modulation on the RF signal. A level fluctuation of less than 1 dB (<5% to 10%) p-p at the AD8361's output is a reasonable value. A considerably longer time-constant will needlessly lower the AGC bandwidth, while a short time-constant can degrade the accuracy of the true-rms measurement process. Components C1, R2, and R3 set the control loop's bandwidth and stability. The maximum stable loop bandwidth will be limited by the rms detector's averaging time constant as discussed above.

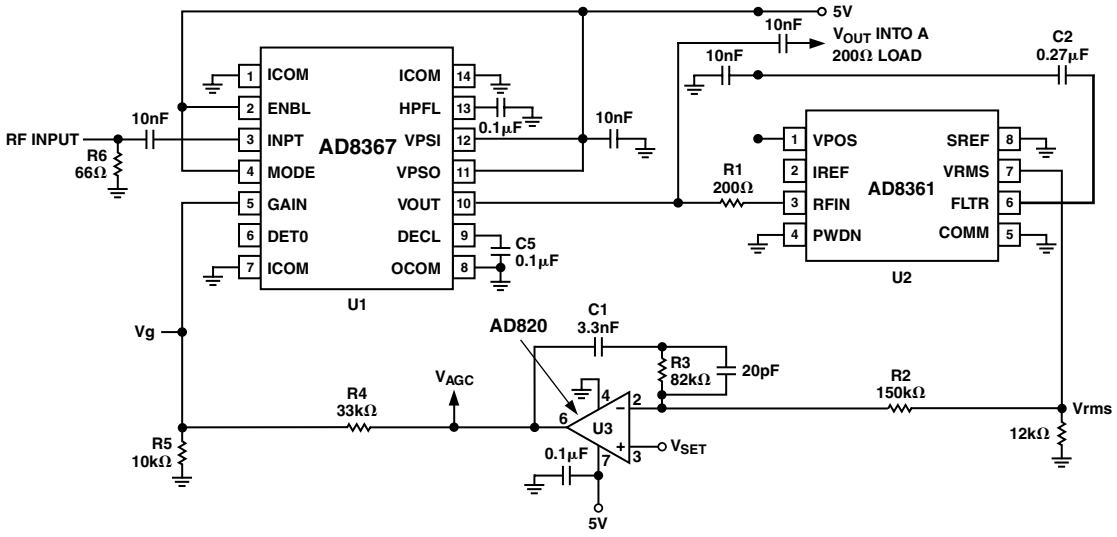


Figure 12. Example of Using an External Detector to Form an AGC Loop

For an input signal consisting of a 4.096 MS/s QPSK modulated carrier, the relationship between V_{SET} and the output power for this setup is shown in Figure 13. The exponential shape reflects the linear-in-magnitude response of the AD8361. The adjacent channel power ratio (ACPR) as a function of output power is illustrated in Figure 14. The minima occur where the distortion and integrated noise powers cross over.

The component values shown in Figure 12 were chosen for a 64-QAM signal at 500 kS/s at a carrier frequency of 150 MHz. The response time of the loop as shown is roughly 5 ms for an abrupt input level change of 40 dB. Figure 15 shows the dynamic performance of the loop with a step-modulated CW signal applied to the input for a V_{SET} of about 1 V.

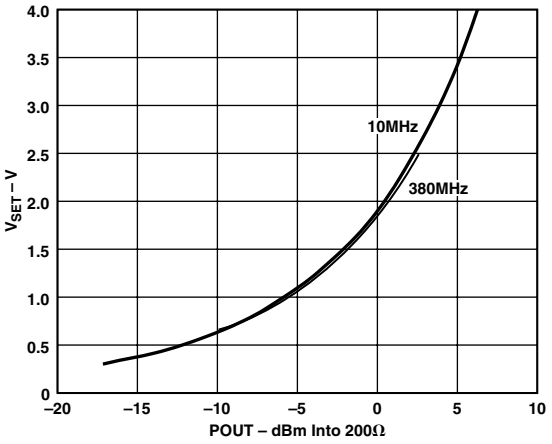


Figure 13. AGC Set-Point Voltage vs. Output Power (QPSK: 4.096 MS/s; α = 0.22; 1 User)

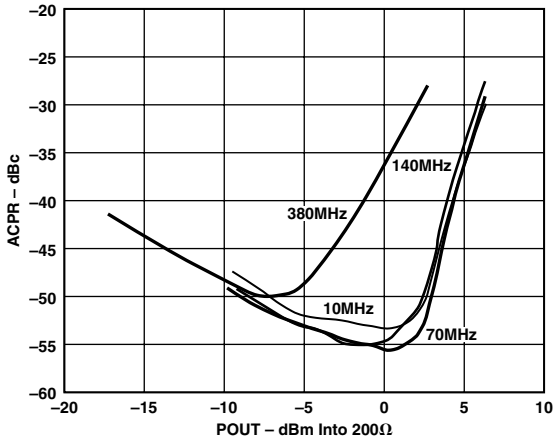


Figure 14. ACPR versus Output Power for QPSK Waveform (4.096 MS/s; α = 0.22; 1 User)

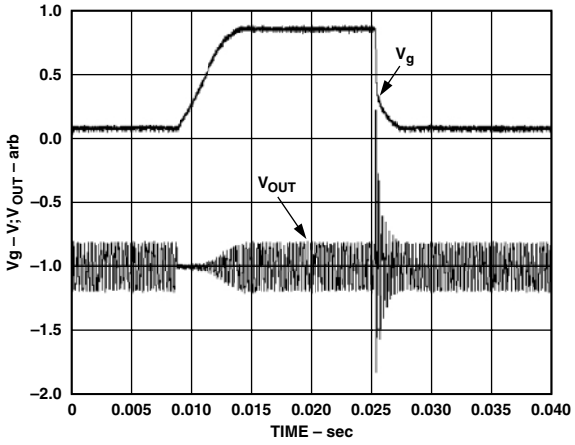


Figure 15. AGC Dynamic Response: 8367 AGC with an External Detector

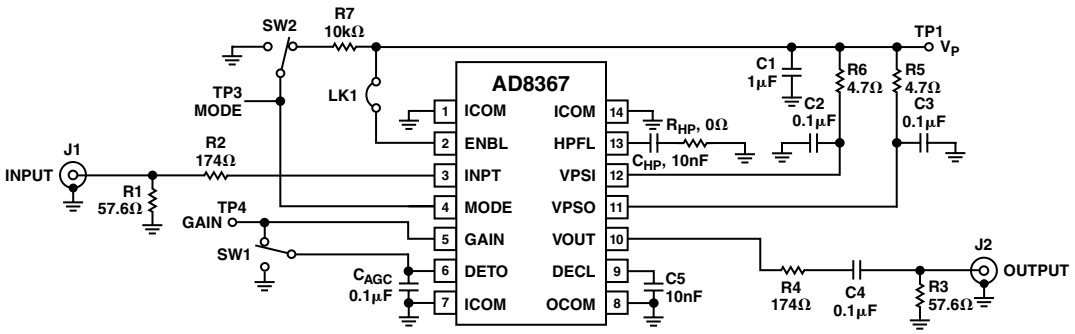


Figure 16. Evaluation Board Schematic

Table III. Suggested Component Values For External AGC Detector Circuit

Modulation Type	Rate Sym/s	C1 μF	C2 μF	R2 kΩ	R3 kΩ
QPSK	1.23 M	0.0022	0.033	150	62
QPSK	4 M	0.0022	0.015	150	39
π/4 DQPSK	24.3 K	0.033	0.68	150	51
64 QAM	100 K	0.015	1.5	150	51
64 QAM	500 K	0.0068	0.33	150	62
64 QAM	4 M	0.0022	0.068	150	100

Evaluation Board

Figure 16 shows the schematic of the AD8367 evaluation board. The board is powered by a single supply of 2.7 V to 5.5 V. Table IV details the various configuration options of the evaluation board.

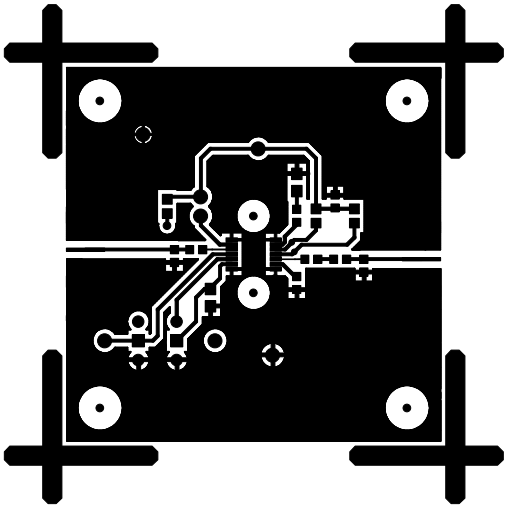


Figure 17. Layout of Component Side

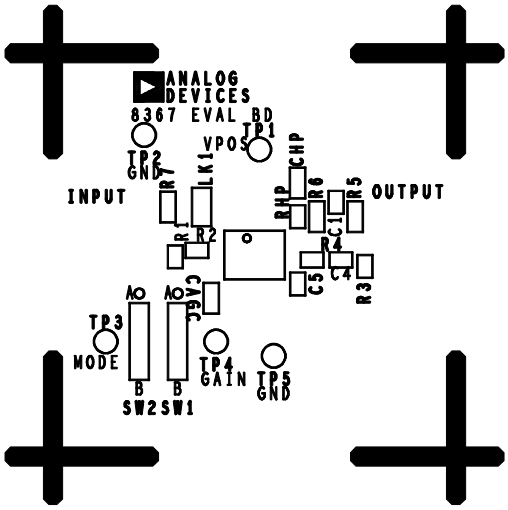


Figure 18. Silkscreen of Component Side

Characterization Setup and Methods

Minimum-loss L-pad matching networks were used to interface standard 50 Ω test equipment to the 200 Ω input impedance during the characterization process. Using a 57.6 Ω shunt resistor followed by a 174 Ω series resistor provides a broadband match between the 50 Ω test equipment and the 200 Ω device impedance as illustrated in Figure 19. The insertion loss of this network is 11.5 dB.

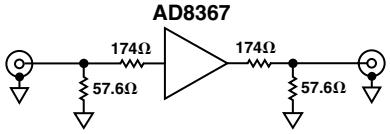


Figure 19. Characterization Test Setup

Table IV. Evaluation Board Configuration Options

Component	Function	Default Condition
TP1, TP2	Supply and Ground Vector Pins	Not Applicable
TP3, TP4	Mode and Gain Vector Pins	Not Applicable
SW1	VGA/AGC Select: Used to select VGA (position A) or AGC (position B) mode of operation. SW2 must be set for position A for AGC mode of operation.	SW1 = A
SW2	MODE Select: Used to select positive or negative VGA slope. Set to position B for an increasing gain with V_{GAIN}, position A for decreasing gain law.	SW2 = B
LK1	Device Enable: When LK1 is installed, the ENBL pin is connected to the positive supply and the AD8367 is in operating mode.	SW3 = PWUP
R1, R2	Input Interface: R1 and R2 are used to provide an L-pad impedance-transforming network. The broadband matching network transforms a 50 Ω source to match a 200 Ω load with 11.5 dB of insertion loss.	R1 = 57.6 Ω (Size 0603) R2 = 174 Ω (Size 0603)
R3, R4, C4	Output Interface: R3 and R4 are used to transform a 50 Ω load termination to look like a 200 Ω load with 11.5 dB of insertion loss. The AC coupling capacitor, C4, can be increased to obtain a lower high-pass corner frequency.	R3 = 57.6 Ω (Size 0603) R4 = 174 Ω (Size 0603) C4 = 0.1 μF (Size 0603)
C1, C2, C3, R5, R6	Power Supply Decoupling: The nominal supply decoupling consists of a 1 μF capacitor to ground, a 4.7 Ω series resistor, and a 0.1 μF capacitor to ground. The same de-coupling network should be used on both VPSI and VPSO supply lines.	C1 = 1 μF (Size 0603) R5 = R6 = 4.7 Ω (Size 0805) C2 = C3 = 0.1 μF (Size 0603)
C5	Internal Supply Decoupling: Capacitor C5 provides mid-supply decoupling.	C5 = 10 nF (Size 0603)
C_{HPFL}	Filter Capacitor: HPFL capacitor, sets the high pass corner frequency.	C_{HPFL} = 0.1 μF (Size 0805) R_{HP} = 0 Ω (Size 0603)
C_{AGC}	AGC Filter Capacitor: Capacitor, C_{AGC}, sets closed loop AGC response time.	C_{AGC} = 0.1 μF (Size 0805)
R7	Mode Pullup Resistor	R7 = 10 kΩ (Size 0805)

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

14-Lead (TSSOP)
(RU-14)