SGS-THOMSON MICROELECTRONICS

TDA9110

LOW-COST DEFLECTION PROCESSOR FOR MULTISYNC MONITORS

PRODUCT PREVIEW

HORIZONTAL

- EXTREMELY LOW JITTER LEVEL
- SELF-ADAPTATIVE
- DUAL PLL CONCEPT
- 150kHz MAXIMUM FREQUENCY
- X-RAY PROTECTION INPUT
- I^2C CONTROLS : HORIZONTAL DUTY-CYCLE, H-POSITION

VERTICAL

- VERTICAL RAMP GENERATOR
- 50 TO 165Hz AGC LOOP
- GEOMETRY TRACKING WITH V-POS & AMP
- I^2C CONTROLS : V-AMP, V-POS, S-CORR, C-CORR
- DC BREATHING COMPENSATION

I^2C GEOMETRY CORRECTIONS

- VERTICAL PARABOLA GENERATOR (Pincushion, Keystone)
- HORIZONTAL SIZE CONTROL (Amplitude)
- HORIZONTAL DYNAMIC PHASE (Side Pin Balance & Parallelogram)
- HORIZONTAL AND VERTICAL DYNAMIC FOCUS (Horizontal Focus Amplitude, Horizontal Focus Symmetry, Vertical Focus Amplitude)

GENERAL

- SYNCHRO PROCESSOR
- 12V SUPPLY VOLTAGE
- 8V REFERENCE VOLTAGE
- HOR. & VERT. LOCK UNLOCK OUTPUTS
- READ/WRITE I^2C INTERFACE
- HORIZONTAL AND VERTICAL MOIRE

DESCRIPTION

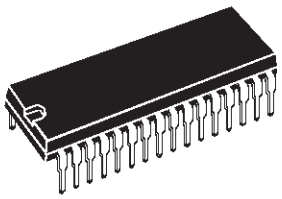
The TDA9110 is a monolithic integrated circuit assembled in 32-pin shrunk dual in line plastic package. This IC controls all the functions related to the horizontal and vertical deflection in multimode or multi-frequency computer display monitors.

The internal synchro processor, combined with the very powerful geometry correction block make the TDA9110 suitable for very high performance monitors with very few external components.

The horizontal jitter level is extremely low. (Typical standard deviation : 300ps @ 31kHz).

It is particularly well suited for high-end 15” and 17” monitors.

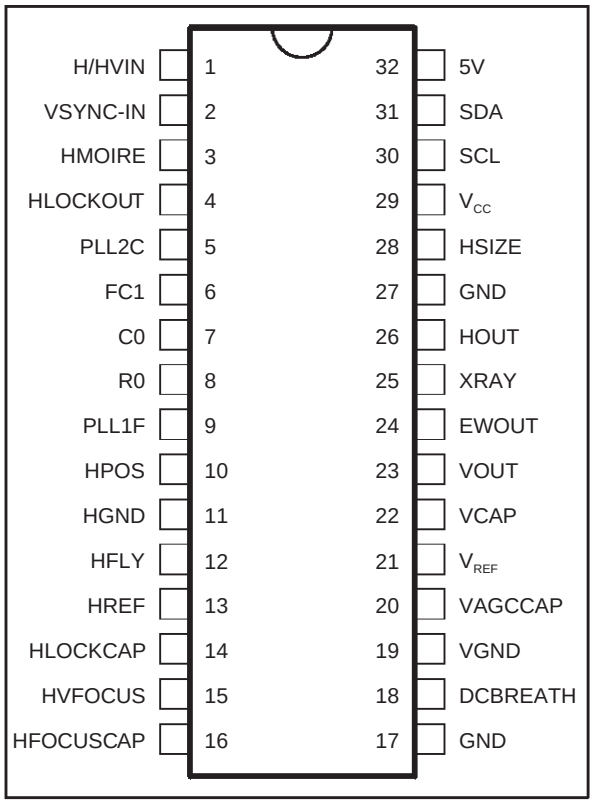
Combined with ST7275 Microcontroller family, TDA9206 (Video preamplifier) and STV942x (On-Screen Display controller) the TDA9110 allows to built fully I^2C bus controlled computer display monitors, with a reduce number of external components.



SHRINK32
(Plastic Package)

ORDER CODE : TDA9110

PIN CONNECTIONS



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PIN CONNECTIONS

Pin	Name	Function
1	H/HVIN	TTL compatible Horizontal Synchro Input
2	VSYNCIN	TTL compatible Vertical Synchro Input (for separated H&V)
3	HMOIRE	Horizontal Moire Output (to be connected to PLL2C through a resistor divider)
4	HLOCKOUT	First PLL Lock/Unlock Output (0V unlocked - 5V locked)
5	PLL2C	Second PLL Loop Filter
6	FC1	High Threshold VCO Decoupling Filter
7	C0	Horizontal Oscillator Capacitor
8	R0	Horizontal Oscillator Resistor
9	PLL1F	First PLL Loop Filter
10	HPOS	Horizontal Position Decoupling Filter
11	HGND	Horizontal Section Ground
12	HFLY	Horizontal Flyback Input (positive polarity)
13	HREF	Horizontal Section Reference Voltage (to be filtered)
14	HLOCKCAP	First PLL Lock/Unlock Time Constant Capacitor
15	FOCUSOUT	Mixed Horizontal and Vertical Dynamic Focus Output
16	HFOCUSCAP	Horizontal Dynamic Focus Oscillator Capacitor
17	GND	Ground (related internal reference)
18	BREATH	DC Breathing Input Control
19	VGND	Vertical Section Ground
20	VAGCCAP	Memory Capacitor for Automatic Gain Control Loop in Vertical Ramp Generator
21	V_{REF}	Vertical Section Reference Voltage (to be filtered)
22	VCAP	Vertical Sawtooth Generator Capacitor
23	VOUT	Vertical Ramp Output (with frequency independant amplitude and S or C Corrections if any). It is mixed with vertical position reference voltage output and vertical moire.
24	EWOUT	East/West Pincushion Correction Parabola Output
25	XRAY	X-RAY protection input (with internal latch function)
26	HOUT	Horizontal Drive Output (int. trans. open collector)
27	GND	General Ground (referenced to V_{CC})
28	HSIZE	DC HSize Control Output
29	V_{CC}	Supply Voltage (12V Typ)
30	SCL	I^2C Clock Input
31	SDA	I^2C Data Input
32	5V	Supply Voltage (5V Typ.)

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QUICK REFERENCE DATA

Parameter	Value	Unit
Horizontal Frequency	15 to 150	kHz
Autosynch Frequency (for given R0 and C0)	1 to 4.5 F0	
± Horizontal Synchro Polarity Input	YES	
Polarity Detection (on both Horizontal and Vertical Sections)	YES	
TTL Composite Synchro	YES	
Lock/Unlock Identification (on both Horizontal 1st PLL and Vertical Section)	YES	
I^2C Control for H-Position	± 10	%
XRay Protection	YES	
I^2C Horizontal Duty Adjust	30 to 60	%
I^2C Free Running Adjustment	NO	
Stand-by Function	YES	
Two Polarities H-Drive Outputs	NO	
Supply Voltage Monitoring	YES	
PLL1 Inhibition Possibility	NO	
Horizontal Blanking Output	YES	
Vertical Frequency	35 to 200	Hz
Vertical Autosync (for 150nF)	50 to 150	Hz
Vertical S-Correction	YES	
Vertical C-Correction	YES	
Vertical Amplitude Adjustment	YES	
DC Breathing Control on Vertical Amplitude	YES	
Vertical Position Adjustment	YES	
East/West Parabola Output	YES	
Pin Cushion Correction Amplitude Adjustment	YES	
Keystone Adjustment	YES	
Internal Dynamic Horizontal Phase Control	YES	
Side Pin Balance Amplitude Adjustment	YES	
Parallelogram Adjustment	YES	
Tracking of Geometric Corrections	YES	
Reference Voltage (both on Horizontal and Vertical)	YES	
Dynamic Focus (both Horizontal and Vertical)	YES	
I^2C Horizontal Dynamic Focus Amplitude Adjustment	YES	
I^2C Horizontal Dynamic Focus Keystone Adjustment	YES	
I^2C Vertical Dynamic Focus Amplitude Adjustment	YES	
Type of Input Synchro Detection (supplied by 5V Digital Supply)	YES	
Vertical Moiré Output	YES	
I^2C Controlled V-Moiré Amplitude	YES	
Frequency Generator for Burn-in	NO	
Fast I^2C Read/Write	400	kHz
Horizontal Moiré Output	YES	
I^2C controlled H-Moiré Amplitude	YES	
DC HSize Output Amplitude Control	YES	

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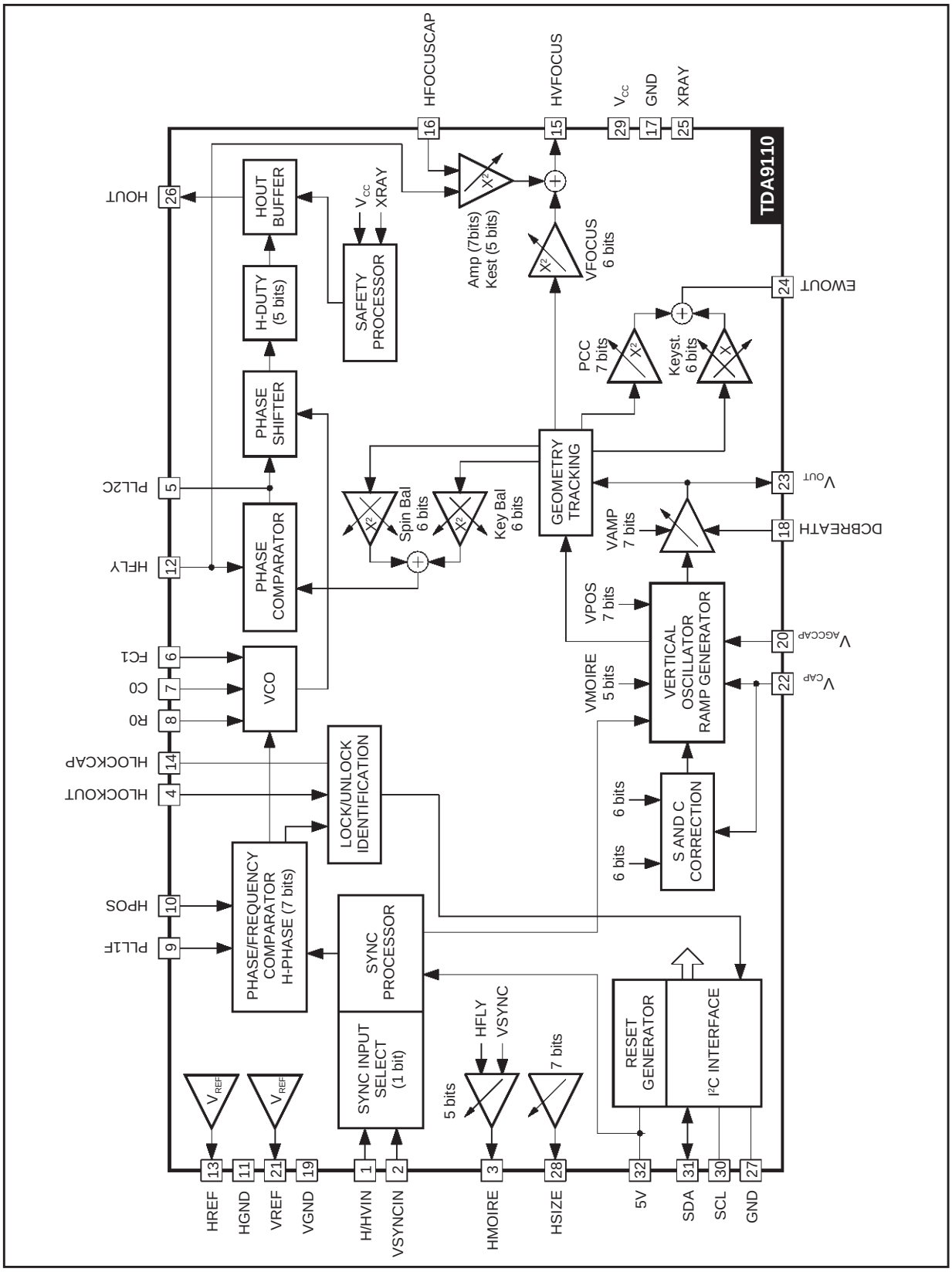
BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage (Pin 29)	13.5	V
V_{DD}	Supply Voltage (Pin 32)	5.7	V
V_{IN}	Max Voltage on Pin 12 Pin 5 Pin 16 Pin 7 Pins 8, 9, 14, 20, 22 Pin 15, 18, 23, 24, 25, 26, 28 Pins 1, 2, 3, 4, 30, 31	1.8 4.0 5.5 6.4 8.0 V_{CC} V_{DD}	V V V V V V V
VESD	ESD susceptibility Human Body Model,100pF Discharge through 1.5kΩ EIAJ Norm,200pF Discharge through 0Ω	2 300	kV V
HSize Cur	Max. Sourced Current (Pin 28) Max. Sunk Current (Pin 28)	2.5 100	mA µA
T_{stg}	Storage Temperature	-40, +150	°C
T_j	Junction Temperature	+150	°C
T_{oper}	Operating Temperature	0, +70	°C

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THERMAL DATA

Symbol	Parameter	Value	Unit
$R_{th\ (j-a)}$	Junction-ambient Thermal Resistance Max.	65	°C/W

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SYNCHRO PROCESSOR

Operating Conditions (V_{DD} = 5V, T_{amb} = 25°C)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
HsVR	Horizontal Synchro Input Voltage	Pin 1	0		5	V
MinD	Minimum Horizontal Input Pulses Duration	Pin 1	0.7			µs
Mduty	Maximum Horizontal Input Signal Duty Cycle	Pin 1			25	%
VsVR	Vertical Synchro Input Voltage	Pin 2	0		5	V
VSW	Minimum Vertical Synchro Pulse Width	Pin 2	5			µs
VSmD	Maximum Vertical Synchro Input Duty Cycle	Pin 2			15	%
VextM	Maximum Vertical Synchro Width on TTL H/Vcomposite	Pin 1			750	µs

Electrical Characteristics (V_{DD} = 5V, T_{amb} = 25°C)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
VINTH	Horizontal and Vertical Input Threshold Voltage (Pins 1, 2)	Low Level High Level	 2.2		0.8	V V
RIN	Horizontal and Vertical Pull-Up Resistor	Pins 1, 2		200		kΩ
VOut	Output Voltage (Pin 4)	Low level High Level		0 5		V V
TfrOut	Falling and Rising Output CMOS Buffer	Pin 4, Cout = 20pF			200	ns
VHlock	Horizontal 1st PLL Lock Output Status (Pin 4)	Locked Unlocked		0 5		V V
VoutT	Extracted Vsync Integration Time (% of T_H) on H/V Composite	C0 = 820pF	26	35		%

I²C READ/WRITE

Electrical Characteristics (V_{DD} = 5V,T_{amb} = 25°C)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I²C PROCESSOR						
Fscl	Maximum Clock Frequency	Pin 30			400	kHz
Tlow	Low period of the SCL Clock	Pin 30	1.3			µs
Thigh	High period of the SCL Clock	Pin 30	0.6			µs
Vinth	SDA and SCL Input Threshold	Pins 30,31		2.2		V
VACK	Acknowledge Output Voltage on SDA input with 3mA	Pin 31			0.4	V

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See also I²C Table Control and I2C Sub Address Control

HORIZONTAL SECTION
Operating Conditions

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
VCO						
$R_{0(Min.)}$	Minimum Oscillator Resistor	Pin 8	4			kΩ
$C_{0(Min.)}$	Minimum Oscillator Capacitor	Pin 7	390			pF
$F_{(Max.)}$	Maximum Oscillator Frequency				150	kHz
OUTPUT SECTION						
I12m	Maximum Input Peak Current	Pin 12			2	mA
HOI	Horizontal Drive Output Maximum Current	Pin 26, Sunk current			30	mA

Electrical Characteristics (V_{CC} = 12V, T_{amb} = 25°C)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
SUPPLY AND REFERENCE VOLTAGES						
V_{CC}	Supply Voltage	Pin 29	10.8	12	13.2	V
V_{DD}	Supply Voltage	Pin 32	4.5	5	5.5	V
I_{CC}	Supply Current	Pin 29		50		mA
I_{DD}	Supply Current	Pin 32		5		mA
V_{REF-H}	Horizontal Reference Voltage	Pin 13, I = 5mA	7.4	8	8.6	V
V_{REF-V}	Vertical Reference Voltage	Pin 21, I = 5mA	7.4	8	8.6	V
I_{REF-H}	Max. Sourced Current on V_{REF-H}	Pin 13			5	mA
I_{REF-V}	Max. Sourced Current on V_{REF-V}	Pin 21			5	mA
1st PLL SECTION						
HpolT	Polarity Integration Delay		0.75			ms
V_{VCO}	VCO Control Voltage (Pin9) V_{REF-H} = 8V f_0 f_H(Max.)		V_{REF-H} / 6 6.2			 V V
Vcog	VCO Gain (Pin 9)	R_0 = 5.9kΩ, C_0 = 820pF, dF/dV = $1/11R_0C_0$		18.8		kHz
Hph	Horizontal Phase Adjustment	% of Horizontal Period		±10		%
Hphmin Hphtyp Hphmax	Horizontal Phase Setting Value Minimum Value Typical Value Maximum Value	Sub-Address 01 Byte x1111111 Byte x1000000 Byte x0000000		 2.6 3.2 3.8		 V V V
f_0	Free Running Frequency	R_0 = 5.9kΩ, C_0 = 820pF, $f_0 = 0.97/8R_0C_0$		25		kHz
dF0/dT	Free Running Frequency Thermal Drift (No drift on external components)	See Note		-150		ppm/C
CR	PLL1 Capture Range	R_0 = 6.49kΩ, C_0 = 820pF, from f_0+0.5kHz to $4.5F_0$ f_H(Min.) f_H(Max.) Component accuracy : C_0 = 2%, R_0 = 1%	 100		 28	 kHz kHz

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Note : This parameter is not tested on each unit. It is measured during our internal qualification.

HORIZONTAL SECTION (continued)
Electrical Characteristics (V_{CC} = 12V, T_{amb} = 25°C) (continued)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
2nd PLL SECTION AND HORIZONTAL OUTPUT SECTION						
FBth	Flyback Input Threshold Voltage (Pin 12)		0.65	0.75		V
Hjit	Horizontal Jitter	Horizontal Freq. = 31kHz		60		ppm
HDmin HDmax	Horizontal Drive Output Duty-Cycle (Pin 26) (see Notes 1 & 2) Low Level High Level	Sub-Address 00 Byte xxx11111 Byte xxx00000		 30 60		 % %
XRAYth	X-RAY Protection Input Threshold Voltage	Pin 25		8		V
Vphi2	Internal Clamping Levels on 2nd PLL Loop Filter (Pin 5)	Low Level High Level		1.6 3.7		V V
VSCinh	Threshold Voltage To Stop H-Out,V-Out when V_{CC} < VSCinh	Pin 29		7.5		V
HDvd	Horizontal Drive Output (low level)	Pin 26 I_{OUT} = 30mA			0.4	V
HORIZONTAL DYNAMIC FOCUS FUNCTION						
HDFst	Horizontal Dynamic Focus Sawtooth Minimum Level Maximum Level	HfocusCap = C_0 = 820pF, TH=TBD, Pin 16		 2 4.7		 V V
HDFdis	Horizontal Dynamic Focus Sawtooth Discharge Width	Start by HDFstart		400		ns
HDFstart	Internal fixed Phase Advance versus Hfly Middle	Fixed for each frequency (Pin 16)		860		ns
HDFDC	Bottom DC Output Level	R_{LOAD} = 10kΩ, Pin 15		2		V
TDHDF	DC Output Voltage Thermal Drift			200		ppm/C
HDFamp	Horizontal Dynamic Focus Amplitude Min Byte x1111111 Typ Byte x1000000 Max Byte x0000000	Sub-Address 03, Pin 15, FH = 50kHz, Keystone Typ		 1.1 1.7 3.5		 V_{PP} V_{PP} V_{PP}
HDFKeyst	Horizontal Dynamic Focus Keystone Min A/B Byte xxx11111 Typ Byte xxx10000 Max A/B Byte xxx00000	Sub-Address 04, FH = 50kHz, Typ Amp B/A A/B A/B		 2.5 1.0 2.5		
VERTICAL DYNAMIC FOCUS FUNCTION (positive parabola)						
AMPVDF	Vertical Dynamic Focus Parabola (added to horizontal one) Amplitude with VOUT and VPOS Typical Min. Byte 000000 Typ. Byte 100000 Max. Byte 111111	Sub-Address 0F		 0 0.5 1		 V_{PP} V_{PP} V_{PP}
VDFAMP	Parabola Amplitude Function of VAMP (tracking between VAMP and VDF) with VPOS Typ. (see Figure 1 and Note 3)	Sub-Address 05 Byte 10000000 Byte 11000000 Byte 11111111		 0.6 1 1.5		 V_{PP} V_{PP} V_{PP}
VHDFKeyt	Parabola Assymetry Function of VPOS Control (tracking between VPOS and VDF) with VAMP Max.	Sub-Address 06 Byte x0000000 Byte x1111111		 0.52 0.52		

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Notes : 1. Duty Cycle is the ratio of power transistor OFF time period. Power transistor is OFF when output transistor is OFF.
2. Initial Condition for Safe Operation Start Up
3. S and C correction are inhibited so the output sawtooth has a linear shape.

VERTICAL SECTION
Operating Conditions

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
OUTPUTS SECTION						
VEWM	Maximum EW Output Voltage	Pin 24			6.5	V
VEWm	Minimum EW Output Voltage	Pin 24	1.8			V
R_{LOAD}	Minimum Load for less than 1% Vertical Amplitude Drift	Pin 20	65			MΩ

Electrical Characteristics (V_{CC} = 12V, T_{amb} = 25°C)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
VERTICAL RAMP SECTION						
VRB	Voltage at Ramp Bottom Point	V_{REF-V}=8V, Pin 22		2		V
VRT	Voltage at Ramp Top Point (with Synchro) V_{REF-V}	Pin 22		5		V
VRTF	Voltage at Ramp Top Point (without Synchro)	Pin 22		VRT-0.1		V
VSTD	Vertical Sawtooth Discharge Time Duration (Pin 22)	With 150nF Cap		70		µs
VFRF	Vertical Free Running Frequency (see Notes 4 & 5)	$C_{OSC\ (Pin\ 22)}$ = 150nF Measured on Pin22		100		Hz
ASFR	AUTO-SYNC Frequency	C_{22} = 150nF ±5% See Note 6	50		165	Hz
RAFD	Ramp Amplitude Drift versus Frequency at Maximum Vertical Amplitude	C_{22} = 150nF 50Hz < f and f < 165Hz		200		ppm/Hz
Rlin	Ramp Linearity on Pin 22 (see Notes 4 & 5)	2.5 < V_{22} and V_{22} < 4.5V		0.5		%
Vpos	Vertical Position Adjustment Voltage (Pin23 - VOUT centering)	Sub Address 06 Byte x0000000 Byte x1000000 Byte x1111111	 3.65	 3.2 3.5 3.8	 3.3 	 V V V
VOR	Vertical Output Voltage (peak-to-peak on Pin 23)	Sub Address 05 Byte x0000000 Byte x1000000 Byte x1111111	 3.5	 2.25 3 3.75	 2.5 	 V V V
VOI	Vertical Output Maximum Current (Pin23)			±5		mA
dVS	Max Vertical S-Correction Amplitude x0xxxxxx inhibits S-CORR x1111111 gives max S-CORR	Subaddress 07 $\Delta V/V_{PP}$ at T/4 $\Delta V/V_{PP}$ at 3T/4		 -4 +4		 % %
Ccorr	Vertical C-Corr Amplitude x0xxxxxx inhibits C-CORR	SubAddress 08 Byte x1000000 Byte x1100000 Byte x1111111		 -3 0 3		 % % %

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Notes : 4. With Register 07 at Byte x0xxxxxx (Vertical S-Correction Control) then the S correction is inhibited, consequently the sawtooth has a linear shape.
5. With Register 08 at Byte x0xxxxxx (Vertical C - Correction Control) then the C correction is inhibited, consequently the sawtooth has a linear shape.
6. It is the frequency range for which the VERTICAL OSCILLATOR will automatically synchronize, using a single capacitor value on Pin 22 and with a constant ramp amplitude.

VERTICAL SECTION (continued)
Electrical Characteristics (V_{CC} = 12V, T_{amb} = 25°C) (continued)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
EAST/WEST FUNCTION						
EW_{DC}	DC Output Voltage with Typ Vpos,Keystone, Corner and Corner Balance Inhibited	Pin 24, see Figure 2		2.5		V
$TDEW_{DC}$	DC Output Voltage Thermal Drift	See Note 7		100		ppm/C
EWpara	Parabola Amplitude with Vamp Max, V-Pos Typ, Keystone Inhibited	Subaddress 0A Byte 11111111 Byte 10100000 Byte 10000000		 2.5 1.25 0		 V V V
EWtrack	Parabola Amplitude Function of V-AMP Control (tracking between V-AMP and E/W) with Typ Vpos, Keystone, EW Typ Amplitude (see Note 8)	Subaddress 05 Byte 10000000 Byte 11000000 Byte 11111111		 0.45 0.8 1.25		 V V V
KeyAdj	Keystone Adjustment Capability with Typ Vpos, EW Inhibited and Vertical Amplitude Max. (see Note 8 and Figure 4)	Subaddress 09 Byte 1x000000 Byte 1x111111		 0.9 0.9		 V_{PP} V_{PP}
KeyTrack	Intrinsic Keystone Function of V-POS Control (tracking between V-POS and EW) with EW Max Amplitude and Vertical Amplitude Max. (see Note 8) A/B Ratio B/A Ratio	Subaddress 06 Byte x0000000 Byte x1111111		 0.52 0.52		
DC HSIZE OUTPUT CONTROL						
HSize out	DC HSize Output Level (Pin 28)	Subaddress 0B Byte 00000000 Byte 01000000 Byte 01111111		 0.5 2.5 4.5		 V V V
INTERNAL HORIZONTAL DYNAMIC PHASE CONTROL FUNCTION						
SPBpara	Side Pin Balance Parabola Amplitude (Figure 3) with Vamp Max, V-POS Typ and Parallelogram Inhibited (see Notes 8 & 9)	Subaddress 0D Byte x1111111 Byte x1000000		 +1.4 -1.4		 %TH %TH
SPBtrack	Side Pin Balance Parabola Amplitude function of Vamp Control (tracking between Vamp and SPB) with SPB Max, V-POS Typ and Parallelogram Inhibited (see Notes 8 & 9)	Subaddress 05 Byte 10000000 Byte 11000000 Byte 11111111		 0.5 0.9 1.4		 %TH %TH %TH
ParAdj	Parallelogram Adjustment Capability with Vamp Max, V-POS Typ and SPB Max (see Notes 8 & 9)	Subaddress 0E Byte x1111111 Byte x1000000		 +1.4 -1.4		 %TH %TH
Partrack	Intrinsic Parallelogram Function of Vpos Control (tracking between V-Pos and DHPC) with Vamp Max, SPB Max and Parallelogram Inhibited (see Notes 8 & 9) A/B Ratio B/A Ratio	Subaddress 06 Byte x0000000 Byte x1111111		 0.52 0.52		
VERTICAL MOIRE						
VMOIRE	Vertical Moire (measured on VOUTDC) (Pin 23)	Subaddress 0C Byte 01x11111		 6		 mV
BREATHING COMPENSATION						
BRADj	Vertical Output Variation versus DC Breathing Control (Pin 23)	$V_{18} > V_{REF-V}$ $V_{18} = V_{REF-V}$ $V_{18} = V_{REF-V}$ - 4V		0 0 -10		% % %

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Notes : 7. These parameters are not tested on each unit. They are measured during our internal qualification
8. Refers to Notes 4 & 5 from last section.
9. TH is the Horizontal PLL Period Duration.

Figure 1 : Vertical Dynamic Focus Function

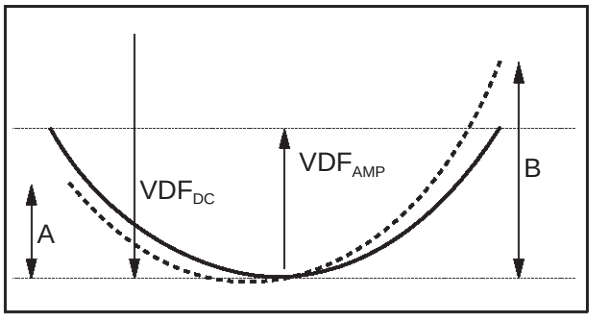


Figure 2 : E/W Output

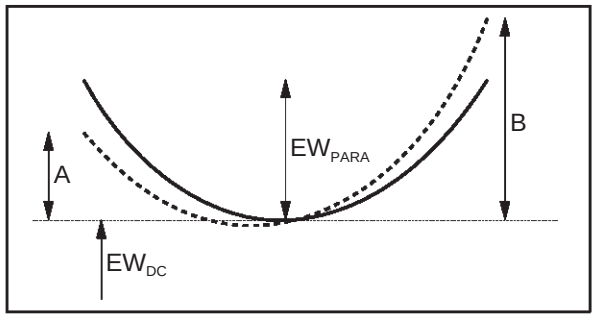


Figure 3 : Dynamic Horizontal Phase Control Output

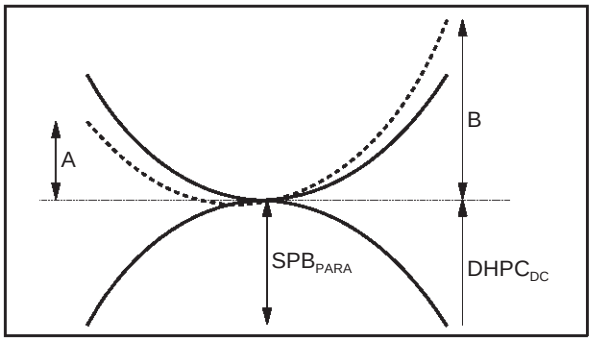
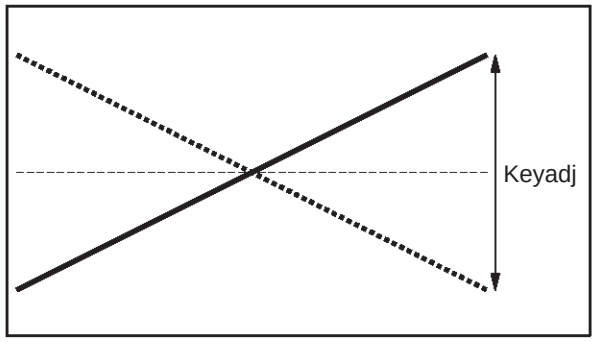
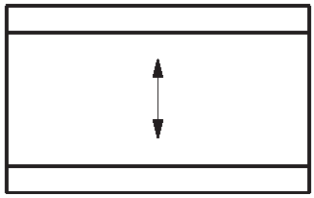
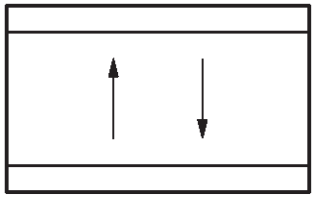
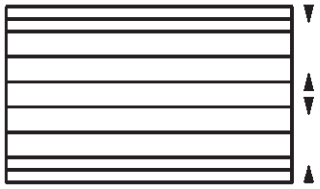
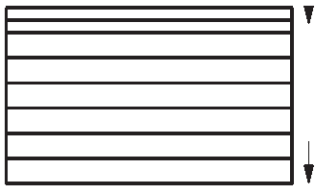


Figure 4 : Keystone Effect on E/W Output (PCC Inhibited)

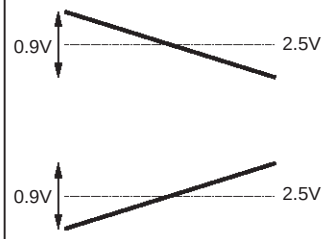
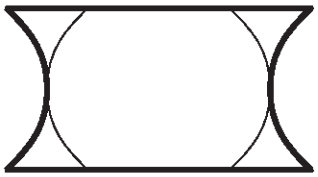
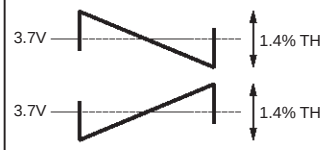
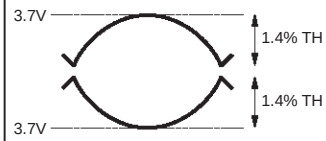
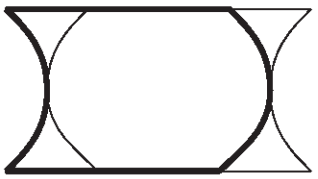
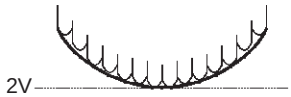


TYPICAL VERTICAL OUTPUT WAVEFORMS

Function	Sub Address	Pin	Byte	Specification	Picture Image
Vertical Size	05	23	10000000 11111111	V_{OUTDC} 2.25V V_{OUTDC} 3.75V	
Vertical Position DC Control	06	23	x0000000 x1000000 x1111111	3.2V 3.5V 3.8V	
Vertical S Linearity	07	23	0xxxxxxx Inhibited 1x111111	ΔV V_{PP} $\frac{\Delta V}{V_{PP}} = 4\%$	
Vertical C Linearity	08	23	1x000000 1x111111	ΔV V_{PP} $\frac{\Delta V}{V_{PP}} = 3\%$ ΔV V_{PP} $\frac{\Delta V}{V_{PP}} = 3\%$	

9110-06.TBL / 9110-07.EPS TO 9110-13.EPS

GEOMETRY OUTPUT WAVEFORMS

Function	Sub Address	Pin	Byte	Specification	Picture Image
Trapezoid Control	09	24	EWamp Inhibited. 1X000000 1X111111		
Pin Cushion Control	0A	24	Keystone Inhibited 10000000 11111111		
Parrallelogram Control	0E	Internal	SPB Inhibited 1x000000 1x111111		
Side Pin Balance Control	0D	Internal	Parallelogram Inhibited 1x000000 1x111111		
Vertical Dynamic Focus with Horizontal		32			

9110-07.TBL / 9110-14.EPS TO 9110-22.EPS

I²C BUS ADDRESS TABLE

Sub Address Definition

Slave Address (8C) : *Write Mode*

	D8	D7	D6	D5	D4	D3	D2	D1	
0	x	x	x	x	0	0	0	0	Horizontal Drive Selection / Horizontal Duty Cycle
1	x	x	x	x	0	0	0	1	Horizontal Position
2	x	x	x	x	0	0	1	0	Horizontal Moiré Control
3	x	x	x	x	0	0	1	1	Synchro Priority / Horizontal Focus Amplitude
4	x	x	x	x	0	1	0	0	Refresh / Horizontal Focus Keystone
5	x	x	x	x	0	1	0	1	Vertical Ramp Amplitude
6	x	x	x	x	0	1	1	0	Vertical Position Adjustment
7	x	x	x	x	0	1	1	1	S Correction
8	x	x	x	x	1	0	0	0	C Correction
9	x	x	x	x	1	0	0	1	E/W Keystone
A	x	x	x	x	1	0	1	0	E/W Amplitude
B	x	x	x	x	1	0	1	1	Horizontal Size Control
C	x	x	x	x	1	1	0	0	Vertical Moiré
D	x	x	x	x	1	1	0	1	Side Pin Balance
E	x	x	x	x	1	1	1	0	Parallelogram
F	x	x	x	x	1	1	1	1	Vertical Dynamic Focus Amplitude

Slave Address (8D) : *Read Mode*

	D8	D7	D6	D5	D4	D3	D2	D1	
0	x	x	x	x	0	0	0	0	Synchro and Polarity Detection

I^2C BUS ADDRESS TABLE (continued)

	D8	D7	D6	D5	D4	D3	D2	D1
WRITE MODE								
00		HDrive 0, off [1], on		Horizontal Duty Cycle				
				[0]	[0]	[0]	[0]	[0]
01	Xray 1, reset [0]	Horizontal Phase Adjustment						
		[1]	[0]	[0]	[0]	[0]	[0]	[0]
02	HMoire 1, on [0], off			Horizontal Moire Amplitude				
				[0]	[0]	[0]	[0]	[0]
03	Sync 0, Comp [1], Sep	Horizontal Focus Amplitude						
		[1]	[0]	[0]	[0]	[0]	[0]	[0]
04	Detect Refresh [0], off			Horizontal Focus Keystone				
				[1]	[0]	[0]	[0]	[0]
05	Vramp 0, off [1], on	Vertical Ramp Amplitude Adjustment						
		[1]	[0]	[0]	[0]	[0]	[0]	[0]
06		Vertical Position Adjustment						
		[1]	[0]	[0]	[0]	[0]	[0]	[0]
07	S Select 1, on [0]		S Correction					
			[1]	[0]	[0]	[0]	[0]	[0]
08	C Select 1, on [0]		C Correction					
			[1]	[0]	[0]	[0]	[0]	[0]
09	EW Key 0, off [1]		East/West Keystone					
			[1]	[0]	[0]	[0]	[0]	[0]
0A	EW Sel 0, off [1]	East/West Amplitude						
		[1]	[0]	[0]	[0]	[0]	[0]	[0]
0B	Test H 1, on [0], off	HSize Control						
		[1]	[0]	[0]	[0]	[0]	[0]	[0]
0C	Test V 1, on [0], off	Moire 1, on [0]		Vertical Moire				
				[0]	[0]	[0]	[0]	[0]
0D	SPB Sel 0, off [1]		Side Pin Balance					
			[1]	[0]	[0]	[0]	[0]	[0]
0E	Parallelo 0, off [1]		Parallelogram					
			[1]	[0]	[0]	[0]	[0]	[0]
0F			Vertical Dynamic Focus Amplitude					
			[1]	[0]	[0]	[0]	[0]	[0]
READ MODE								
00	Hlock 0, on [1], no	Vlock 0, on [1], no	Xray 1, on [0], off	Polarity Detection		Synchro Detection		
				H/V pol [1], negative	V pol [1], negative	Vext det [0], no det	H/V det [0], no det	V det [0], no det

[ ] initial value

Data are transferred with vertical sawtooth retrace.

OPERATING DESCRIPTION

I - GENERAL CONSIDERATIONS

I.1 - Power Supply

The typical values of the power supply voltages V_{CC} and V_{DD} are 12V and 5V respectively. Perfect operation is obtained for V_{CC} between 10.8 and 13.2V and V_{DD} between 4.5 and 5.5V.
In order to avoid erratic operation of the circuit during transient phase of V_{CC} switching on, or off, the value of V_{CC} is monitored and the outputs of the circuit are inhibited if V_{CC} is less than 7.5V typically.
Similarly,V_{DD} is monitored and internally set-up until V_{DD} reaches 4V (see I^2C Control Table for power on reset).
In order to have a very good power supply rejection, the circuit is internally supplied by several voltage references (typical value : 8V). Two of these voltage references are externally accessible, one for the vertical and one for the horizontal part. If needed, these voltage references can be used (if I_{LOAD} is less than 5mA). It is necessary to filter the a.m. voltage references by external capacitors connected to ground, in order to minimize the noise and consequently the "jitter" on vertical and horizontal output signals.

I.2 - I^2C Control

TDA9110 belongs to the I^2C controlled device family. Instead of being controlled by DC voltages on dedicated control pins, each adjustment can be done via the I^2C Interface.
The I^2C bus is a serial bus with a clock and a data input. The general function and the bus protocol are specified in the Philips-bus data sheets.
The interface (Data and Clock) is TTL-level compatible. The internal threshold level of the input comparator is 2.2V (when V_{DD} is 5V). Spikes (up to 50ns) are filtered by an integrator and the clock speed is limited to 400kHz.
The data line (SDA) can be used bidirectionally (i.e. in read-mode the IC clocks out a reply information (1 byte) to the micro-processor).
The bus protocol prescribes always a full-byte transmission. The first byte after the start condition is used to transmit the IC-address(7 bits-8C) and the read/write bit (0 write - 1 read).

I.3 - Write Mode

In write mode the second byte sent contains the subaddress of the selected function to adjust (or controls to affect) and the third byte the corresponding data byte. It is possible to send more than one data byte to the IC. If after the third byte no stop or start condition is detected, the circuit increments automatically by one the momentary subaddress in the subaddress counter (auto-increment mode). So it is possible to transmit immediately the next data bytes without sending the IC address or subaddress. It can be useful to reinitialize the whole controls very quickly (flash manner). This procedure can be finished by a stop condition.
The circuit has 16 adjustment capabilities : 2 for the Horizontal part, 4 for the Vertical, 2 for the E/W correction, 2 for the Dynamic Horizontal phase control, 2 for the Moire options, 3 for the Horizontal and Vertical Dynamic Focus and 1 for the HSize amplitude control.
15 bits are also dedicated to several controls (ON/OFF, Synchro Priority, Detection Refresh and Xray reset).

I.4 - Read Mode

During the read mode the second byte transmits the reply information.
The reply byte contains the Horizontal and Vertical Lock/Unlock status, the Xray activation status and, the Horizontal and Vertical polarity detection. It also contains the Synchro detection status which is used by the MCU to assign the Synchro priority.
A stop condition always stops all the activities of the bus decoder and switches to high impedance both for the data and the clock line (SDA and SCL).
See I^2C Subaddress and control tables.

I.5 - Synchro Processor

The internal Synchro Processor allows the TDA9110 to accept any kind of input synchro signals :
- separated Horizontal & Vertical TTL-compatible synchro signals,
- composite Horizontal &Vertical TTL-compatible synchro signals.

I.6 - Synchro Identification Status

The MCU can choose via the I^2C the synchro priority thanks to the system identification status provided by the TDA9110. The extracted Vertical synchro pulse is available when this identification status has been received and when the 12V is supplied. Even in Power management mode the IC is able to inform the MCU that synchro signals were detected due to its 5V supply. We recommend to use the device as following : first, refresh the synchro detection by I^2C, then check the status of H/V det and Vdet by I^2C read.

Sync priority choice should be :

Vext det	H/V det	V det	Sync priority Subaddress 03		Comment
			D8	D7	Synchro type
No	Yes	Yes	1	1	Separated H & V
Yes	Yes	No	0	1	Composite TTL H&V

OPERATING DESCRIPTION (continued)

Of course, when the choice is done, we can refresh the synchro detections and verify that the extracted Vsync is present and that no synchro type change have occured.

Synchro processor is also giving synchro polarity information.

I.7 - IC status

The IC can inform the MCU about the 1st Horizontal PLL or Vertical section status (locked or not), and about the Xray protection (activated or not).

Resetting the Xray internal latch can be done either by decreasing the V_{CC} supply or directly resetting via the I^2C interface.

I.8 - Synchro Inputs

Both H/HVin and Vsyncin inputs are TTL compatible triggers with Hysterisis to avoid erratic detection. It includes pull up resistor to V_{DD}.

I.9 - Synchro Processor Output

The synchro processor delivers the Hlockout signal on a TTL-compatible CMOS output.

Hlockout is the Horizontal 1st PLL status (5V when locked). It allows the MCU to check the Horizontal IC locking.

II - HORIZONTAL PART

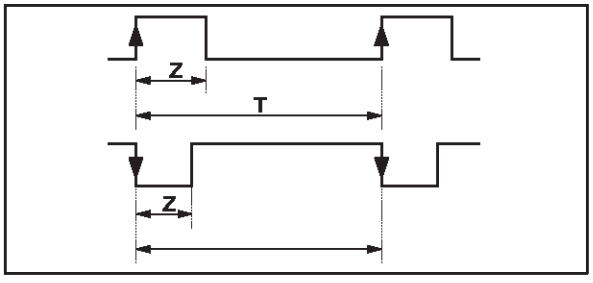
II.1 - Internal Input Conditions

A digital signal (Horizontal synchro pulse or TTL composite) is sent by the synchro processor to the horizontal part.

Positive or negative signal can be applied to the Horizontal part input (see Figure 6).

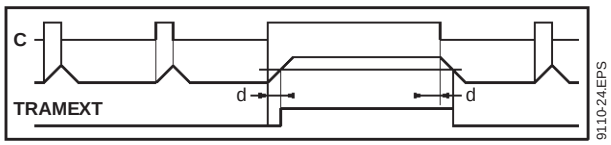
Using internal integration, both signals are recognized if Z/T < 25%. Synchronization occurs on the leading edge of the internal synchro signal. The minimum value of Z is 0.7µs.

Figure 6



An other integration is able to extract vertical pulse of composite synchro if duty cycle is higher than 25% (typically d = 35%) (see Figure 7).

Figure 7



The last feature performed is the removing of equalizing pulses to avoid parasitic pulses on phase comparator input (which is sensitive to wrong or missing pulses).

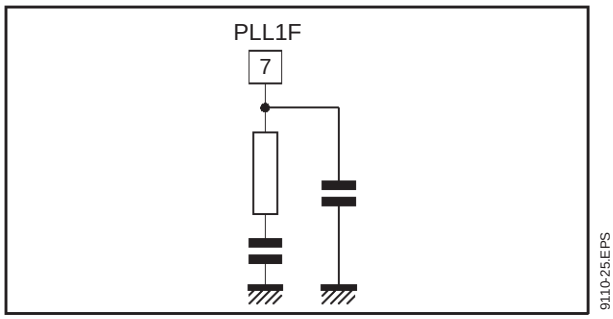
II.2 - PLL1

The PLL1 consists of a phase comparator, an external filter and a voltage control oscillator (VCO).

The phase comparator is a "phase frequency" type designed in CMOS technology. This kind of phase detector avoids locking on false frequencies. It is followed by a "charge pump", composed of two current sources sunk and sourced (Typically I = 1mA when locked and I = 140µA when unlocked). This difference between lock/unlock permits a smooth catching of the horizontal frequency by the PLL1. This effect is reinforced by an internal original slow down system when the PLL1 is locked, avoiding the Horizontal frequency to change too fast.

The dynamic behaviour of the PLL1 is fixed by an external filter which integrates the current of the charge pump. A "CRC" filter is generally used (see Figure 8).

Figure 8



The PLL1 is internally inhibited during extracted vertical synchro (if any) to avoid taking in account missing pulses or wrong pulses on phase comparator. The inhibition results from the opening of a switch located between the charge pump and the filter (see Figure 9).

The VCO uses an external RC network. It delivers a linear sawtooth obtained by the charge and the discharge of the capacitor, with a current proportionnal to the current in the resistor. The typical thresholds of the sawtooth are 1.6V and 6.4V.

OPERATING DESCRIPTION (continued)

Figure 9 : Principle Diagram

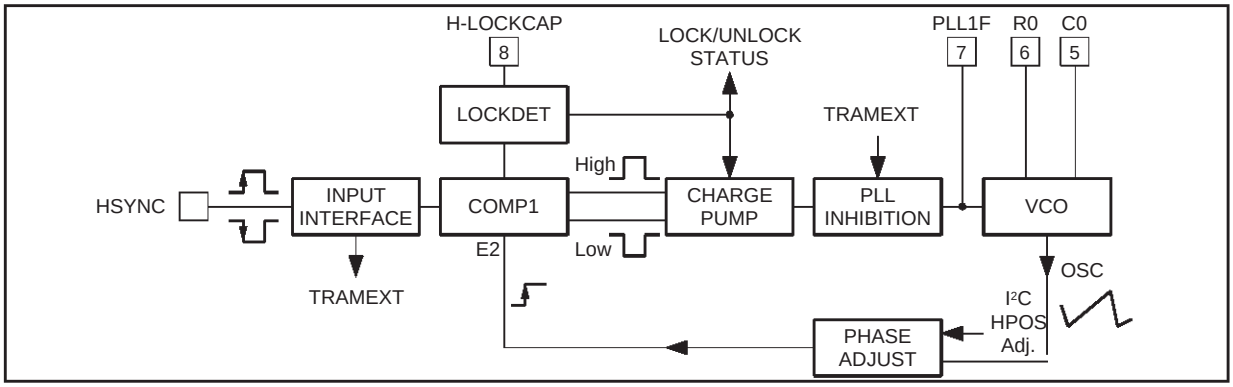
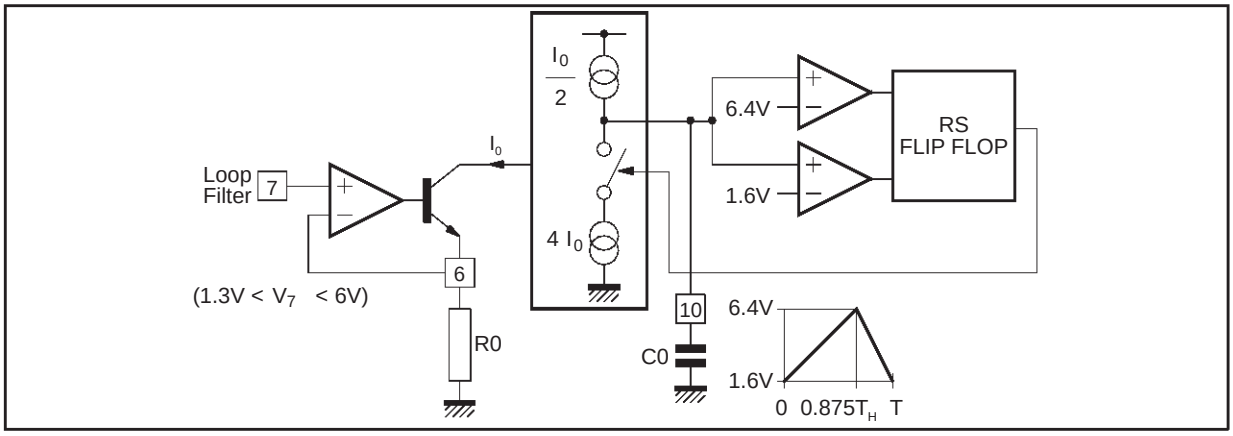


Figure 10 : Details of VCO

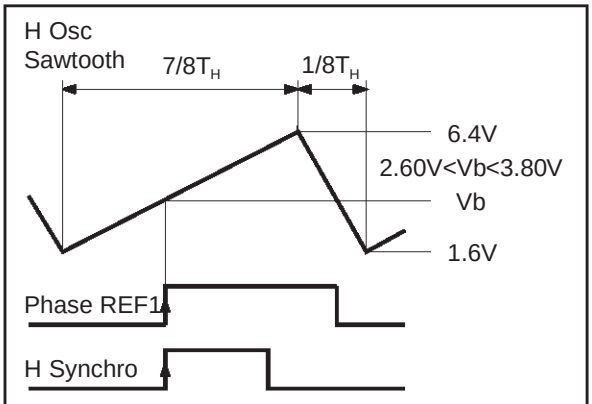


The control voltage of the VCO is between 1.33V and 6V (see Figure 10). The theorical frequency range of this VCO is in the ratio of 1 to 4.5. The effective frequency range has to be smaller (1 to 4.2) due to clamp intervention on filter lowest value. In order to increase this effective frequency range, to a possible range of 1 to 6.0 one can add a resistor from Pin 6 to Href leading.

The synchro frequency must always be higher than the free running frequency. For example, when using a synchro range between 31kHz and 96kHz, the suggested free running frequency is 25kHz.

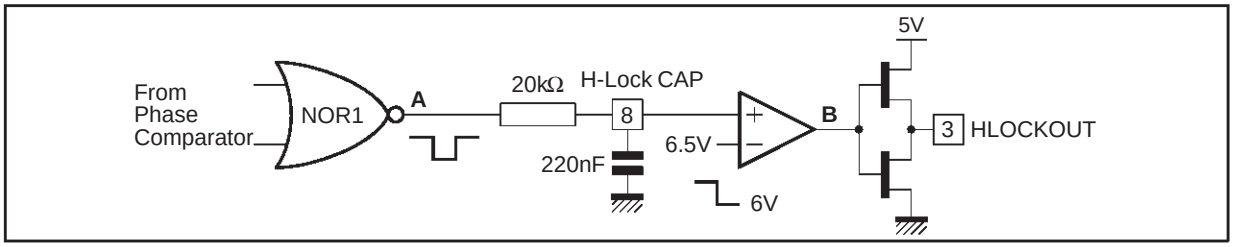
The PLL1 ensures the coincidence between the leading edge of the synchro signal and a phase reference obtained by comparison between the sawtooth of the VCO and an internal DC voltage which is I^2C adjustable between 2.65V and 3.75V (corresponding to ± 10%) (see Figure 11).

Figure 11 : PLL1 Timing Diagram



OPERATING DESCRIPTION (continued)

Figure 12 : LOCK/UNLOCK Block Diagram



The TDA9110 also includes a Lock/Unlock identification block which senses in real time whether the the PLL1 is locked or not on the incoming horizontal synchro signal. The resulting information is available on Hlockout (see Synchro Processor). The block function is described in Figure 12.

The NOR1 gate receive the phase comparator output pulses (which also drive the charge pump). When the PLL1 is locked, we have on point A a very small negative pulse (about 100ns) at each horizontal cycle, so after the RC filter, there is a high level on Pin 14 which forces Hlockout to high level. The hysterisis comparator detects locking when Pin 14 reachs 6.5V and unlocking when Pin 14 decreases to 6.0V.

When the PLL1 is unlocked, the 100ns negative pulse on A becomes much larger and consequently the average level on Pin 14 decreases. It forces Hlockout to low level.

The Pin 14 status is approximately the following :
- near 0V when there is no H-Sync
- between 0 and 4V with H-Sync frequency different from VCO
- between 4 to 8 V when VCO frequency reaches H-Sync one (but not already in phase)
- near 8V when PLL1 is locked.

It is important to notice that Pin 14 is not an output pin but is only used for filtering purpose (see Figure 12).

The lock/unlock information is also available through the I^2C read.

II.3 - PLL2

The PLL2 ensures a constant position of the shaped flyback signal in comparison with the sawtooth of the VCO (Figure 13).

The phase comparator of PLL2 (phase type comparator) is followed by a charge pump (typical output current : 0.5mA).

The flyback input consists of an NPN transistor. This input must be current driven. The maximum recommanded input current is 5mA (see Figure 14).

The duty cycle is adjustable through I^2C from 30% to 60%. For Start Up safe operation, the initial duty cycle (after Power on reset) is 60% in order to avoid to have a too long conduction of the BU transistor.

The maximum storage time is about 38% ($T_{FLY}/2.T_H$). Typically, T_{FLY}/T_H is around 20% which means that Ts max is around 28%.

Figure 13 : PLL2 Timing Diagram

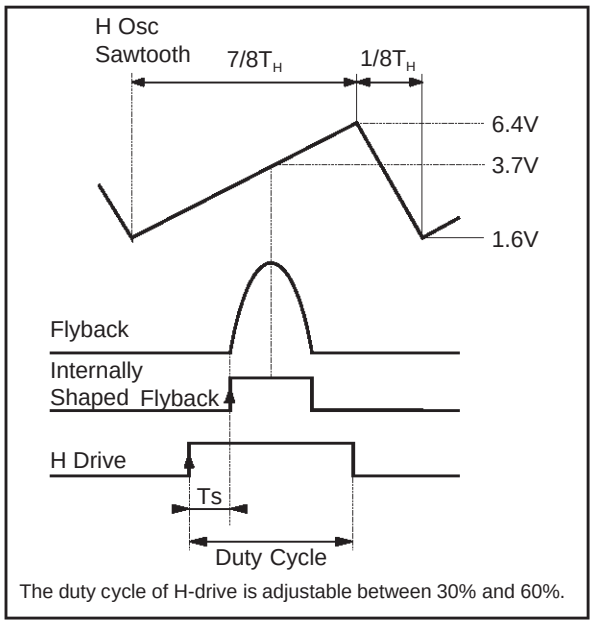
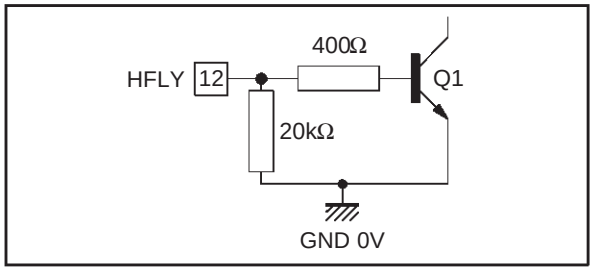


Figure 14 : Flyback Input Electrical Diagram



OPERATING DESCRIPTION (continued)

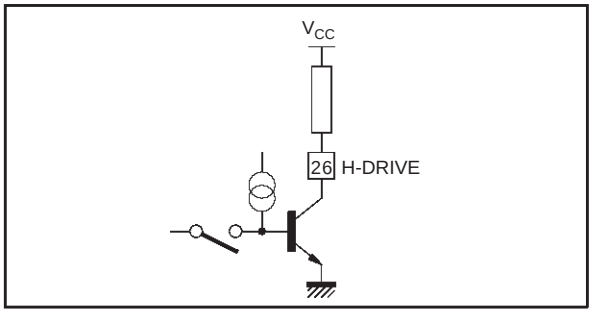
II.4 - Output Section

The H-drive signal is sent to the output through a shaping block ensuring Ts and H-drive duty cycle (I2C adjustable) (see Figure 13). In order to secure the scanning power part operation, the output is inhibited in the following cases :

- when V_{CC} is too low,
- when the Xray protection is activated,
- during the Horizontal flyback,
- when the HDrive I^2C bit control is off.

The output stage consists of a NPN bipolar transistor. Only the collector is accessible (see Figure 15).

Figure 15



The output NPN is in off-state when the power scanning transistor is also in off-state.

The maximum output current is 30mA, and the corresponding voltage drop of the output V_{CEsat} is 0.4V typically.

Obviously the power scanning transistor cannot be directly driven by the integrated circuit. An interface has to be added between the circuit and the power transistor either of bipolar or of MOS type.

II.5 - X-RAY Protection

The X-Ray protection is activated by application of a high level on the X-Ray input (8V on Pin 25). The consequencies of X-Ray protection are :

- inhibition of H-Drive output
- activation of vertical blanking output.

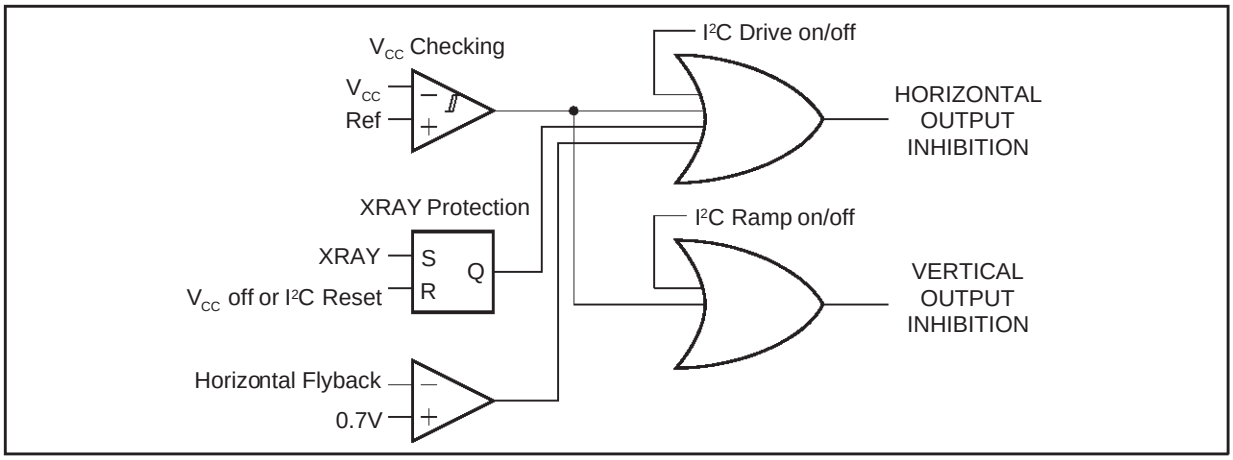
This protection is reset either by V_{CC} switch off or by I^2C (see Figure 16).

II.6 - Horizontal and Vertical Dynamic Focus

The TDA9110 delivers a horizontal parabola which is added on a vertical parabola waveform on Pin 15. This horizontal parabola comes from a sawtooth. The phase advance versus Horizontal flyback middle is kept constant for each frequency (about 860ns). This sawtooth is present on Pin 16 where the horizontal focus capacitor is the same as C0 to obtain a controlled amplitude (from 2 to 4.7V typically).

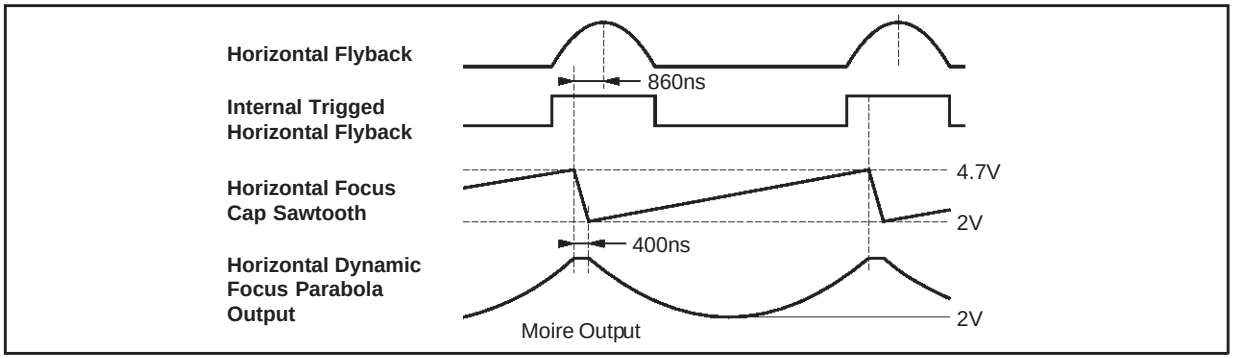
Symmetry (keystone) and amplitude are I^2C adjustable (see Figure 17). The Vertical dynamic focus is tracked with VPOS and VAMP. Its amplitude can be adjusted. It is also affected by S and C corrections. This positive signal has to be connected to the CRT focusing grids.

Figure 16 : Safety Functions Block Diagram



OPERATING DESCRIPTION (continued)

Figure 17



II.7 - Moire Output

The moire output is intented to correct a beat between the horizontal video pixel period and the current CRT pixel width.

The moire signal is a combination of the Horizontal and the Vertical frequency signals.

To achieve a moire cancellation, the moire output has to be connected to any point of the chassis controlling the horizontal position. We recommend to introduce this " Horizontal Controlled Jitter" on the relative ground of PLL2 capacitor where this "controlled jitter" frequency type will directly affect the horizontal position.

The amplitude of the signal is I^2C adjustable.

If the H-Moire feature is not necessary in the application, the H-Moire output (Pin 3) can be used as a 5 bits DAC output (0.3V to 2.2V). If the H-Moire output is not used at all, so the Pin 3 must be either kept to high impedance or grounded via a resistor.

OPERATING DESCRIPTION (continued)

III - VERTICAL PART

III.1 - Geometric Corrections

The principle is represented on Figure 20.

Starting from the vertical ramp, a parabola shaped current is generated for E/W correction, dynamic horizontal phase control correction, and vertical dynamic Focus correction.

The parabola generator is made by an analog multiplier, the output current of which is equal to :

$$\Delta I = k \cdot (V_{OUT} - V_{DCOUT})^2$$

where Vout is the vertical output ramp (typically between 2 and 5V) and Vdcout is the vertical DC output adjustable in the range 3.2V to 3.8V which generate a dissymetric parabola if needed (keystone adjustment).

In order to keep a good screen geometry for any end user preferences adjustment, we implemented the "geometry tracking".
Due to large output stages voltage range (E/W, FOCUS), the combination of tracking function with maximum vertical amplitude max or min vertical position and maximum gain on the DAC control may lead to the output stages saturation. This must be avoided by limiting the output voltage with appropriate I^2C registers values.

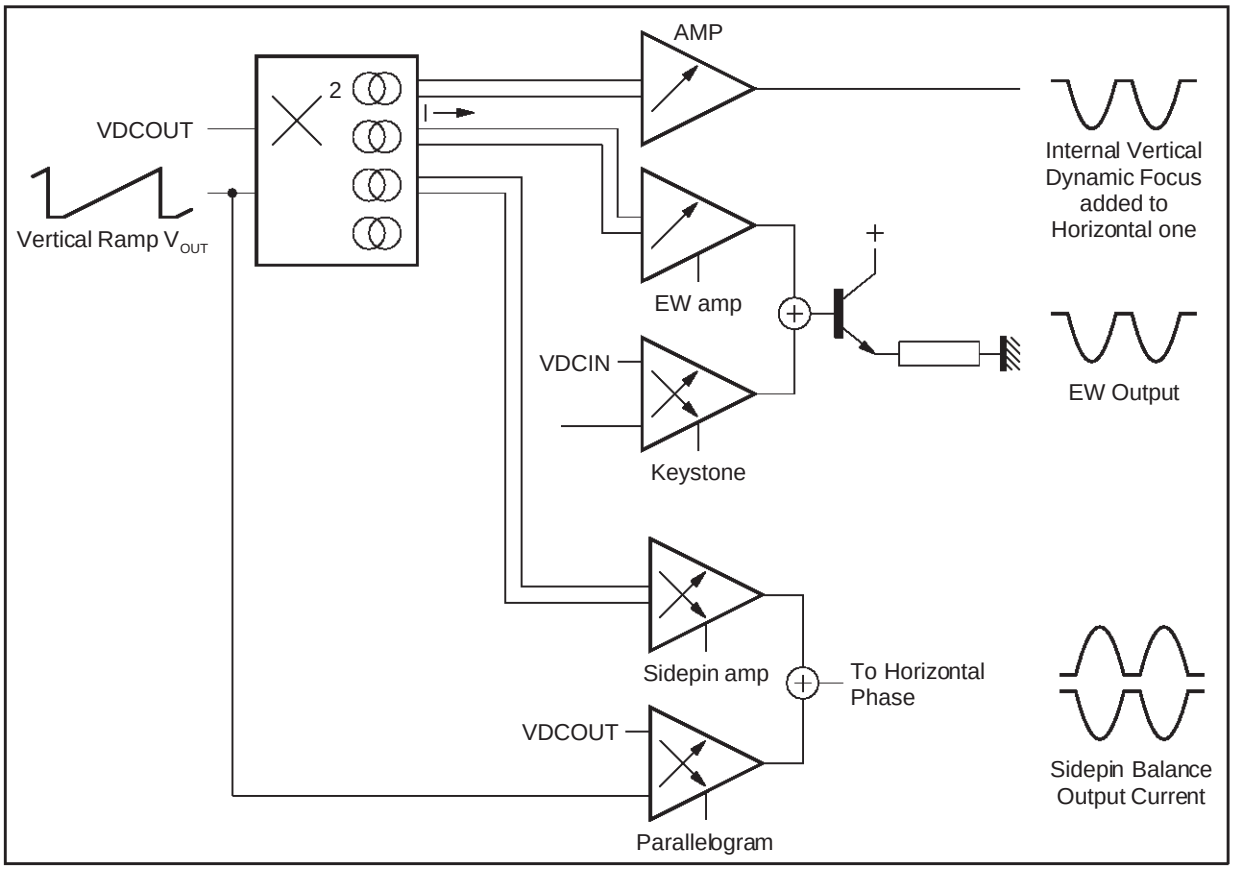
For the E/W part and the Dynamic Horizontal phase control part, a sawtooth shaped differential current in the following form is generated :

$$\Delta I' = k' \cdot (V_{OUT} - V_{DCOUT})$$

Then ΔI and $\Delta I'$ are added and converted into voltage for the E/W part.

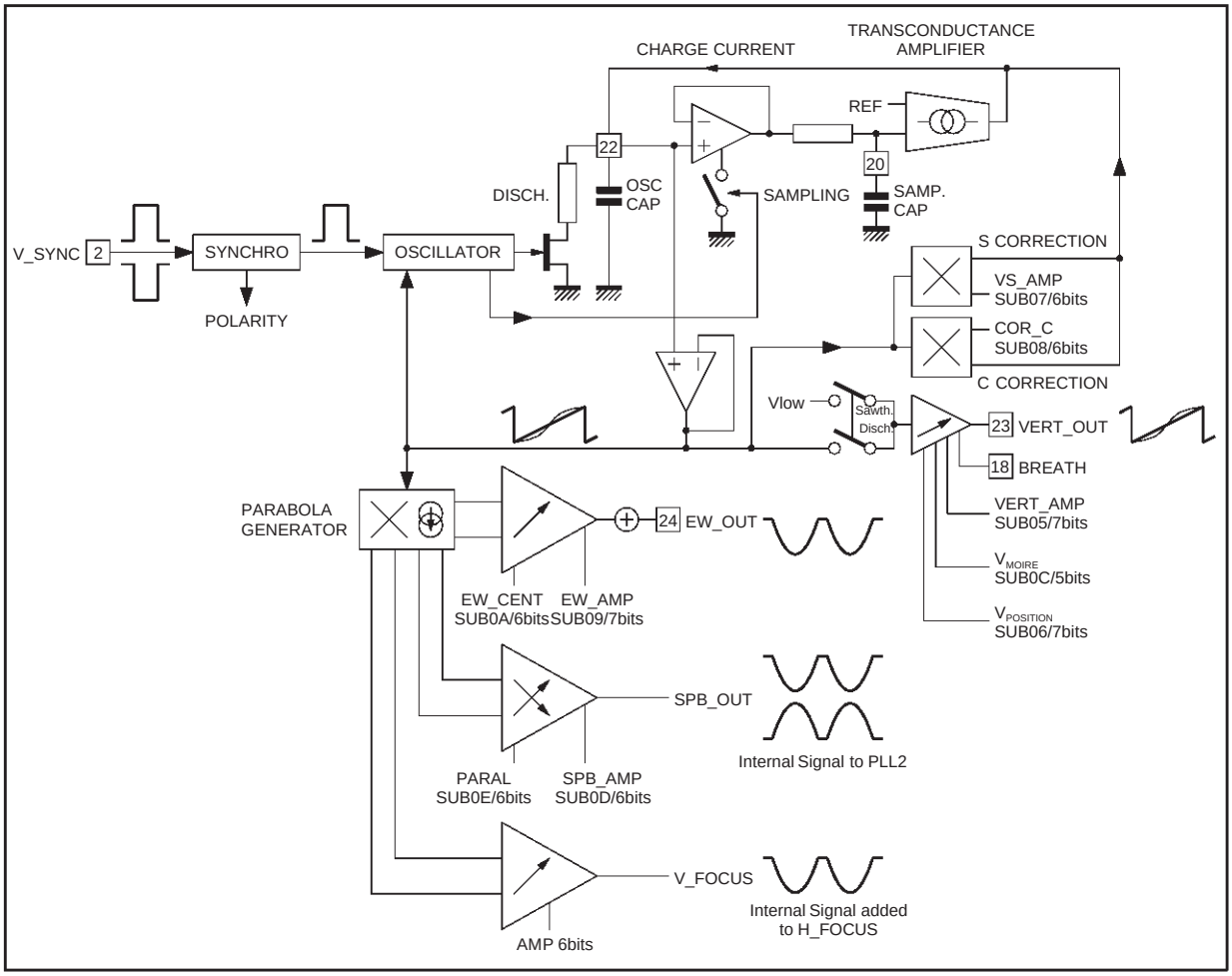
Each of the two E/W components or the two Dynamic Horizontal phase control ones may be inhibited by their own I^2C select bit.
The E/W parabola is available on Pin 24 via an emitter follower which has to be biased by an external resistor (10kΩ). It can be DC coupled with external circuitry.
The Vertical Dynamic Focus is combined with the Horizontal one on Pin 15.
The dynamic Horizontal phase control current drives internally the H-position, moving the Hfly position on the Horizontal sawtooth in the range of ± 1.4% T_H both on SidePin Balance and Parallelogram.

Figure 20 : Geometric Corrections Principle



OPERATING DESCRIPTION (continued)

Figure 21 : Vertical Part Block Diagram



III.2 - EW

$$EWOUT = 2.5V + K1\,(V_{OUT} - V_{DCOUT})^2 + K2\,(V_{OUT} - V_{DCOUT})$$

K1 is adjustable by the EW amplitude I^2C register
K2 is adjustable by the Keystone I^2C register

III.3 - DC HSize Output Control

A 7 bits D/A converter is available on Pin 28. The output is a NPN transistor emitter follower output with an internal 100mA current source from output to ground (max. sunk current). The Max. current the output is able to source is 2.5mA. The output level is between 0.5V to 4.5V. This DAC can be used to control the H-Size.

III.4 - Dynamic Horizontal Phase Control

$$I_{OUT} = K5\,(V_{OUT} - V_{DCOUT})^2 + K6\,(V_{OUT} - V_{DCOUT})$$

K5 is adjustable by the SidePin Balance I^2C register
K6 is adjustable by the Parallelogram I^2C register

III.5 - Function

When the synchronization pulse is not present, an internal current source sets the free running frequency. For an external capacitor, C_{OSC} = 150nF, the typical free running frequency is 106Hz.

The typical free running frequency can be calculated by :

$$f_0\,(Hz) = 1.6\,e^{-5} \cdot \frac{1}{C_{OSC}}$$

A negative or positive TTL level pulse applied on Pin 2 (VSYNC) as well as a TTL composite synchro on Pin 1 can synchronize the ramp in the range [fmin , fmax]. This frequency range depends on the external capacitor connected on Pin 22. A capacitor in the range [150nF, 220nF] ± 5% is recommanded for application in the following range : 50Hz to 120Hz.

OPERATING DESCRIPTION (continued)

Typical maximum and minimum frequency, at 25°C and without any correction (S correction or C correction), can be calculated by :

$$f_{(Max.)} = 2.5 \times f_0 \text{ and } f_{(Min.)} = 0.33 \times f_0$$

If S or C corrections are applied, these values are slighty affected.

If a synchronization pulse is applied, the internal oscillator is automaticaly caught but the amplitude is no more constant. An internal correction is activated to adjust it in less than a half a second : the highest voltage of the ramp Pin 22 is sampled on the sampling capacitor connected on Pin 20 at each clock pulse and a transconductance amplifier generates the charge current of the capacitor. The ramp amplitude becomes again constant.

The read status register enables to have the vertical Lock-Unlock and the vertical Synchro Polarity informations.

We recommand to use a AGC capacitor with low leakage current. A value lower than 100nA is mandatory.

A good stability of the internal closed loop is reached by a 470nF ± 5% capacitor value on Pin 20 (VAGC).

III.6 - I²C Control Adjustments

Then, S and C correction shapes can be added to this ramp. These frequence independent S and C corrections are generated internally. Their amplitudes are adjustable by their respective I²C register. They can also be inhibited by their Select bit.

Finally, the amplitude of this S and C corrected ramp can be adjusted by the vertical ramp amplitude control register.

The adjusted ramp is available on Pin 23 (V_{OUT}) to drive an external power stage.

The gain of this stage is typically 25% depending on its register value.

The DC value of this ramp is driven by its own I²C register (vertical Position). Its value is $V_{CDOUT} = 7/16 \cdot V_{REF} \pm 300mV$.

The V_{DCOUT} voltage is correlated with DC value of V_{OUT}. It increases the accuracy when temperature varies.

By using the vertical moire, V_{DCOUT} can be modulated from frame to frame. This function is intended to correct slightly the vertical video line to line period from actual CRT line to line width.

III.7 - Basic Equations

In first approximation, the amplitude of the ramp on Pin 23 (Vout) is :

$$V_{OUT} - V_{MID} = (V_{OSC} - V_{MID}) \cdot (1 + 0.25 (V_{AMP}))$$

with $V_{MID} = 7/16 \cdot V_{REF}$; typically 3.5V, the middle value of the ramp on Pin 22
$V_{OSC} = V_{22}$, ramp with fixed amplitude
V_{AMP} is -1 for minimum vertical amplitude register value and +1 for maximum

On V_{DCOUT}, the voltage (in volts) is calculated by :

$$V_{DCOUT} = V_{MID} + 0.3 \text{ (VPOS)}$$

with VPOS equals -1 for minimum vertical position register value and +1 for maximum

The current available on Pin 22 is :

$$I_{OSC} = \frac{3}{8} \cdot V_{REF} \cdot C_{OSC} \cdot f$$

with C_{OSC} : capacitor connected on Pin 22
f : synchronization frequency

INTERNAL SCHEMATICS

Figure 22

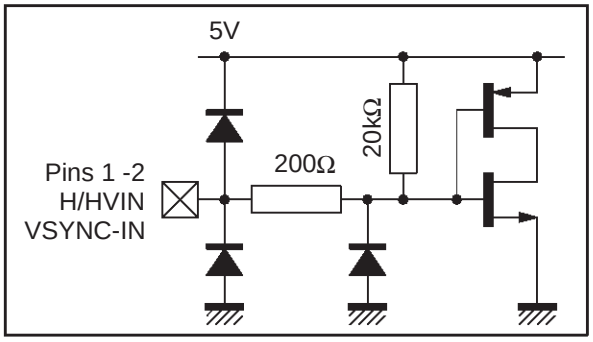


Figure 23

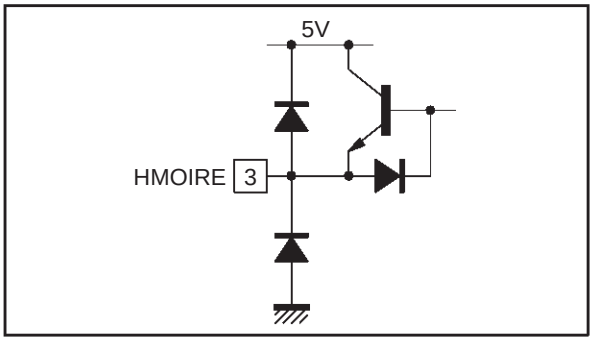


Figure 24

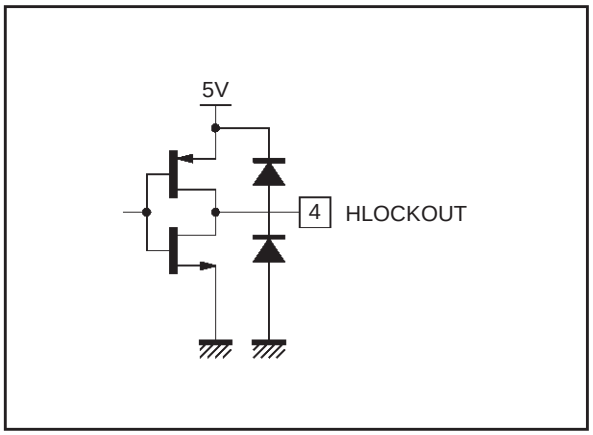


Figure 25

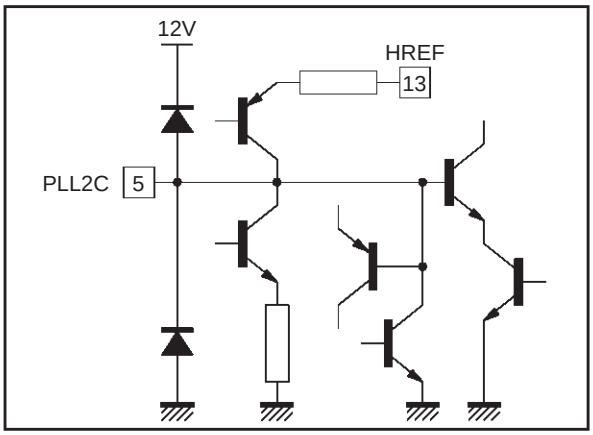


Figure 26

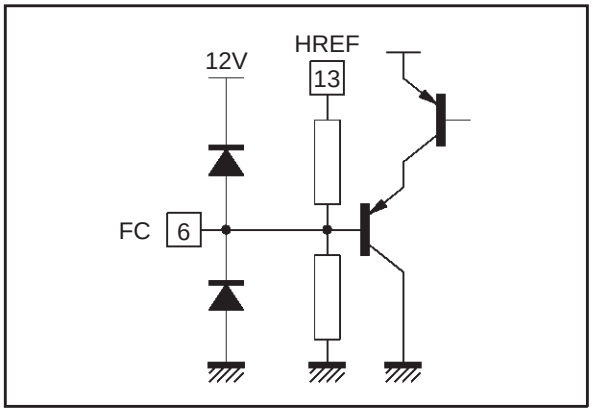
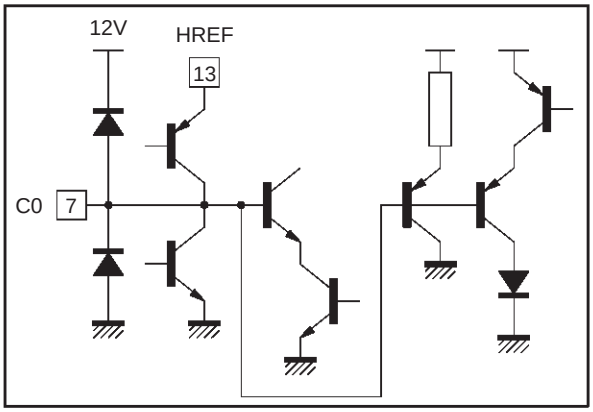


Figure 27



INTERNAL SCHEMATICS (continued)

Figure 28

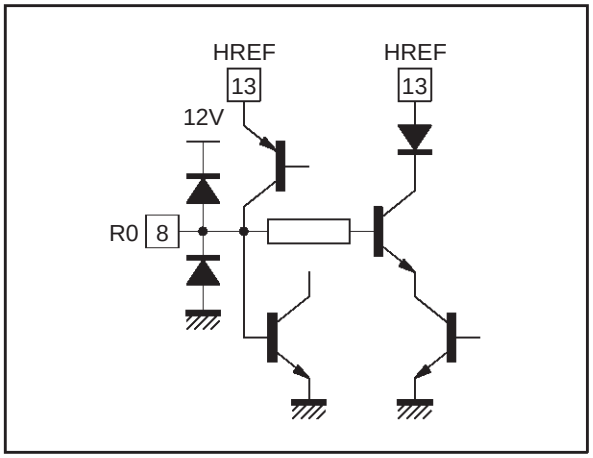


Figure 29

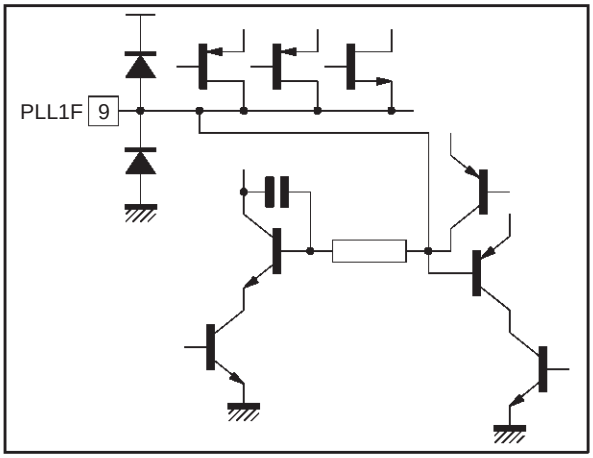


Figure 30

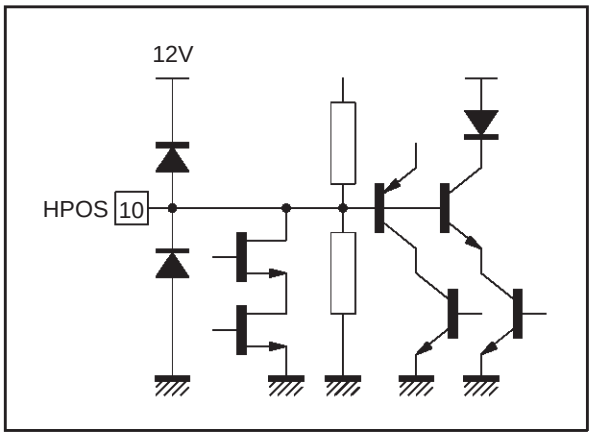


Figure 31

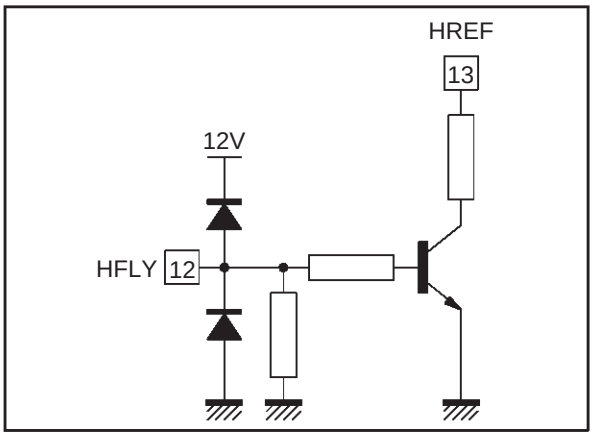


Figure 32

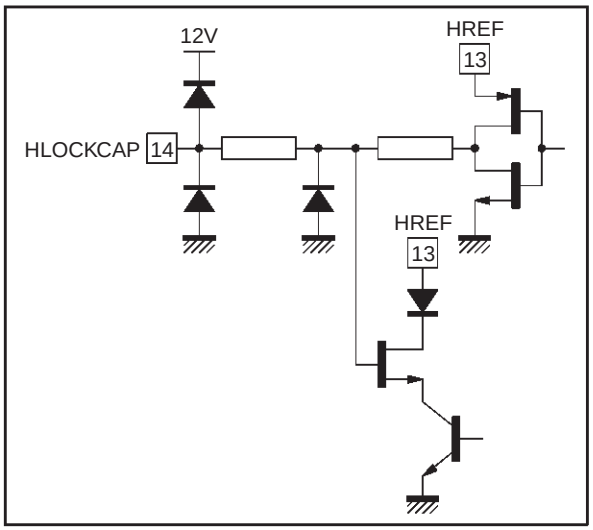
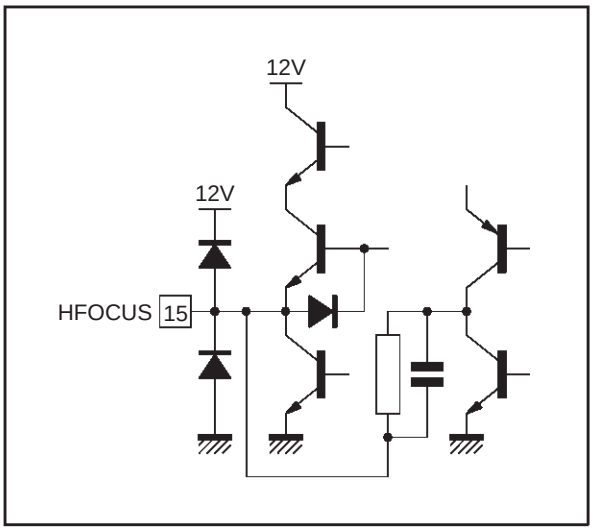


Figure 33



INTERNAL SCHEMATICS (continued)

Figure 34

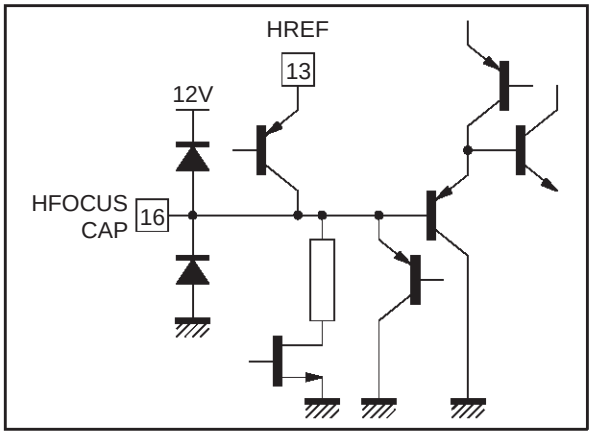


Figure 35

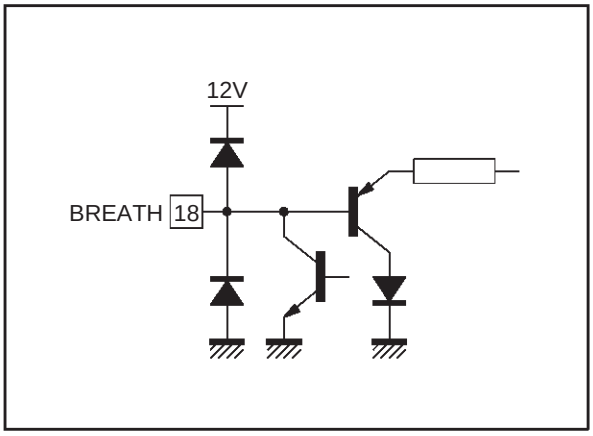


Figure 36

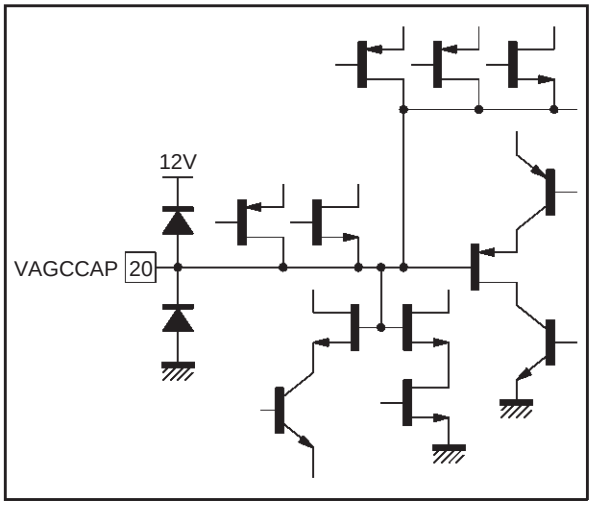


Figure 37

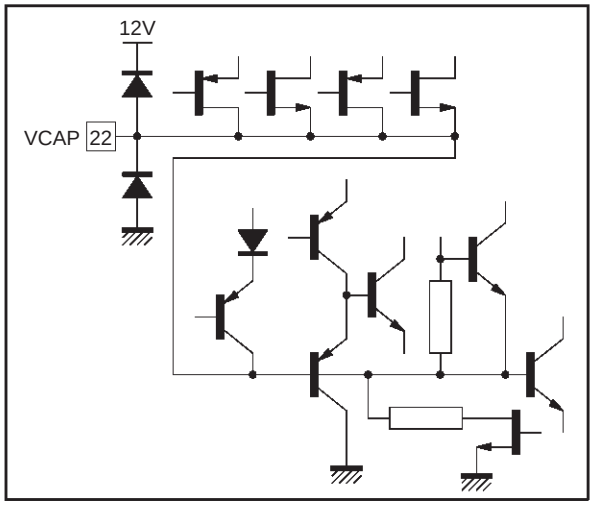


Figure 38

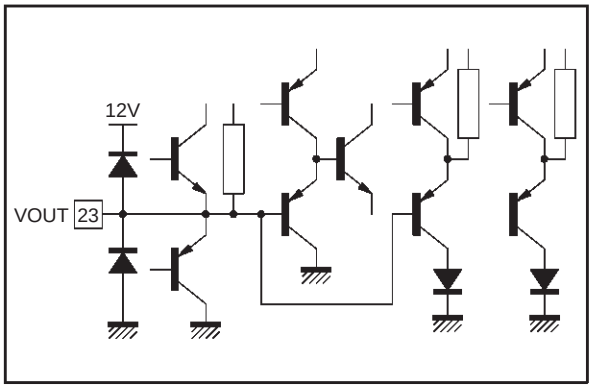
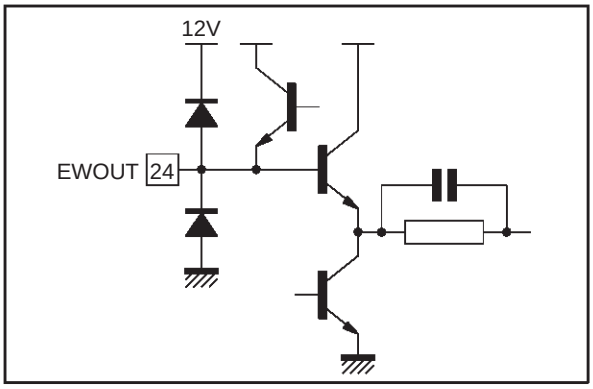


Figure 39



INTERNAL SCHEMATICS (continued)

Figure 40

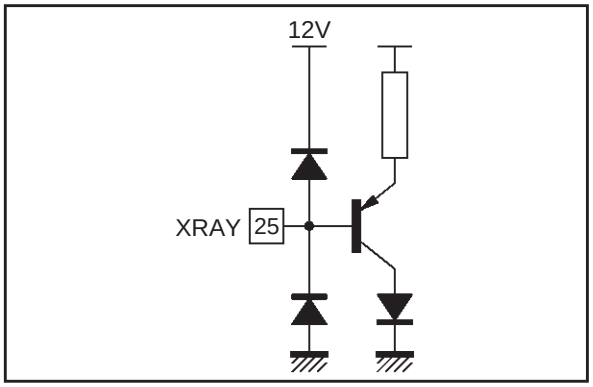


Figure 41

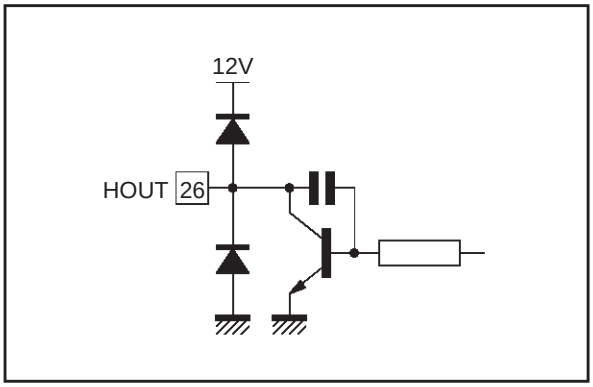


Figure 42

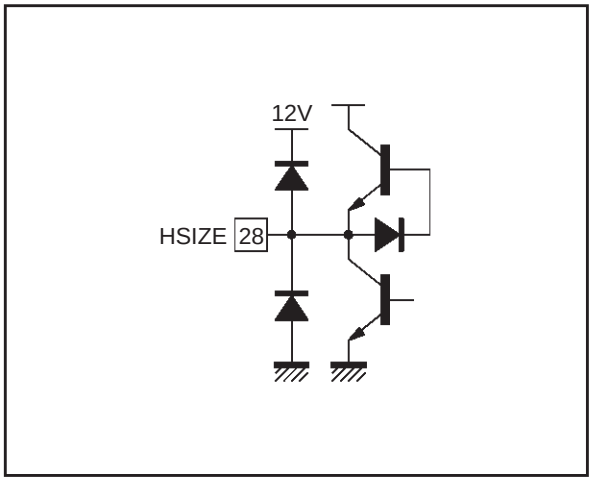
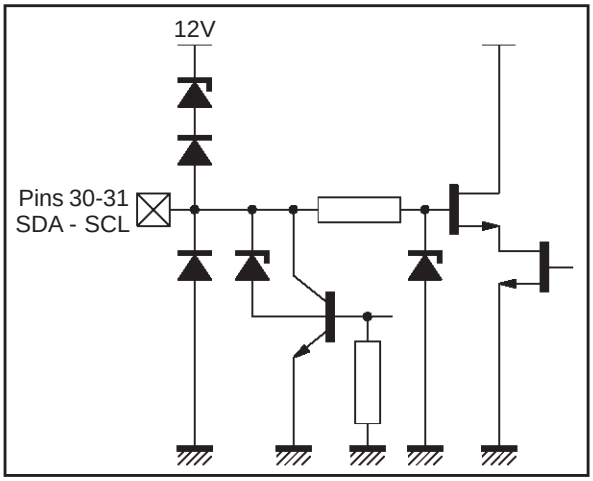
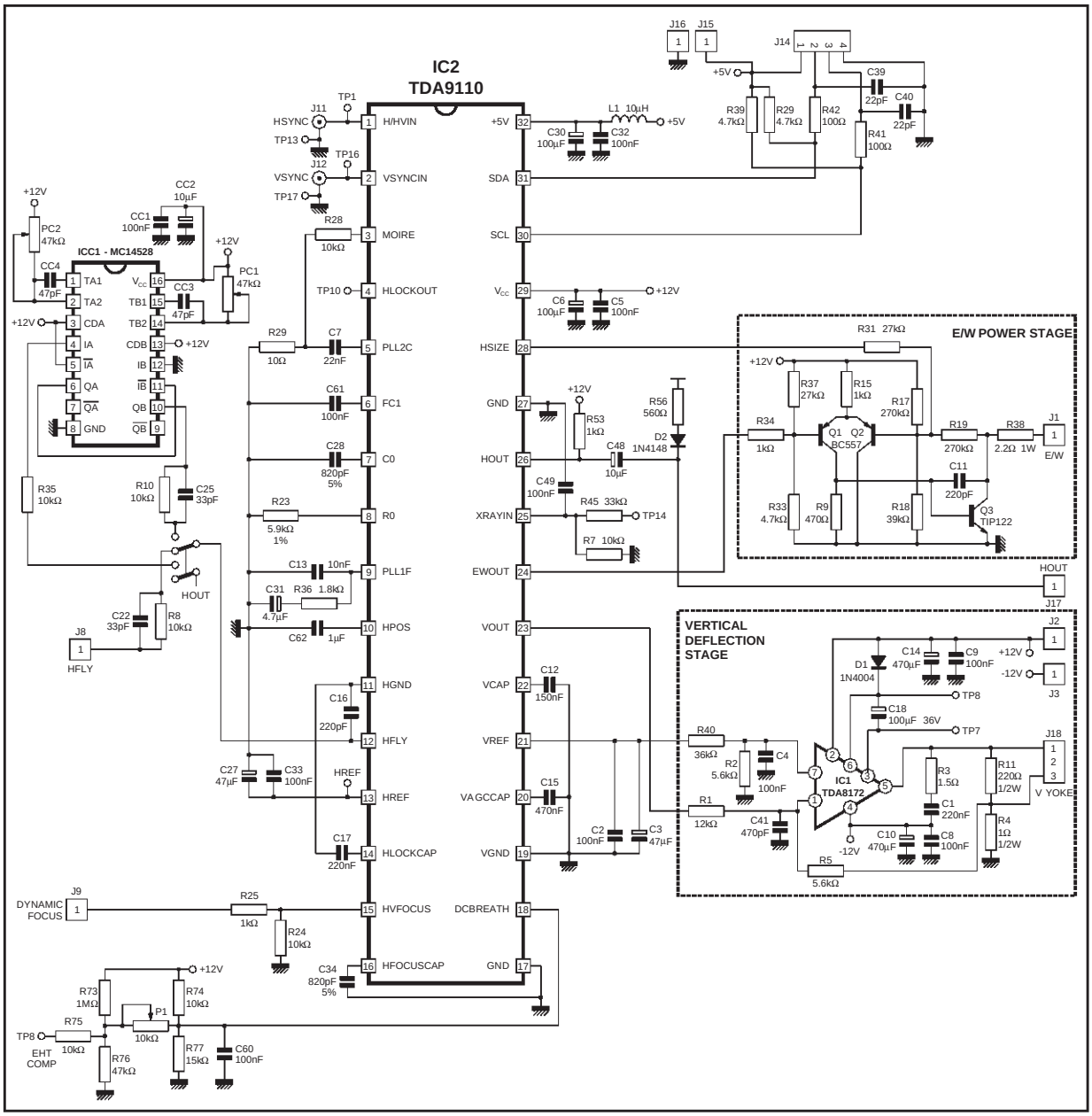


Figure 43

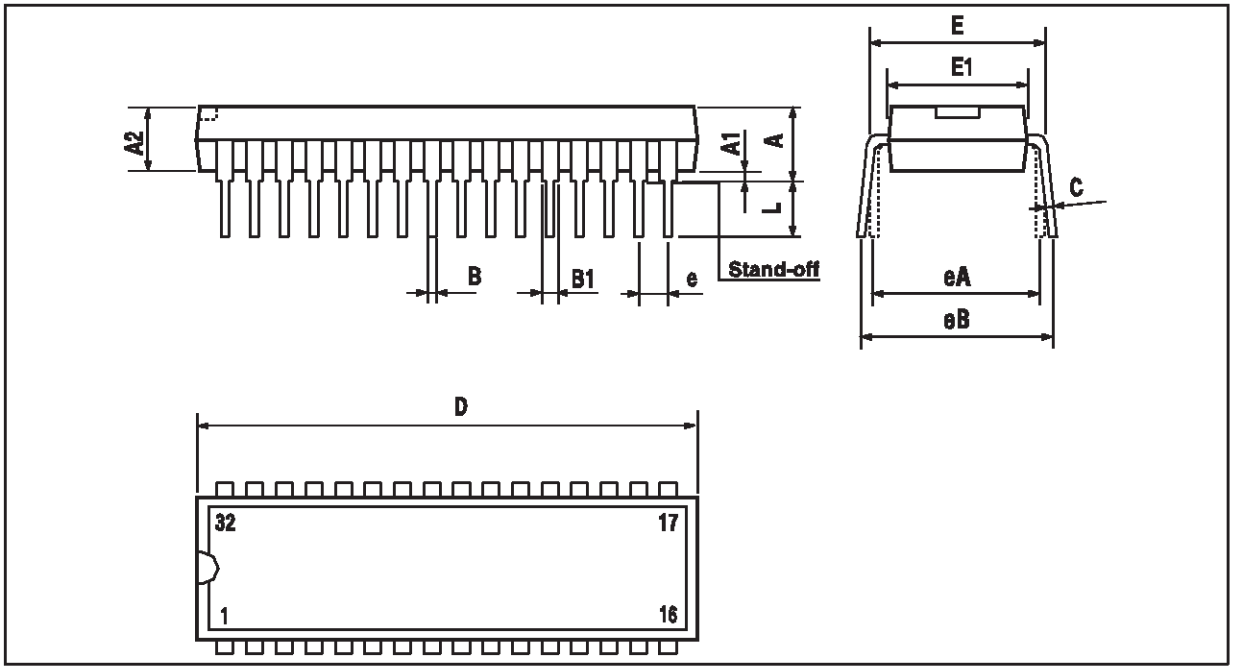


DEMONSTRATION BOARD



PACKAGE MECHANICAL DATA

32 PINS - PLASTIC SHRINK DIP



PMSDIP32.EPS

Dimensions	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	3.556	3.759	5.080	0.140	0.148	0.200
A1	0.508			0.020		
A2	3.048	3.556	4.572	0.120	0.140	0.180
B	0.356	0.457	0.584	0.014	0.018	0.023
B1	0.762	1.016	1.397	0.030	0.040	0.055
C	0.203	0.254	0.356	0.008	0.010	0.014
D	27.43	27.94	28.45	1.080	1.100	1.120
E	9.906	10.41	11.05	0.390	0.410	0.435
E1	7.620	8.890	9.398	0.300	0.350	0.370
e		1.778			0.070	
eA		10.16			0.400	
eB			12.70			0.500
L	2.540	3.048	3.810	0.100	0.120	0.150

SDIP32.TBL