

TOSHIBA Bi-CMOS INTEGRATED CIRCUIT SILICON MONOLITHIC

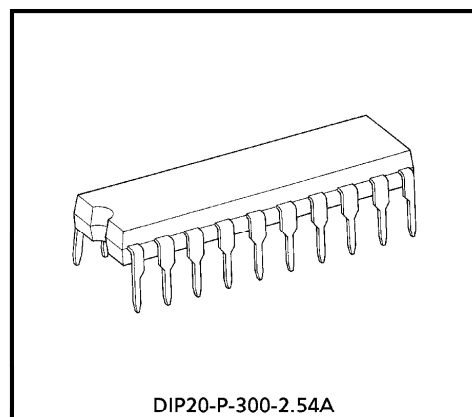
# TD62C851P, TD62C852P

## 8BIT SERIAL-IN PARALLEL-OUT SHIFT REGISTER / LATCH DRIVERS

The TD62C851P and TD62C852P are monolithic circuits designed to be used together with Bi-CMOS integrated circuits. The devices consist of a 8bit shift register, 8bit latches, and 8 output circuits (integral clamp diodes for switching inductive loads).

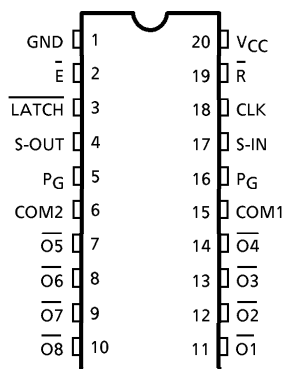
### FEATURES

- 8bit serial-in parallel-out shift register / latch driver (Bi-CMOS process)
- Output sustaining voltage ; 50V
- Output current ; TD62C851P 200mA / ch (Low saturation type)  
TD62C852P 500mA / ch (darlington type)
- Built-in output clamp diodes
- CMOS compatible inputs
- Package ; DIP20-P-300A



DIP20-P-300-2.54A  
Weight : 2.25g (Typ.)

### PIN CONNECTION (TOP VIEW)



961001EBA2

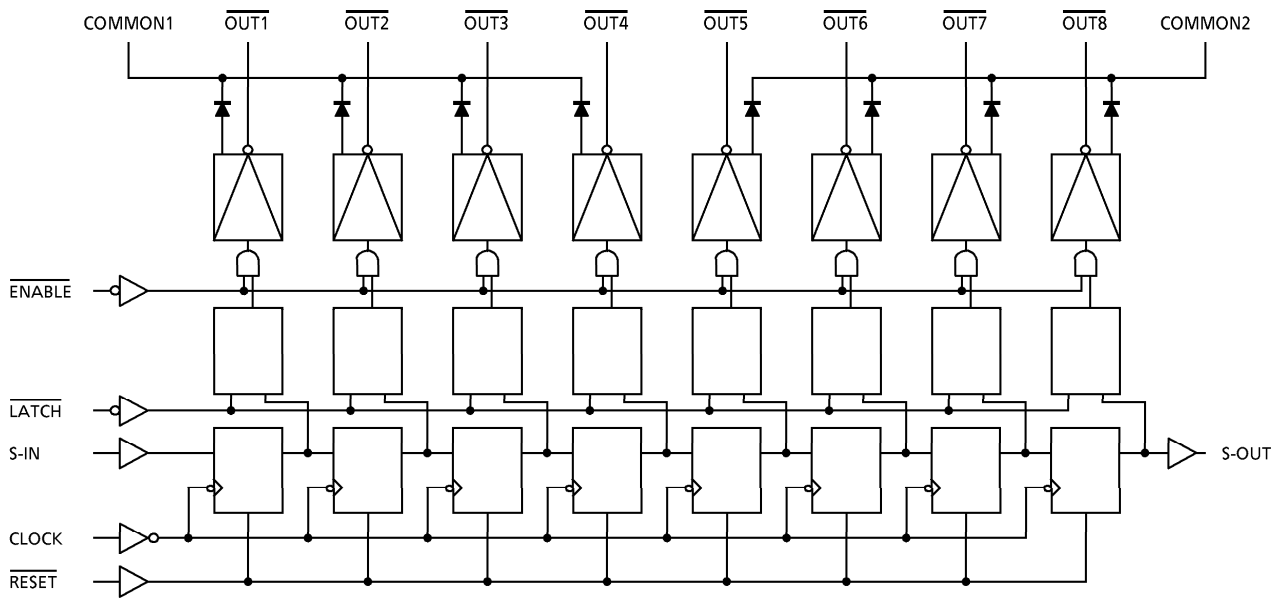
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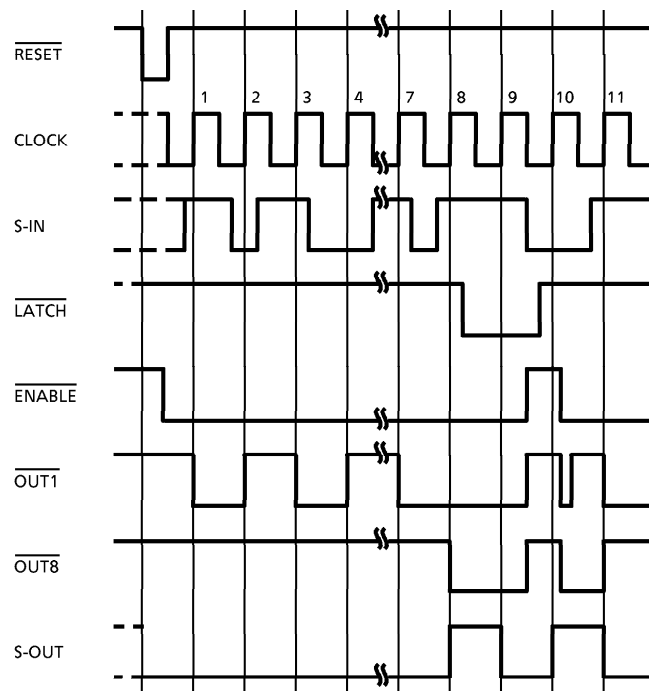
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**BLOCK DIAGRAM**

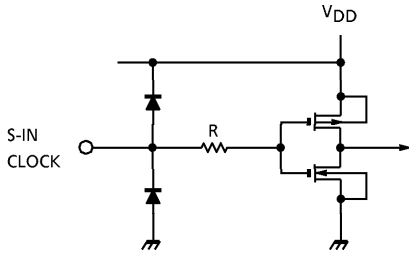


**TIMING DIAGRAM**

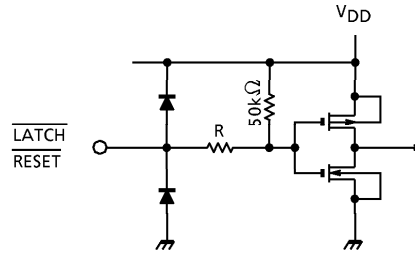


**EQUIVALENT OF INPUTS AND OUTPUTS**

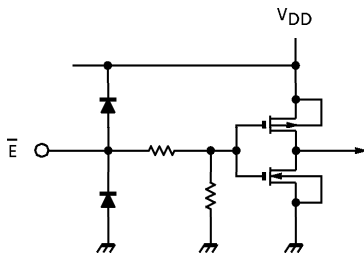
S-IN, clock terminal equivalent circuits



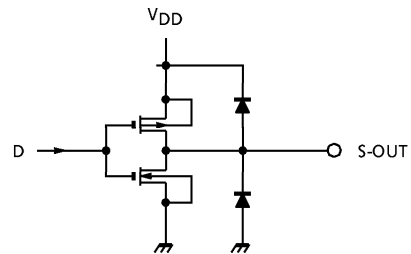
$\overline{\text{LATCH}}$ ,  $\overline{\text{RESET}}$  terminal equivalent circuits



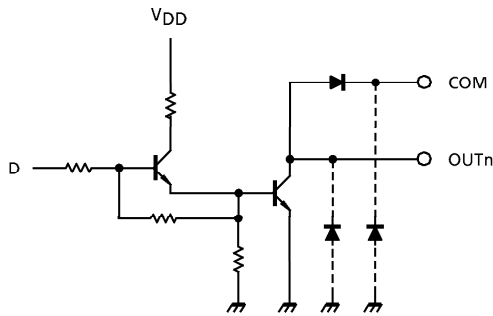
$\overline{\text{ENABLE}}$  terminal equivalent circuits



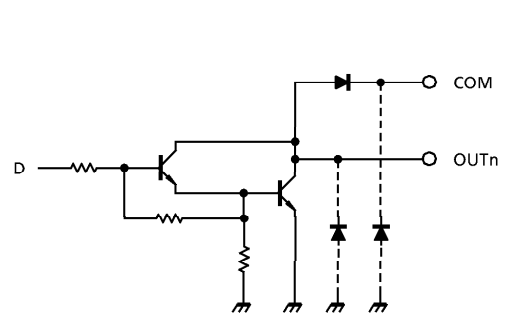
S-OUT terminal equivalent circuits



Output terminal equivalent circuits  
(TD62C851P)



Output terminal equivalent circuits  
(TD62C852P)



(Note) The output parasitic diode cannot be used as clamp diode.

**TRUTH TABLE**

CK	$\bar{E}$	$\bar{R}$	$\overline{\text{LATCH}}$	S-IN	OUT		S-OUT
					O1	$\overline{O_n}$	
	L	H	H	L	OFF	$\overline{O_{n-1}}$	Q7
	L	H	H	H	ON	$\overline{O_{n-1}}$	Q7
	L	H	L	(*)	NC	NC	Q7
	H	H	(*)	(*)	OFF	NC	Q7
	(*)	(*)	(*)	(*)	NC	NC	Q7
(*)	(*)	L	H	(*)	OFF	OFF	L
(*)	H		L	(*)	NC	NC	L

CK = CLOCK  
 $\bar{E}$  = ENABLE  
 $\bar{R}$  = RESET  
 $\overline{\text{LATCH}}$  = LATCH  
 S-IN = SERIAL IN  
 OUT = PARALLEL OUT  
 S-OUT = SERIAL OUT

(\*) = DON'T CARE  
 NC = NO CHANGE  
 L = LOW LEVEL  
 H = HIGH LEVEL

**MAXIMUM RATINGS (Ta = 25°C)**

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	$V_{DD}$	- 0.3~7.0	V
Output Sustaining Voltage	$V_{CE(SUS)}$	- 0.5~50	V
Output Current	TD62C851P	200	mA / ch
	TD62C852P	500	
Input Voltage	$V_{IN}$	~0.4~ $V_{DD} + 0.3$	V
Power Dissipation	$P_D$	1.47	W
Operating Temperature	$T_{opr}$	- 40~85	°C
Storage Temperature	$T_{stg}$	- 55~150	°C

**RECOMMENDED OPERATING CONDITIONS (Ta = -40~85°C)**

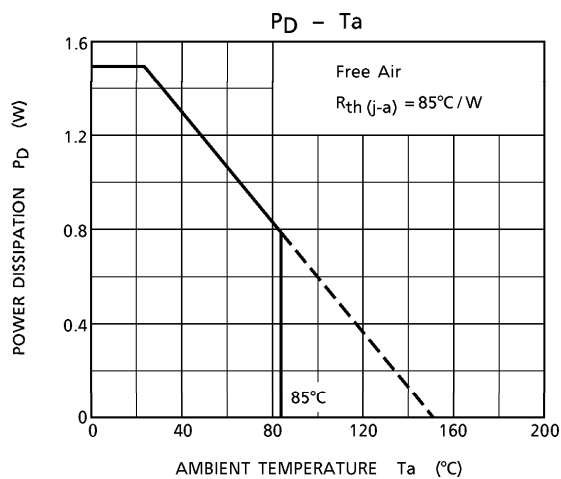
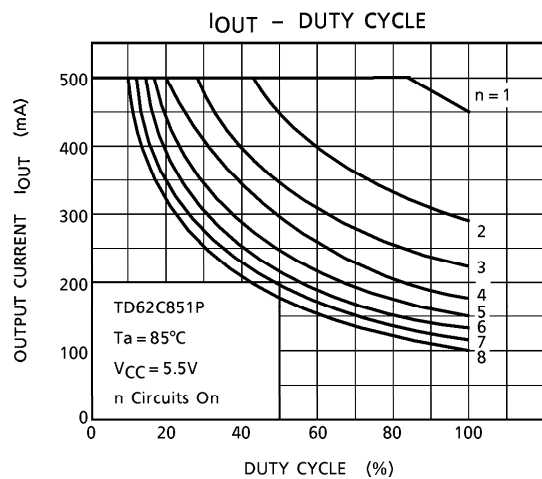
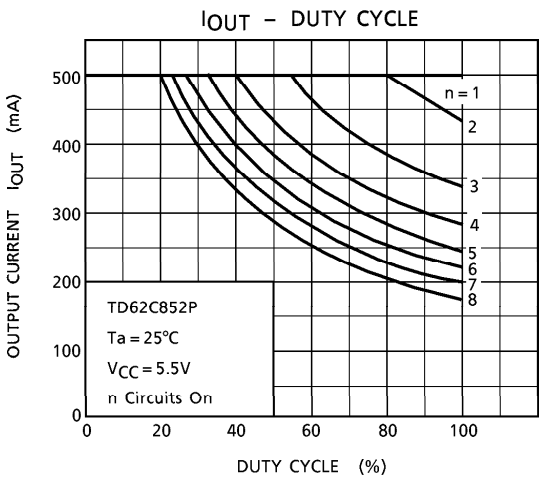
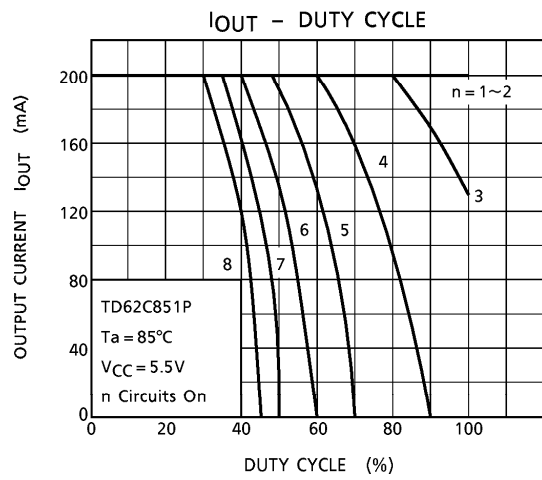
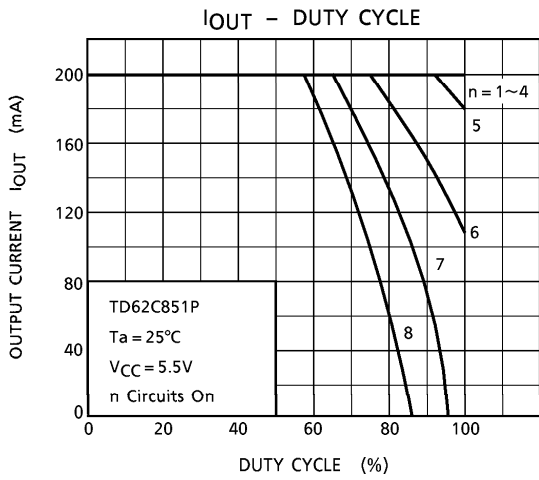
CHARACTERISTIC		SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT	
Supply Voltage		$V_{DD}$	—	4.5	5.0	5.5	V	
Input Voltage		$V_{IN}$	—	0	—	$V_{DD}$	V	
Output Current ("H" Level)	S-OUT	$I_{OH}$	Ta = 25°C	—	—	-0.4	mA	
Output Voltage ("L" Level)	$\overline{On}$	$V_{OH}$	—	0	—	50	V	
Output Current ("L" Level)	S-OUT	$I_{OL}$	—	—	—	0.4	mA / ch	
			DC 1 circuit, Ta = 25°C	0	—	160		
			8 circuit on T <sub>pw</sub> = 25ms Ta = 85°C V <sub>DD</sub> = 5.5V	Duty = 10%	0	—		160
				Duty = 40%	0	—		95
			DC 1 circuit, Ta = 25°C	0	—	400		
			8 circuit on T <sub>pw</sub> = 25ms Ta = 85°C V <sub>DD</sub> = 5.5V	Duty = 10%	0	—		400
Duty = 50%	0	—		170				
Clock Frequency		f <sub>CLOCK</sub>	—	1.5	—	—	MHz	
Clock Pulse Width		f <sub>w</sub> CLOCK	—	0.33	—	—	μs	
Data Set Up Time		t <sub>setup</sub>	—	100	—	—	ns	
Data Hold Time		t <sub>hold</sub>	—	100	—	—	ns	
Clamp Diode Reverse Voltage		V <sub>R</sub>	—	0	—	50	V	
Clamp Diode Forward Current	TD62C851P	I <sub>F</sub>	—	0	—	160	mA	
	TD62C852P		—	0	—	400		

**ELECTRICAL CHARACTERISTICS (Ta = -40~85°C)**

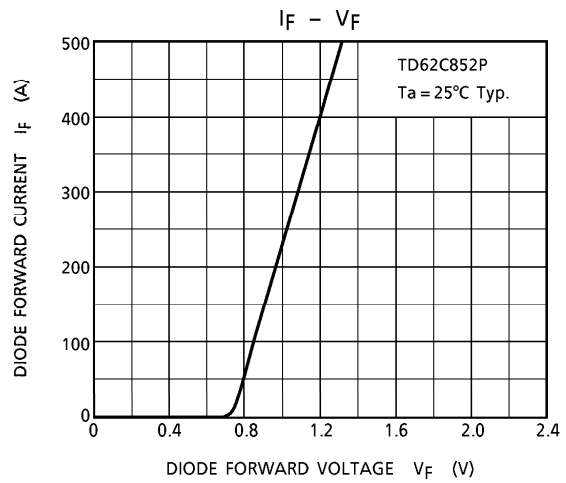
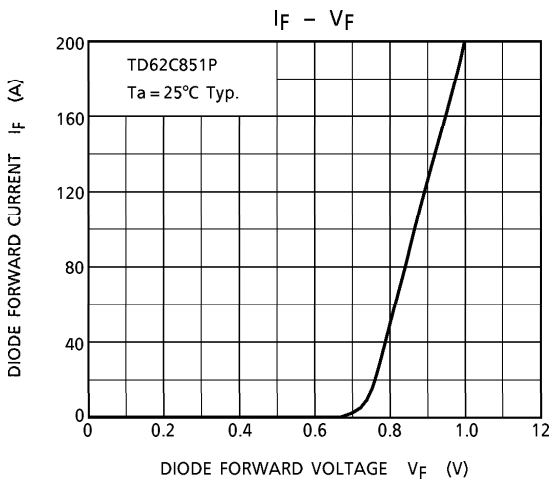
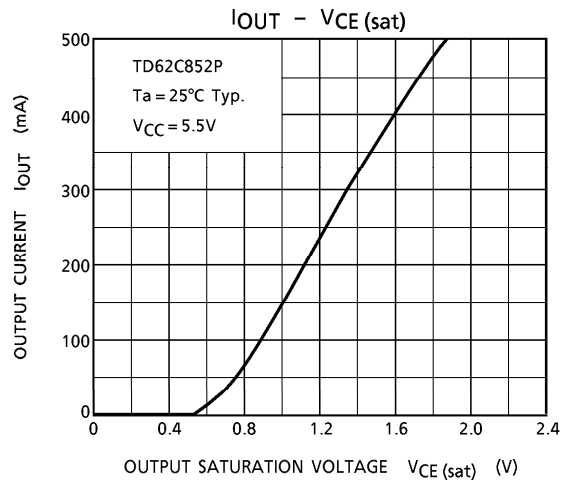
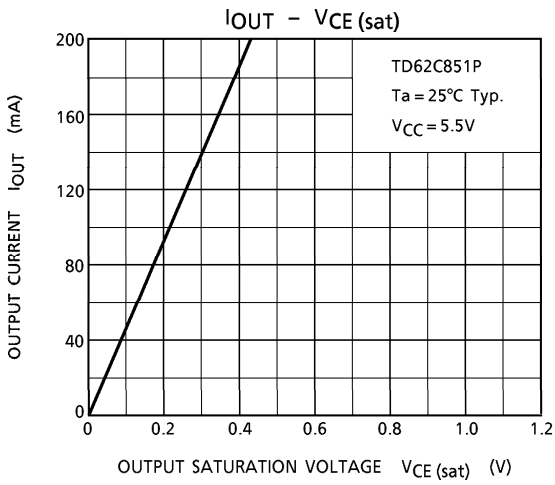
CHARACTERISTIC		SYM-BOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT			
Input Voltage	"H" Level	V <sub>IH</sub>	—	—	0.7 V <sub>DD</sub>	—	—	V			
	"L" Level	V <sub>IL</sub>	—	—	—	—	0.3 V <sub>DD</sub>				
Input Current	"H" Level	I <sub>IH</sub>	—	ENABLE, V <sub>DD</sub> = 5.5V V <sub>IH</sub> = V <sub>DD</sub>	28	55	110	μA			
	"L" Level	I <sub>IL</sub>	—	LATCH, RESET V <sub>DD</sub> = 5.5V, V <sub>IL</sub> = GND	-55	-110	-275				
		I <sub>IN</sub>	—	CLOCK, S-IN V <sub>IN</sub> = V <sub>CC</sub> or GND	—	—	±1.0				
Output Voltage	"H" Level	S-OUT	V <sub>OH</sub>	—	V <sub>DD</sub> = 4.5V I <sub>OH</sub> = -10μA	3.9	4.1	—	V		
	"L" Level	S-OUT	V <sub>OL</sub>	—	V <sub>DD</sub> = 4.5V	I <sub>OL</sub> = 0.8mA	—	0.2	0.4	V	
		On				I <sub>OL</sub> = 100mA	—	0.29	0.50		
						I <sub>OL</sub> = 160mA	—	0.39	0.65		
						I <sub>OL</sub> = 250mA	—	1.24	1.90		
I <sub>OL</sub> = 400mA	—		1.54	2.30							
Output Current	"H" Level	On	I <sub>OH</sub>	—	V <sub>DD</sub> = 5.5V, V <sub>OH</sub> = 50.0V	—	—	100	μA		
Operating Supply Current			I <sub>DD1</sub>	—	V <sub>DD</sub> = 5.5V Ta = 25°C	ENABLE = "H"	—	130	200	mA	
			I <sub>DD2</sub>			f <sub>CLK</sub> = 1MHz Output open DATA = 1 / 2 f <sub>CLK</sub>	—	2.0	5.0		
			TD62C851P			I <sub>DD3</sub>	1 circuit on f <sub>CLK</sub> = 1MHz ENABLE = "L"	—	35		40
							TD62C851P	—	1.0		1.5
Clamp Diode Reverse Current		I <sub>R</sub>	—	V <sub>R</sub> = 50V	—	—	50	μA			
Clamp Diode Forward Voltage	TD62C851P	V <sub>F</sub>	—	I <sub>F</sub> = 160mA	—	1.0	2.0	V			
	TD62C852P			I <sub>F</sub> = 400mA	—	1.5	2.0				

**SWITCHING CHARACTERISTICS (Ta = 25°C)**

CHARACTERISTIC		SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Propagation Delay Time	Low-to-High	CK-S-OUT	t <sub>pLH</sub>	V <sub>DD</sub> = 5.0V, V <sub>IH</sub> = 5.0V V <sub>IL</sub> = 0V, Duty = 50% R <sub>L</sub> = { 300Ω (TD62C851P) 120Ω (TD62C852P) }	—	0.40	0.65	μs
		CK-On			—	1.80	3.00	
		L-On			—	2.10	3.50	
		R-On			—	1.50	2.50	
		E-On			—	1.50	2.50	
	High-to-Low	CK-S-OUT	t <sub>pHL</sub>		—	0.33	0.55	
		CK-On			—	0.41	0.70	
		L-On			—	0.30	0.50	
		R-S-OUT			—	0.25	0.42	
		E-On			—	0.21	0.35	
Maximum Clock Frequency		f <sub>MAX</sub>	—	1.5	2.0	—	MHz	
Minimum Pulse Width	CLOCK	t <sub>wCK</sub>	—	—	250	330	ns	
	LATCH	t <sub>wL</sub>		—	116	160		
	RESET	t <sub>wR</sub>		—	107	140		
Data Set Up Time		t <sub>setup</sub>	—	—	30	60	ns	
Data Hold Time		t <sub>hold</sub>	—	—	14	40	ns	
Maximum Clock Rise Time		t <sub>r</sub>	—	—	70	—	ns	
Maximum Clock Fall Time		t <sub>f</sub>	—	—	70	—		





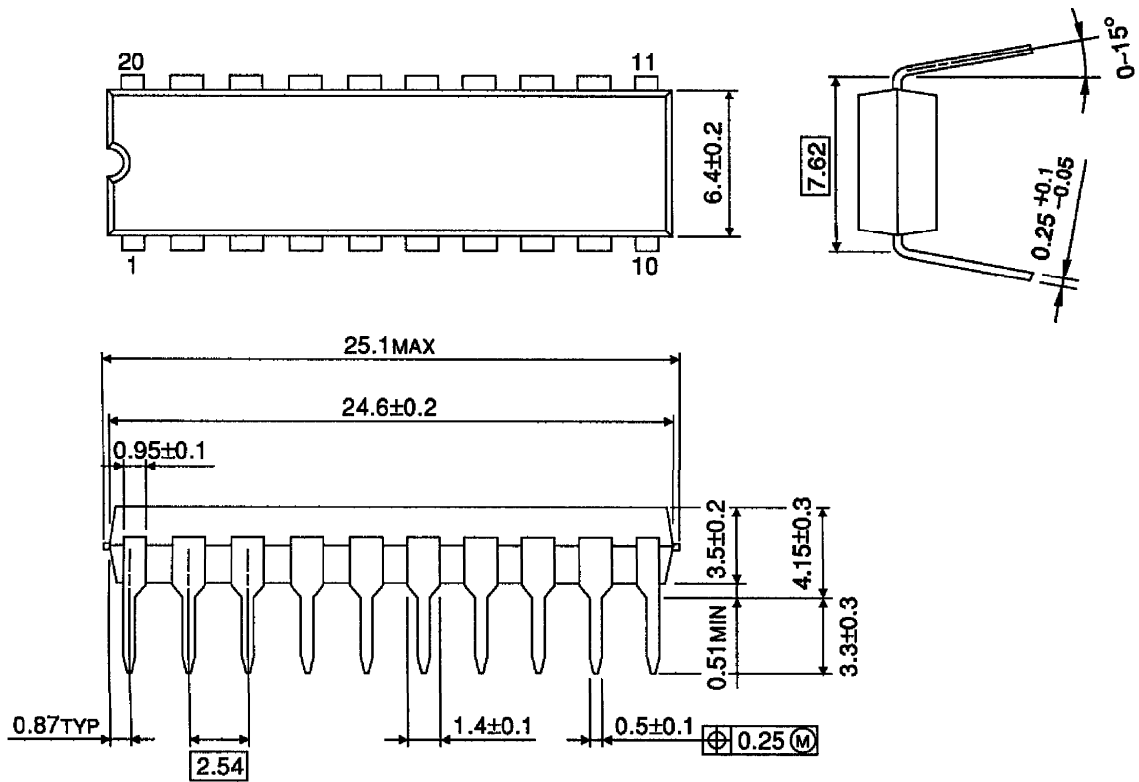


**PRECAUTIONS for USING**

Utmost care is necessary in the design of the output line,  $V_{CC}$  and GND line since IC may be destroyed due to short-circuit between outputs, air contamination fault, or fault by improper grounding.

**OUTLINE DRAWING**  
DIP20-P-300-2.54A

Unit : mm



Weight : 2.25g (Typ.)