

# TC74HC237AP, TC74HC237AF

## 3 - TO - 8 LINE DECODER / LATCH

The TC74HC237A is a high speed CMOS 3 - to - 8 LINE DECODER ADDRESS LATCH fabricated with silicon gate C<sup>2</sup>MOS technology.

It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

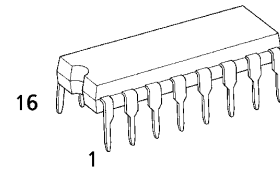
It is composed of a 3 - bit input latches with a common  $\overline{GL}$  enable input and 3 - to - 8 line decoder with enable inputs G1 and  $\overline{G2}$ . The 3 - bit binary data is stored into the input latch on the high level of  $\overline{GL}$ . The value of this data determines which one of the outputs will go low.

When the enable input G1 is held low or  $\overline{G2}$  is held high, decoding function is inhibited and all the 8 outputs go high. The two enable inputs are provided to ease cascade connection and permits the application address decoder for memory system.

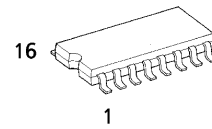
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

### FEATURES :

- High Speed..... $t_{pd} = 12ns$ (typ.) at  $V_{CC} = 5V$
- Low Power Dissipation..... $I_{CC} = 4\mu A$ (Max.) at  $T_a = 25^\circ C$
- High Noise Immunity..... $V_{NIH} = V_{NIL} = 28\% V_{CC}$  (Min.)
- Output Drive Capability..... 10 LSTTL Loads
- Symmetrical Output Impedance...  $|I_{OH}| = |I_{OL}| = 4mA$ (Min.)
- Balanced Propagation Delays.....  $t_{PLH} \approx t_{PHL}$
- Wide Operating Voltage Range.....  $V_{CC}$  (opr.) = 2V ~ 6V
- Pin and Function Compatible with 74LS237

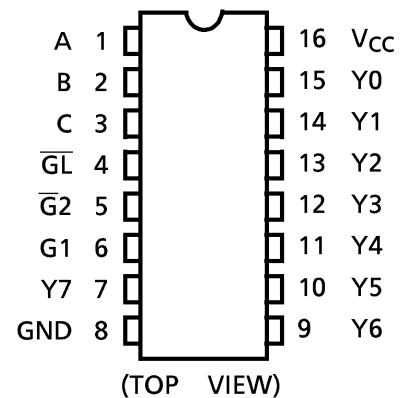


P (DIP16-P-300-2.54A)  
Weight : 1.00g (Typ.)

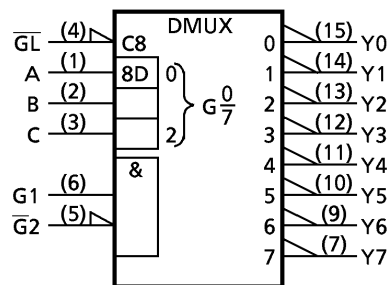
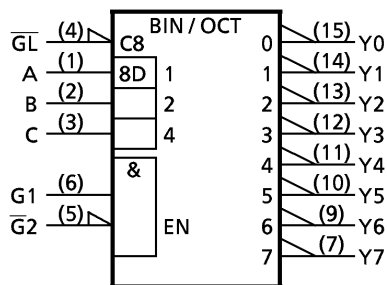


F (SOP16-P-300-1.27)  
Weight : 0.18g (Typ.)

### PIN ASSIGNMENT



### IEC LOGIC SYMBOL

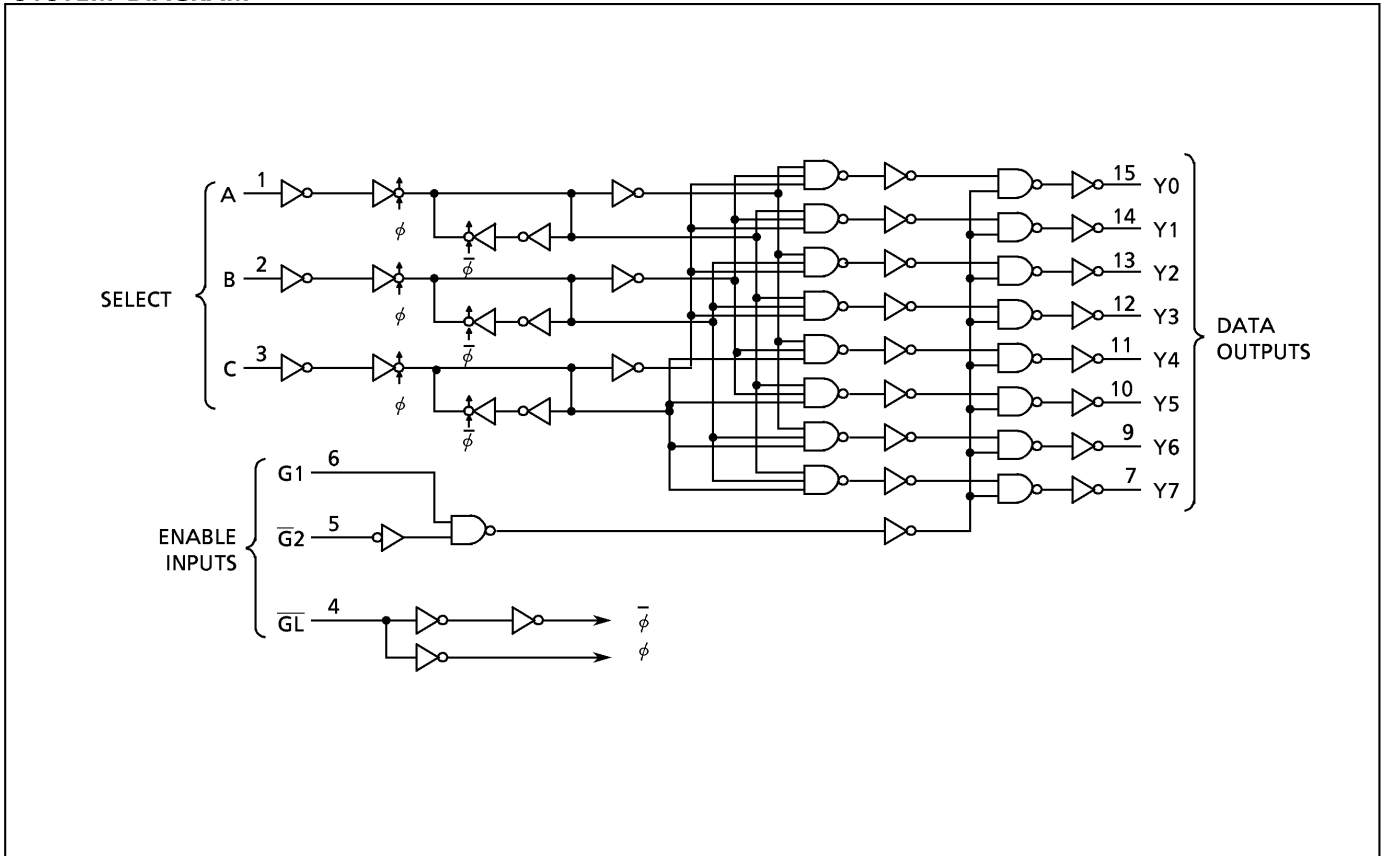


TRUTH TABLE

INPUTS						OUTPUTS							
ENABLE			ADDRESS			Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
$\overline{GL}$	$\overline{G2}$	G1	C	B	A								
X	X	L	X	X	X	L	L	L	L	L	L	L	L
X	H	X	X	X	X	L	L	L	L	L	L	L	L
L	L	H	L	L	L	H	L	L	L	L	L	L	L
L	L	H	L	L	H	L	H	L	L	L	L	L	L
L	L	H	L	H	L	L	L	H	L	L	L	L	L
L	L	H	L	H	H	L	L	L	H	L	L	L	L
L	L	H	H	L	H	L	L	L	L	H	L	L	L
L	L	H	H	H	L	L	L	L	L	L	H	L	L
L	L	H	H	H	H	L	L	L	L	L	L	H	L
L	L	H	H	H	H	L	L	L	L	L	L	L	H
H	L	H	X	X	X	Depends upon the address previously applied while GL was at a low level							

X : Don't care

SYSTEM DIAGRAM



**ABSOLUTE MAXIMUM RATINGS**

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	$V_{CC}$	-0.5~7	V
DC Input Voltage	$V_{IN}$	-0.5~ $V_{CC}+0.5$	V
DC Output Voltage	$V_{OUT}$	-0.5~ $V_{CC}+0.5$	V
Input Diode Current	$I_{IK}$	± 20	mA
Output Diode Current	$I_{OK}$	± 20	mA
DC Output Current	$I_{OUT}$	± 25	mA
DC $V_{CC}$ /Ground Current	$I_{CC}$	± 50	mA
Power Dissipation	$P_D$	500 (DIP)* / 180 (SOP)	mW
Storage Temperature	$T_{stg}$	-65~150	°C

\*500mW in the range of  $T_a = -40^{\circ}\text{C} \sim 65^{\circ}\text{C}$ . From  $T_a = 65^{\circ}\text{C}$  to  $85^{\circ}\text{C}$  a derating factor of  $-10\text{mW}/^{\circ}\text{C}$  shall be applied until 300mW.

**RECOMMENDED OPERATING CONDITIONS**

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	$V_{CC}$	2~6	V
Input Voltage	$V_{IN}$	0~ $V_{CC}$	V
Output Voltage	$V_{OUT}$	0~ $V_{CC}$	V
Operating Temperature	$T_{opr}$	-40~85	°C
Input Rise and Fall Time	$t_r, t_f$	0~ 1000 ( $V_{CC} = 2.0\text{V}$ ) 0~ 500 ( $V_{CC} = 4.5\text{V}$ ) 0~ 400 ( $V_{CC} = 6.0\text{V}$ )	ns

**DC ELECTRICAL CHARACTERISTICS**

PARAMETER	SYMBOL	TEST CONDITION	$V_{CC}$ (V)	$T_a = 25^{\circ}\text{C}$			$T_a = -40 \sim 85^{\circ}\text{C}$		UNIT	
				MIN.	TYP.	MAX.	MIN.	MAX.		
High - Level Input Voltage	$V_{IH}$		2.0	1.50	—	—	1.50	—	V	
			4.5	3.15	—	—	3.15	—		
			6.0	4.20	—	—	4.20	—		
Low - Level Input Voltage	$V_{IL}$		2.0	—	—	0.50	—	0.50	V	
			4.5	—	—	1.35	—	1.35		
			6.0	—	—	1.80	—	1.80		
High - Level Output Voltage	$V_{OH}$	$V_{IN} = V_{IH}$ or $V_{IL}$	$I_{OH} = -20\mu\text{A}$	2.0	1.9	2.0	—	1.9	—	V
				4.5	4.4	4.5	—	4.4	—	
			$I_{OH} = -4\text{ mA}$ $I_{OH} = -5.2\text{ mA}$	4.5	4.18	4.31	—	4.13	—	
				6.0	5.68	5.80	—	5.63	—	
Low - Level Output Voltage	$V_{OL}$	$V_{IN} = V_{IH}$ or $V_{IL}$	$I_{OL} = 20\mu\text{A}$	2.0	—	0.0	0.1	—	0.1	V
				4.5	—	0.0	0.1	—	0.1	
			$I_{OL} = 4\text{ mA}$ $I_{OL} = 5.2\text{ mA}$	4.5	—	0.17	0.26	—	0.33	
				6.0	—	0.18	0.26	—	0.33	
Input Leakage Current	$I_{IN}$	$V_{IN} = V_{CC}$ or GND	6.0	—	—	± 0.1	—	± 1.0	$\mu\text{A}$	
Quiescent Supply Current	$I_{CC}$	$V_{IN} = V_{CC}$ or GND	6.0	—	—	4.0	—	40.0		

**TIMING REQUIREMENTS (Input  $t_r = t_f = 6ns$ )**

PARAMETER	SYMBOL	TEST CONDITION	$V_{CC}(V)$	$T_a = 25^\circ C$		$T_a = -40 \sim 85^\circ C$	UNIT
				TYP.	LIMIT	LIMIT	
Minimum Pulse Width ( $\overline{GL}$ )	$t_{w(L)}$		2.0	—	75	95	ns
			4.5	—	15	19	
			6.0	—	13	16	
Minimum Set-up Time (A, B, C- $\overline{GL}$ )	$t_s$		2.0	—	50	65	
			4.5	—	10	13	
			6.0	—	9	11	
Minimum Hold Time (A, B, C- $\overline{GL}$ )	$t_h$		2.0	—	25	30	
			4.5	—	5	6	
			6.0	—	5	5	

**AC ELECTRICAL CHARACTERISTICS ( $C_L = 15pF$ ,  $V_{CC} = 5V$ ,  $T_a = 25^\circ C$ , Input  $t_r = t_f = 6ns$ )**

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time	$t_{TLH}$ $t_{THL}$		—	4	8	ns
Propagation Delay Time (G1-Y)	$t_{PLH}$ $t_{PHL}$		—	12	24	
Propagation Delay Time ( $\overline{G2}$ -Y)	$t_{PLH}$ $t_{PHL}$		—	12	24	
Propagation Delay Time ( $\overline{GL}$ -Y)	$t_{PLH}$ $t_{PHL}$		—	17	33	
Propagation Delay Time (A, B, C-Y)	$t_{PLH}$ $t_{PHL}$		—	15	31	

**AC ELECTRICAL CHARACTERISTICS ( $C_L = 50pF$ , Input  $t_r = t_f = 6ns$ )**

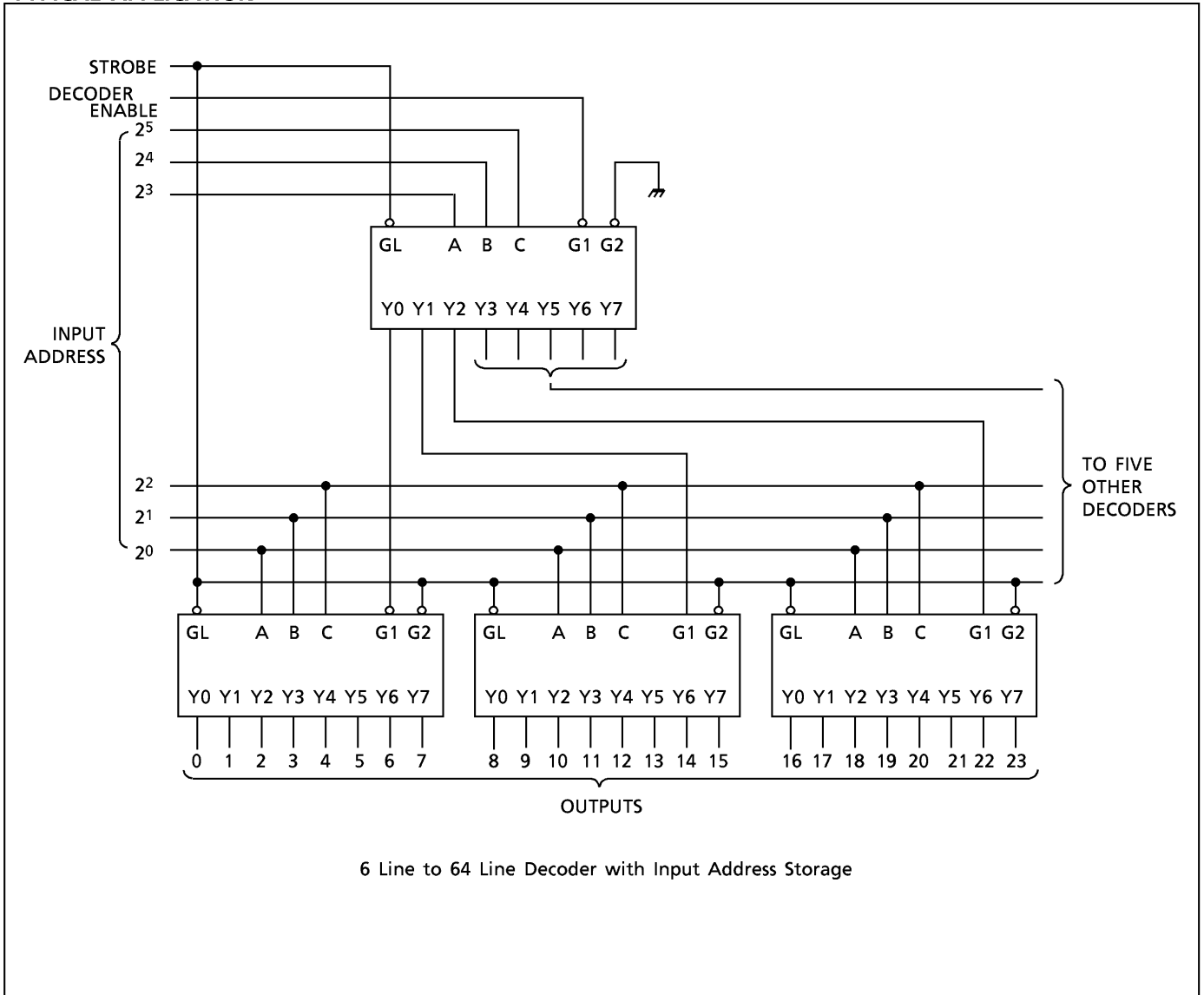
PARAMETER	SYMBOL	TEST CONDITION	$V_{CC}(V)$	$T_a = 25^\circ C$			$T_a = -40 \sim 85^\circ C$		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	$t_{TLH}$ $t_{THL}$		2.0	—	30	75	—	95	ns
			4.5	—	8	15	—	19	
			6.0	—	7	13	—	16	
Propagation Delay Time (G1-Y)	$t_{PLH}$ $t_{PHL}$		2.0	—	45	140	—	175	
			4.5	—	15	28	—	35	
			6.0	—	13	24	—	30	
Propagation Delay Time ( $\overline{G2}$ -Y)	$t_{PLH}$ $t_{PHL}$		2.0	—	45	140	—	175	
			4.5	—	15	28	—	35	
			6.0	—	13	24	—	30	
Propagation Delay Time ( $\overline{GL}$ -Y)	$t_{PLH}$ $t_{PHL}$		2.0	—	65	190	—	240	
			4.5	—	21	38	—	48	
			6.0	—	18	32	—	41	
Propagation Delay Time (A, B, C-Y)	$t_{PLH}$ $t_{PHL}$		2.0	—	60	180	—	225	
			4.5	—	19	36	—	45	
			6.0	—	16	31	—	38	
Input Capacitance	$C_{IN}$			—	5	10	—	10	pF
Power Dissipation Capacitance	$C_{PD}(1)$			—	52	—	—	—	

Note (1)  $C_{PD}$  is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation :

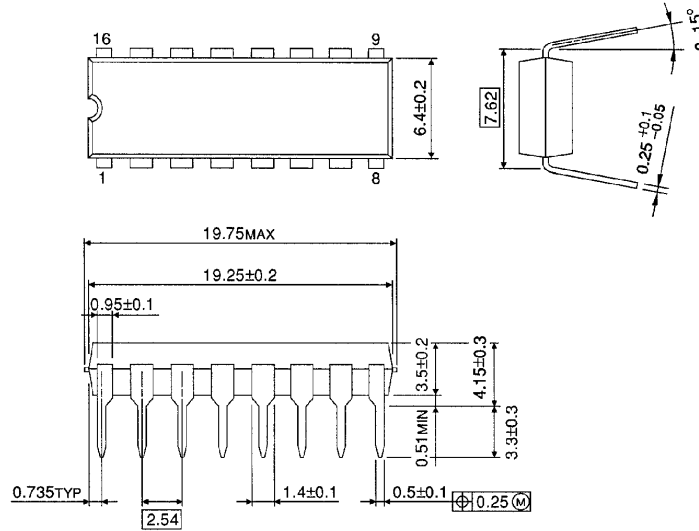
$$I_{CC}(opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

TYPICAL APPLICATION



**DIP 16PIN PACKAGE DIMENSIONS (DIP16-P-300-2.54A)**

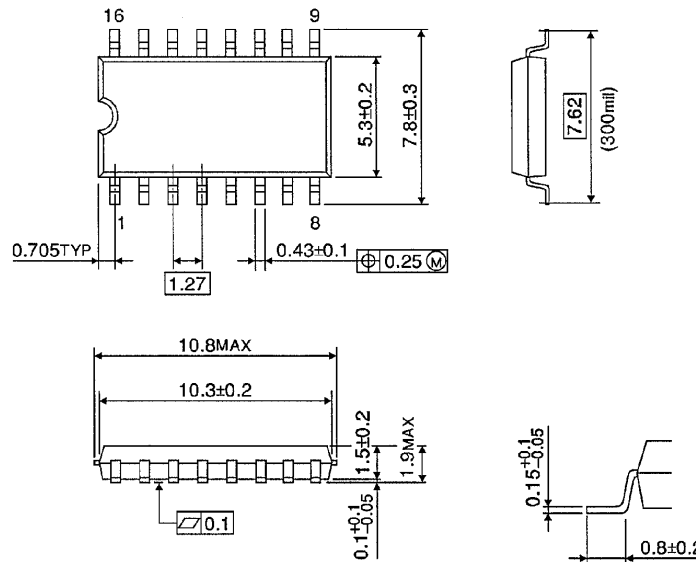
Unit in mm



Weight : 1.00g (Typ.)

**SOP 16PIN (200mil BODY) PACKAGE DIMENSIONS (SOP16-P-300-1.27)**

Unit in mm



Weight : 0.18g (Typ.)

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