HDM8515 Users Manual

DVB/DSS Compliant Receiver

Dec. 2000
Priliminary

Direct Broadcast Satellite (DBS) has been one of the most successful new product introductions in the history of consumer electronics. This product represents the first application of digital video compression for broadcast television. Originally intended to provide cable quality television services to remote areas, this product is now offering a competitive replacement to cable services in many urban areas.

The first operational systems employ closed proprietary signaling structures. The European Broadcasting Union (EBU) has developed the first open standard (DVB-S) for DBS services. The broadcasting community has embraced this standard which is now being adopted for new systems throughout the world. This widely accepted open standard is essential for DBS to achieve full market potential.

The HDM8515^{TM} is a fully DVB-S&DSS compliant ADC/QPSK demodulator/FEC device which provides an MPEG-2 stream to be processed by the conditional access and video decompression circuits. The demodulator clocked with a fixed frequency is true variable rate over the range of 1 to 55M symbols-per-second. This product achieves the highest performance and flexibility. It minimizes the cost of external circuits, thus reducing overall system cost.

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1. Introduction to the HDM8515

The HDM8515 digital demodulator for direct broadcast satellite receivers is a single chip solution fully compliant with the European Telecommunications Standards Institute (ETSI) specification ETS 300 421. This chip integrates an A/D converter, a variable rate matched filter, a variable rate QPSK demodulator with a Viterbi decoder, a deinterleaver and a Reed Solomon decoder.

The HDM8515, which is implemented in a 0.25 micron CMOS, Four Layer Metal Process, provides variable rate capability while operating with a fixed frequency sampling clock. Digital samples of baseband I and Q data are generated by an internal A/D converter, then provided to the demodulator at a fixed sample rate. The root raised cosine filter is implemented internally with fully digital techniques. Similarly, the symbol timing recovery and carrier phase tracking functions are performed entirely in the digital domain. This approach provides minimum constraints on external circuits, thus reducing overall system costs.

The HDM8515 may be configured by an external processor for a specific symbol rate, and carrier frequency along with loop gain parameters. The HDM8515 provides an external AGC signal which is used to control the gain of the analog signal which is applied to the down-converters. And it also provides a digital AGC internally which controls the gain of the signal out of the matched filters. In addition, the HDM8515 provides fully programmable sweep circuitry to aid in initial acquisition when large frequency offsets may be present.

The digital frequency translation capability of the HDM8515 permits this part to be used in frequency multiplexing applications. In this application, an entire transponder bandwidth containing many signals is sampled at a fixed rate. The digital oscillator within the HDM8515 is programmed to the specific desired carrier frequency within that band to permit the selected signal to be passed through the baseband filter and processed by the demodulator circuits.

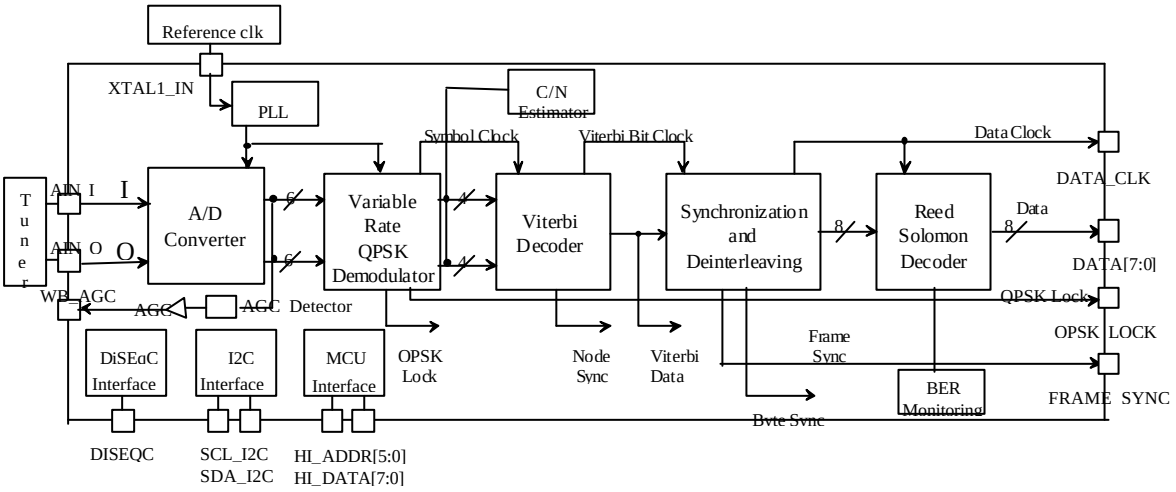

FIGURE 1: TOP LEVEL BLOCK DIAGRAM

1.1 Features and Benefits

* Fully DVB&DSS compliant
* Dual 6bit A/D converters
* Continuously variable symbol rate from 1Msps to 66Msps (90MHz clock)
* Internal digital root raised cosine filter
* Less than 0.5 dB implementation loss
* Frequency multiplexing capability
* Automated frequency search
* Internal bias cancellation
* Both wideband and narrowband AGC
* Noise calibration for antenna steering
* Output data rate as high as 82Mbps
* Fixed frequency sampling clock
* Simple interface with tuner and analog processing
* Microcontroller interface
* Eight bit parallel or I2C monitor and control interface
* I2C by-pass mode
* DiSeqC 1.2 interface support
* Dual Carrier Loop Filter

Part code	Package
HDM8515P	100PQFP

2. Hardware Specification

Table 1: Absolute Maximum Ratings

Rating	Value	Unit
Ambient Temperature under Bias	-10 to 70	c
Storage Temperature	-65 to 150	c
Ambient Humidity under Bias	85(85 c,500hrs)	%
Thermal Resistance(Ja)	45	c/W
Junction Temperature	120	c
Voltage on Any Pin	Vss - 0.3V to V_{DD} + 0.5V	V
VDD, IOVDD	4.5	V
Package Material	- Compound : CEL-4630SX - Lead Frame : Copper	

Table 2: DC Characteristics

Symbol	Parameter	Min.	Max.	Units	Test Conditions
I_{DD}	Dynamic Current	-	390	mA	V_{DD}=2.7, Freq=90Mhz
IOVDD	Interface Power Supply Voltage	3	3.6	V	Normal Operation
VDD	Core Power Supply Voltage	2.3	2.7	V	Normal Operation
V	ADC Power Supply Voltage	2.3	2.7	V	Normal Operation
V_{IL}	Input Low Voltage	0	0.3V_{DD}	V	
V_{IH}	Input High Voltage	0.7V_{DD}	V_{DD}+ 0.5	V	
V_{OL}	Output Low Voltage	-	0.4	V	I_{OL} = 4 mA
V_{OH}	Output High Voltage	2.4	-	V	I_{OH} = 4 mA
I_{IH}	Input High Current	-10	10	uA	V_{IN} =3.6, V_{DD} =3.6
I_{IL}	Input Low Current	-10	10	uA	V_{DD} = 3.6, V_{IN} =0
C_{IN}	Input Capacitance	-	10	pF	Typical 5.75pF
C_{OUT}	Output Capacitance	-	10	pF	Typical 5.97pF

Table 3: Demodulator Specifications

Parameter	Min.	Max.
Sampling Clock Frequency	1MHz	90MHz
Analog Input Full Scale Range	0.9 Vpp	1.1 Vpp
Symbol Rate	1Msps	66Msps
Viterbi Data Rate	-	90Mbps
Reed Solomon Data Rate	-	82Mbps
Implementation Loss	-	0.5 dB
Symbol Rate Resolution	Clock/(2^{20})	-
Carrier Frequency Resolution	Clock/(2^{20})	-
Acquisition Sweep Range	-	**+ or -** Clock/2

Table 4: AC Characteristics

Symbol	Parameter	Min.	Max.	Unit
t_{su1}	Input Data Setup before Clock	6	-	ns
t_{h1}	Input Data Hold after Clock	2	-	ns
t_{pw1}	Low Pulse Width of Clock	8.7	-	ns
t_{pw2}	High Pulse Width of Clock	8.1	-	ns

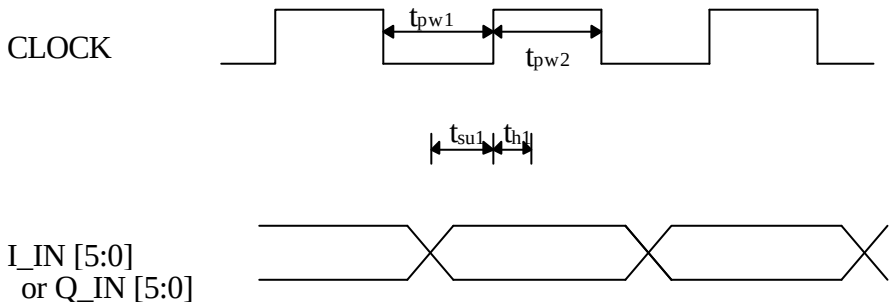

FIGURE 2: INPUT DATA TIMING DIAGRAM

Table 5: Intel 80C88A Read Cycle Timing Parameters (Busmode = 1)

Symbol	Parameter	Min.	Max.	Unit
t_{su1}	Input Address and /CE Setup before /RE Inactive	35	-	ns
t_{h1}	Input Address and /CE Hold after /RE Inactive	5	-	ns
t_{pw1}	/RE Low Duration	200	-	ns
t_{d1}	Delay from /CE to DTACK Active	-	35	ns
t_{doz1}	Delay from /RE Inactive to DTACK in Tristate Mode	-	10	ns
t_{doz2}	Delay from /RE Inactive to HI_DATA [7:0] Tristate Mode	10	-	ns

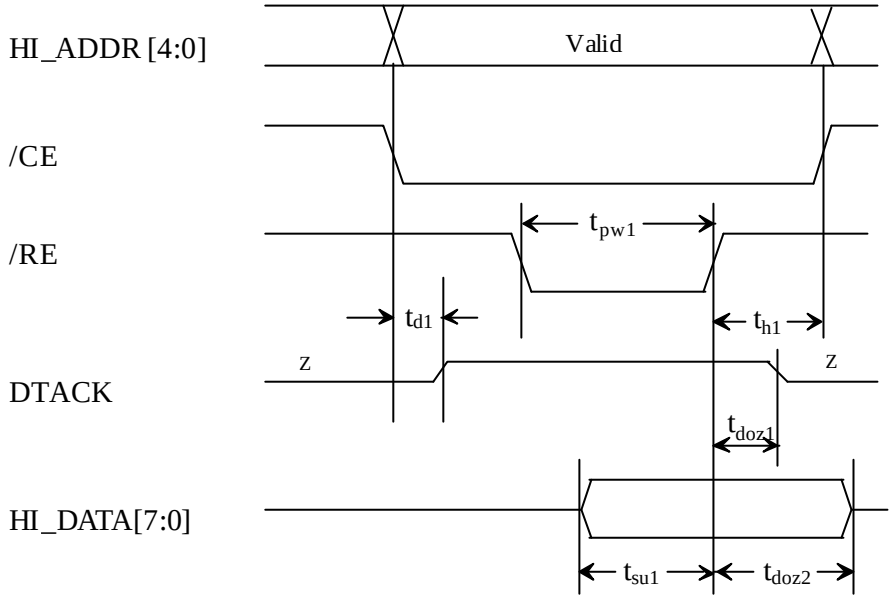

FIGURE 3: INTEL 80C88A READ TIMING DIAGRAM

Note: HI_ADDR[4:0] is derived from the processor(80C88A) A15-A8 bus and HI_DATA[7:0] is connected to the AD7 - AD0 bus.

#This page is only for HDM8515P.

Table 6: Intel 80C88A Write Cycle Timing Parameters (Busmode = 1)

Symbol	Parameter	Min.	Max.	Unit
t_{su1}	Input Data Setup before /WE Inactive	20	-	ns
t_{h1}	Input Address, Data and /CE Hold after /WE Inactive	8	-	ns
t_{pw1}	/WE Low Duration	200	-	ns
t_{d1}	Delay from /CE to DTACK Active	-	35	ns
t_{doz1}	Delay from /WE Inactive to DTACK in Tristate Mode	-	15	ns

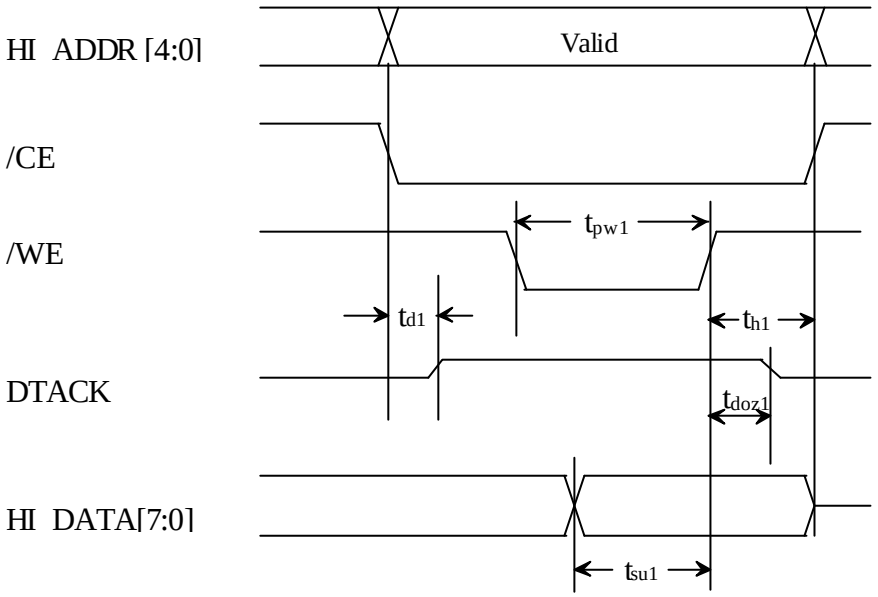

FIGURE 4: INTEL 80C88A WRITE TIMING DIAGRAM

Note: HI_ADDR[4:0] is derived from the processor(80C88A) A15-A8 bus and HI_DATA[7:0] is connected to the AD7 - AD0 bus.

#This page is only for HDM8515P.

Table 7: Intel 8051 Read Cycle Timing Parameters (Busmode = 1)

Symbol	Parameter	Min.	Max.	Unit
t_{su1}	Input Address Setup before /CE Active	5	-	ns
t_{h1}	Input Address and /CE Hold after /RE Inactive	5	-	ns
t_{pw1}	/RE Active Duration	400	-	ns
t_{pd1}	Delay from /RE Active to HI_DATA [7:0] Valid	-	40	ns
t_{doz1}	Delay from /RE Inactive to HI_DATA[7:0] Tristate Mode	10	-	ns

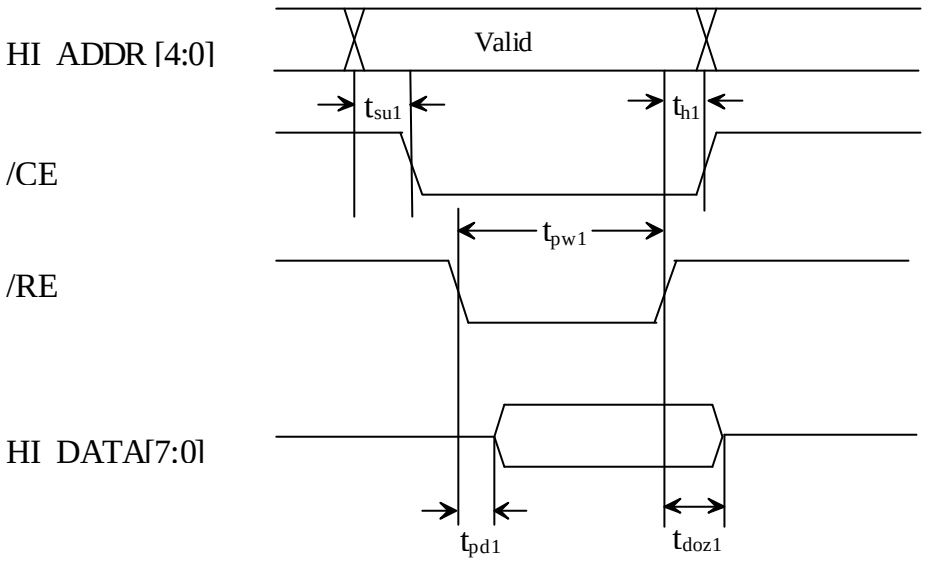

FIGURE 5: INTEL 8051 READ TIMING DIAGRAM

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Table 8: Intel 8051 Write Cycle Timing Parameters (Busmode = 1)

Symbol	Parameter	Min.	Max.	Unit
t_{su1}	Input Address and Data Setup before /WE Active	5	-	ns
t_{h1}	Input Address and Data Hold after /WE Inactive	5	-	ns
t_{pw1}	/WE Active Duration	400	-	ns
t_{su2}	/CE Setup to /WE Active	5	-	ns
t_{h2}	/CE Hold after /WE Inactive	5	-	ns

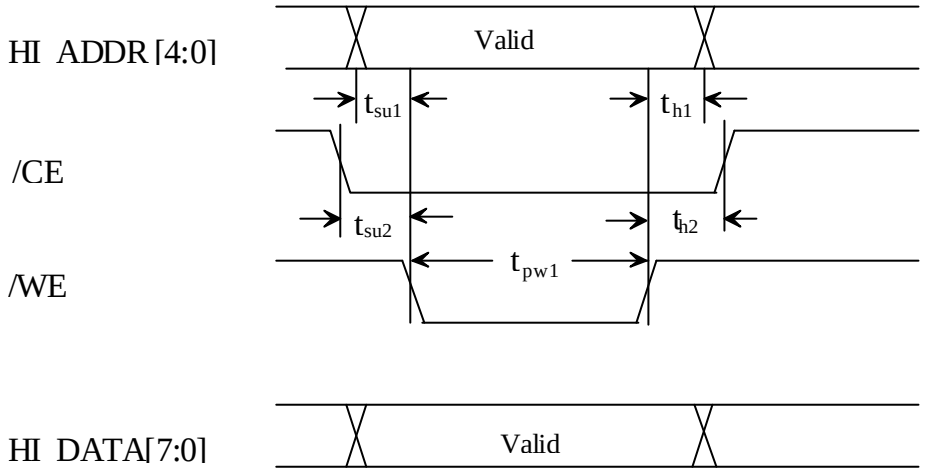

FIGURE 6: INTEL 8051 WRITE TIMING DIAGRAM

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Table 9: Motorola Read Cycle Timing Parameters (Busmode =0)

Symbol	Parameter	Min.	Max.	Unit
t_{su1}	Setup Time of R/W with respect to /CE Active	5	-	ns
t_{su2}	Address Setup with respect to /DS Active	5	-	ns
t_{d1}	Delay from DTACK Active to Data Valid	-	30	ns
t_{h1}	R/W Hold with respect to /DS Inactive	5	-	ns
t_{h2}	Address Hold with respect to /DS Inactive	5	-	ns
t_{h3}	Data Hold with respect to /DS Inactive	10	-	ns

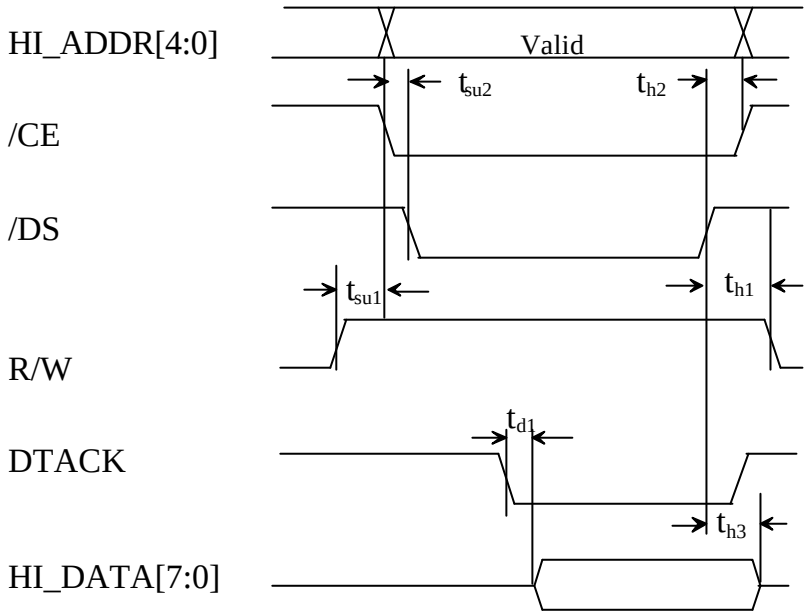

FIGURE 7: MOTOROLA READ TIMING DIAGRAM

Note: External pull-up resistor is required on DTACK.

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Table 10: Motorola Write Cycle Timing Parameters (Busmode =0)

Symbol	Parameter	Min.	Max.	Unit
t_{su1}	Data Setup to /DS Active	5	-	ns
t_{su2}	R/W Setup to /CS and Address	3	-	ns
t_{d1}	/DS Delay from R/W	5	-	ns
t_{d2}	DTACK Delay from /DS Active	-	40	ns
t_{d3}	DTACK Delay from /DS Inactive	-	10	ns
t_{pw1}	/DS Active Duration	5	-	ns
t_{h1}	Address, /CS and R/W Hold from /DS Inactive	5	-	ns
t_{h2}	Data Hold from /DS Inactive	5	-	ns

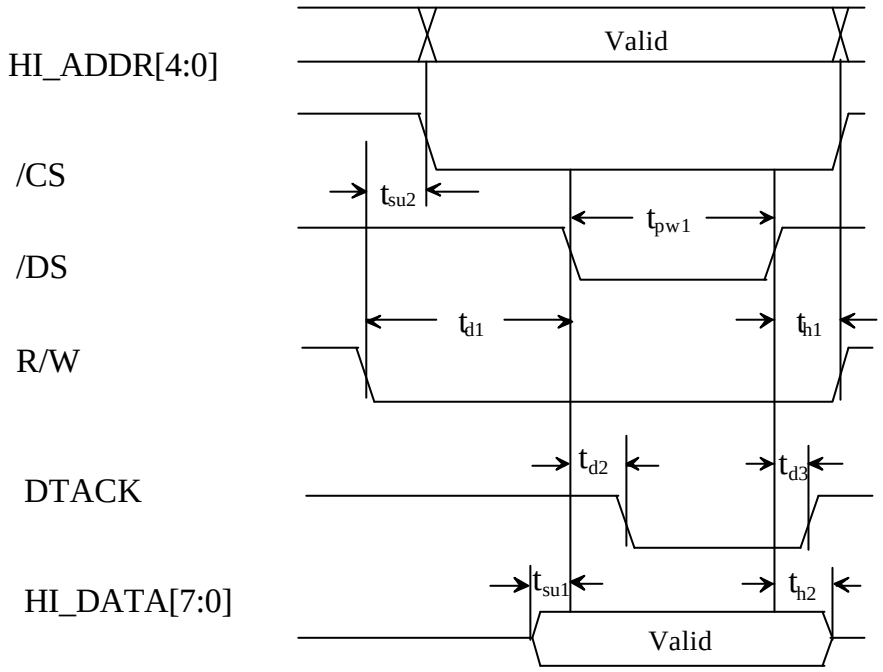


FIGURE 8: MOTOROLA WRITE TIMING DIAGRAM

Note: External pull up resistor is required on DTACK.

#This page is only for HDM8515P.

Table 11: Output Timing

Symbol	Parameter	Min.	Max.	Unit
t_{su}	Output Data Setup before DATA_CLK and DATA_STB	5	-	ns
t_{hd}	Output Data Hold after DATA_CLK and DATA_STB	10	-	ns

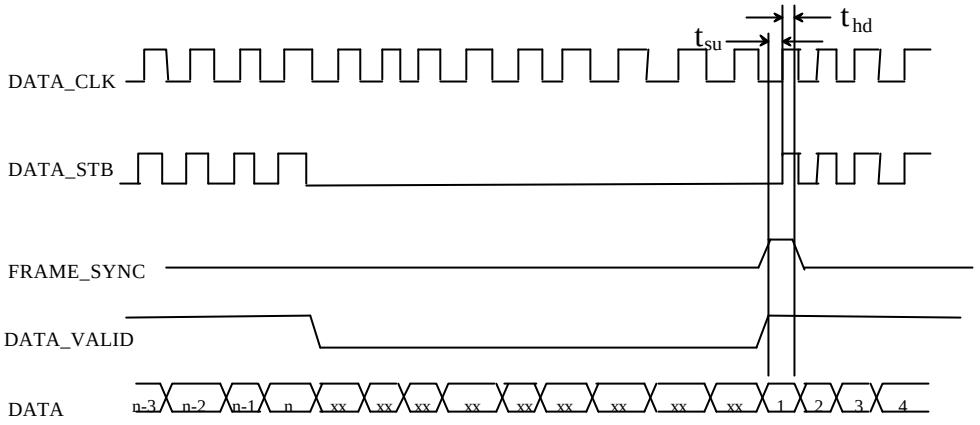


FIGURE 9: OUTPUT TIMING DIAGRAM FOR NORMAL PARALLEL

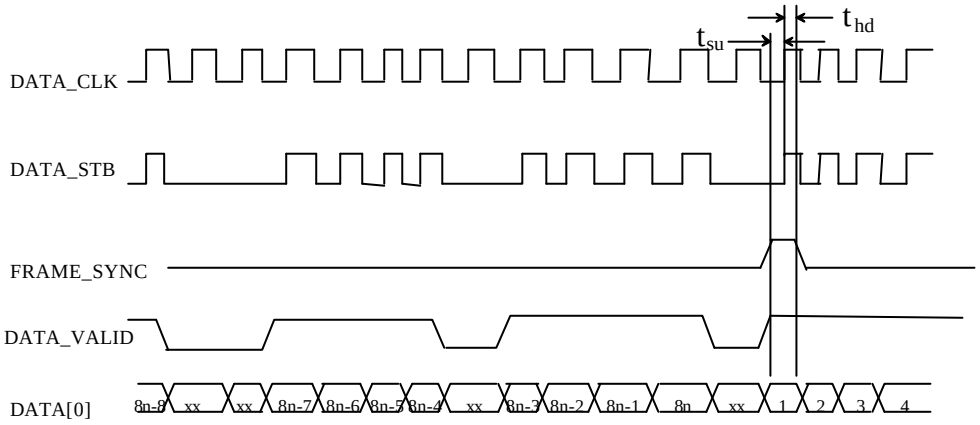


FIGURE 10: OUTPUT TIMING DIAGRAM FOR NORMAL SERIAL

NOTE : In case of DVB, n is 188
In case of DSS, n is 144

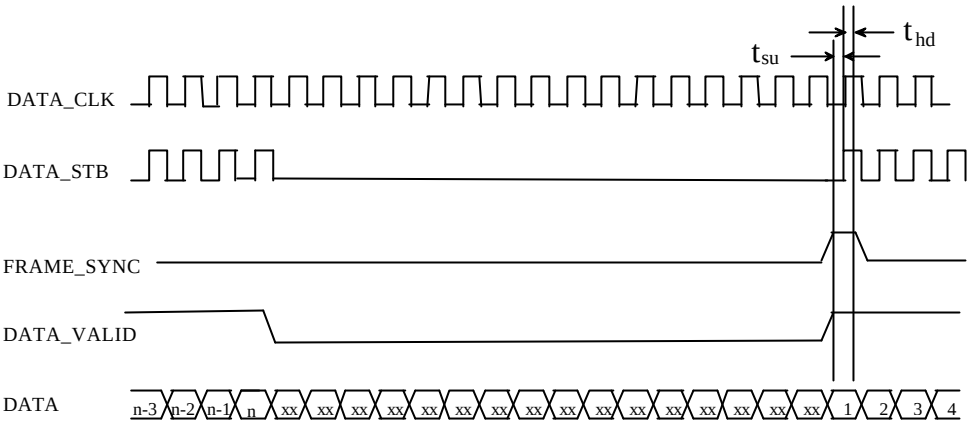


FIGURE 11: OUTPUT TIMING DIAGRAM FOR REGULATED PARALLEL

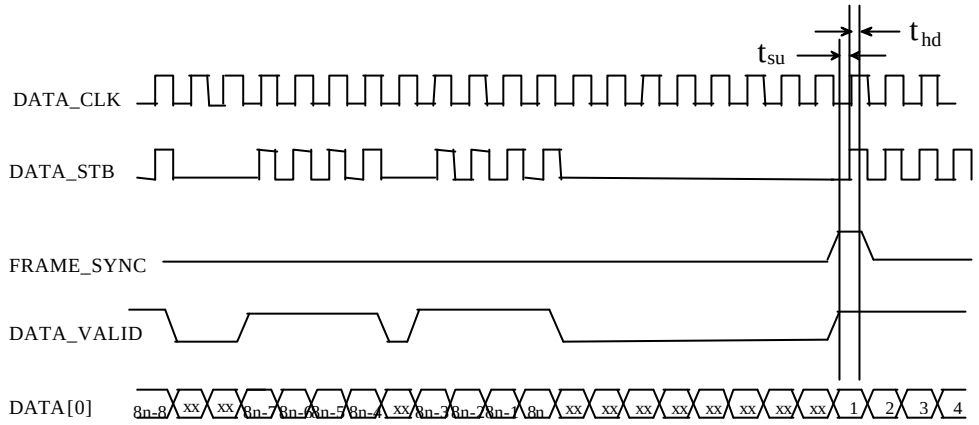


FIGURE 12: OUTPUT TIMING DIAGRAM FOR REGULATED SERIAL

NOTE : In case of DVB, n is 188
In case of DSS, n is 144

3. Technical Overview

3.1 Dual Channel Analog to Digital Converter

The block diagram shown below illustrates internal configuration of the Dual Channel ADC. Baseband signals, in-phase(I) and quadrature phase(Q), which are generated by down converters, are applied to the dual channel ADC and quantized to 6-bit digital codes respectively. The ADC is optimized to allow AC coupled inputs with full scale input range of 1V + or - 10%. An LSB weight is approximately 15.6 mV.

The full scale input analog conversion range (Vpp) is determined by the voltages of VTOP and VBOT and simply equal to (VTOP - VBOT). The full scale range is defined as the voltage range that accommodates 63 codes of equally spaced LSBs. Also the ADC supplies its own reference voltages for A/D conversions. The voltages can be monitored by external reference pins. The VTOP, VBOT represent top and bottom reference voltages respectively. REF_I, REF_Q represent middle reference voltages for each channel. All these 4 reference voltage pins should be by-passed to GND via 0.1uF capacitors. The values of internally generated voltage of VTOP and VBOT are 2.0V and 1.0V respectively. Vpp can be adjusted by externally applying voltages to both VTOP and VBOT pins respectively when different conversion ranges are necessary. VTOP can be adjusted as high as 2.3V and VBOT can be as low as 0.5V. A larger input range can be established by taking VTOP higher and VBOT lower than on-chip generated voltages.

To supply necessary bias voltages for AC coupled applications, REF_I and REF_Q, which are middle reference voltages for I and Q channel, are connected to the analog input pins (AIN_I and AIN_Q) respectively through 40 kohm resistors, as shown in the block diagram. For DC coupled applications, these voltages can be used to feed back offset compensation signals.

To insure optimum performance, a low impedance analog ground plane is recommended and should be separated from other digital ground planes. The analog power supplies should be by-passed at device to analog ground through 0.1uF ceramic capacitors.

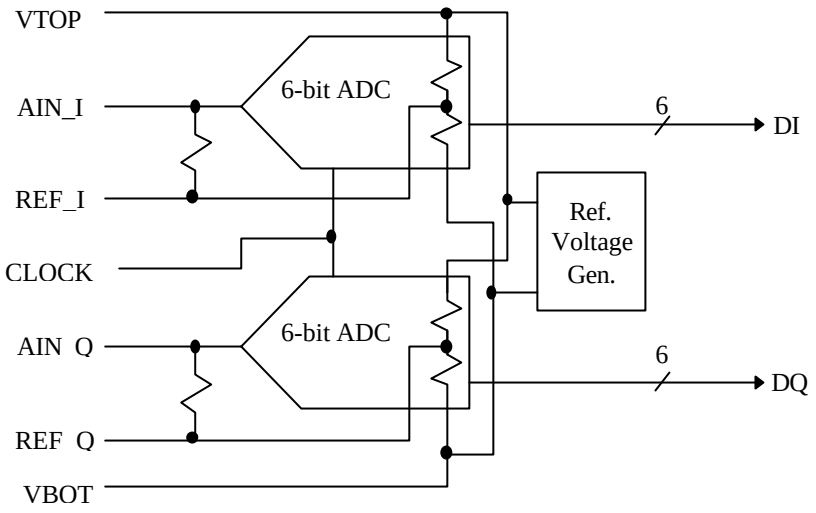


FIGURE 13: ADC BLOCK DIAGRAM

3.2 Variable Rate Demodulator

The block diagram illustrates the overall configuration of the variable rate QPSK demodulator. Baseband in-phase (I) and quadrature (Q) inputs are applied to the demodulator at a fixed sampling rate. These digital samples are produced by A/D converters which employ AC coupling to minimize DC offset.

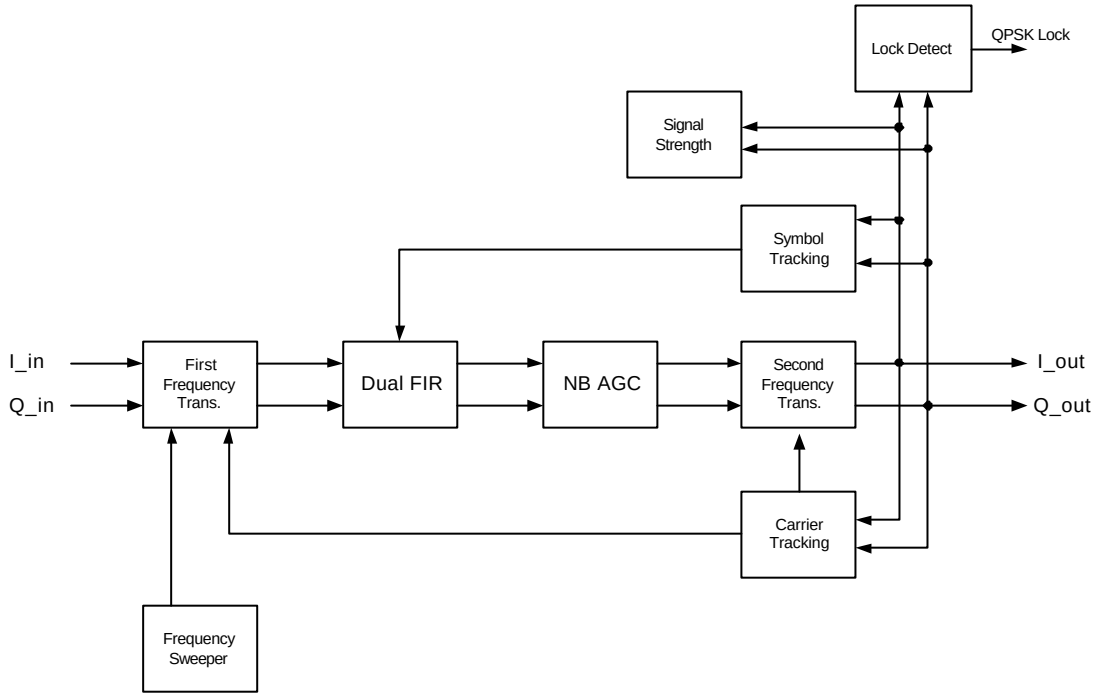


FIGURE 14 DEMODULATOR BLOCK DIAGRAM

The only significant change to this configuration over the HDM8513A is the addition of the Second Frequency Translator. The carrier tracking block produces two outputs, one is the frequency correction which is provided to the First Frequency Translator. This insures that the input to the Dual FIR is always centered at zero frequency error, although there may be a phase error at this point. The second output of the Carrier Tracking function provides the phase correction to the Second Frequency Translator.

The carrier frequency error associated with these samples is removed digitally during tracking operations by a complex multiplier and a digitally controlled oscillator, sometimes called a numerically controlled oscillator (NCO). During initial acquisition, coarse frequency error is removed by a combination of the digital AGC within the HDM8515 and external analog tuning circuits.

A Dual filter performs the root raised cosine filtering of the frequency corrected baseband samples. This filter, which implements the function of equation (1), is always configured to have an impulse response duration of 8 symbols regardless of the programmed symbol rate. For low symbol rates, a large number of samples are used, while for high symbol rates a relatively low number of samples are processed for each filter output. The outputs of the daul filters are applied to a digital

narrowband AGC which insures that the signal is optimally scaled to the Viterbi decoder to an accuracy of **+ or -** 0.5 dB to insure optimum FEC performance.

$$y[k] = \Sigma\ h[n]\ x[k-n] \qquad (1)$$

In addition to optimizing performance of the Viterbi decoder, the digital narrowband AGC also insures that the performance of the symbol timing and carrier tracking loops is independent of signal level variations. An analog wideband AGC is also employed to insure that the analog signal applied to the A/D converters is properly scaled.

Both the symbol timing and carrier tracking loops are implemented digitally, which eliminates the need for external connections to analog tuning components during steady state operation. This causes the requirements on the analog presampling filter to be relaxed, permitting a lower cost analog front end. For systems which require a narrow band presampling filter, and have the potential for significant frequency error in the LNB (several MHz) the HDM8515 provides a high resolution measure of carrier frequency to permit periodic readjustment of the front end tuner frequency to compensate for drift. The host processor periodically reads the frequency register, then computes appropriate correction to the tuner frequency.

The nominal symbol rate and the nominal carrier frequency are programmed into the demodulator to an accuracy provided by 20 bits of resolution, and the system accuracy is equivalent to that of the fixed frequency sampling clock.

During initial acquisition, the HDM8515 provides an automated sweep program to facilitate carrier acquisition. The host processor loads a 20 bit register which determines the initial carrier frequency. A 16 bit register is programmed with the number of symbol times the receiver will dwell at each frequency. If the receiver remains at the initial frequency for the programmed number of symbol times without achieving lock, the carrier frequency is incremented by the step frequency value programmed into another 16 bit register. If no lock is achieved, the receiver will continue to increment the frequency until the maximum number of search frequencies, as determined by the value in an 8 register, is achieved. When the maximum number of search frequencies is reached, the carrier frequency returns to the initial value and the entire process is repeated. Once the host processor determines that lock is achieved by observing the lock flag, it then inhibits the sweep function and programs loop bandwidth parameters which are optimized for steady state performance.

3.3 Noise Measurement Circuit

When the DBS system is being installed in any place, the most difficult part of the installation is accurate pointing of the antenna toward the satellite. Inaccurate pointing results in loss of margin and greater potential for outages in adverse weather conditions. Existing systems use information from the demodulator forward error correction circuits to provide a measure of antenna pointing. Unfortunately, this method is useful over a range of only several dB above system threshold.

The HDM8515 employs a unique circuit for accurate measure of signal strength over a 20 dB range of signal to noise ratio. This method, illustrated in the block diagram, makes use of the fact that the demodulator provides 8 bits of resolution for each of the quadrature output components. This high resolution provides a means of measuring the noise component with great accuracy.

The eight bit in-phase demodulator filter output is detected by an absolute value circuit, then passed through an IIR to provide a measure of average signal amplitude. Each sample is then subtracted from this average amplitude to provide an instantaneous noise sample. The absolute value of these noise samples are then averaged by a second IIR to provide a measure of the noise which is roughly proportional to the noise power and inversely proportional to signal to noise ratio.

Finally, the Figure 16 illustrates the results of simulations under different noise conditions. This figure illustrates that for signal-to-noise ratio as high as 19 dB, the noise measurement circuit provides a meaningful measure of signal power with worst case resolution of 1 dB.

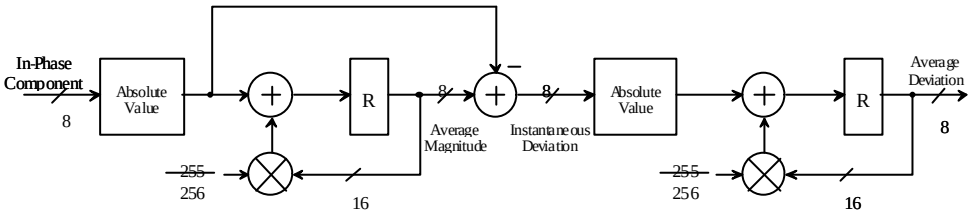


FIGURE 15: NOISE MEASUREMENT CIRCUIT

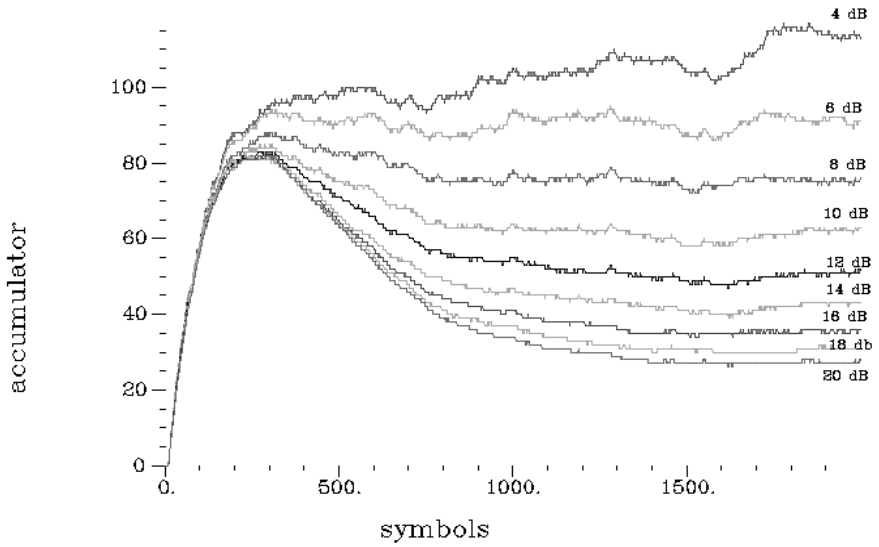


FIGURE 16: NOISE ACCUMULATOR AS A FUNCTION OF SNR AND TIME

3.4 Viterbi Decoder

The Viterbi decoder accepts 4 bit soft decision samples of the in-phase (I) and quadrature (Q) components of the received signal. Once QPSK lock has been achieved, the decoder searches for the correct code rate, starting with rate 3/4, then proceeding to rate 2/3, 5/6, 7/8 and finally rate 1/2. Each of the possible synchronization phases at each rate is tested as well as the two possible carrier phase ambiguity conditions. Polarity reversal is corrected in the word synchronization logic. Viterbi lock is achieved when the trellis traceback algorithm converges, on the average, within a prescribed number of symbols.

Although the algorithm automatically tests for carrier phase ambiguity, there is no provision to automatically correct for phase reversal. Phase reversal can occur if the receiver chain, consisting of an LNB and the tuner, provides an odd number of high side frequency translation operations. A system may be required to operate with different LNBs, some of which provide phase reversal. This condition may be corrected by the host processor, which can set a bit in the down converter to correct for phase reversal.

The Viterbi decoder employs the radix two algorithm. The output buffer reserializes the data which is made available, along with the Viterbi data clock as external signals. These signals permit verification of the DVB specification which is referenced to the Viterbi decoder output.

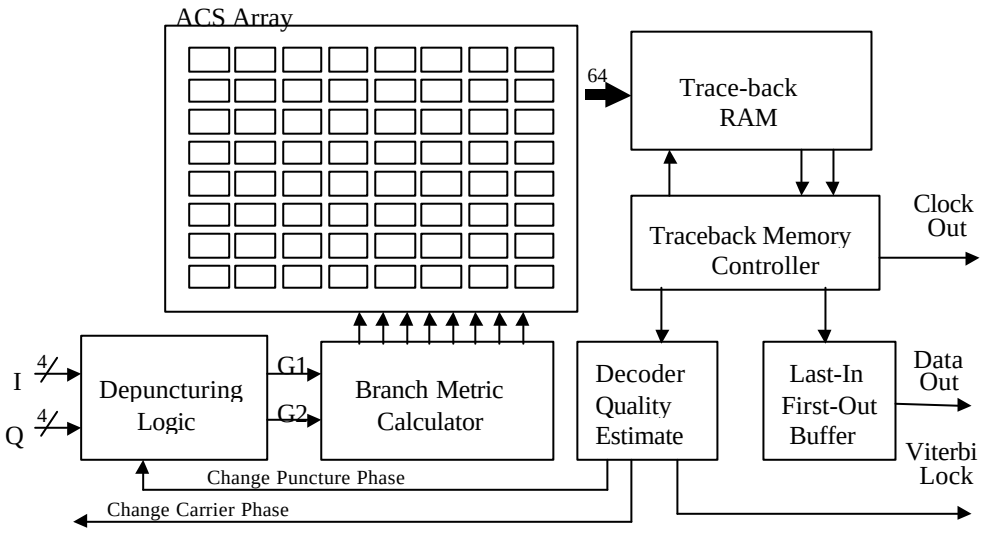


FIGURE 17: VITERBI DECODER

3.5 Autonomous Acquisition

The HDM8515 provides several features to permit signal acquistion with minimal interaction with the host microcontroller. The host microcontroller must configure the HDM8515 for a specific symbol rate, carrier frequency, carrier sweep conditions, and tracking loop bandwidth. The microcontroller also must monitor lock status to determine when acquisition is achieved. There are many provisions in the HDM8515 to enable the system designer to implement custom algorithms for specific requirements.

The microcontroller first must set the lower edge of the carrier search range in the Carrier Frequency registers (04, 05 and 06). Then the processor configures the Carrier Sweep Step Size register (09, 0A) to a value which is less than two times the carrier pull-in range. The number of symbols per dwell is defined in registers (0B,0C), and is typically set to a value of 500 to 1000. The total search range is set by the Number of Search Frequencies as defined in register 0D. The total sweep frequency range is this number times the Carrier Sweep Step Size. The sweep process stops once QPSK carrier lock is detected. If no lock is detected, the sweep process continuously repeats.

The QPSK demodulator may lock to any one of four different phase reference states, only one of which produces true I and Q data as it was modulated at the transmitter. If the local phase reference is plus 90 degrees or minus 90 degrees with respect to the true phase, the information provided to the Viterbi decoder will be unintelligible. If the Viterbi decoder is unable to achieve valid lock, it will reattempt lock with a 90 degree phase shift, without external intervention.

In the event that the local phase is 180 degrees from the true phase, the data provided to the Viterbi decoder will be inverted, but otherwise valid. The code employed by the Viterbi decoder is transparent, thus the data from the Viterbi decoder will be inverted if the input is inverted. This situation is corrected in the word synchronization circuit. This circuit searches for the unscrambled sync word which occurs once per frame (every 204 bytes at the Viterbi output). Once correlation with the sync word is found, the data is reformatted as a series of bytes with the beginning of each 204 byte frame identified to provide the synchronization information required for the deinterleaver and the Reed Solomon decoder. If the polarity of the sync word is incorrect, the data is inverted before further processing without external interaction.

The HDM8515 supports five different code rates, including 1/2, 2/3, 3/4, 5/6 and 7/8. When rate 1/2 is employed, there is a one-to-one correspondence between incoming I and Q samples and G1 and G2 terms required by the Viterbi decoder. The higher rates employ punctured coding techniques which periodically cause either a G1 or G2 term to be deleted. The puncturing pattern can have 6 possible ambiguity states for rate 2/3, 4 states for rate 3/4, 6 states for rate 5/6 and 8 states for rate 7/8. As part of the Viterbi decoding acquisition process, each puncturing state of each code must be tested. Total acquisition requires search of 26 different conditions. The process starts with rate 3/4 coding and proceeds sequentially to rate 2/3, 5/6, 7/8, and finally rate 1/2.

In some systems, it may be possible to experience spectral inversion. This might occur when different combinations of LNBs and tuners are employed which implement different frequency translation schemes. Correction of spectral inversion must be corrected with host processor interaction. If the host processor detects that QPSK lock is achieved, but Viterbi lock has not occurred within a specified time, then a bit must be set in the demodulator which reverses the spectrum.

The table below illustrates a typical acquisition timing. For this example, the symbol rate is one half of the clock rate. The code rate is set to 5/6, which requires 13 trial and errors before node sync is achieved. The carrier search logic requires 10 dwells at different frequencies (500 symbols per dwell) before demodulator lock is achieved.

Table 12: Example of Acquisition Timing

	Bit Times	Symbols	Clock Cycles
Carrier Search	8,333	5,000	10,000
Viterbi Node Sync	2,652	1,591	3,182
Byte Sync	16,000	9,600	19,200
Deinterleaver Flush	19,584	11,750	23,500
Reed Solomon	1,632	979	1,958
Total Timing	48,201	26,950	57,840

The total time required for acquisition could vary widely, depending upon the carrier search range and the time required for Viterbi node sync. For this example, however, the Byte Sync time and the time required to flush the deinterleaver dominates the total time. If a 90MHz clock were employed, the total acquisition time would be 0.642 milliseconds for this example

3.6 Reed Solomon Decoder

The serial output from the Viterbi is provided to the Word Sync circuits which searches for the eight bit frame sync word which occurs every 204 bytes. By detecting the polarity of the sync word, this module can correct polarity reversals in the data provided by the Viterbi decoder.

Byte serial data is provided to the convolutional deinterleaver, which reorders the received symbols. This process causes errors, which typically occur in bursts from the Viterbi decoder, to be distributed randomly over many blocks. This deinterleaved data is then provided to the Reed Solomon decoder which can reduce an error rate of 2×10^{-4} from the Viterbi decoder to less than 1 in 10^{-10}. The Reed Solomon decoder accepts input data in blocks of 204 bytes and produces error corrected blocks of 188 bytes. Maximum 8 bytes per a RS block can be corrected in RS decoder. Reedsolomon block includes on-chip BER calculator at the output of Viterbi to monitor signal quality or estimate the SNR of incoming signal. The calculated value can be read by accessing two read registers via utility bus such as I2C. It represents the number of errors among 2^{20} data bits.

The next process is descrambling, not to be confused with the descrambling which is part of conditional access. The purpose of scrambling the transmitted data and performing the inverse in the receiver is to insure that the spectrum of the transmitted waveform is always evenly distributed without significant discrete spectral lines. Without the scrambling/descrambling process, a transmitted sequence of all ones or all zeroes would result in strong spectral components and could interfere with other signals in the same satellite transponder.

The final process is data regulation. Viterbi Data and Viterbi Clock occur irregularly according to the code rate. Data clock regulation makes it possible to interface with external common interface devices. To make external bus interface more flexible, interface mode such as parallel or serial can be selected by mode selection register.

Parameter	Register
Regulate_data_clk	Bit 5 of 14H register
Mode_serial	Bit 0 of 18H register
Clk_pol	Bit 7 of 14H register

- **NORMAL INTERFACE MODE (parallel/serial)**
  If regulate_data_clk is reset, both parallel interface and serial interface work in normal operation which is same as HDM8513A. Parallel interface or serial interface can be alternated by modifying mode_serial bit (Refer to Figure 9 and Figure 10)

- **REGULATED INTERFACE MODE (parallel/serial)**
  If regulate_data_clk is set,all interfaces are from internal FIFO designed to regulate irregular interface signals. Data clock cycle is a little bit faster than the average of cycle of irregular data clock, so meaningless data can be output in invalid data period. Parallel interface or serial interface can be alternated by modifying mode_serial bit (Refer to Figure 11 and Figure 12)

- **CLOCK POLARITY**
  This bit is used to select the DATA_CLK polarity either for serial or parallel transport interface. If this bit is set to zero(default value), the transport data and control signals are latched at the positive edge of DATA_CLK. Otherwise, the signals are latched at the negative edge of DATA_CLK.

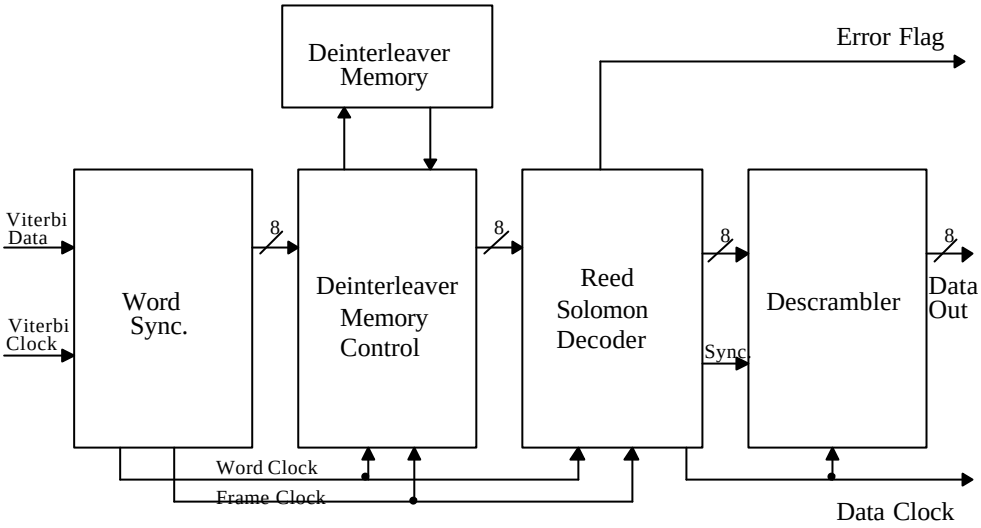


FIGURE 18: REED SOLOMON DECODER

3.7 Clock Generation PLL

An integrated VCO is locked to MxN times a reference frequency provided by a external clock.

1.Determining Output Frequency

Fully programmable feedback and reference divider capability allows virtually any frequency to be generated, not just simple multiples of reference frequency.
There are two status exist

(1) PLL Disable mode : The PLL is bypassed and the external clock is directly connected to the Internal clock.
(2) PLL Enable mode : The internal clock is connected to the generated clock of the PLL.

1.1 PLL disable mode
PLL control setting is as follows
TDM (Bit 7 of 0x23 register) is set to one and BYPASS (Bit 4 of 0x23 register) is set to one.

1.2 Normal Frequency mode
Output frequency range is limited to 160MHz.
PLL control setting is as follows:
TDM (Bit 7 of 0x23 register) is set to zero, and BYPASS (Bit 4 of 0x23 register) is set to zero.
At this condition, the output frequency, F(ck), is actually determined by the following equation.

$$F(ck) = \frac{F(ref) \times (\text{Feedback divisor})}{(\text{Reference divisor})}$$

F(ck) : Frequency of output
F(ref): Frequency of reference input
Feedback divisor : M[13:0]+2 , (0x25 and 0x26 registers)
Reference divisor : N[7:0]+1 , (0x27 register)

1.3 Extended Frequency mode
Output frequency range is limited to 320MHz.
PLL control setting is as follows
TDM (Bit 7 of 0x23 register) is set to zero, and BYPASS (Bit 4 fo 0x23 register) is set to one.
At this condition, the output frequency, F(ck), is actually determined by the following Equation

$$F(ck) = \frac{F(ref) \times (\text{Feedback divisor}) \times (\text{Pre divisor})}{(\text{Reference divisor})}$$

Pre divisor : $2^{P[1:0]+1}$, P is Bit 2 and 3 of 0x23 register

2. PLL Control Parameter setting

Besides of M (Feedback divisor), N (Reference divisor), P (Pre divisor) , You must determine vc (VCO range control vector), lfm (Loop filter mode selector), icp (Charge pump bias current control

vector) values appropriately.

2.1vc value setting

According to Output clock frequency, determine the vc values.

vc[1:0]	p[1:0]	Output Clock Frequency	
		min	max
00	00	40MHz	100MHz
	01	20MHz	50MHz
	10	10MHz	25MHz
	11	5MHz	12.5MHz
01	00	60MHz	100MHz
	01	30MHz	50MHz
	10	15MHz	25MHz
	11	7.5MHz	12.5MHz
10	00	80MHz	100MHz
	01	40MHz	50MHz
	10	20MHz	25MHz
	11	10MHz	12.5MHz
11	00	100MHz	100MHz
	01	50MHz	50MHz
	10	25MHz	25MHz
	11	12.5MHz	12.5MHz

2.2 lfm value setting

According to the table, determine the lfm value

lfm	(Reference Frequency)/(Reference Divisor)/15
7	Less than 0.01555
0	Less than 0.0258
1	Less than 0.0421
2	Less than 0.070
3	Less than 0.114
4	Less than 0.187
5	Less than 0.309
6	Greater than 0.309

2.3 icp value setting

According to the lfm value, you determine zero value, pole value, rlf value.

lfm	Zero value	Pole value	rlf value
7	External filter used	External filter used	External filter used
0	0.008	0.03	40
1	0.013	0.050	24.1
2	0.021	0.082	40
3	0.032	0.135	24.1
4	0.060	0.221	24.1
5	0.100	0.360	14.7
6	0.160	0.600	8.9

Step 1: According to the following formula, Kvcop is determined

$$Kvcop = \frac{100}{2^{p}}$$

P: Pre Divisor

Step 2: According to the following formula, Kpll is determined

$$Kpll = (Zero\ value * Pole\ value)^{1/2}$$

Step 3: According to the following formula, Kpd is determined

$$Kpd = 1000.0 * Kpll * Feedback\ Divisor / Kvcop / rlf$$

Step 4: According to the following formula, temp value is determined

$$Temp\ value = 2.0 * 3.14 * Kpd$$

Step 5: Finally, According to the following formula, icp is determined

$$icp = 16.5 - 16.0 / 40.0 * temp\ value$$

If icp value has fraction, truncate it.

3.8 DBS Receiver

The HDM8515 DVB Demodulator including a dual A/D converter and the MPEG-2 decoder provide the core digital processing technology for a DBS receiver conforming with the DVB standard.

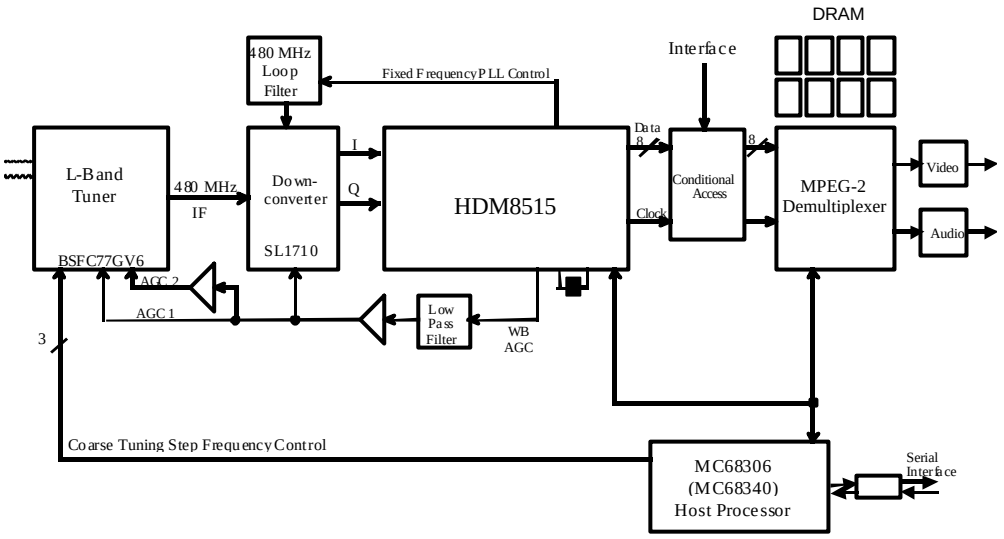


FIGURE 19: TYPICAL SET TOP BOX DEMODULATOR

A tuner accepts an L-band RF input from the antenna/LNB assembly located outside the building. A host processor controls the tuner to the nominal center frequency of the target signal. Baseband I and Q outputs from the downconverter are applied to an A/D converter pair which is sampled at a fixed rate, 90MHz as illustrated in this example. The tuner is required to filter the received baseband signal to a bandwidth less than half the sampling rate, but is not required to perform matched filtering.

Once the HDM8515 has locked to the target signal, the host processor may read the internal registers to determine the steady state frequency error. This error would be used to make period corrections to the programmed frequency of the tuner PLL.

The HDM8515 provides an output which can be used to control the analog AGC in the tuner. This digital signal must be filtered and amplified before applying it to the AGC control element. When the loop is closed, the signal applied to the A/D converters is optimally scaled.

3.9 DiSEqC Interface

The DiSEqC system is a communication bus between satellite receivers and satellite peripheral equipment, using only the existing coaxial cable.

1.1 DiSEqC mode

According to the value of DiSEqC_mode of 0x31 register, DiSEqC mode can be changed

0: 22KHz tone off
1: 22KHz tone on
2: Burst mode - on for 12.5ms ='0'
3: Burst mode - modulated 1:2 for 12.5ms ='1'
4: Modulated with bytes from DiSEqC instruction

1.2 DiSEqC instruction

Up to eight instruction data bytes are loaded into a bank of registers(0x29 -0x30). I2C automatic
register address incrementing is turn on. The number of bytes in the DiSEqC instruction must be defined in the DiSEqC_length of 0x31 register.

When the DiSEqC instruction data bytes have been loaded, set DiSEqC_mode of 0x31 register. At the same time, program DiSEqC_length of 0x31 register. The instruction data is modulated onto
22KHz signal and output from the DISEQC pin.

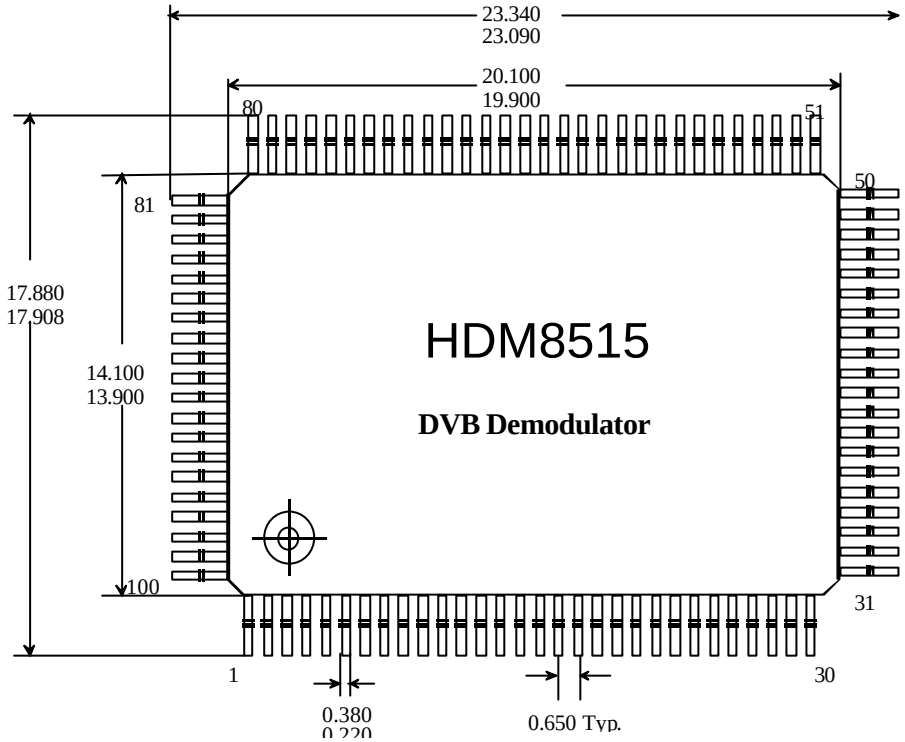
4. Mechanical Specifications

4.1 100 Pin Quad Flat Pack

4.1.1 Pin Assignment

1	DATA_CLK	**26**	TEST6	**51**	HI_ADDR5	**76**	DTACK
2	FRAME_ERROR	**27**	VDDA	**52**	HI_ADDR4	**77**	SDA_I2CO
3	FRAME_SYNC	**28**	VSSA	**53**	HI_ADDR3	**78**	SDA_I2C
4	VDD	**29**	VTOP	**54**	HI_ADDR2	**79**	SCL_I2CO
5	VSS	**30**	AIN_I	**55**	HI_ADDR1	**80**	SCL_I2C
6	DISEQC	**31**	IOVDDA	**56**	HI_A DDR0	**81**	VDD5
7	SIGMADELTA	**32**	IOVSSA	**57**	VDD	**82**	VSS
8	SYMBOL_CLOCK	**33**	REF_I	**58**	HI_DATA7	**83**	R/W(/RE)
9	WB_AGC	**34**	REF_Q	**59**	HI_DATA6	**84**	/CE
10	QPSK_LOCK	**35**	AIN_Q	**60**	HI_DATA5	**85**	/DS(/WE)
11	IOVDD	**36**	VBOT	**61**	HI_DATA4	**86**	VDD
12	IOVSS	**37**	TEST5	**62**	IOVDD	**87**	VSS
13	TEST15	**38**	TEST4	**63**	IOVSS	**88**	DATA7
14	TEST14	**39**	TEST3	**64**	HI_DATA3	**89**	DATA6
15	TEST13	**40**	VDDP	**65**	HI_DATA2	**90**	DATA5
16	TEST12	**41**	VSSP	**66**	HI_DATA1	**91**	LOCK
17	VDD	**42**	TEST2	**67**	HI_DATA0	**92**	DATA4
18	VSS	**43**	TEST1	**68**	VDD	**93**	DATA3
19	TEST11	**44**	TEST0	**69**	VSS	**94**	IOVDD
20	TEST10	**45**	CLOCK	**70**	VB_NODESYNC	**95**	IOVSS
21	TEST9	**46**	XTAL1_IN	**71**	VB_CLOCK	**96**	DATA2
22	TEST8	**47**	XTAL1_OUT	**72**	VB_DATA	**97**	DATA1
23	IOVDD	**48**	IOVDD	**73**	VDD	**98**	DATA0
24	IOVSS	**49**	IOVSS	**74**	VSS	**99**	DATA_VALID
25	TEST7	**50**	RESET	**75**	BUSMODE	**100**	DATA_STB

4.1.2 Package Dimensions



All Dimensions in mm

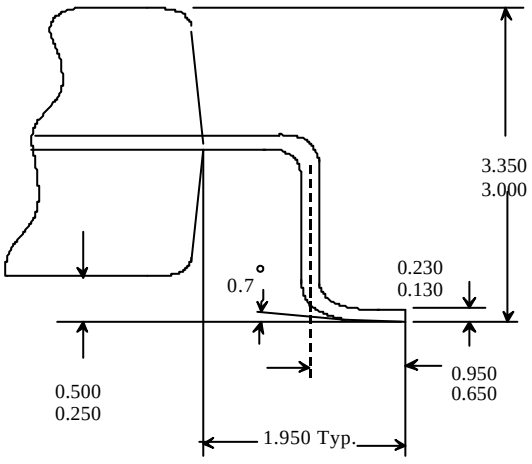


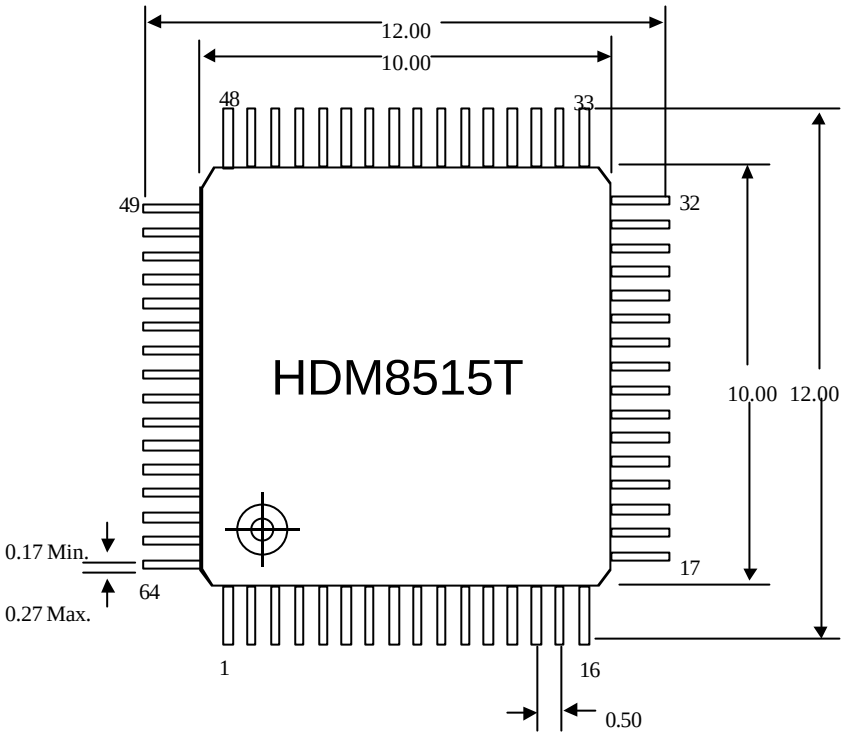
FIGURE 20: MECHANICAL CONFIGURATION

4.2 64 Pin Thin Quad Flat Pack

4.2.1 Pin Assignment (will be changed)

1	FRAME_ERROR	**17**	VSSA	**33**	VDD	**49**	IOVSS
2	FRAME_SYNC	**18**	VDDA	**34**	VSS	**50**	VDD
3	LNB_SYNC	**19**	REF_I	**35**	I2C_ADD2	**51**	VSS
4	WB_AGC	**20**	REF_Q	**36**	IOVDD	**52**	DATA7
5	IOVDD	**21**	AIN_Q	**37**	IOVSS	**53**	DATA6
6	IOVSS	**22**	VBOT	**38**	I2C_ADD1	**54**	DATA5
7	TEST13	**23**	VSSA	**39**	I2C_ADD0	**55**	LOCK
8	TEST12	**24**	VDD	**40**	VDD	**56**	DATA4
9	VDD	**25**	VSS	**41**	VSS	**57**	DATA3
10	VSS	**26**	N/C	**42**	VB_CLOCK	**58**	IOVDD
11	TEST11	**27**	N/C	**43**	VB_DATA	**59**	DATA2
12	TEST10	**28**	N/C	**44**	BUSMODE	**60**	DATA1
13	TEST9	**29**	XTAL1	**45**	SDA_I2C0	**61**	DATA0
14	TEST8	**30**	IOVDD	**46**	SDA_I2C	**62**	DATA_VALID
15	VTOP	**31**	IOVSS	**47**	SCL_I2C0	**63**	DATA_STB
16	AIN_I	**32**	RESET	**48**	SCL_I2C	**64**	DATA_CLK

4.2.2 Package Dimensions



All Dimensions in mm

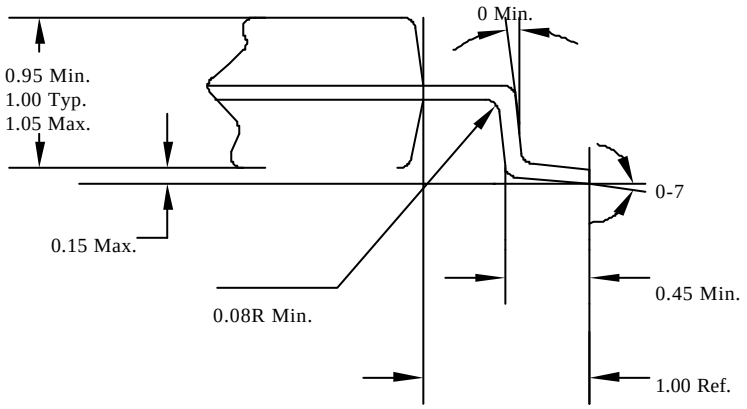


FIGURE 21: MECHANICAL CONFIGURATION

4.3 Recommended Analog Pin Connection

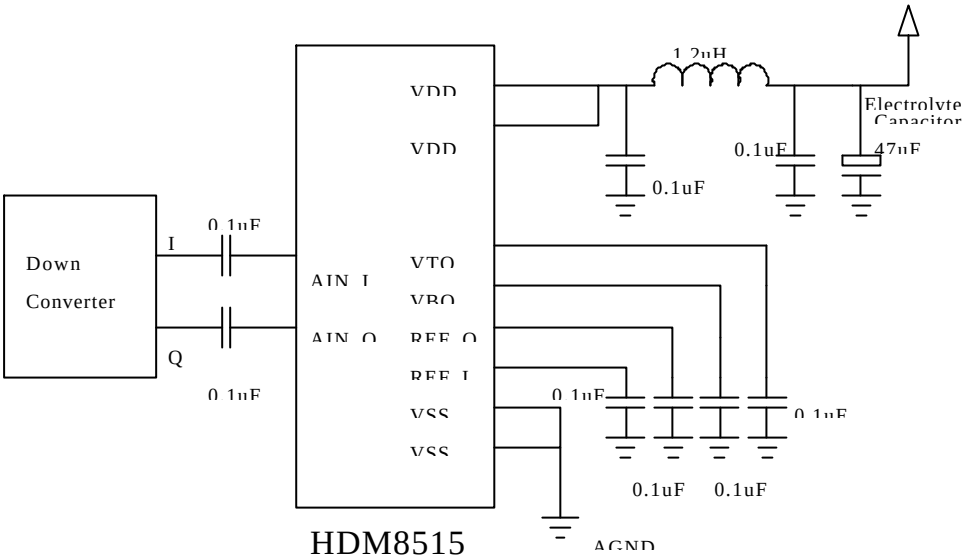


FIGURE 22: ANALOG PIN CONNECTION

4.4 Recommended Clock Generation Circuit

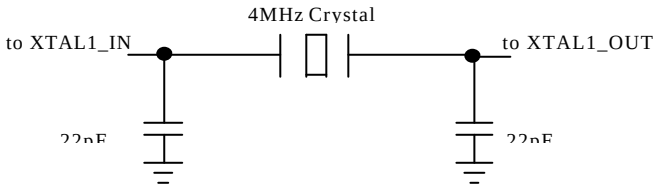


FIGURE 23: CLOCK GENERATION CIRCUIT

5. Signal Description

5.1 Inputs

XTAL1	XTAL1 can be configured either for sampling clock input or PLL reference clock input. The sampling clock rate must be a minimum of 1.33 times the symbol rate of the signal to be processed and at least equal to the total bandwidth of the signal to be processed.
RESET	A low on this signal causes the chip to be initialized. I/O registers are not cleared by this signal. This signal is asynchronous with respect to the clock.
AIN_I	Analog Input Signal for I channel. This should be AC coupled with Analog Input Source via 0.1uF capacitor.
AIN_Q	Analog Input Signal for I channel. This should be AC coupled with Analog Input Source via a 0.1uF capacitor.

5.2 Outputs

VTOP	Top Reference Voltage Output of about 2.0V. It should be bypassed to GND by 0.1uF capacitor. External bias voltage can be applied if necessary.
VBOT	Bottom Reference Voltage Output of 1.0V. It should be bypassed to GND by a 0.1uF capacitor. External bias voltage can be applied if necessary.
REF_I	Middle Reference Voltage for I Channel. It should be bypassed to GND by a 0.1uF capacitor.
REF_Q	Middle Reference Voltage for Q Channel. It should be bypassed to GND by a 0.1uF capacitor.
DATA [7:0]	The eight bit output data is provided in parallel format to be handed to an MPEG decoder for video and audio decompression.

DATA_CLK The DATA_CLK is used to latch data and control signal of transport stream. The data and control signals can be programmed to be latched either at positive or negative edge of DATA_CLK. This signal is used in conjunction with DATA_VALID to transfer data from the HDM8515. The DATA_CLK will continue to toggle during the 16 bytes that the DATA_VALID signal indicates that no data is available (see figure 9 and 10).

DATA_VALID When this signal is true, data is valid. This signal is not true during the time the 16 bytes of redundancy information is transmitted for the Reed Solomon decoder.

FRAME_SYNC This signal is true at the first byte of a block of 188/144 bytes.

DATA_STB This signal is used to transfer data from the HDM8515 to an MPEG decoder. This signal goes from low to high when a new byte of a 188 /144byte MPEG2 data stream block is available. This signal is inactive during the time the 16 redundancy bytes are transferred.

FRAME_ERROR This signal goes true when the Reed Solomon decoder detects that an uncorrectable number of errors have occurred. The error flag in the MPEG2 output stream is also set when this flag goes high.

WB_AGC This one bit output provides a measure of the external analog gain required for optimizing the signal applied to the analog to digital converters. This signal must be filtered, then applied to the analog gain control.

CLOCK This is a buffered clock output signal which may be used to drive other devices with the same clock which drives the HDM8515.

QPSK_LOCK This signal goes true when the QPSK demodulator has achieved phase lock.

VB_NODESYNC This signal goes true when the Viterbi decoder has achieved node synchronization.

LOCK This signal goes true when the output data is valid and all synchronization functions have been performed.

SYMBOL_CLOCK This signal, used for test purposes, goes true for a duration of one clock cycle for each received symbol. For symbol rates equal or greater than half the clock frequency, this signal at times may remain high for two successive clock cycles to indicate that two symbols have occurred.

VB_DATA The serial output of the Viterbi Decoder is provided on this pin. The information rate at this point is less than the rate of the input clock (less than 60Mbps if a 60MHz clock is employed). As long as valid convolutional encoding is employed, there is no constraint that the input signal adheres to MPEG2 format. This data is tapped priod to the polarity correction circuitry, so the data at this point may be inverted.

VB_CLOCK	The positive edge of this signal indicates that VB_DATA is valid.
SIGMADELTA	This is an one bit Sigma Delta D/A converter which has 8 bits of resolution. This output must be filtered with an analog low pass filter off the chip. This output may be used for any external analog control.
DISEQC	This is a DiSEqC output to control the LNB.
TEST[15:0]	The data provided on the test output signals is defined by data value of register 14H. Refer to register 14H.

5.3 Monitor and Control Interface

Three different modes are supported for the monitor and control interface. Two of the modes are 8 bit parallel interfaces, one which supports Intel microcontrollers and the other intended for Motorola microcontrollers. The third mode is a serial interface conforming to the I2C standard.

The I2C mode is activated by placing BUSMODE high at the same time both /RE and /WE are low simultaneously. When this mode is active, the seven bit I2C slave address of the HDM8515 is configured by the seven least significant bits of the HI_DATA[7:0] bus.

HI_DATA [7:0] This bi-directional data bus is used for transferring control parameters to the demodulator and for reading the status registers within the demodulator.

/CE Chip enable is an active low input to the demodulator which signifies that the other control signals are active.

/RE Read Enable is an active low input to the device which, when active at the same time chip enable is true, permits the device to drive the HI_DATA [7:0] lines. When BUSMODE is 0 (Motorola), this pin is read / not write (see timing diagrams).

/WE Write enable is an active low input to the device which, when true at the same time chip enable is true, causes input data on the HI_DATA [7:0] bus to be transferred to the register defined by the HI_ADDR [4:0] bus. When BUSMODE is 0 (Motorola), this pin is not data strobe (see timing diagrams).

HI_ADDR [4:0] The address bus defines which location within the device is to be accessed during a read or write operation.

BUSMODE BUSMODE selects the type of microcontroller/processor used to setup the chip. When high, an Intel processor/microcontroller interface is used. When low, a Motorola processor interface is used.

DTACK Data Acknowledge/Data Ready is a tristate output signal which informs the controlling processor that a data transfer has been acknowledged by the HDM8515.

SCL_I2C This pin provides the clock for the I2C interface when that mode is active.

SDA_I2C This pin is the data for the I2C interface and requires an external pull-up resistor as per the I2C standard.

SDA_I2CO This pin, which can be by-passed, is the data for the I2C interface.

SCL_I2CO This pin, which can be by-passed, provides the clock for the I2C interface.

5.4 I2C Mode

The HDM8515 utilizes the subaddress technique when the I2C mode is employed. In all cases, the HDM8515 behaves as the slave device (transmitter or receiver), whilst the host behaves as the master device. The seven bit slave address of the HDM8515 is user selectable, being defined by the inputs to HI_DATA[6:0] when the HDM8515 is in I2C mode.

Further information on the I2C bus formats and protocols is contained in the Philips Semiconductors I2C specification.

In a 100pin configuration, SDA_I2CO and SCL_I2CO are added to provide a by-passing function. When I2C bypass bit is set to zero, SDA_I2CO and SCL_I2CO are disabled.

5.4.1 I2C Write to HDM8515

The master initiates communication with the HDM8515 by generating a start condition and then sending the HDM8515 the slave address defined by the seven bit hardwired address on HI_DATA [6:0]. Per I2C convention, the eighth bit in the address byte is a read/not write bit, and should be set to zero. The HDM8515 will acknowledge the correctly sent slave address, following which the master sends an eight bit word address; this is the address of the first HDM8515 register to be written to. Once the word address has been acknowledged by the HDM8515, the master can then transmit the byte to be written to the word address. Once this byte is acknowledged by the HDM8515, the word address is automatically incremented and further data bytes may be transmitted by the master as necessary; one transmission may therefore contain a number of bytes of data to be written to a sequential set of addresses (dummy bytes should be written to addresses not defined in the HDM8515 register set to continue this process). The process is terminated by the master generating a stop condition. Figure 24 depicts this protocol.

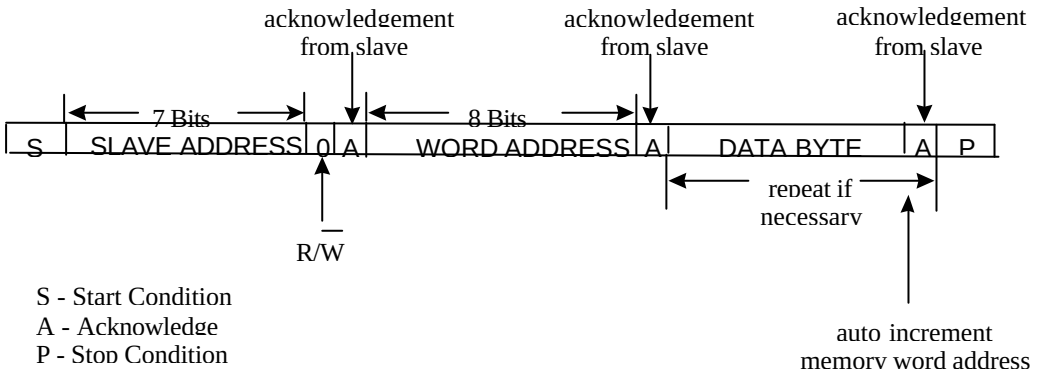


FIGURE 24: I2C WRITE TO THE HDM8515

5.4.2 I2C Read from the HDM8515

To read information from the HDM8515, the master must first write the desired word address. Hence the master must first generate a start condition and transmit the seven bit HDM8515 slave address defined on HI_DATA[6:0], with the eighth bit (read/not write) set to zero. Once this has been acknowledged by the HDM8515, the master transmits the first word address from which it wishes to read information. The master must then generate a second start condition and

retransmit the HDM8515 slave address, this time with the read/not write bit set to one (read). This will be acknowledged by the HDM8515, which then assumes the role of slave transmitter and transmits the requested byte. This byte should be acknowledged by the master receiver. If no stop condition is generated by the master, the HDM8515 will increment its word address pointer and transmit the next byte of information. This process is detailed in Figure 25.

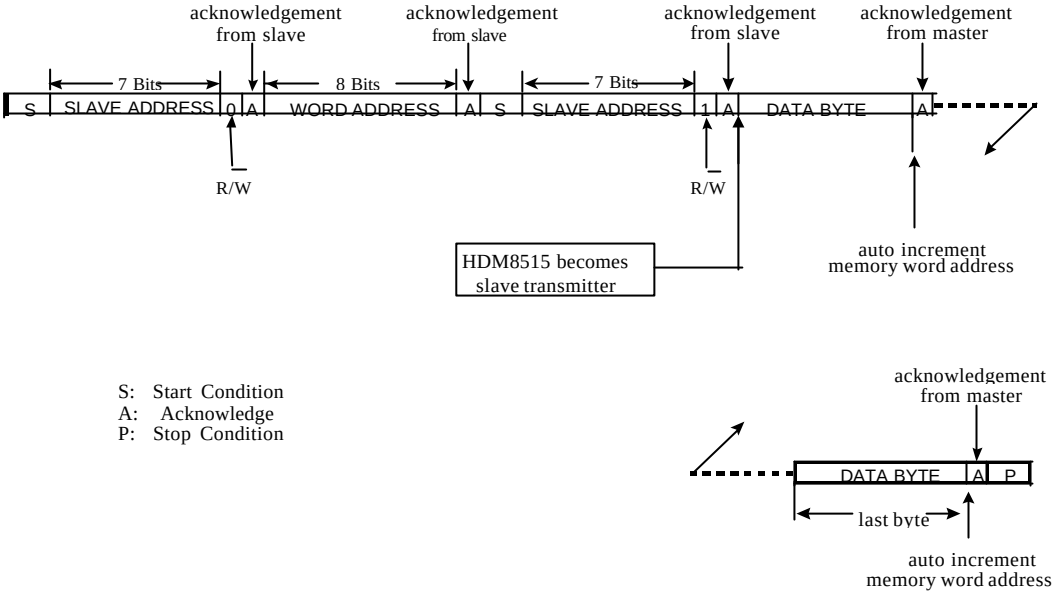


FIGURE 25: I2C READ FROM THE HDM8515

Table 13: I2C Slave Address

I2C ADD0	I2C ADD1	I2C ADD2	I2C Address
0	0	0	0000000
1	0	0	0000011
0	1	0	0001100
1	1	0	0001111
0	0	1	0110000
1	0	1	0110011
0	1	1	0111100
1	1	1	0111111

6. Register Definitions

6.1 Write Registers

ADDRESS (Hex)

00, 01, 02 **Symbol Timing Frequency**

The 20 bit straight binary number in this field establishes the symbol timing frequency utilized within the demodulator. Bit 7 of address 00 is the MSB and bit 4 of address 02 is the LSB. If Rs is the symbol rate and f_c is the clock frequency, the value to be stored in this 20 bit field is the integer portion of $R_S(2^{20})/f_C$.

03 **Symbol Timing Loop Gain Control**

This field establishes the K1 and K2 gain values for the second order loop filter of the symbol tracking loop. Bits 0,1,2 and 3 determine the straight-through gain, and bits 4,5,6 and 7 determine the integration path gain. The nominal value of this parameter in Hex, is expressed below for different ranges of symbol rate to clock rate ratios:

Clock/Symbol Rate	Value
2	FB
4	DA
8	B9
16	98
32	77
64	56

04, 05, 06 **Carrier Frequency**

The 20 bit, two's complement number in this field establishes the nominal carrier frequency of the demodulator. Bit 7 of address 04 is the MSB and bit 4 of address 06 is the LSB. The number in this 20 bit field multiplied by the clock frequency divided by 2^{20} is the carrier frequency in Hertz. When the carrier sweep function is active, this value defines the starting frequency.

07, 08 **Carrier Loop Filter Control**

This field establishes the K1 and K2 gain values for the second order loop filter of the carrier tracking loop. Bits 0,1,2 and 3 determine the straight-through gain, and bits 4,5,6 and 7 determine the integration path gain. The nominal value of this parameter in Hex, is expressed below for different ranges of symbol rate to clock rate ratios. Two loop filter configurations are provided at each symbol rate, one for steady state operation(08) and one which is used only for acquisition(07) to permit greater frequency pull-in. Initially the gains are set to acquisition values. When QPSK_LOCK is achieved, they are automatically switched to steady state values.

Clock/Symbol Rate	Steady State	Acqu.
2	C7	C7
4	A7	A7
8	87	87
16	67	67
32	47	47
64	27	27

09, 0A **Carrier Sweep Step Size**

This 16 bit value defines the size of the step of each carrier frequency dwell. Bit 7 of address 09 is the MSB and bit 0 of address 0A is the LSB. The number in this register is divided by 2^{16}, and multiplied by the clock frequency to determine the frequency step increment.

0B, 0C **Symbols Per Dwell**

This 16 bit value defines the time, in symbol periods, for which the demodulator will dwell before making the next frequency step in a sweep. Bit 7 of address 0B is the MSB and bit 0 of address 0C is the LSB.

0D **Number of Search Frequencies**

This 8 bit field determines the number of frequency steps which occur during the frequency sweeping process. Combined with the frequency step size, this determines the frequency span of the carrier sweep.

0E **Narrow Band AGC initial value**

This 8 bit field establishes the initial gain of the narrow band AGC. High numbers correspond to low gain associated with low symbol rates. If the narrowband AGC function is enabled, this number is used as a starting point and the closed loop will seek the optimum setting without processor interaction.

0F **Control Parameters**

Bit 0. Binary/Two's Complement

When this bit is a zero, the system expects the six bit modulation input samples in two's complement format, otherwise the input should be in offset binary format.

Bit 1. Spectrum Invert

When this bit is set to zero, the spectrum of the received signal is inverted. This has the effect of complementing the in-phase channel only.

Bit 2. Bias Cancel Enable

When this bit is a one, the internal circuit which cancels DC bias on the I and Q inputs is enabled. When this function is enabled, it is assumed that the input signal is scrambled with no significant DC component on either the I or Q.

Bit 3. Symbol Track Enable

When this bit is set to one, the symbol tracking function is enabled. When this bit is zero the symbol tracking frequency is forced to the nominal 20 bit programmed value.

Bit 4. Carrier Track Enable

When this bit is set to one, the carrier phase tracking function is enabled. When this bit is zero, the carrier frequency is forced to the 20 bit programmed value.

Bit 5. Sweep Hold

When this bit is set to one, the sweeping process is inhibited, and the nominal carrier frequency remains at the last value.

Bit 6. Narrowband AGC Mode 1 Enable

When this bit is set to one and the narrowband AGC is in Mode 1, the narrowband AGC self-adjusts to the optimum gain setting. When the bit is set to zero, the most recent value is held without updating.

Bit 7. Automatic Detection of Spectrum Inversion

When this bit is set to one, the spectrum inversion is detected automatically.

10 **Reset Functions**

Bit 0. Symbol Timing Frequency Accumulator

When this bit is set to zero, the frequency accumulator in the symbol tracking loop is cleared to zero. This bit must be set to one in normal tracking operation to implement a second order tracking loop, otherwise the loop is first order.

Bit 1. Carrier Phase Tracking Frequency Accumulator

When this bit is set to zero, the frequency accumulator in the carrier phase tracking loop is cleared to zero. This bit must be set to one in tracking operation to implement a second order loop filter otherwise the loop is first order.

Bit 2. Wideband AGC Accumulator

When this bit is set to zero, the accumulator in the wideband AGC is cleared to zero. In normal operation, this bit is set to one. When the wideband AGC is set to Mode 1, this bit has no effect as the integrator must be implemented in the external analog circuits.

Bit 3. Narrowband AGC Accumulator

When this bit is set to zero, the accumulator in the narrowband AGC is cleared to the initial value defined in location 0E. In normal operation, this bit is set to one.

Bit 4. Unused

Bit 5. Carrier Sweep Function

When this bit is set to zero, the sweep function is disabled and the carrier frequency is forced to the preset value defined in register locations 04, 05 and 06.

Bit 6. Viterbi Reset

When this bit is set to zero, the accumulator for the signal quality is cleared to zero. In normal operation, this bit is set to one.

Bit 7. Reed Solomon Error Counter

When this bit is set to zero, the counters for the number of corrected errors and the number of uncorrected code words are cleared to zero.

11 **Wideband AGC Control**

Bit 0. Wideband AGC Mode

When this bit is set to one (Mode 0), the WB AGC output must be filtered with an external integrating analog filter to implement a first order feedback loop. When this bit is zero (Mode 1), a digital integrator within the HDM8515 performs this function and the only external analog function required is a low pass filter to remove the high frequency components of the sigma delta converter output.

Bit 1. WB AGC Invert

When this bit is set to zero a high duty factor on the WB AGC output corresponds to too much gain. When the control bit is set to one, high duty factor corresponds to not enough gain.

Bit 2. WB AGC Hold

During normal tracking operation, this bit is set to one. When this bit is set to zero and the wideband AGC is in Mode 1, the digital integrator is held to the most recent value and loop updates are inhibited.

Bit 3. LNB Hold

When this bit is set to one, the output of LNB-Tone is held on zero.

Bit 4. I2C By-pass

When this bit is set to zero, SCL_I2CO and SDA_I2CO are disabled. The default is one and Data/clock can be by-passed.

Bits [7:5]. WB AGC Gain

This three bit field defines the time constant of the WB AGC in Mode 1. A value of zero corresponds to the shortest time constant and 7 corresponds to the slowest time constant.

12 **LNB Tone**

This eight bit value establishes the control for LNB tone generator. If f_t is the desired frequency and f_C is the clock frequency, the value to be stored in this 8 bit field is the integer portion of $f_t(2^{17})/f_C$. The default value(20H) generates 22KHz tone at 90MHz sampling clock.

13 **Sigma Delta**

This eight bit input value establishes the control for Sigma Delta converter. This function is independent of other demodulator functions and is provided as control for external analog components.

The eight bit data written to this location defines the data presented on the 16 bit test bus. For configurations where the data is updated once per symbol period, the data changes at the rising edge of SYMBOL_CLOCK
(in the case that SYMBOL_CLOCK remains high for consecutive CLOCK
cycles, the test port data will also change accordingly during the high period of SYMBOL_CLOCK due to the arrival of another symbol).

Bits [2:0]. Test port configuration

00H Output is tristate.

01H Test bits [13:8] provide the I baseband filter output. Test bits [5:0] provide the Q baseband filter output. This information is updated once per symbol period.

02H Test bits [15:0] provide the sixteen most significant bits of the demodulator carrier phase test bits. This information is updated once per
symbol period.

03H Test bits [15:0] provide the sixteen most significant bits of the demodulator symbol phase test bits. This information is updated once per
symbol period.

04H Test bits [15:8] provide the Reed Solomon output data. Test bits [7:0] provide the deinterleaver output data. This information is updated at the Reed Solomon clock rate; when the transport stream output is configured to parallel output mode, DATA_CLK may be used as an output clock for this data.

05H All Zero.

06H Test bits [13:8] provide the six bit I-channel data from the ADC. Test bits [5:0] provides the six bit Q-channel data from the ADC. This information is updated at the fixed rate sample clock.

07H In this mode the test pins are used as input pins. The internal ADC is disabled, and the inputs at the test pins are fed directly to the demodulator. Test bits [13:8] are used as I-channel input and test bits [5:0] are used as Q-channel input. This information is updated at the fixed rate sample clock.

Bit 3. Transport error Indicator Enable/Disable

Enables/Disables the transport error indicator,1 bit indicator in transport header. When this bit is set to 1 and if transport error is internally detected the transport error indicator bit is set to 1. When zero this functionality is disabled.

Bit 4. This bit should be fixed to zero

Bit 5. Regulated Data Clock

Enables/Disables the data and data clock regulator. When this bit is set to 1, data output and data clock are regulated by FIFO operation. When this bit is set to 0, internal data output and internal data clock are by-passed

Bit 6. This bit should be fixed to zero.

Bit 7. Clock Polarity

This bit is used to select the DATA_CLK polarity either for serial or parallel transport interface. If this bit is set to zero(default value), the transport data and control signals are latched at the positive edge of DATA_CLK. Otherwise, the signals are latched at the negative edge of DATA_CLK.

15 **Viterbi Lock Threshold**

Register 15 to 17 contain control parameters for synchronization in Viterbi decoder. Ordinary users are recommended to use the default value.

Bit[7:4] defines the lock threshold for VB_NODESYNC. Viterbi decoder decides that the correct code rate has been found. A large number means it takes longer to find the correct code rate in automatic detection mode. It should be greater than 7. The default value is 12.

Bit[3:0] defines the lock fail threshold. Viterbi decoder rejects a code rate and moves on to the next code rate. A small number means Viterbi decoder tries more data before it moves to the next code rate. It should be less than 7. The default value is 2.

16 **Viterbi Unlock Threshold**

This number defines the threshold to maintain the Viterbi lock state. A large number means it needs more bad data to get out of the viterbi lock state and re-start searching the correct code rate. The default value is 1.

17 **Viterbi Byte-Sync control**

Once the viterbi lock(VB_NODESYNC) is achieved, the Viterbi decoder tries to find the byte-sync. This 8-bit register is used to set “unlock-threshold” for the byte-sync. Large number means it needs more bad-data to get out of the byte-sync state, i.e. less sensitive to noise. The default value is 1.

18 **Control Parameters for Viterbi and RS Decoders**

Bit 0. Parallel or Serial Output

Controls the transport stream output of the 8515 to serial or parallel mode.
"0" (default) means the 8515 MPEG output is parallel.
"1" means the 8515 MPEG output is serial. The LSB of the data bus(data[0] - pin 98) is used as the serial output pin.

Bit 1. MPEG2 Data

"0" (default) means the incoming data is MPEG2 decoded. In this mode a sync byte is expected every 188 bytes.
"1" means non-MPEG2 data. The Viterbi decoder doesn't check the existence of the sync byte.

Bit [4:2]. Depuncturing Rate

It defines the depuncturing rate of the Viterbi decoder. When vb_autocode is disabled, the depuncturing rate is set to this value.

0 --- 1/2
1 --- 2/3
2 --- 3/4
3 --- 5/6
4 --- 7/8
5 --- 6/7

Bit 5. Viterbi Auto Decoding Mode

When this bit is set to 1, the Viterbi decoder automatically finds the correct code rate of the incoming signal. When this bit is set to 0, the code rate is set to the user-defined value at bit[4:2]. The default is 0.

Bit 6. DSS Mode

When this bit is set to 0, this device operates as DVB mode. When this bit is set to 1, this device operates as DSS mode. In that case, the roll-off factor of the Nyquist filter is set to 0.2. The default is 0 (DVB).

Bit 7. BPSK Mode

When this bit is set to 0, the demodulator assumes the incoming data is QPSK-modulated. When this bit is set to 1, the demodulator assumes the incoming data is BPSK-modulated.

19 **Rate 1/2 Threshold Select**

This seven bit parameter defines the threshold used in the Viterbi decoder node synchronization process. For rate 1/2, the nominal value is 30 (1EH).

1A **Rate 2/3 Threshold Select**

This seven bit parameter defines the threshold used in the node synchronization process. For rate 2/3, the nominal value is 30 (1EH).

1B **Rate 3/4 Threshold Select**

This seven bit parameter defines the threshold used in the node synchronization process. For rate 3/4, the nominal value is 40 (28H).

1C **Rate 5/6 Threshold Select**

This seven bit parameter defines the threshold used in the node synchronization process. For rate 5/6, the nominal value is 60 (3CH).

1D **Rate 6/7 Threshold Select**

This seven bit parameter defines the threshold used in the node synchronization process. For rate 6/7, the nominal value is 60 (3CH).

1E **Rate 7/8 Threshold Select**

This seven bit parameter defines the threshold used in the node synchronization process. For rate 7/8, the nominal value is 60 (3CH).

Bit 7. This bit should be fixed to zero.

1F **Bit 7.** This bit should be fixed to zero.

20 **Unused**

21 **Wideband AGC threshold**

Bits [5:0]. Wideband AGC threshold

It determines the threshold of wide band AGC accumulator. This value controls the magnitude of ADC input.

Bit 6. Unused

Bit 7. Wideband AGC Frequency down

It regulates wide band AGC frequency. When this bit is set to zero, system clock for wide band AGC frequency is sampling clock. Otherwise, system clock for wide band AGC frequency become sixteen times of sampling clock frequency.

22 **Scaling factor**

Bits [2:0]. Scaling factor

This value manages to scale the soft decision demodulator outputs to the proper levels for the 4 bit soft decision Viterbi inputs. If an overflow is detected, the output is limited to maximum or minimum 6 bit values. The upper four bits of this result are passed to the Viterbi decoder.

00H QPSK output

01H QPSK output * 1.25

02H QPSK output * 1.5

03H QPSK output * 1.75

04H QPSK output * 2.00

05H QPSK output * 2.25

06H QPSK output * 2.5

07H QPSK output * 2.75

23 **Clock Generation PLL Control Parameter-1**

Bits [1:0]. VCO range control vector

Default value is 1.

Bits [3:2]. Pre divisor

In case of Extended Frequency mode, this value is used the calculation of
output Frequency. Default value is 0.

Bit 4. Digital part test mode

When this bit is set to 1and Bit 7 of this register is set to 1, the PLL is bypassed and the external clock signal is directly connected to the internal clock. When this bit is set to 0, the generated clock of the PLL is connected to the internal clock. The default is 1.

Bit 5. VCO power down mode

When this bit is set to 1, VCO power down and does not oscillate

Bit 6. PLL power down mode except VCO

When this bit is set to 1, PLL power down and digital circuits do not operate and charge pump is disabled.

Bit 7. PLL By-pass

If this bit is set to 0 and Digital part test mode (Bit 4 of this register) is set to 0, then PLL Normal frequency mode is selected. Else if this bit is set to 1 and digital part test mode is set to 0, then PLL Extended frequency mode is selected.

24 **Clock Generation PLL Control Parameter-1**

Bits [1:0]. Unused

Bit 2. Counter toggle test

Internal used Only. The default is 0.

Bits [5:3]. Loop filter mode selector

The default is 5H.

Bits [7:6]. Charge pump test mode

Internal used Only. The default is 0.

25, 26 **M Divider Ratio**

This 14 bit value defines a feedback divider with a divider ratio M. Bit 5 of address 25 is the MSB and bit 0 of address 26 is the LSB. The default value is 002Bh

27 **N Divider Ratio**

It defines a reference divider with a divider ratio N. The default value is 01h

28 **Charge pump bias current control vector**

Bits [3:0]. The default value is 1.

29 **DiSEqC message frame byte**

It defines the format of frame in DiSEqC message

2A **DiSEqC message address byte**

It defines the format of slave address in DiSEqC message

2B **DiSEqC message command byte**

It defines the format of command in DiSEqC message.

2C, 2D, 2E, 2F, 30 **DiSEqC message data byte(s)**

For some DiSEqC message, additional data is carried in one or more subsequent data byte(s).

31 **DiSEqC Mode Control**

Bit 0. DiSEqC By-pass

When this bit is set to 1, the function of DiSEqC interface is disabled. When this bit is set to 0, DiSEqC interface is enabled, The default is 1.

Bits [3:1] DiSEqC mode

It determines one of following DiSEqC modes.

0: 22KHz off
1: 22KHz on continuous
2: Burst mode - on for 12.5ms ='0'
3: Burst mode - modulated 1:2 for 12.5ms ='1'
4: Modulated with bytes from DiSEqC instruction.
5-7: Reserved

Bits [7:4] DiSEqC message length

Number of byte in DiSEqC instruction, to output on DISEQC pin.

6.2 Read Registers

ADDRESS (Hex)

00 **Narrowband AGC Accumulator**

The current value of the 8 bit AGC accumulator may be read from this location.

01, 02, 03 **Symbol Timing Frequency Accumulator**

The current value of the 24 bit frequency accumulator in the symbol timing loop filter may be read from these 3 locations.

04, 05, 06 **Phase Tracking Frequency Accumulator**

The current value of the 24 bit frequency accumulator in the carrier phase loop filter may be read from these 3 locations.

07 **QPSK Lock Status**

Bit 0. QPSK Lock Flag

When this bit is set to one, the QPSK demodulator is phase locked.

08 **Wide Band AGC Accumulator**

This eight bit value represents the most significant bits of the accumulator in the first order wideband AGC loop. This data only has meaning when the wideband AGC is in Mode 0.

09, 0A **Sweep Frequency**

The 16 bit sweep accumulator is available at this location. Bit 7 of address 09 is the MSB and bit 0 of address 0A is the LSB. The receiver frequency is determined by adding the Sweep Frequency with the carrier frequency accumulator (read addresses 04, 05 and 06) and the nominal carrier start frequency (write addresses 04, 05 and 06).

0B **In-Phase**

The six LSB bit output of the In-phase baseband filter is available at this location. This data is updated once per symbol.

0C **Quadrature**

The six LSB bit output of the quadrature baseband filter is available at this location. This data is updated once per symbol.

0D **Noise Power**

This eight bit output provides a measure of the noise component of the signal when QPSK lock is achieved. Higher numbers correspond to lower signal-to-noise ratio conditions. The quality of this metric is improved if the narrowband AGC is disabled for a minimum of 1000 symbol periods before this parameter is read.

0E, 0F **BER Calculator**

The current value of the 16bit BER is used to monitor the signal quality or estimate the SNR of incoming signal at the output of Viterbi. Bit 7 of address 0E is the MSB and bit 0 of address 0F is the LSB. It represents the number of errors among 2^{20} data bits.

10, 11, 12 **Carrier Frequency_1**

This 24 bit value represents the carrier frequency of the first frequency translator.

13, 14, 15 **Carrier Frequency_2**

This 20 bit value represents the carrier frequency of second frequency translator. Bit 7 of address 13 is the MSB and bit 4 of address 15 is the LSB.

16,17,18 **Signal Quality**

This 24 bit signal provides a measure of quality of the signal processed by the Viterbi decoder. This parameter can be used to infer bit error rate and input signal-to-noise ratio for signals which are within a few dB of threshold. Bit 7 of address 16 is the MSB and bit 0 of address 18 is the LSB.
The specific definition of this signal for each coding rate is TBD.

19 **Viterbi Rate**

This three bit number represents the code rate of the Viterbi decoder.

Rate 1/2	0
Rate 2/3	1
Rate 3/4	2
Rate 5/6	3
Rate 7/8	4

1A **Reed Solomon Errors**

The four bit number at this location indicates the number of errors corrected in the most current block of 188 bytes. This number may range from 0 to 8.

1B **FEC Lock**

Bit 0. Viterbi Node Sync

When this bit is set to one, the Viterbi decoder has successfully established node synchronization.

Bit 1. Frame Sync

When this bit is set to one, the FEC chip has successfully established word sync and frame sync.

Bit 2. Viterbi Byte Sync

When this bit is set to one, the Viterbi decoder has successfully established byte-synchronization.

Bit 3. Pi Ambiguity

When this bit is set to one, the Viterbi decoder has successfully resolved pi ambiguity in the input data. (i.e inverted data)

Bit 4. Pi/2 Ambiguity

When this bit is set to one, the Viterbi decoder has successfully resolved pi/2 ambiguity in the input data

1C,1D **Accumulated Reed Solomon Errors**

These two registers present a count of corrected errors since it was last reset. Bit 7 of address 1C is the MSB and bit 0 of address 1D is the LSB. These registers are reset by writing value to address 10H.

1E **Accumulated Reed Solomon Data**

This register presents a count of the uncorrected code words since it was last reset. When it reaches its maximum count(255), it rolls back to zero
and starts counting again. This register is reset by writing value to address 10H.

1F **Device Identifier**

This register present device identifier. The current value of this register is
F0H

23 **Reference Divider Test Output**

Internal used Only.

24, 25 **Feedback Divider Test Output**

Internal used Only.

26 **PLL Lock Indicator**

Bit 0. This 1 bit value represents the staus of PLL lock
If PLL is locked, this value is 1, else 0.

Appendix

A1. Loop Filter Programming Application Note

To illustrate that the symbol timing recovery loop and the carrier phase recovery loop are both programmable, several simulations were performed with different loop parameter conditions. These simulations were performed with a symbol rate of two samples per symbol, corresponding to 30M symbols-per-second if a 60MHz clock were utilized.

Figure A1 illustrates the transient response of the symbol phase with three different loop conditions (K1=5, K2=10; K1=4, K2=9; and K1=8, K2=7). The vertical scale represents phase over a 360 degree range (524,287 to -524,288). All test cases were run at high signal-to-noise ratio. The highest gain condition could be used for fast acquisition as well as for steady state with high code rate conditions, while the intermediate gain is a suitable steady state setting for rate 1/2 codes (minimum E_b/N_0 of 4 dB). The lowest gain setting corresponds to ultra low loop bandwidth and may be considered for maintaining lock without phase jumps during deep signal fades.

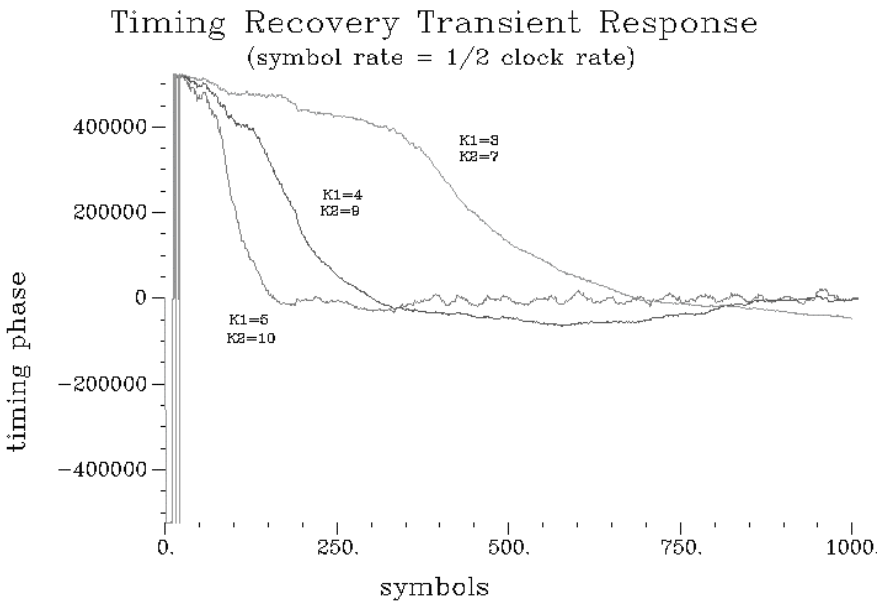


FIGURE A1: SYMBOL TIMING RECOVERY TRANSIENT RESPONSE

Figure A2 illustrates the transient response of the carrier tracking loop with the same loop bandwidth settings at high signal-to-noise ratio. The phase step for this test corresponds to 45 degrees. The actual bandwidth of the carrier loop is greater than that of the symbol loop for the same settings because the carrier loop must cope with greater dynamics (such as frequency offset and drift). Figure A3 illustrates the transient response of the carrier phase tracking loop under the same conditions at minimum signal-to-noise ratio (E_b/N_0 of 4 dB with rate 1/2 coding). The highest bandwidth case will pull in with a carrier frequency error of + or - .005 of the symbol rate at this minimum signal level. Higher loop bandwidth may be programmed to provide greater pull-in with higher signal-to-noise ratio conditions.

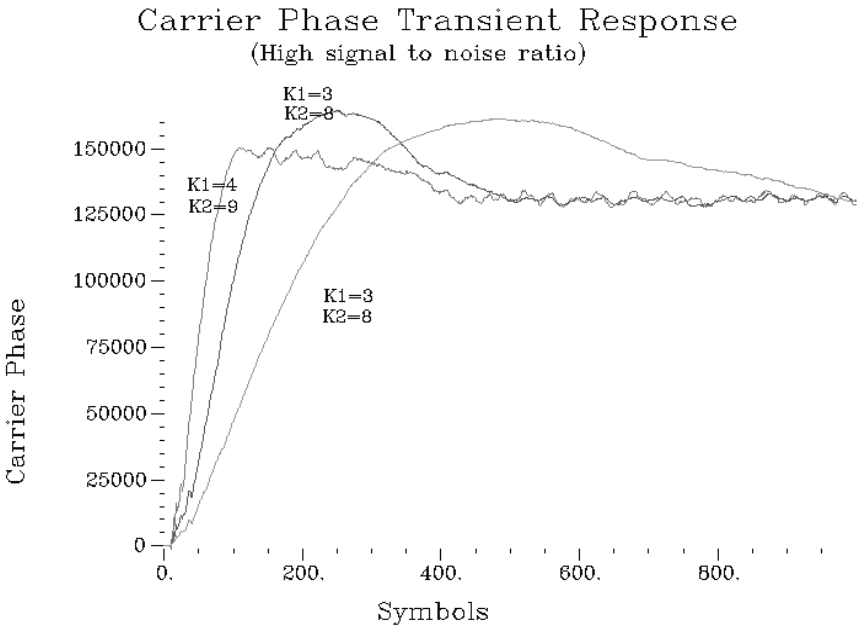


FIGURE A2: CARRIER PHASE RECOVERY TRANSIENT RESPONSE

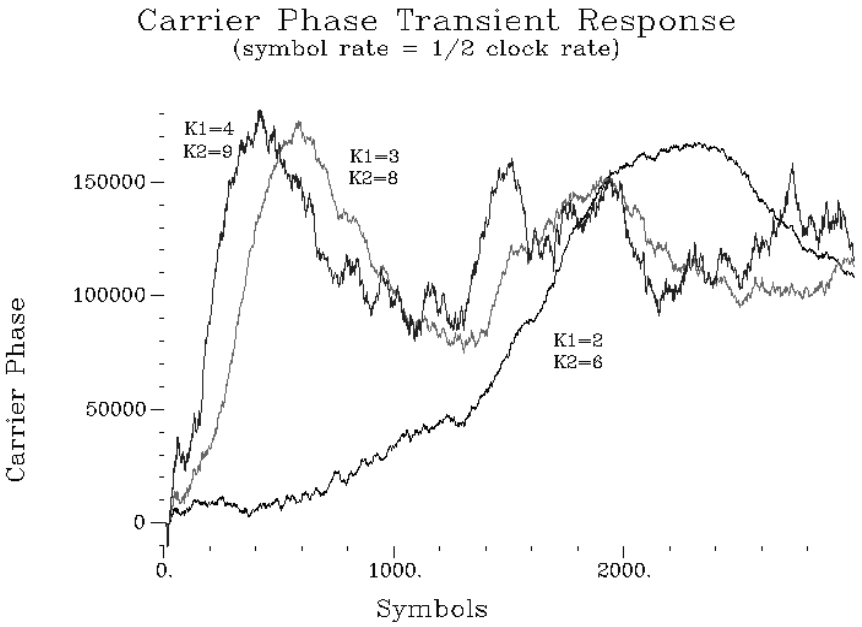


FIGURE A3: CARRIER PHASE RECOVERY TRANSIENT RESPONSE WITH LOW SNR

A2. False Lock Escape Application Note

A QPSK signal will have inherent false lock states at frequency offsets of + or - n/4 of the symbol rate. Most DBS signals which have symbol rates of 20M symbols-per-second or higher will not experience false lock because the carrier frequency uncertainty is less than 1/4 of the symbol rate.

The HDM8515 is designed to process low data rate signals which may experience false lock, particularly at high signal-to-noise ratio conditions. The HDM8515 will permit recovery from false lock with some added host processor interaction. Specifically, the processor must initialize the internal carrier frequency search hardware to search over a carrier frequency range of 1/4 of the symbol rate. If QPSK lock is achieved, but no Viterbi lock is achieved, the processor would assume this is a false carrier lock, then program the HDM8515 to search another carrier frequency range covering 1/4 of the symbol rate. When both QPSK lock and Viterbi lock have been achieved, the search is completed. This technique is reliable because the HDM8515 utilizes a fixed frequency clock which is not subject to inaccuracy associated with analog VCOs. This accuracy insures that the multiple search ranges are perfectly continuous with respect to each other with no overlap.

A3. Performance with Interference.

In order to evaluate the filter employed within the HDM8515 with respect to attenuating out-of-band interference, a test was performed utilizing the COSSAP simulator. The desired signal, at zero frequency, was configured to utilize 16 samples-per-symbol (corresponding to 3.75MHz symbol rate if a 60MHz clock is employed). An interfering signal was added with the same characteristics, except that the amplitude was made to be 10dB higher than that of the desired signal, the data pattern was different and the carrier frequency was offset from that of the desired signal. Several offset frequencies were evaluated for this case. Figure A4 illustrates the spectrum of the test condition when the offset frequency is 1.35 times the symbol rate.

Figure A5 illustrates the measured bit error rate for various conditions. The error rate on the I channel was measured separately from that of the Q channel, and the horizontal axis is scaled in dB for one component (I or Q of the signal). For example, the point labeled 1dB corresponds to SNR (noise bandwidth = symbol rate) of 4dB or E_b/N_0 of 4dB if rate 1/2 coding is employed.

The theoretical performance for coherent PSK is shown with the solid line. The curve closest to theoretical is the demodulator performance with no other interferers and corresponds to an implementation loss of about 0.2dB. When the interferer was placed at a frequency of either 2.0 or 1.35 times the symbol rate away from the desired carrier, there is an additional degradation ranging from 0dB to 0.1dB. The worst case occurs when the interferer is placed at only 1.28 times the symbol rate from the carrier of the desired signal. In this case, the performance has degraded with respect to the no interference case by 0.3 to 0.5dB.

Figure A6 illustrates performance with an interferer which is 20dB higher than the desired signal and separated in frequency by 2 times the symbol rate. In this case, the performance has degraded by 0.7 to 0.8dB from the case with no interferer.

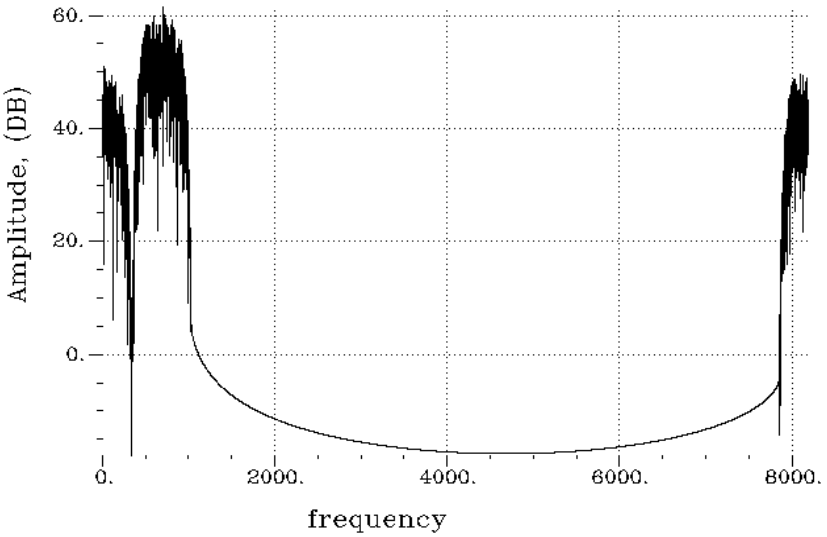


FIGURE A4: ADJACENT CHANNEL INTERFERENCE OF 10 DB, 1.35 SPACING

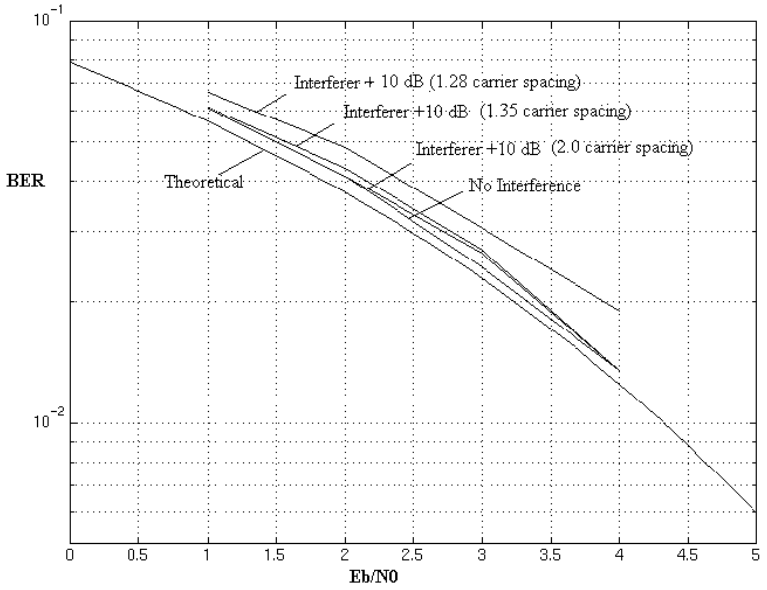


FIGURE A5: PERFORMANCE WITH INTERFERER AT DIFFERENT CARRIER SPACINGS

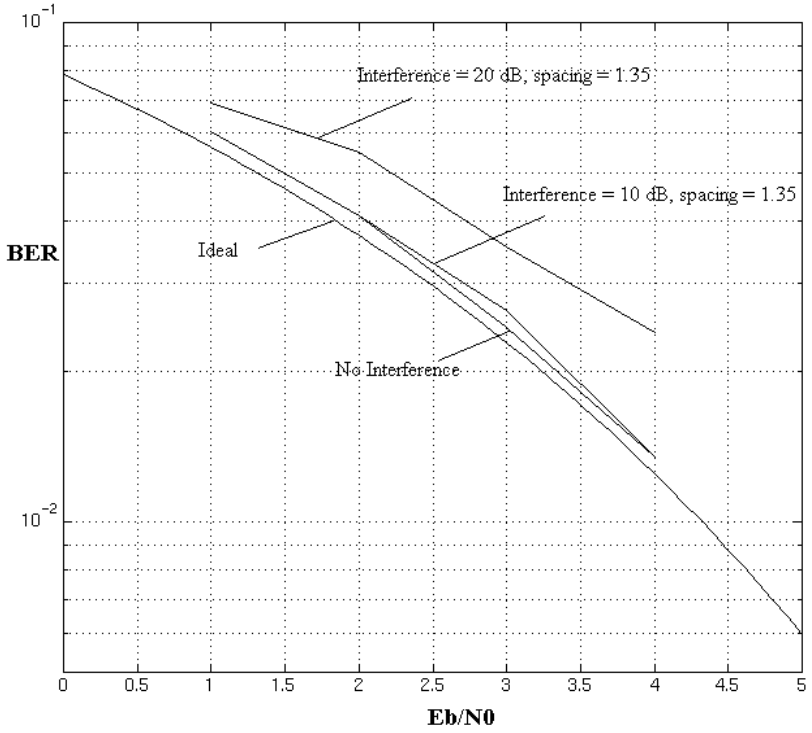


FIGURE A6: PERFORMANCE WITH +10 DB INTERFERER

A4. Nyquist Criteria Considerations

The HDM8515 is clocked at 60MHz, yet processes signals with symbol rates as high as 45M symbols-per-second. At first thought, this might appear to be violating the Nyquist criteria which states that the sampling rate must be at least twice the highest frequency component. The total bandwidth of the 45Msps signal, with 35% excess bandwidth, is about 60MHz.

The samples provided to the HDM8515 are complex samples, which is equivalent to 120M samples-per-second, which does satisfy the Nyquist criteria. Another way of looking at this is to examine the baseband signal. The signal bandwidth covers 60MHz, but the baseband spectrum covers from -30MHz to +30MHz. There are no baseband frequency components greater than 30MHz, and the 60MHz clock is adequate as long as complex samples are taken.