



Micro Commercial Components
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SMCJ5348 THRU SMCJ5388

Silicon
5.0 Watt
Zener Diodes

Features

- Surface Mount Application
- 11 thru 200 Volt Voltage Range
- Built-in strain relief
- Glass passivated junction
- Low inductance

Mechanical Data

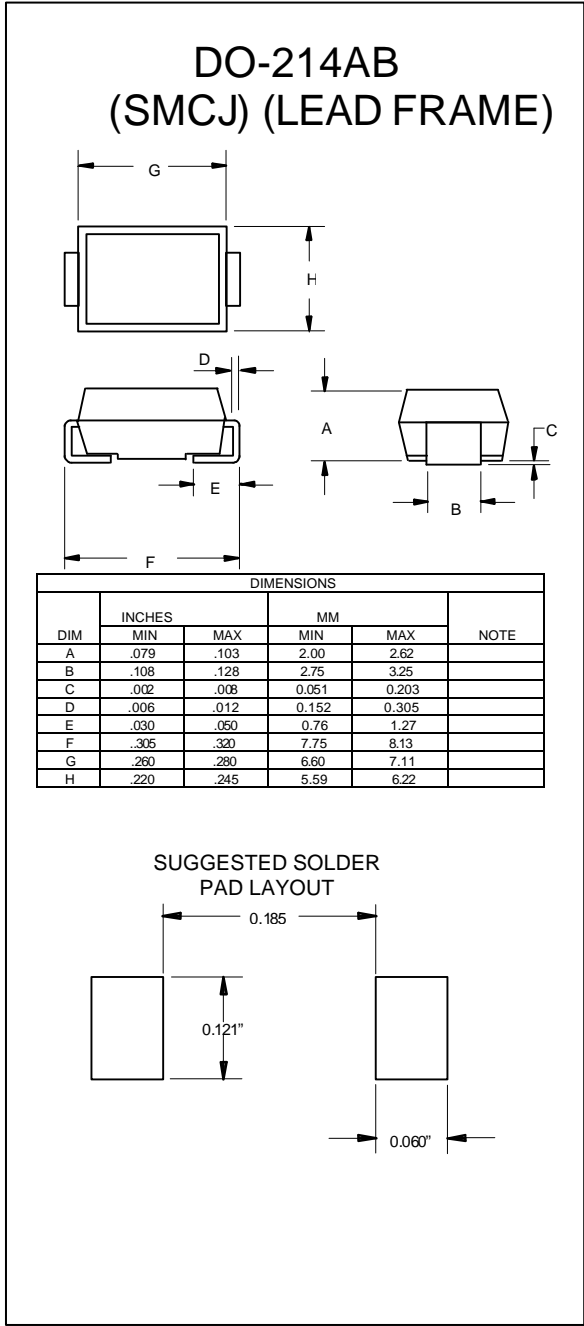
- Case: JEDEC DO-214AB Molded plastic over passivated junction
- Terminals solderable per MIL-STD-750, Method 2026
- Standard Packaging: 16mm tape(EIA-481)
- Maximum temperature for soldering: 260°C for 10 seconds.
- Plastic package has Underwriters Laboratory Flammability Classification 94V-0

Maximum Ratings @ 25°C Unless Otherwise Specified

DC Power Dissipation	P_D	5.0W	(Note: 1)
Peak forward Surge Current 8.3ms single half	I_{FSM}	See Fig.5	(Note:1,2)
Operation And Storage Temperature	T_J, T_{STG}	-55°C to +150°C	

NOTES:

1. Mounted on 8.0mm² copper pads to each terminal.
2. 8.3ms single half sine-wave, or equivalent square wave, duty cycle = 4 pulses per minute maximum.



SMCJ5348 thru SMCJ5388



ELECTRICAL CHARACTERISTICS ($T_A=25\text{ }^{\circ}\text{C}$) unless otherwise noted, $V_F=1.2\text{ Max @ }I_F=1\text{A}$ for all types.

Type No. (Note 1.)	Nominal Zener Voltage $V_Z @ I_{ZT}$ volts (Note 2.)	Test current I_{ZT} mA	Maximum Zener Impedance		Max reverse Leakage Current			Max Surge Current I_r Amps (Note 3.)	Max Voltage Regulation ΔV_Z , Volts (Note 4.)	Maximum Regulator Current I_{ZM} mA (Note 5.)	Device Marking Code
			$Z_{ZT} @ I_{ZT}$ Ohms (Note 2.)	$Z_{ZK} @ I_{ZK} = 1$ mA Ohms (Note 2.)	I_r mA	@ V_R Volts					
						Non & A Suffix	B-Suffix				
SMCJ5348	11	125	2.5	125	5	8	8.4	8	0.25	430	348B
SMCJ5349	12	100	2.5	125	2	8.6	9.1	7.5	0.25	395	349B
SMCJ5350	13	100	2.5	100	1	9.4	9.9	7	0.25	365	350B
SMCJ5351	14	100	2.5	75	1	10.1	10.6	6.7	0.25	340	351B
SMCJ5352	15	75	2.5	75	1	10.8	11.5	6.3	0.25	315	352B
SMCJ5353	16	75	2.5	75	1	11.5	12.2	6	0.3	295	353B
SMCJ5354	17	70	2.5	75	0.5	12.2	12.9	5.8	0.35	280	354B
SMCJ5355	18	65	2.5	75	0.5	13	13.7	5.5	0.4	265	355B
SMCJ5356	19	65	3	75	0.5	13.7	14.4	5.3	0.4	250	356B
SMCJ5357	20	65	3	75	0.5	14.4	15.2	5.1	0.4	237	357B
SMCJ5358	22	50	3.5	75	0.5	15.8	16.7	4.7	0.45	216	358B
SMCJ5359	24	50	3.5	100	0.5	17.3	18.2	4.4	0.55	198	359B
SMCJ5360	25	50	4	110	0.5	18	19	4.3	0.55	190	360B
SMCJ5361	27	50	5	120	0.5	19.4	20.6	4.1	0.6	176	361B
SMCJ5362	28	50	6	130	0.5	20.1	21.2	3.9	0.6	170	362B
SMCJ5363	30	40	8	140	0.5	21.6	22.8	3.7	0.6	158	363B
SMCJ5364	33	40	10	150	0.5	23.8	25.1	3.5	0.6	144	364B
SMCJ5365	36	30	11	160	0.5	25.9	27.4	3.3	0.65	132	365B
SMCJ5366	39	30	14	170	0.5	28.1	29.7	3.1	0.65	122	366B
SMCJ5367	43	30	20	190	0.5	31	32.7	2.8	0.7	110	367B
SMCJ5368	47	25	25	210	0.5	33.8	35.8	2.7	0.8	100	368B
SMCJ5369	51	25	27	230	0.5	36.7	38.8	2.5	0.9	93	369B
SMCJ5370	56	20	35	280	0.5	40.3	42.6	2.3	1	86	370B
SMCJ5371	60	20	40	350	0.5	43	45.5	2.2	1.2	79	371B
SMCJ5372	62	20	42	400	0.5	44.6	47.1	2.1	1.35	76	372B
SMCJ5373	68	20	44	500	0.5	49	51.7	2	1.5	70	373B
SMCJ5374	75	20	45	620	0.5	54	56	1.9	1.6	63	374B
SMCJ5375	82	15	65	720	0.5	59	62.2	1.8	1.8	58	375B
SMCJ5376	87	15	75	760	0.5	63	66	1.7	2	54.5	376B
SMCJ5377	91	15	75	760	0.5	65.5	69.2	1.6	2.2	52.5	377B
SMCJ5378	100	12	90	800	0.5	72	76	1.5	2.5	47.5	378B
SMCJ5379	110	12	125	1000	0.5	79.2	83.6	1.4	2.5	43	379B
SMCJ5380	120	10	170	1150	0.5	86.4	91.2	1.3	2.5	39.5	380B
SMCJ5381	130	10	190	1250	0.5	93.6	98.8	1.2	2.5	36.6	381B
SMCJ5382	140	8	230	1500	0.5	101	106	1.2	2.5	34	382B
SMCJ5383	150	8	330	1500	0.5	108	114	1.1	3	31.6	383B
SMCJ5384	160	8	350	1650	0.5	115	122	1.1	3	29.4	384B
SMCJ5385	170	8	380	1750	0.5	122	129	1	3	28	385B
SMCJ5386	180	5	430	1750	0.5	130	137	1	4	26.4	386B
SMCJ5387	190	5	450	1850	0.5	137	144	0.9	5	25	387B
SMCJ5388	200	5	480	1850	0.5	144	152	0.9	5	23.6	388B

NOTE:

1. TOLERANCE AND VOLTAGE DESIGNATION - The JEDEC type numbers shown indicate a tolerance of $\pm 10\%$ with guaranteed limits on only V_Z , I_R , I_r , and V_F as shown in the electrical characteristics table. Units with guaranteed limits on all seven parameters are indicated by suffix "B" for $\pm 5\%$ tolerance.
2. ZENER VOLTAGE (V_Z) AND IMPEDANCE (Z_{ZT} & Z_{ZK}) - Test conditions for Zener voltage and impedance are as follows; I_Z is applied 40 μs prior to reading. Mounting contacts are located from the inside edge of mounting clips to the body of the diode. ($T_A=25\text{ }^{\circ}\text{C}$).

3. SURGE CURRENT (I_r) - Surge current is specified as the maximum allowable peak, non-recurrent square-wave current with a pulse width, PW, of 8.3 ms. The data given in Figure 5 may be used to find the maximum surge current for a square wave of any pulse width between 1 ms and 1000ms by plotting the applicable points on logarithmic paper. Examples of this, using the 6.8v and 200V zeners, are shown in Figure 6. Mounting contact located as specified in Note 3. ($T_A=25^\circ\text{C}$).
4. VOLTAGE REGULATION (ΔV_z) - Test conditions for voltage regulation are as follows: V_z measurements are made at 10% and then at 50% of the $I_{z\text{max}}$ value listed in the electrical characteristics table. The test currents are the same for the 5% and 10% tolerance devices. The test current time duration for each V_z measurement is 40 μs to 10 ms. ($T_A=25^\circ\text{C}$). Mounting contact located as specified in Note 2.
5. MAXIMUM REGULATOR CURRENT ($I_{z\text{M}}$) - The maximum current shown is based on the maximum voltage of a 5% type unit. Therefore, it applies only to the B-suffix device. The actual $I_{z\text{M}}$ for any device may not exceed the value of 5 watts divided by the actual V_z of the device. $T_L=75^\circ\text{C}$ at maximum from the device body.

APPLICATION NOTE:

Since the actual voltage available from a given zener diode is temperature dependent, it is necessary to determine junction temperature under any set of operating conditions in order to calculate its value. The following procedure is recommended:

Lead Temperature, T_L , should be determined from:

$$T_L = \theta_{LA} P_D + T_A$$

θ_{LA} is the lead-to-ambient thermal resistance ($^\circ\text{C}/\text{W}$)

and P_D is the power dissipation.

Junction Temperature, T_J , may be found from:

$$T_J = T_L + \Delta T_{JL}$$

ΔT_{JL} is the increase in junction temperature above the lead temperature and may be found from Figure 3 for a train of power pulses or from Figure 4 for dc power.

$$\Delta T_{JL} = \theta_{JL} P_D$$

For worst-case design, using expected limits of I_z , limits

of P_D and the extremes of T_J (ΔT_{JL}) may be estimated.

Changes in voltage, V_z , can then be found from:

$$\Delta V_z = \alpha_{Vz} \Delta T_J$$

α_{Vz} , the zener voltage temperature coefficient, is found from Figures 2.

Under high power-pulse operation, the zener voltage will vary with time and may also be affected significantly by the zener resistance. For best regulation, keep current excursions as low as possible.

Data of Figure 3 should not be used to compute surge capability. Surge limitations are given in Figure 5. They are lower than would be expected by considering only junction temperature, as current crowding effects cause temperatures to be extremely high in small spots resulting in device degradation should the limits of Figure 5 be exceeded.

TEMPERATURE COEFFICIENTS

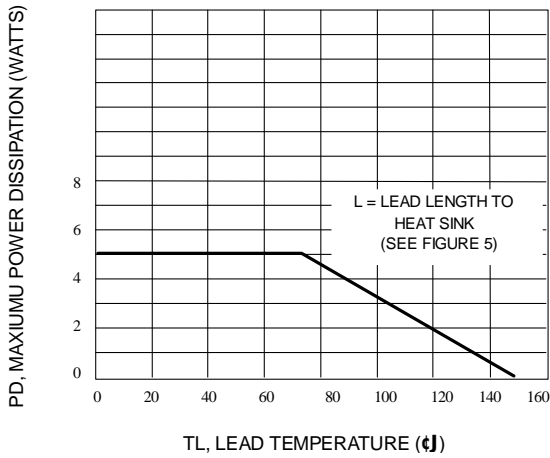


Fig. 1-POWER TEMPERATURE DERATING CURVE

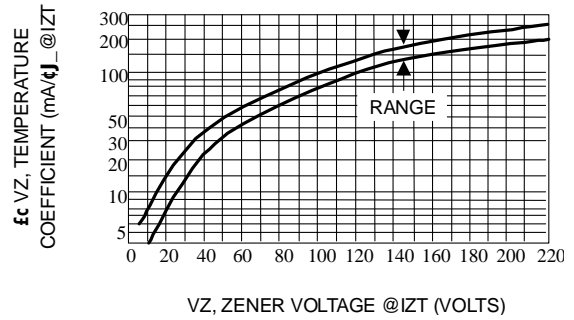


Fig. 2-TEMPERATURE COEFFICIENT-RANGE FOR UNITS 6 TO 220 VOLTS

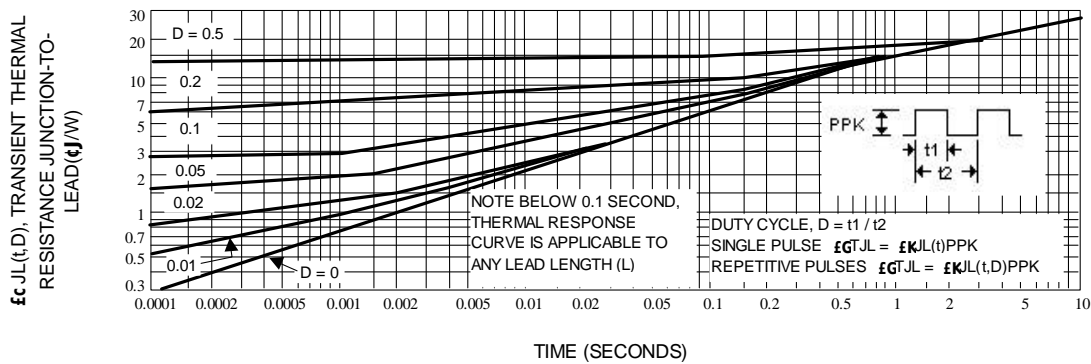


Fig. 3-TYPICAL THERMAL RESPONSE

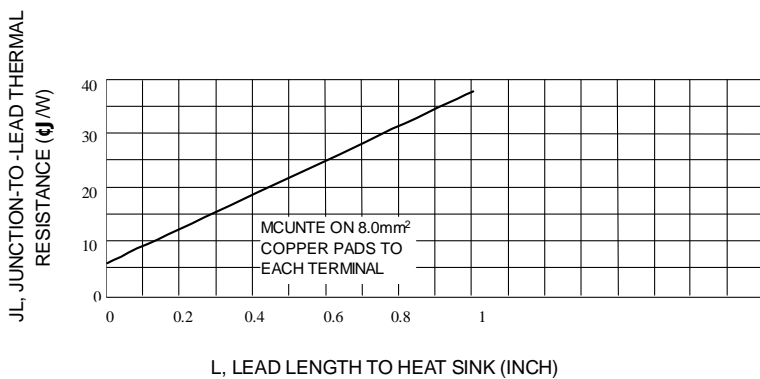


Fig. 4-TYPICAL THERMAL RESISTANCE

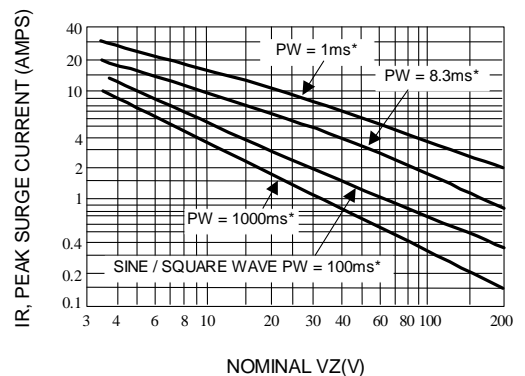


Fig. 5-MAXIMUM NON-REPETITIVE SURGE CURRENT VERSUS NOMINAL ZENER VOLTAGE (SEE NOTE 3)

SMCJ5348 thru SMCJ5388

RATING AND CHARACTERISTICS CURVES



ZENER VOLTAGE VERSUS ZENER CURRENT (FIGURES 7,8, AND 9)

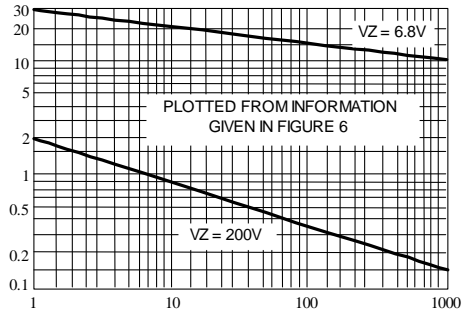


Fig. 6-PEAK SURGE CURRENT VERSUS PULSE WIDTH(SEE NOTE 3)

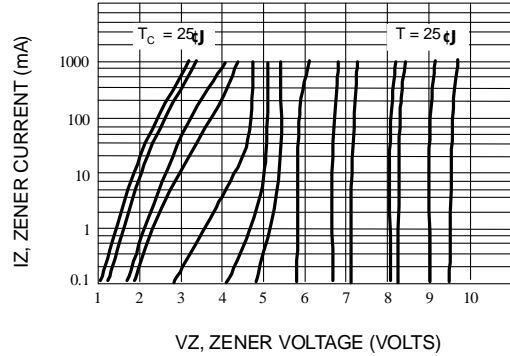


Fig. 7-ZENER VOLTAGE VERSUS ZENER CURRENT
VZ = 6.8 THRU 10 VOLTS

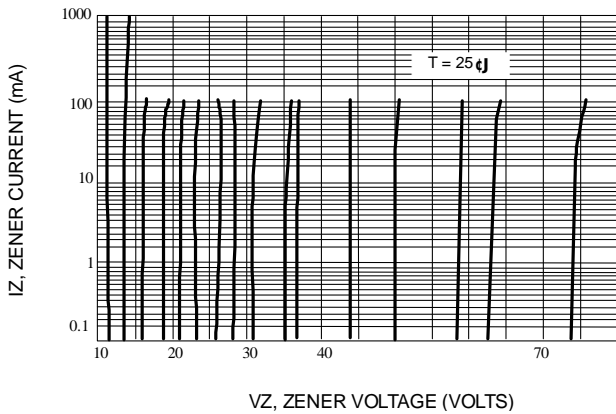


Fig. 8-ZENER VOLTAGE VERSUS ZENER CURRENT
VZ = 11 THRU 75 VOLTS

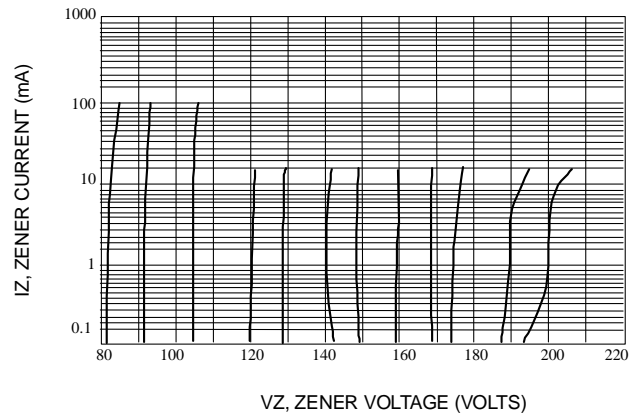


Fig. 9-ZENER VOLTAGE VERSUS ZENER CURRENT
VZ = 82 THRU 200 VOLTS

*** Data of Figure 3 should not be used to compute surge capability. Surge limitations are given in Figure 5. They are lower than would be expected by considering only junction temperature, as current crowding effects cause temperatures to be extremely high in small spots resulting in device degradation should the limits of Figure. 5 be exceeded