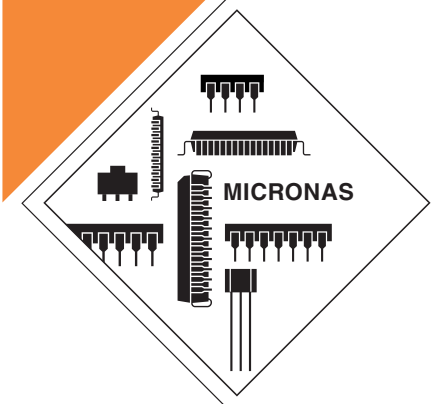

PRELIMINARY DATA SHEET

MAS 3507D
MPEG 1/2 Layer 2/3
Audio Decoder

Edition March 16, 2000
6251-459-3PD

MICRONAS

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MPEG 1/2 Layer 2/3 Audio Decoder

Release Note: Revision bars indicate significant changes to the previous edition.
This data sheet applies to MAS 3507D version G10 and following versions.

1. Introduction

The MAS 3507D is a single-chip MPEG layer 2/3 audio decoder for use in audio broadcast or memory-based playback applications. Due to embedded memories, the embedded DC/DC up-converter, and the very low power consumption, the MAS 3507D is ideally suited for portable electronics.

In MPEG 1 (ISO 11172-3), three hierarchical layers of compression have been standardized. The most sophisticated and complex, layer 3, allows compression rates of approximately 12:1 for mono and stereo signals while still maintaining CD audio quality. Layer 2 (widely used in DVB, ADR, and DAB) achieves a compression of 8:1 providing CD quality.

In order to achieve better audio quality at low bit rates (<64 kbit/s per audio channel), three additional sampling frequencies are provided by MPEG 2 (ISO 13818-3). The MAS 3507D decodes both layer 2 and layer 3 bit streams as defined in MPEG 1 and 2. The multichannel/multilingual capabilities defined by MPEG 2 are not supported by the MAS 3507D. An extension to the MPEG 2 layer 3 standard developed by FhG Erlangen, Germany sometimes referenced as MPEG 2.5, for extremely low bit rates at sampling frequencies of 12, 11.025, or 8 kHz is also supported by the MAS 3507D.

1.1. Features

- Serial asynchronous MPEG bit stream input (SDI)
- Parallel (PIO-DMA) Input
- Broadcast and multimedia operation mode
- Automatic locking to given data rate in broadcast mode
- Data request triggered by 'demand signal' in multimedia mode
- Output audio data delivered (in various formats) via an I^2S bus (SDO)
- Digital volume / stereo channel mixer / Bass / Treble
- Output sampling clocks are generated and controlled internally.
- Ancillary data provided via I^2C interface
- Status information accessible via PIO pins or I^2C
- "CRC Error" and "MPEG Frame Synchronization" Indicators at Pins in serial input mode
- Power management for reduced power consumption at lower sampling frequencies
- Low power dissipation (30 mW @ $f_s \leq 12$ kHz, 46 mW @ $f_s \leq 24$ kHz, 86 mW @ $f_s > 24$ kHz @ 2.7 V)
- Supply voltage range: 1.0 V to 3.6 V due to built-in DC/DC converter (1-cell/2-cell battery operation)
- Adjustable power supply supervision
- Power-off function
- Additional functionality achievable via download software (CELP voice Decoder, ADPCM encoder / decoder)

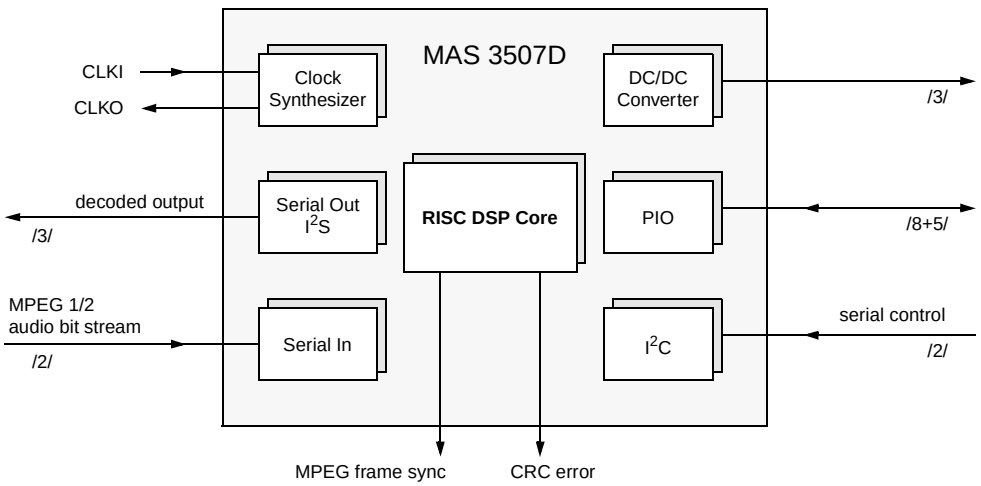


Fig. 1–1: MAS 3507D block diagram

1.2. Application Overview

The MAS 3507D can be applied in two major environments: in multimedia mode or in broadcast mode. For both modes, the DAC 3550A fits perfectly to the requirements of the MAS 3507D. It is a high-quality multi sample rate DAC (8 kHz ... 50 kHz) with internal crystal oscillator, which is only needed for generating the decoder clock, and integrated stereo headphone amplifier plus 2 stereo inputs.

1.2.1. Multimedia Mode

In a memory-based multimedia environment, the easiest way to incorporate a MAS 3507D decoder is to use its data-demand pin. This pin can be used directly to request input bit stream data from the host or memory system.

While the demand pin is active, the data stream shall be transmitted to the MAS 3507D. The bit stream clock should be higher than the actual data rate of the MPEG bit stream (1 MHz bit stream clock works with all MPEG bit rates). The demand signal will be active until the input buffer of the MAS 3507D is filled.

A delayed response of the host to the demand signal (by several milliseconds) or an interrupted response of the host will be tolerated by the MAS 3507D as long as the input buffer does not run empty. A PC might use its DMA capabilities to transfer the data in the background to the MAS 3507D without interfering with its foreground processes.

The source of the bit stream may be a memory (e.g. ROM, Flash) or PC peripherals, such as CD-ROM drive, an ISDN card, a hard disk or a floppy disk drive.

1.2.2. Broadcast Mode

In environments where the bit stream is delivered from an independent transmitter to one or more receivers, the MAS 3507D cannot act as master for the bit stream clock. In this mode, it synchronizes itself to the incoming bit stream data rate by a digital PLL and generates a synchronized digital audio sample clock for the required output sample rates.

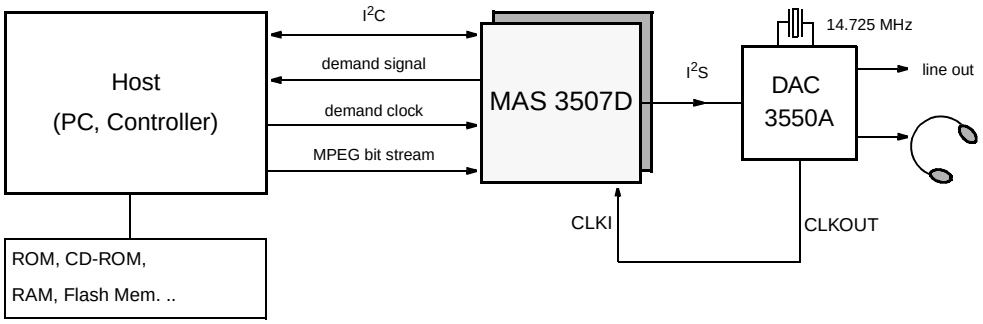


Fig. 1–2: Block diagram of a MAS 3507D, decoding a stored bit stream in multimedia mode

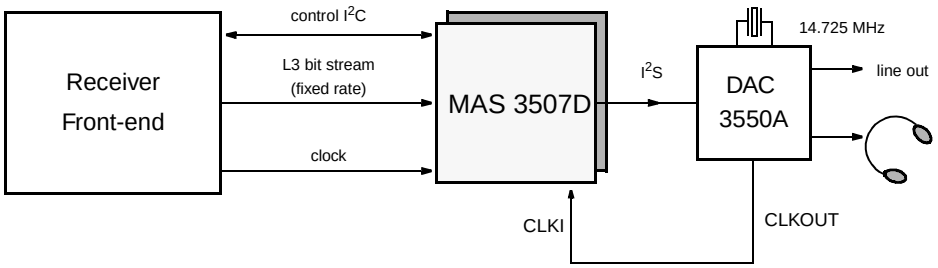


Fig. 1–3: Block diagram of a MAS 3507D in a broadcast environment

2. Functional Description of the MAS 3507D

2.1. DSP Core

The hardware of the MAS 3507D consists of a high performance RISC Digital Signal Processor (DSP) and appropriate interfaces (see Fig. 2–1). The internal processor works with a memory word length of 20 bits and an extended range of 32 bits in its accumulators. The instruction set of the DSP is highly optimized for audio data compression and decompression. Thus, only very small areas of internal RAM and ROM are required. All data input and output actions are based on a ‘non cycle stealing’ background DMA that does not cause any computational overhead.

2.2. Firmware (Internal Program ROM)

A valid MPEG 1/2/2.5 layer 2/3 data signal is taken as input. The signal lines are a clock line SIC and the data line SID. The MPEG decoder performs the audio decoding. The steps for decoding are

– synchronization,

– side information extraction,

– audio data decoding,

– ancillary data extraction, and

– volume and tone control.

For the supported bit rates and sample rates, see Table 3–12 on page 32. Frame synchronization and CRC-error signals are provided at the output pins of the MAS 3507D in serial input mode.

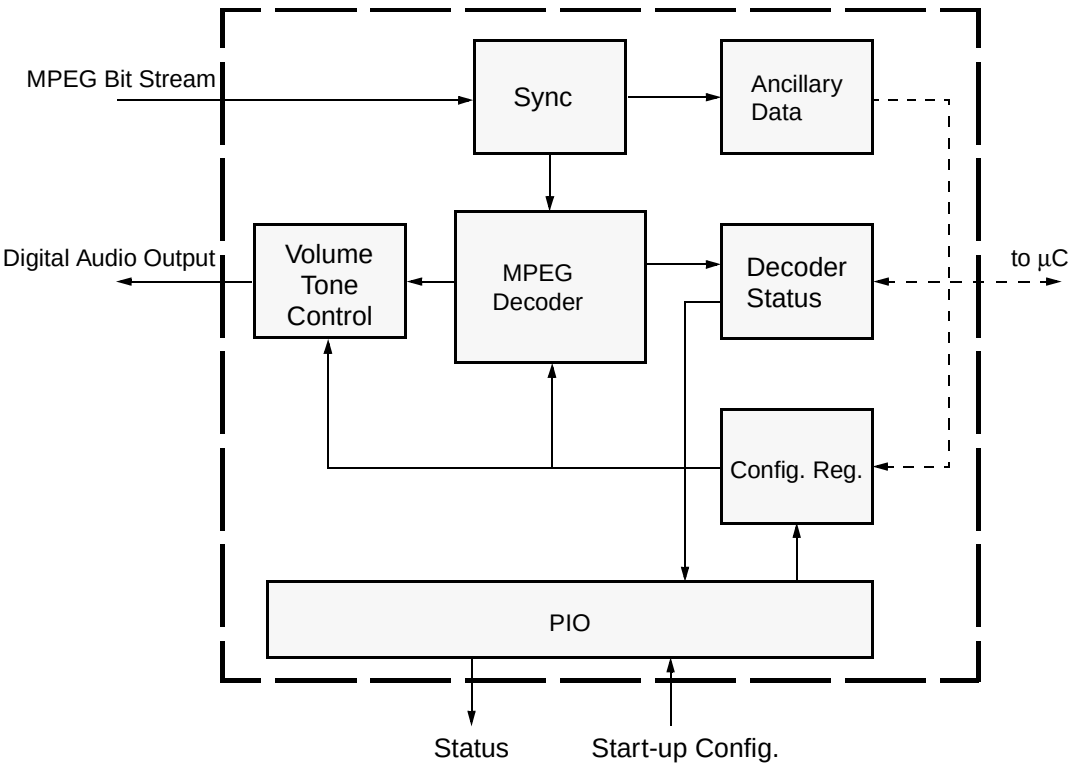


Fig. 2–1: Block diagram of the MPEG Decoder in serial input mode

2.3. Program Download Feature

This is an additional feature that is not required for the MPEG decoding function.

The overall function of the MAS 3507D can be altered by downloading up to 1 kWord program code into the internal RAM and executing this code instead of the ROM code. During this time, MPEG decoding is not possible.

The code must be downloaded by the ‘write to memory’ command (see Section 3.3.) into an area of RAM that is switchable from data memory to program memory. A ‘run’ command (see Section 3.3.1.) starts the operation.

Micronas provides modules for voice-decoding using the CELP algorithm (performing good speech quality at very low bit rates) and for encoding and decoding audio data with ADPCM.

Detailed information about downloading is provided in combination with the MAS 3507D software development package from Micronas.

For commercial issues and detailed information please contact our sales department.

2.4. Baseband Processing

2.4.1. Volume Control / Channel Mixer

A digital volume control matrix is applied to the digital stereo audio data. This performs additional balance control and a simple kind of stereo basewidth enhancement. The 4 factors LL, LR, RL, and RR are adjustable via the controller with 20-bit resolution. See Fig. 3–2 and Section 3.7.3. for details.

2.4.2. Mute / Bypass Tone Control

A special bit enables a fast and simple mute functionality without changing the current volume setting. Another bit allows to bypass the complete bass / treble / volume control. See for details Section 3.6.2.

2.4.3. Bass / Treble Control

Tone control is implemented in the MAS 3507D. It allows the control of bass and treble in a range up to ±15 dB, as Table 3–9 shows. To prevent overflow or clipping effects, the prescaler is built-in. The prescaler decreases the overall gain of the tone filter, so the full range up to +15 dB is usable without clipping.

Due to the different frequency ranges in MPEG 1, MPEG 2, or MPEG 2.5, the bass cutoff frequencies differ.

Table 2–1: Cutoff Frequencies

Cutoff	Bass	Treble
MPEG 1	100 Hz	10 kHz
MPEG 2	200 Hz	10 kHz
MPEG 2.5	400 Hz	10 kHz

For details see Section 3.6.3..

2.5. Clock Management

The MAS 3507D should be driven by a single clock at a frequency of 14.725 MHz. It is possible to drive the MAS 3507D with other reference clocks (see Section 3.7.2.1. on page 36).

The CLKI signal acts as a reference for the embedded clock synthesizer that generates the internal system clock. Based on the reference input clock CLKI, a synchronized output clock CLKO that depends on the audio sample frequency of the decompressed bit stream is generated and provided as 'master clock' to external D/A converters. Some of them need master clocks that have a fixed relation to the sampling frequencies. A scaler can be switched on during start-up, optionally, by setting the PI8 pin to 0. Then, the clock-out will automatically be divided by 1, 2, or 4 as defined in Table 2–2.

Table 2–2: CLKO Frequencies

f_S/kHz	CLKO/MHz scaler on	CLKO/MHz scaler off
48, 32	24.576	24.576
44.1	22.5792	22.5792
24, 16	12.288	24.576
22.05	11.2896	22.5792
12, 8	6.144	24.576
11.025	5.6448	22.5792

2.6. Power Supply Concept

The MAS 3507D offers an embedded controlled DC/DC converter for battery based power supply concepts. It works as an up-converter.

2.6.1. Internal Voltage Monitor

An internal voltage monitor compares the input voltage at the VSENS pin with an internal reference value that is adjustable via I^2C bus. The PUP output pin becomes inactive when the voltage at the VSENS pin drops below the programmed value of the reference voltage.

It is important that the WSEN must not be activated before the PUP is generated. The PUP signal thresholds are listed in Table 3–8. The internal voltage monitor will be activated with a high level at Pin DCEN.

2.6.2. DC/DC Converter

The DC/DC converter of the MAS 3507D is used to generate a fixed power supply voltage even if the chip set is powered by battery cells in portable applications. The DC/DC converter is designed for the application of 1 or 2 batteries or NiCd cells as shown in Fig. 2–3 which shows the standard application circuit. The DC/DC converter is switched on by activating the DCEN pin. Its output power is sufficient for other ICs as well.

Note: Connecting DCEN directly to VDD leads to unexpected states of the DCCF register.

The PUP signal should be read out by the system controller.

A 22 µH inductor is required for the application. The important specification item is the inductor saturation current rating, which should be greater than 2.5 times the DC load current. The DC resistance of the inductor is important for efficiency. The primary criterion for selecting the output filter capacitor is low equivalent series resistance (ESR), as the product of the inductor current variation and the ESR determines the high-frequency amplitude seen on the output voltage. The Schottky diode should have a low voltage drop V_D for a high overall efficiency of the DC/DC converter. The current rating of the diode should also be greater than 2.5 times the DC output current. The VSENS pin has to be always connected to the output voltage.

2.6.3. Stand-by Functions

The digital part of the MAS 3507D and the DC/DC converter are turned on by setting WSEN. If only the DC/DC converter should work, it can remain active by setting DCEN alone to supply other parts of the application even if the audio decoding part of the MAS 3507D is not being used. The WSEN power-up pin of the digital part may be handled by the controller.

Please pay attention to the fact, that I^2C protocol is working only if the processor and its interfaces works (WSEN = 1)

2.6.4. Start-up Sequence

The DC/DC converter starts from a minimum input voltage of 0.9 V. There should be no output load during startup. In case WSEN is active, the MAS 3507D is in the DSP operation mode. The start-up script should be as follows:

1. Enable the DC/DC-converter with a high signal (VDD, AVDD) at pin DCEN.
2. Wait until PUP goes “high”.
3. Wait one more millisecond to guarantee that the output voltage has settled (recommended).
4. Enable the MAS 3507D with a “high” signal at pin “WSEN”.

Please also refer to Figure 2–2.

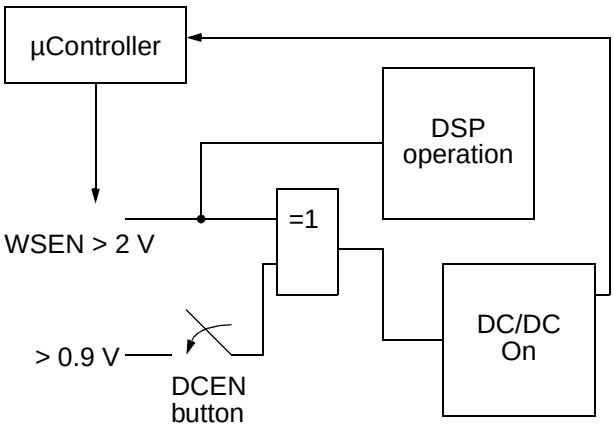


Fig. 2–2: DC/DC operation

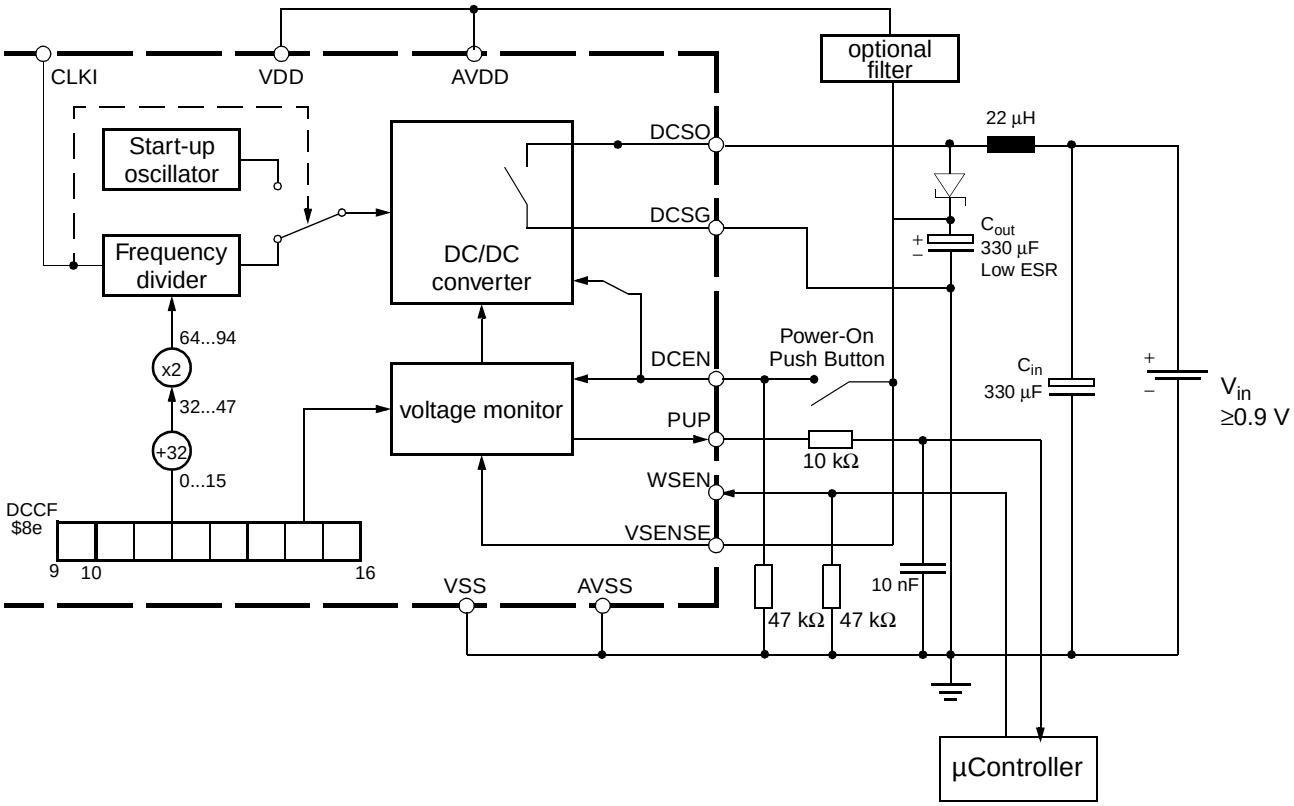


Fig. 2–3: DC/DC converter connections

2.7. Interfaces

The MAS 3507D uses an I^2C control interface, 2 selectable serial input interfaces for MPEG bit stream (SDI, SDI*) , a parallel I/O interface (PIO) for MPEG- or ADPCM-data and a digital audio output interface (SDO) for the decoded audio data (I^2S or similar). Additionally, the parallel I/O interface (PIO) may be used for monitoring and mode selection tasks. The PIO lines are defined by the internal firmware.

2.7.1. MPEG Bit Stream Interface (SDI)

The MPEG bit stream input interface uses the three pins: SIC, *SII*, and SID. For MPEG decoding operation, the SII pin must always be connected to VSS.

The serial interface has to be initialized before the first use. Otherwise no output signal is produced. After Power-up or a rising slope on Pin PORQ, write the following I^2C-command, while SIC is hold low:

W $3A 68 93 B0 00 02
(write $0020 into register $3B)

W $3A 68 00 01
(execute “RUN 1” command)

The MPEG input signal format is shown in Fig. 2–4. The data values are latched with the falling edge of the SIC signal.

The MPEG bit stream generated by an encoder is unformatted. It will be formatted (e.g. 8 bit or 16 bit) by storing on a media (Flash-RAM, Harddisk). The serial data required from the MPEG bit stream interface must be in the same bit order as produced by the encoder.

2.7.2. SDI* Selection

An alternative serial input (SDI*) is available. The alternative serial input can be selected by setting register SI1M0 at address $4f (see Table 2–3).

Table 2–3: SDI* Selection via Register SI1M0, $4f (write)

Value	Function
0	use SDI lines
2	use PI14...PI16 pins for serial input (named SDI*)

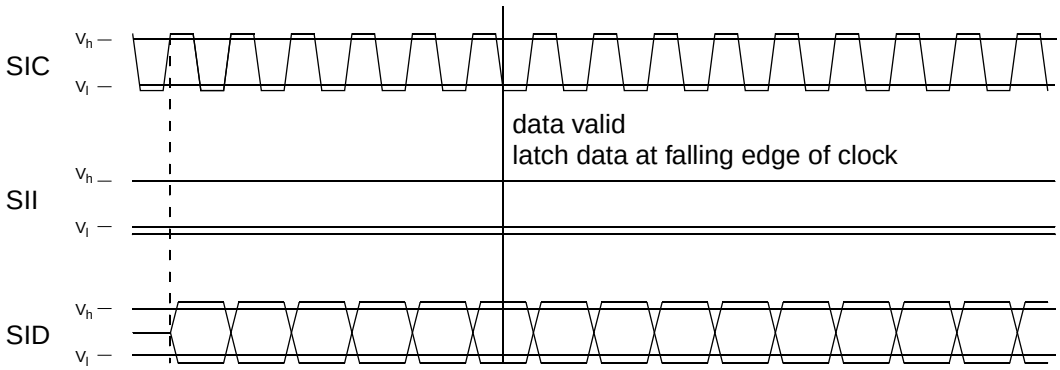


Fig. 2–4: Schematic timing of the SDI (MPEG) input

2.7.3. Parallel Input Output Interface (PIO)

The parallel interface of the MAS 3507D uses the lines PI0...PI4, PI8, PI12...PI19, and several control lines.

2.7.3.1. PIO-DMA Input Mode

By setting the PIO pin PI4 to “1”, the PIO-DMA input mode of the MAS 3507D is activated after reset.

Normally, the input mode should not be altered in a customer’s application. Should this nonetheless be desired, the necessary changes are described in Table 2–4 and Table 2–5.

2.7.3.2. Writing MPEG Data to the PIO-DMA

The PIO-DMA mode enables the writing of 8-bit parallel MPEG data to the MAS 3507D. In this mode, PIO lines PI19...PI12 are switched to the MAS 3507D data input which hence will be an 8-bit parallel input port with MSB first (at position PI19) for the MPEG bit stream data. In order to write data to this parallel port successfully, a special handshake protocol has to be used by the controller (see Fig. 2–5).

Note: Either SII has to be set to “1”, or SIC clock input has to be stopped (“0”) in this mode.

Table 2–4: Switching from SDI- to PIO-DMA-Input

Address [1)]	Value
$e6, Bit 4	1
[1)] Startup Configuration Register	

Table 2–5: Switching from PIO-DMA- to SDI-Input

Step	Address [1)]	Value
1	$e6, Bit 4	0
2	$4b	$82
[1)] PIO Configuration Register **Note: These 2 steps must be done in above order!**		

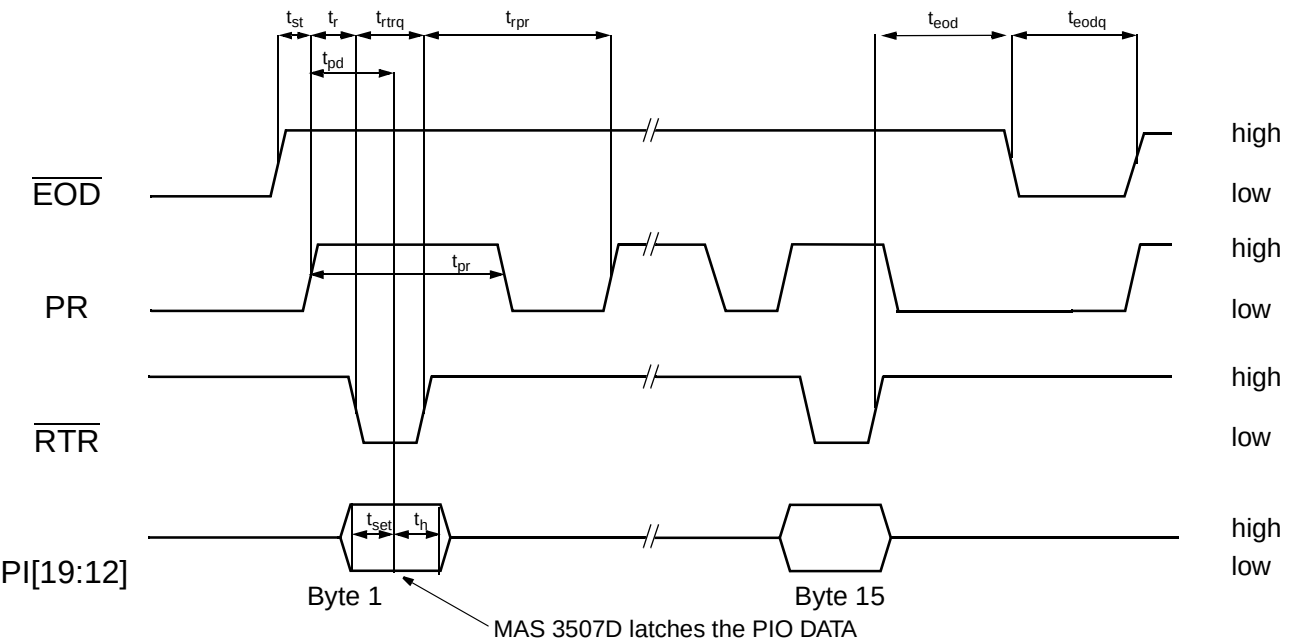


Fig. 2–5: Handshake protocol for writing MPEG data to the PIO-DMA

2.7.3.3. DMA Handshake Protocol

The data transfer can be started after the **$\overline{\text{EOD}}$** pin of the MAS 3507D is set to “high”. After verifying this, the controller signalizes the sending of data by activating the **PR** line. The MAS 3507D responds by setting the **$\overline{\text{RTR}}$** line to the “low” level. The MAS 3507D reads the data **PI[19:12]** t_{pd} ns after rising edge of the **PR**. The next data word write operation will again be initialized by setting the **PR** line via the controller. Please refer to Figure 2–5 and Table 2–6 for the exact timing

2.7.3.4. End of DMA Transfer

The above procedure will be repeated until the MAS 3507D sets the **$\overline{\text{EOD}}$** signal to “0”, which indicates that the transfer of one data block has been executed. Subsequently, the controller should set **PR** to “0”, wait until **$\overline{\text{EOD}}$** rises again, and then repeat the procedure (see Section 2.7.3.3.) to send the next block of data. The DMA buffer is 15 bytes long.

The recommended PIO-DMA conditions and the characteristics of the PIO timing are given in Table 2–6

2.7.4. Audio Output Interface (SDO)

The audio output interface of the MAS 3507D is a standard I^2S interface. It is possible to choose between two standard interfaces (16 bit with delay or 32 bit without delay and inverted SOI) via start-up configuration. These setup modes meet the performance of the most common DACs. It is also possible to select other interface modes via I^2C commands (see Section 2.7.4.3.).

Table 2–6: PIO DMA Timing

Symbol	PIO Pin	Min.	Max.	Unit
t_{st}	PR, $\overline{\text{EOD}}$	0.010	2000	µs
t_r	PR, $\overline{\text{RTR}}$	40	160	ns
t_{pd}	PR, PI[19:12]	120	480	ns
t_{set}	PI[19:12]	160	no limit	ns
t_h	PI[19:12]	160	no limit	ns
t_{rtrq}	$\overline{\text{RTR}}$	200	30000	ns
t_{pr}	PR	120	no limit	ns
t_{rpr}	PR, $\overline{\text{RTR}}$	40	no limit	ns
t_{eod}	PR, $\overline{\text{EOD}}$	40	160	ns
t_{eodq}	$\overline{\text{EOD}}$	0	500	µs

2.7.4.1. Mode 1: 16 Bits/Sample (I^2S Compatible Data Format)

A schematic timing diagram of the SDO interface in 16 bit/sample mode is shown in Fig. 2–6.

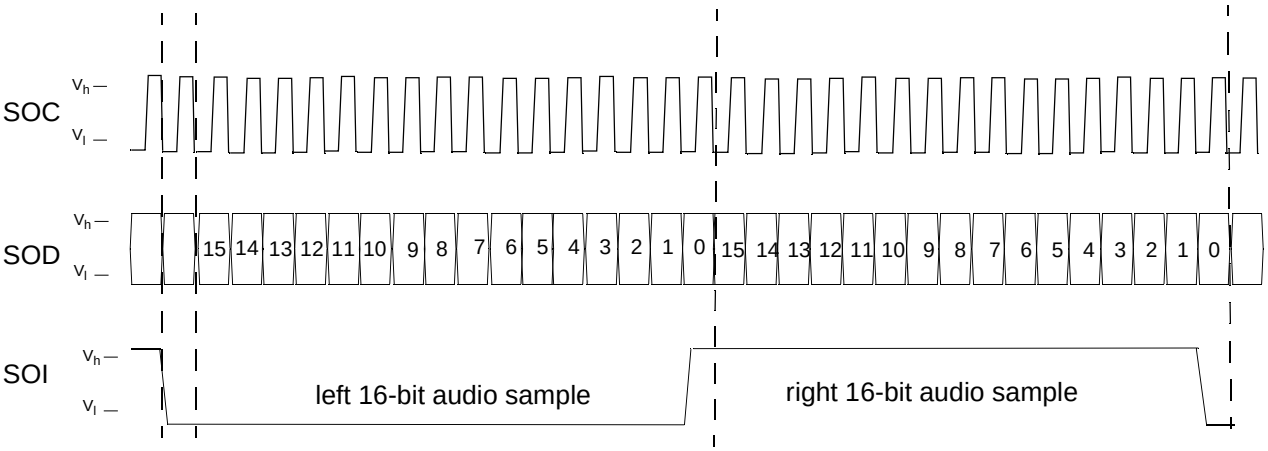


Fig. 2–6: Schematic timing of the SDO interface in 16 bit/sample mode

2.7.4.2. Mode 2:32 Bit/Sample (Inverted SOI)

If the serial output generates 32 bits per audio sample, only the first 20 bits will carry valid audio data. The 12 trailing bits are set to zero by default (see Fig. 2–7)

The 12 trailing bits for left and right channel of the SDO interface can be accessed by writing to registers as shown in Table 2–7.

Table 2–7: Access for Trailing Bits

Register	Bit 0 ... 11
$c5	Left Channel
$c6	Right Channel

2.7.4.3. Other Output Modes

The interface is also configurable by software to work in different modes. It is possible to choose:

- 16 or 32 bit/sample modes,
- inverted or noninverted word strobe (SOI),
- no delay or delay of data related to word strobe
- inverted or noninverted I^2S-Clock (SOC).

For further details see Section 3.7.2.2.

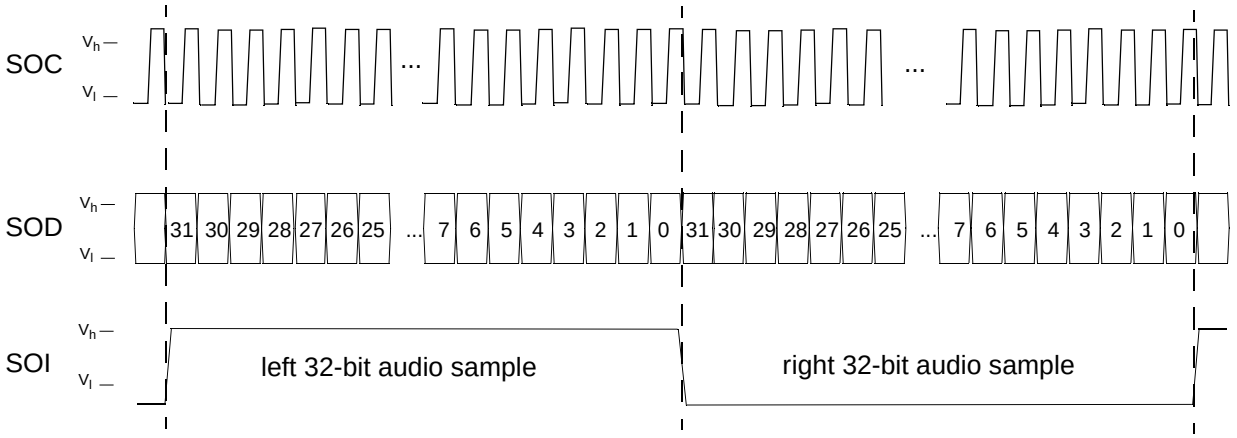


Fig. 2–7: Schematic timing of the SDO interface in 32 bit/sample mode

2.8. Start-up Configuration

Basic operation of the MAS 3507D is possible without controller interaction. Configuration and the most important status information are available by the PIO interface. The start-up configuration is selected according to the levels of several PIO pins. The levels should be set via high impedance resistors (for example 10 kΩ) to VSS or VDD and will be copied into the StartupConfig register directly after power up / reset. After start-up, the PIO will be reconfigured as output.

To enable greater flexibility, it is possible to configure the MAS 3507D without using the PIO pins or to reconfigure the IC after start-up. The procedure for this is to send two I^2C commands to the MAS 3507D:

– Writing the StartupConfig register (see Section 3.6. on page 26)

– Execute a ‘run $0fcd’ command (see Section 3.3.1.).

The configuration will be active up to a reset. Then, the new configuration will be loaded again via PIO.

2.8.1. Parallel Input Output Interface (PIO)

During start-up, the PIO will read the start-up configuration. This is to define the environment for the MAS 3507D. The following pins must be connected via resistors to VSS or VDD:

Table 2–8: Start-up configuration[1)]

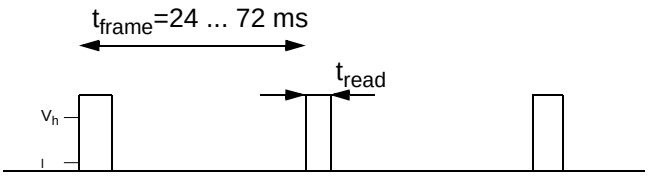
PIO Pin	“0”	“1”
PI8	divide CLKO by 1, 2, or 4 (according to MPEG 1, 2, or 2.5)	CLKO fixed at 24.576 or 22.5792 MHz
PI4	SDI input mode	PIO-DMA input mode
PI3	Enable layer 3	Disable layer 3
PI2	Enable layer 2	Disable layer 2
PI1	SDO output: 32 bit	SDO output: 16 bit
PI0	input: Multimedia mode (PLL off)	input: Broadcast mode (PLL on)

1) Start-up setting can be changed by I^2C commands after reset.

2.9. Status Pins in SDI Input Mode

After having read the start-up configuration, the PIO will be switched to 'µP-mode'. In µP-mode, the additional PIO control lines (PR, $\overline{PCS}$) are evaluated. If the MPEG decoder firmware detects PR = '1' and the $\overline{PCS}$ = '0'. Then, all PIO interface lines are configured as output and display some status information of the MPEG decoder. The PIO lines can be read by an external controller or directly used by dedicated hardware blocks (e.g. for sample rate indication or display units). The internal MPEG decoder firmware attaches specific functions to the following pins.

The MPEG-FRAME-SYNC signal is set to '1' after the internal decoding for the MPEG header has been finished for one frame. The rising edge of this signal could be used as an interrupt input for the controller that triggers the read out of the control information and ancillary data. As soon as the MAS 3507D has recognized the corresponding read command ('read control interface data' (see Section 3.3.2. on page 21), the MPEG-FRAME-SYNC is reset. This behavior reduces the possibility of missing the MPEG-FRAME-SYNC active state.



MPEG-FRAME-SYNC

Fig. 2–8: Schematic timing of MPEG-FRAME-Sync

The time t_{read} depends on the response time of the controller. This time must not exceed 1/2 of the MPEG-frame length t_{frame}. The MPEG frame lengths are given in Table 2–10

Table 2–9: PIO output signals during MPEG decoding in SDI mode

PIO Pin	Name	Comment
PI19	Demand PIN %0 %1	 no input data exp. input data request
PI18, PI17	MPEG INDEX %00 %01 %10 %11	 MPEG 2.5 reserved MPEG 2 MPEG 1
PI13, PI12	MPEG Layer ID %00 %01 %10 %11	 reserved Layer 3 Layer 2 Layer 1[1)]
PI8	MPEG CRC-ERROR %0 %1	 no error CRC-error, MPEG decoding not successful
PI4	MPEG-FRAME-SYNC	see following text
PI3, PI2	Sampling frequency %00 %01 %10 %11	in kHz[2)] 44.1 / 22.1 / 11.0 48 / 24 / 12 32 / 16 / 8 reserved
PI1, PI0	Deemphasis %00 %01 %10 %11	 none 50/15 µs reserved CCITT J.17

1) Layer 1 bit streams will not be decoded
2) Sampling frequency also defined by MPEG index (see Table 3–12 for additional information)

.

Table 2–10: Frame length in MPEG layer 2 / 3

f_S in kHz	Frame Length Layer 2	Frame Length Layer 3
48	24 ms	24 ms
44.1	26.12 ms	26.12 ms
32	36 ms	36 ms
24	24 ms	24 ms
22.05	26.12 ms	26.12 ms
16	32 ms	32 ms
12	not available	48 ms
11.025	not available	52.24 ms
8	not available	72 ms

3. Control Interfaces

3.1. I²C Bus Interface

3.1.1. Device and Subaddresses

The MAS 3507D is controlled via the I²C bus slave interface.

The IC is selected by transmitting the MAS 3507D device addresses. (see Table 3–1).

Writing is done by sending the device write address, ($3a) followed by the subaddress byte ($68), two or more bytes of data. Reading is done by sending the write device address ($3a), followed by the subaddress byte ($69). Without sending a stop condition, reading of the addressed data is completed by sending the device read address ($3b) and reading n-bytes of data.

By means of the RESET bit in the CONTROL register, the MAS 3507D can be reset by the controller.

Due to the internal architecture of the MAS 3507D, the IC cannot react immediately to an I²C request. The typical response time is about 0.5 ms. If the MAS 3507D cannot accept another complete byte of data until it has performed some other function (for example, decoding MP3 data), it will hold the clock line I2C_CL LOW to force the transmitter into a wait state. The positions within a transmission where this may happen are indicated by 'Wait' in section 3.4. The maximum wait period of the MAS 3507D during normal operation mode is less than 4 ms.

Table 3–1: I²C Bus Device Addresses

MAS 3507D Device Address	Write	Read
MAS_I2C_ADR	$3a	$3b

Table 3–2: I²C Bus Subaddresses

Name	Binary Value	Hex Value	Mode	Function
CONTROL_MAS	0000 0000	$6a	Write	control subaddress (see Table 3–3)
WR_MAS	0110 1000	$68	Write	write subaddress
RD_MAS	0110 1001	$69	Write	read subaddress

Table 3–3: Control Register (Subaddress: $6a)

Name	Subaddress	Bit : 8	Bit : 0-7, 9-15
CONTROL	$6a	1 : Reset 0 : normal	0

Note: S = I^2C-Bus Start Condition from master
P = I^2C-Bus Stop Condition from master
ACK = Acknowledge-Bit: LOW on I2C_DA from slave or master
NAK = Not Acknowledge-Bit: HIGH on I2C_DA from master to indicate ‘End of Read’

Wait = I^2C-Clock line is held low, while the MAS 3507D is processing the I^2C command.

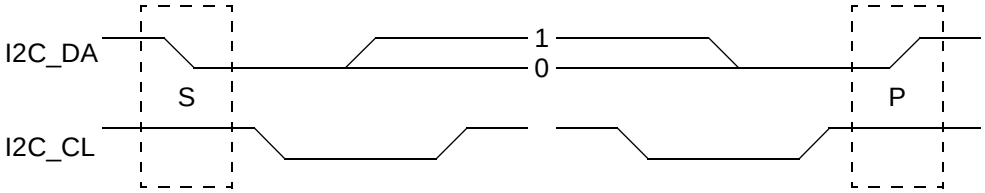


Fig. 3–1: I^2C bus protocol (MSB first; data must be stable while clock is high)

3.2. Command Structure

The I^2C control of the MAS 3507D is done completely via the I^2C data register by using a special command syntax. The commands are executed by the MAS 3507D during its normal operation without any loss or interruption of the incoming data or outgoing audio data stream. These I^2C commands allow the controller to access internal states, RAM contents, internal hardware control registers, and even a download of an alternative software module. The command structure allows sophisticated control of the MAS 3507D. The registers of the MAS 3507D are either general purpose, e.g. for program flow control, or specialized registers that directly affect hardware blocks. The unrestricted access to these registers allows the system controller to overrule the firmware configuration of the serial interfaces or the default input line selection.

The control interface is also used for low bit rate data transmission, e.g. MPEG-embedded ancillary data transmission. The data information is performed by sending a ‘read memory’ command to the MAS 3507D and by reading the memory block that temporarily contains the required information. The synchronization between the controller and the MAS 3507D is done via a MPEG-FRAME-SYNC signal or by monitoring the MPEGFrameCount register (at the cost of a higher work load for the controller).

The MAS 3507D firmware scans the I^2C interface periodically and checks for pending or new commands. However, due to some time critical firmware parts, a certain latency time for the response has to be expected. The theoretical worst case response time does not exceed 4 ms. Table 3–4 shows the basic controller commands that are available by the MAS 3507D.

3.2.1. The Internal Fixed Point Number Format

Internal register or memory values can easily be accessed via the I^2C interface. In this document, two number representations are used: the fixed point notation ‘v’ and the 2’s complement number notation ‘r’.

The conversion between the two forms of notation is easily done (see the following equations).

$r = v \times 524288.0 + 0.5; (-1.0 \leq v < 1.0)$ (EQ 1)

$v = r / 524288.0; (-524288 < r < 524287)$ (EQ 2)

3.2.2. Conventions for the Command Description

The description of the various controller commands uses the following formalism:

– A data value is split into 4-bit nibbles which are numbered beginning with 0 for the least significant nibble.

– Data values in nibbles are always shown in hexadecimal notation indicated by a preceding $.

– A hexadecimal 20-bit number d is written, e.g. as d = $17C63, its five nibbles are d0 = $3, d1 = $6, d2 = $C, d3 = $7, and d4 = $1.

– **Abbreviations** used in the following descriptions:
  a address
  d data value
  n count value
  o offset value
  r register number
  x don't care

– **Variables** used in the following descriptions:
  dev_write $3a
  dev_read $3b
  data_write $68
  data_read $69
  control $6a

3.3. Detailed MAS 3507D Command Syntax

3.3.1. Run

S	dev_write	A	data_write	A	a3,a2	A	a1,a0	A	P

The 'run' command causes the start of a program part at address **a** = (a3,a2,a1,a0). The nibble a3 is restricted to **$0** or **$1** which also acts as command selector. Run with address **a = $0** will suspend normal MPEG decoding and only I^2C commands are evaluated. This freezing will be required if alternative software is downloaded into the internal RAM of the MAS 3507D. Detailed information about downloading is provided in combination with a MAS 3507D software development package or together with MAS 3507D software modules available from Micronas.

If the address $1400 ≤ **a** < $1800, the MAS 3507D continues execution of the program with the downloaded code. For detailed information, please refer to the MASC software development kit. This is for starting the downloaded program code.

Example 1: 'run' at address $fcd (override start-up configuration) has the following I^2C protocol:

```
<$3a><$68><$0f><$cd>
```

Example 2: 'run' at address $475 (activate PLLOffset and OutputConfig after change by write command) has the following I^2C protocol:

```
<$3a><$68><$04><$75>
```

Table 3–4: Basic controller commands

Code	Command	Comment
$0 $1	run	Start execution of an internal program. (Run 0 means freeze operating system.)
$3	read Control Information and Ancillary Data	fast read of a block of information organized in 16-bit words (see Section 3.7.1. on page 30)
$9	write register	An internal register of the MAS 3507D can be written directly to by the controller.
$A $B	write to memory	A block of the DSP memory can be written to by the controller. This feature may be used to download alternate programs.
$D	read register	The controller can read an internal register of the MAS 3507D.
$E $F	read memory	A block of the DSP memory can be read by the controller.

3.3.2. Read Control Interface Data

1) send command

S	dev_write	A	data_write	A	S	**$3**, x2	A	x1,x0	A	P

2) get ancillary data values

S	dev_write	A	data_read	A	S	dev_read				
			(ancillary word 0)		A	d3, d2	A	d1,d0		
					....repeat for n data values....					
					A	d3, d2	A	d1,d0	Nak	P

x2...x0: combined count, offset value
d3...d0: 16-bit data values

An internal memory array keeps the status information of the MAS 3507D (see Table 3–10). The ‘read control interface data’ command can be used for quick access to this memory array. A successive range of memory locations may be read by passing a 6-bit offset value “o” and a 6-bit count value “n” as parameter.

Both values are combined in a 12-bit = 4 nibble field x2, x1, x0. If, for example, 4 words (n = 4) starting with one word offset (o = 2), i.e. the MPEG Status 2, the CRCErrorCount, and NumberOfAncillaryBits are read from the control memory array, the 3 nibbles x2, x1 and x0 are evaluated as shown in the following table.

	11	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
6-bit values	offset: 2						number of words: 3					
bit	0	0	0	0	1	0	0	0	0	0	1	1
nibble	0				8				3			

The complete I²C protocol reads as:

```
<$3a><$68><$30><$83>
<$3a><$69><$3b><receive 3 16-bit data values>
```

The ‘read control interface data’ command resets the MPEG-FRAME-SYNC at PI4 pin (see Section 2.9. on page 16).

3.3.3. Write Register

S	dev_write	A	data_write	A	**$9**, r1	A	r0, d0	A	
					d4, d3	A	d2, d1	A	P

The controller writes the 20-bit value (**d** = d4,d3,d2,d1,d0) into the MAS 3507D register (**r** = r1,r0). In contrast to memory cells, registers are always addressed individually, and they may also interact with built-in hardware blocks. A list of useful registers is given in the next section.

Example: Muting can be realized by writing the value 1 into the register with the number $aa:

```
<$3a><$68><$9a><$a1><$00><$00>
```

3.3.4. Write D0 Memory

S	dev_write	A	data_write	A	**$A**, $0	A	$0,$0	
				A	**n3,n2**	A	n1,n0	
				A	a3,a2	A	a1,a0	
				A	**d3,d2**	A	d1,d0	
				A	$0,$0	A	$0,d4	
				....repeat for n data values....				
				A	**d3,d2**	A	d1,d0	
				A	$0,$0	A	$0,d4	A P

n3..n0: number of words
a3..a0: start address in MASD memory
d4..d0: data value

The MAS 3507D has 2 memory areas of 2048 words each called D0 and D1 memory. For both memory areas, read and write commands are provided.

Example: reconfiguration of the output to 16 bit without delay has the following I²C protocol:

```
<$3a><$68><$a0><$00> (write D0 memory)
<$00><$01>           (1 word to write)
<$03><$2f>           (start address)
<$00><$10>           (value = $00010)
<$00><$00>
<$3a><$68><$04><$75> (run command)
```

3.3.5. Write D1 Memory

S	dev_write	A	data_write	A	**$B**, $0	A	$0,$0	
				A	**n3,n2**	A	n1,n0	
				A	a3,a2	A	a1,a0	
				A	**d3,d2**	A	d1,d0	
				A	$0,$0	A	$0,d4	
				....repeat for n data values....				
				A	**d3,d2**	A	d1,d0	
				A	$0,$0	A	$0,d4	A P

n3..n0: number of words to be transmitted
a3..a0: start address in MASD memory
d4..d0: data value

For further details, see ‘write D0 memory’ command.

3.3.6. Read Register

1) send command

S	dev_write	A	data_write	A	**$D**, r1	A	r0,$0	A	P

2) get register value

S	dev_write	A	data_read	A	S	dev_read					
	A	d3, d2	A	d1,d0	A	X,X	A	X, d4	Nak	P	

r1, r0: register **r**
d3...d0: data value in **r**
X: don't care

The MAS 3507D has an address space of 256 registers. Some of the registers (**r** = r1,r0 in the figure above) are direct control inputs for various hardware blocks, others do control the internal program flow. In the next section, those registers that are of any interest with respect to the MPEG decoding are described in detail.

Example:
Read the content of the PIO data register ($c8):

```
<$3a><$68><$dc><$80>
<$3a><$69><$3b>
now read:
<d3,d2><d1,d0><x,x><x,d4>
```

3.3.7. Read D0 Memory

1) send command

S	dev_write	A	data_write	A	**$E**, $0	A	$0,$0		
				A	n3,n2	A	n1,n0		
				A	a3,a2	A	a1,a0	A	P

2) get memory value

S	dev_write	A	data_read	A	S	dev_read				
	A	d3, d2	A	d1,d0	A	$0,$0	A	$0, d4		
				....repeat for n data values....						
	A	d3, d2	A	d1,d0	A	$0,$0	A	$0, d4	NaK	P

n3..n0: number of words
a3..a0: start address in MASD memory
d4..d0: data value

The 'read D0 memory' command is provided to get information from memory cells of the MAS 3507D. It gives the controller access to all memory cells of the internal D0 memory. Direct access to memory cells is an advanced feature of the DSP. It is intended for users of the MASC software development kit.

3.3.8. Read D1 Memory

1) send command

S	dev_write	A	data_write	A	**$F**, $0	A	$0,$0		
				A	n3,n2	A	n1,n0		
				A	a3,a2	A	a1,a0	A	P

2) get memory value

S	dev_write	A	data_read	A	S	dev_read				
	A	d3, d2	A	d1,d0	A	$0,$0	A	$0, d4		
				....repeat for n data values....						
	A	d3, d2	A	d1,d0	A	$0,$0	A	$0, d4	NaK	P

n3..n0: number of words
a3..a0: start address in MASD memory
d4..d0: data value

The 'read D1 memory' command is provided to get information from memory cells of the MAS 3507D. It gives the controller access to all memory cells of the internal D1 memory.

3.3.9. Default Read

S	dev_write	A	data_read	A	S	device_read				
					A	d3,d2	A	d1,d0	Nak	P

The 'default read' command immediately returns the content of the MPEGFrameCount (D0:$300) of the MAS 3507D in the variable (**d** = d3,d2,d1,d0). The 'default read' command is the fastest way to get information from the MAS 3507D. Executing the 'default read' command in a polling loop can be used to detect the availability of new ancillary data.

3.4. Protocol Description

3.4.1. Run Command

S	$3A	ACK	$68	ACK	a3, a2	ACK	a1, a0	Wait	ACK	P

3.4.2. Read Control Interface Data

Send Command

S	$3A	ACK	$68	ACK	$3, x2	ACK	x1, x0	Wait	ACK	P

Get Ancillary Data Values

S	$3A	ACK	$69	ACK	S	$3B	Wait					
					ACK	d3, d2	ACK	d1, d0	Wait			
					.... repeat for n data values							
					ACK	d3, d2	ACK	d1, d0	Wait	Nak	P	

3.4.3. Write to MAS 3507D Register

S	$3A	ACK	$68	ACK	$9,r1	ACK	r0,d0	Wait	ACK	
					d4,d3	ACK	d2,d1	Wait	ACK	P

3.4.4. Write to MAS 3507D D0 Memory

S	$3A	ACK	$68	ACK	$A, $0	ACK	$0, $0	Wait
				ACK	n3, n2	ACK	n1, n0	Wait
				ACK	a3, a2	ACK	a1, a0	Wait
				ACK	d3, d2	ACK	d1, d0	Wait
				ACK	$0, $0	ACK	$0, $d4	Wait
				.... repeat for n data values				
				ACK	d3, d2	ACK	d1, d0	Wait
				ACK	$0, $0	ACK	$0, $d4	Wait	Ack	P

3.4.5. Write to MAS 3507D D1 Memory

S	$3A	ACK	$68	ACK	$B, $0	ACK	$0, $0	Wait
				ACK	n3, n2	ACK	n1, n0	Wait
				ACK	a3, a2	ACK	a1, a0	Wait
				ACK	d3, d2	ACK	d1, d0	Wait
				ACK	$0, $0	ACK	$0, $d4	Wait

.... repeat for n data values

ACK	d3, d2	ACK	d1, d0	Wait		
ACK	$0, $0	ACK	$0, $d4	Wait	Ack	P

3.4.6. Read Register

Send command

S	$3A	ACK	$68	ACK	$D, r1	ACK	r0, $0	Wait	ACK	P

Get register value

S	$3A	ACK	$69	ACK	S	$3B	Wait					
					ACK	d3, d2	ACK	d1, d0	Wait			
					ACK	X, X	ACK	X, d4	Wait	Nak	P	

3.4.7. Read D0 memory

Send Command

S	$3A	ACK	$68	ACK	$E, $0	ACK	$0, $0	Wait		
				ACK	n3, n2	ACK	n1, n0	Wait		
				ACK	a3, a2	ACK	a1, a0	Wait	ACK	P

Get memory values

S	$3A	ACK	$69	ACK	S	$3B	Wait									
					ACK	d3, d2	ACK	d1, d0	Wait	ACK	$0, $0	ACK	$0, d4	Wait		

.... repeat for n data values

ACK	d3, d2	ACK	d1, d0	Wait	ACK	d3, d2	ACK	d1, d0	Wait	Nak	P	

3.4.8. Read D1 memory

Send Command

S	$3A	ACK	$68	ACK	$F, $0	ACK	$0, $0	Wait
				ACK	n3, n2	ACK	n1, n0	Wait
				ACK	a3, a2	ACK	a1, a0	Wait	ACK	P

Get memory values

S	$3A	ACK	$69	ACK	S	$3B	Wait									
					ACK	d3, d2	ACK	d1, d0	Wait	ACK	$0, $0	ACK	$0, d4	Wait		
					.... repeat for n data values											
					ACK	d3, d2	ACK	d1, d0	Wait	ACK	d3, d2	ACK	d1, d0	Wait	Nak	P

3.4.9. Default Read

S	$3A	ACK	$69	ACK	S	$3B	Wait						
					ACK	d3, d2	ACK	d1, d0	Wait	Nak	P		

3.4.10.Write Data to the Control Register

S	$3A	ACK	$6A	ACK	d3, d2	ACK	d1, d0	Wait	ACK	P

3.5. Version Number

Table 3–5 shows where the MAS 3507D hardware version, its software and additional information is located.

Table 3–5: MAS 3507D Version

Addr.	Content	Example Value	
D1:$ff6	name of MAS 3507D version	0x03507	3507
D1:$ff7	hardware/software design code MAS 3507D F10	0x00601 (increases for new versions)	0601
D1:$ff9	description: “MPEG 1/2.5 L23”	0x04d50	MP
D1:$ffa		0x04547	EG
D1:$ffb		0x02031	1
D1:$ffc		0x02f32	/2
D1:$ffd		0x02e35	.5
D1:$ffe		0x0204C	L
D1:$fff		0x03233	23

3.6. Register Table

In Table 3–6, the internal registers that are useful for controlling the MAS 3507D are listed. They are accessible by 'register read/write' I^2C commands (see Section 3.3. on page 20).

Important note! Writing into undocumented registers or read-only registers is always possible, but it is highly recommended not to do so. It may damage the function of the firmware and may even lead to a complete system crash of the decoder operation which can only be restored by a reset.

3.6.1. DC/DC Converter

The DCCF Register controls both the internal voltage monitor and DC/DC converter. Between output voltage of the DC/DC converter and the internal voltage monitor threshold an offset exists which is shown in the following table. Please pay attention to the fact, that I^2C protocol is working only if the processor is active (WSEN = 1). However, the setting for the DCCF register will remain active if the DCEN and WSEN lines are deasserted

Table 3–6: Command Register Table

Address	R/W	Name	Comment	Default
$8e	w	DCCF	Set DC/DC converter mode (see Table 3–7 on page 27)	$08000
$aa	r/w	Mute / Bypass Tone Control	Forces a mute of the digital output bypass Bass / Treble / Volume matrix	$0
$ed[1)]	r	PIOData	Read back the PIO pin levels. The PI0 pin corresponds to bit 0 in the PIOData register. This register can be used to detect the actual state of the PIO pins, regardless of the PIO configuration.	
$e6	r/w	StartupConfig	Shadows the start-up configuration set via PIO pins or I^2C command (valid are bits 8, 4...0 as described in Table 2–8.	
$e7	r/w	KPrescale	responsible for prescale of the tone filter (prevent overflows) (see Section 3.6.3. on page 28)	$80000
$6b	r/w	KBass	responsible for increase / decrease of low frequencies (see Section 3.6.3. on page 28)	$0
$6f	r/w	KTreble	responsible for increase / decrease of high frequencies (see Section 3.6.3. on page 28)	$0

1) In order to get the right information of the PIO pin levels (except for PI19, Demand Pin), register $ed should be read and evaluated. However, the Demand Pin PI19 is shadowed in bit 19 of register $c8.

Table 3–7: DC/DC-converter switch frequency (Bits 8, 13..10 of DCCF-register)

DCCF Value (hex)[1)]	f_{SW}	
	Bit 8 = 0	Bit 8 = 1
0CC00	156 kHz	238 kHz
0C800	160 kHz	245 kHz
0C400	163 kHz	253 kHz
0C000	167 kHz	263 kHz
04C00	171 kHz	272 kHz
04800	175 kHz	283 kHz
04400	179 kHz	295 kHz
04000	184 kHz	307 kHz
01C00	188 kHz	320 kHz
01800	194 kHz	335 kHz
01400	199 kHz	351 kHz
01000	204 kHz	368 kHz
00C00	210 kHz	387 kHz
00800	216 kHz	409 kHz
00400	223 kHz	433 kHz
00000	230 kHz	460 kHz

1) All other bits are set to zero (DC/DC-converter output voltage = 3.0 V)

Table 3–8: DC Converter Output Voltages (Bits 16..14, Bit 9 of DCCF-register)

DCCF Value (hex)[1)]	DC/DC Converter Output	Internal Voltage Monitor [2)]
1C000	3.5 V	3.3 V
18000	3.4 V	3.2 V
14000	3.3 V	3.1 V
10000	3.2 V	3.0 V
0C000	3.1 V	2.9 V
08000	3.0 V	2,8 V
04000	2.9 V	2.7 V
00000	2,8 V	2.6 V
1C200	2.7 V	2.5 V
18200	2.6 V	2.4 V
14200	2.5 V	2.3 V
10200	2.4 V	2.2 V
0C200	2.3 V	2.1 V
08200	2.2 V	2.0 V
04200	2.1 V	1.9 V
00200	2.0 V	1.8 V

1) All other bits are set to zero (f_{SW} = 230 kHz)
2) PUP signal becomes inactive when output below

The DC/DC converter may generate interference noise that could be unacceptable for some applications. Thus the oscillator frequency may be adjusted in 16 steps in order to allow the system controller to select a base frequency that does not interfere with an other application.

The CLKI input provides the base clock f_{CKLI} for the frequency divider whose output is made symmetrical with an additional divider by two. The divider quotient is determined by the content of the DCCF register. This register allows 32 settings generating a DC/DC converter clock frequency f_{dc} between:

$$f_{SW} = \left.\frac{f_{CKLI}}{2 \cdot (m+n)}\right|_{n \in \{0,15\},\, m \in \{16,32\}} \quad \text{(EQ 3)}$$

3.6.2. Muting / Bypass Tone Control

Address	R/W	Name	Comment	Default
$aa	r/w	Mute / Bypass Tone Control	Forces a mute of the digital output	$0
		0 1 2	no mute, Tone control active mute output, but continue decoding bypass Bass / Treble / Volume matrix	

To enable fast and simple mute functionality, set bit 0 in register $aa to ‘1’. Writing a ‘0’ deactivates mute.

It is possible to bypass the complete bass / treble / volume control by setting bit 1 in register $aa (write a ‘2’). Resetting bit 1 to ‘0’ enables tone control again.

3.6.3. Bass and Treble Control

Address	R/W	Name	Comment	Default
$e7	r/w	KPrescale	responsible for prescale of the tone filter (prevent overflows) (see Section 2.4.3. on page 8)	$80000
$6b	r/w	KBass	responsible for increase / decrease of low frequencies (see Section 2.4.3. on page 8)	$0
$6f	r/w	KTreble	responsible for increase / decrease of high frequencies (see Section 2.4.3. on page 8)	$0

Tone control is implemented in the MAS 3507D. It allows the control of bass and treble in a range up to ±15 dB, as Table 3–9 shows. To prevent overflow or clipping effects, the prescaler is built-in. The prescaler decreases the overall gain of the tone filter, so the full range up to +15 dB is usable without clipping.

To select a special setting, max. 3 coefficients have to be written into registers of the MAS 3507D. This has to be done via the ‘write register’ I^2C command (see Section 3.3.3.).

Table 3–9: Tone control registers

Boost in dB	Bass (Reg. $6b)	Treble (Reg. $6f)	Prefactor (Reg $e7)
+15	$61800	$5f800	$e9400
+14	$5d400	$58400	$e6800
+13	$58800	$51800	$e3400
+12	$53800	$49c00	$dfc00
+11	$4e400	$42c00	$dc000
+10	$48800	$3c000	$d7800
+9	$42800	$35400	$d25c0
+8	$3c000	$2ec00	$cd000
+7	$35800	$28400	$c6c00
+6	$2e400	$22000	$bfc00
+5	$27000	$1c000	$b8000
+4	$1f800	$16000	$af400
+3	$17c00	$10400	$a5800
+2	$10000	$ac00	$9a400
+1	$800	$5400	$8e000
0	0	0	$80000
–1	$f7c00	$fac00	$80000
–2	$efc00	$f5c00	$80000
–3	$e8000	$f0c00	$80000
–4	$e0400	$ec000	$80000
–5	$d8c00	$e7e00	$80000
–6	$d1800	$e2800	$80000
–7	$ca400	$de000	$80000
–8	$c3c00	$d9800	$80000
–9	$bd400	$d5000	$80000
–10	$b7400	$d0400	$80000
–11	$b1800	$cbc00	$80000
–12	$ac400	$c6c00	$80000
–13	$a7400	$c1800	$80000
–14	$a2800	$bb400	$80000
–15	$9e400	$b2c00	$80000

3.7. Memory Area

3.7.1. Status Memory

The memory cells given in the following table should be accessed by the ‘read control interface data’ I^2C command (see Section 3.3.2. on page 21) because only the 16 LSBs of these memory blocks are used. The memory area table is a consecutive memory block in the D0 memory that keeps all important status information that monitors the MPEG decoding process. The ‘read control interface data’ command resets the MPEG-FRAME-SYNC at PI4 as described in Section 2.9.

Table 3–10: Status Memory Area

Address	Offset[1)]	R/W	Name	Function
D0:$300	0	r	MPEGFrameCount	counts the MPEG frames
D0:$301	1	r	MPEGStatus1	MPEG header / status information
D0:$302	2	r	MPEGStatus2	MPEG header
D0:$303	3	r	CRCErrorCount	counts CRC errors during MPEG decoding
D0:$304	4	r	NumberOfAncillaryBits	number of bits in ancillary data
D0:$305 ... $321	5	r	AncillaryData	organized in words a 16 bit (MSB first)
1) Offset applies to the ‘read control interface data’ command				

3.7.1.1. MPEG Frame Counter

Address	Offset	R/W	Name	Function
D0:$300	0	r	MPEGFrameCount	counts the MPEG frames

The counter will be incremented with each new frame that is decoded. With an invalid MPEG bit stream as its input (e.g. if an invalid header is detected), the MAS 3507D resets the MPEGFrameCount cell to ‘0’. The MPEGFrame-Count is also returned by the ‘default read’ command as described in Section 3.3.9.

3.7.1.2. MPEG Status 1

Address	Offset	R/W	Name	Function
D0:$301	1	r	MPEGStatus 1	MPEG header / status information

The MPEG Status 1 contains the bits 15...11 of the MPEG header and some status bits. It will be set each frame, directly after the header has been decoded from the bit stream.

Table 3–11: MPEG Status 1

Bits	Name/Value	Comment
19, 15	%xxxx.x	don't care
14, 13	MPEG ID %00 %01 %10 %11	Bits 11, 12 of the MPEG-header MPEG 2.5 reserved MPEG 2 MPEG 1
12, 11	Layer %00 %01 %10 %11	Bits 13, 14 of the MPEG-header reserved Layer 3 Layer 2 Layer 1 (Not supported)
10	%1	not protected by CRC
9...2		private bits
1	%1	CRC Error
0	%1	invalid frame

3.7.1.3. MPEG Status 2

Address	Offset	R/W	Name	Function
D0:$302	2	r	MPEG Status 2	MPEG header

The MPEG Status 2 contains the 16 LSBs of the MPEG header. It will be set directly after synchronizing to the bit stream.

Table 3–12: MPEG Status 2

Bits	Value/Name	Comment		
19, 16		don't care		
15...12	Bit rate index	MPEG 1 (Layer 2) in kbit/s	MPEG 1 (Layer 3) in kbit/s	MPEG 2 in kbit/s (Layer 2 & 3) MPEG 2.5 in kbit/s
	%0000 %0001 %0010 %0011 %0100 %0101 %0110 %0111 %1000 %1001 %1010 %1011 %1100 %1101 %1110 %1111	free 32 48 56 64 80 96 112 128 160 192 224 256 320 384 forbidden	free 32 40 48 56 64 80 96 112 128 160 192 224 256 320 forbidden	free 8 16 24 32 40 48 56 64 80 96 112 128 144 160 forbidden
11, 10	Sampling frequency	MPEG 1	MPEG 2	MPEG 2.5
	%00 %01 %10 %11	44.1 kHz 48 kHz 32 kHz reserved	22.05 kHz 24 kHz 16 kHz reserved	11.025 kHz 12 kHz 8 kHz reserved
9	Padding bit			
8	Private bit			
7, 6	Mode			
	%00 %01 %10 %11	stereo joint_stereo (intensity stereo / ms_stereo) dual channel single_channel		
5, 4	Mode extension (if joint stereo only)	intensity stereo	ms_stereo	
	%00 %01 %10 %11	off on off on	off off on on	
3	%0 / 1	copyright not protected / copyright protected		

Table 3–12: MPEG Status 2

Bits	Value/Name	Comment
2	%0 / 1	copy / original
1, 0	Emphasis	indicates the type of emphasis
	%00 %01 %10 %11	none 50/15 µs reserved CCITT J.17

3.7.1.4. CRC Error Counter

Address	Offset	R/W	Name	Function
D0:$303	3	r	CRCErrorCount	counts CRC errors during MPEG decoding

The counter will be increased by each CRC error in the MPEG bit stream. It will not be reset by losing the synchronization.

3.7.1.5. Number Of Ancillary Bits

Address	Offset	R/W	Name	Function
D0:$304	4	r	NumberOfAncillaryBits	number of bits in ancillary data

This cell displays the number of valid ancillary bits stored beginning at D0:$305.

3.7.1.6. Ancillary Data

Address	Offset	R/W	Name	Function
D0:$305 ... D0:$321	5	r	AncillaryData	organized in words a 16 bit (MSB first)

This memory field contains the ancillary data. It is organized in words 16 bit each. The last ancillary bit transmitted in a frame is placed at bit 0 in D0:$305. The position of the first ancillary data bit is locatable via the content of NumberOfAncillaryBits.

An example: 17 bits ancillary data in a frame:

A possible '*read ancillary data*' algorithm would read the NumberOfAncillaryBits and the complete ancillary data area using the telegram:

```
<$3a><$68><$31><$1e> (offset=4, n=30)
<$3a><$69><$3b><receive 30 16-bit words>
```

For reducing the I^2C protocol transfer traffic, it may be useful to split up the 'read ancillary data' algorithm into a first part that reads NumberOfAncillaryBits and a second that reads only NumberOfAncillaryBits/16+1 words.

Table 3–13: Ancillary data bit assignment

D0: $305	15 MSB	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00 LSB
ancillary data	bit 1	bit 2	bit 3	bit 4	bit 5	bit 6	bit 7	bit 8	bit 9	bit 10	bit 11	bit 12	bit 13	bit 14	bit 15	bit 16

Table 3–14: Ancillary data bit assignment

D0: $306	15 MSB	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00 LSB
ancillary data	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	bit 0

3.7.2. Configuration Memory

The configuration memory allows the controller advanced configuration possibilities, e.g. changing setups for the crystal frequency or changing the digital format of the serial audio output data interface.

Table 3–15: Configuration memory area[1)]

Address	R/W	Name	Function	Default
D0:$36d	r/w	PLLOffset48	PLL offset (if f_S = 48, 24, 12, 32, 16, or 8 kHz), validate by 'run $475' command	
D0:$36e	r/w	PLLOffset44	PLL offset (if f_S = 44.1, 22.05, 11.025 kHz), validate by 'run $475' command	
D0:$36f	r/w	OutputConfig	Configuration of the I^2S audio output interface validate by 'run $475' command	
D1:$7f8	r/w	LL	Left → Left Gain	$80000
D1:$7f9	r/w	LR	Left → Right Gain	0
D1:$7fa	r/w	RL	Right → Left Gain	0
D1:$7fb	r/w	RR	Right → Right Gain	$80000

1) **Important note:** Writing into undocumented memory cells is always possible, but it is highly recommended not to do so. It may damage the function of the firmware and may even lead to a complete system crash of the decoder operation which can only be restored by a reset.

3.7.2.1. PLL Offset for 44/48 kHz Sampling Frequency

Address	R/W	Name	Function	Default
D0:$36d	r/w	PLLOffset48	PLL offset (if f_S = 48, 24, 12, 32, 16, or 8 kHz), validate by 'run $475' command	
D0:$36e	r/w	PLLOffset44	PLL offset (if f_S = 44.1, 22.05, 11.025 kHz), validate by 'run $475' command	

With these memory cells it is possible to choose other frequencies than the standard CLKI frequencies. Please note:

– PLLOffset48 is valid for f_S = 48, 24, 12, 32, 16, or 8 kHz.

– PLLOffset44 is valid for f_S = 44.1, 22.05, 11.025 kHz.

Table 3–16 shows the default values which will be set by the firmware according to the start-up configuration.

Table 3–16: PLLOffset48 and PLLOffset44

f_{CLKI}	PLLOffset48	PLLOffset44
14.725 MHz	0.351986	–0.732862

It is also possible to run the MAS 3507D with other clocks. In broadcast mode, it is necessary to adjust the PLLOffsets to this clock, otherwise it will not lock to the MPEG bit stream. In multimedia mode, it is recommended to adjust the PLLOffsets to the crystal, otherwise it would result in a frequency shift (music will be played faster or slower). For adjusting, the following procedure must be done:

– Calculate the PLLOffsets according to:

$$f_{CLKI} = \frac{24{,}576 \cdot 8}{13 + PLLOffset48} = \frac{22{,}5792 \cdot 8}{13 + PLLOffset44}$$

with –0.74 < PLLOffset < 0.74. This corresponds to a frequency range of 14.31...14.73 MHz for the crystal, if both 44.1 kHz and 48 kHz based sample frequencies are used. The range is extended in an application with a fixed sampling frequency, as Table 3–17 shows.

– Write the PLLOffsets to the memory (PLLOffset48 D0:$36d, PLLOffset44 D0:$36e).

– Send a 'run $475' command. With the jump to this address, the settings in the memory will be valid for the internal processing.

Table 3–17: f_{Clkl} for max./ min. PLLOffsets

PLLOffset	f_{CLKI} for f_S related to 48 kHz	fCLKI for fs related to 44.1 kHz
–0.74	16.0365 MHz	14.7336 MHz
0.74	14.309 MHz	13.1465 MHz

Example:

A very common crystal frequency is 14.31818 MHz (NTSC color subcarrier). The

$$PLLOffset48 = \frac{24{,}576 \cdot 8}{14{,}31818} - 13 = 0{,}7314$$

and

$$PLLOffset44 = \frac{22{,}5792 \cdot 8}{14{,}31818} - 13 = -0{,}3843$$

are inside the range –0.74 ... 0.74.

3.7.2.2. Output Configuration

Address	R/W	Name	Function	Default
D0:$36f	r/w	OutputConfig	Configuration of the I^2S audio output interface validate by ‘run $475’ command	

The content of this memory cell depends on the start-up configuration and will be set by the firmware. Nevertheless, the audio output interface is configurable by the software to work in different 16 bit/sample modes and 32 bit/sample modes (see Section 2.7.4. on page 13). For adjusting to this, the following procedure has to be done:

– Choose the output mode (see Table 3–18).
– Write this value to the memory (D0:$36f).
– Send a ‘run $475’ command. With the jump to this address, the settings in the memory will become valid for the internal processing. This overrides all start-up settings

Table 3–18: Output Configuration

Bits	Value	Comment
19...15	%0000.0	don’t care
14	%0 %1	SOC standard timing SOC inverted timing
13..12	%00.	don’t care
11	%0 %1	no delay additional delay of data related to word strobe
10...6	%000.00	don’t care
5	%0 %1	not invert invert outgoing word strobe signal
4	%0 %1	32 bits/sample 16 bits/sample
3...0	%0000	don’t care

3.7.3. Baseband Volume Matrix

Address	R/W	Name	Function	Default
D1:$7f8	r/w	LL	Left->Left gain	$80000
D1:$7f9	r/w	LR	Left->Right gain	$0
D1:$7fa	r/w	RL	Right->Left gain	$0
D1:$7fb	r/w	RR	Right->Right gain	$80000

The digital Baseband volume Matrix is used for controlling the digital gain and a simple kind of stereo basewidth enlargement as shown in Fig. 3–2. Table 3–20 shows the proposed settings for the 4 volume matrix coefficients for stereo, left and right mono. The gain factors are given in fixed point notation. The gain values may be written to the MAS 3507D by the controller command ’write D1 memory’.

Table 3–19: Bit Assignment of the Volume Cells

Bits	Name Value	Comment
19..0	LL/LR/RL/RR	–524288/524288..524287/524288 = –1.0 .. 1.0 – 2^–19

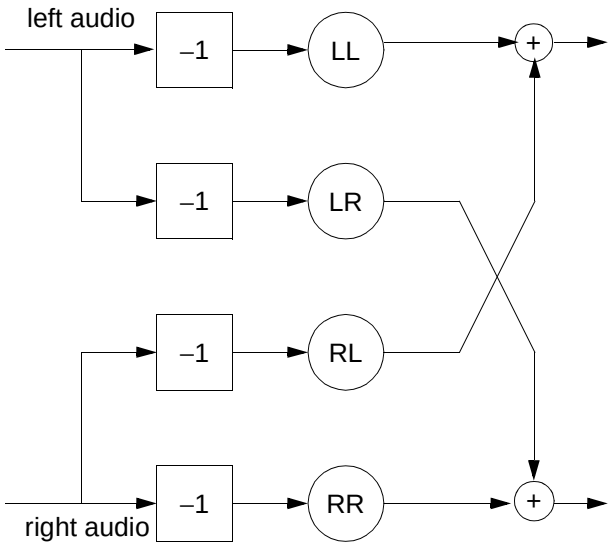


Fig. 3–2: Digital volume matrix

Table 3–20: Settings for the digital volume matrix

Memory location	D1: $7f8	D1: $7f9	D1: $7fa	D1: $7fb
Name	LL	LR	RL	RR
Stereo (default)	–1.0	0	0	–1.0
Mono left	–1.0	–1.0	0	0
Mono right	0	0	–1.0	–1.0

The fixed point gain values correspond to 20 bit 2's complement notation. The conversion between fixed point and 2's complement notation is done easily by the algorithms described in Section 3.2.1.

Table 3–21: Volume matrix conversion (dB into hexadecimal)

Volume (in dB)	Hexa decimal	Volume (in dB)	Hexa decimal	Volume (in dB)	Hexa decimal	Volume (in dB)	Hexa decimal	Volume (in dB)	Hexa decimal
0	80000	–20	F3333	–40	FEB85	–60	FFDF4	–80	FFFCC
–1	8DEB8	–21	F4979	–41	FEDBF	–61	FFE2D	–81	FFFD1
–2	9A537	–22	F5D52	–42	FEFBB	–62	FFE60	–82	FFFD6
–3	A5621	–23	F6F03	–43	FF180	–63	FFE8D	–83	FFFDB
–4	AF3CD	–24	F7EC8	–44	FF314	–64	FFEB5	–84	FFFDF
–5	B8053	–25	F8CD5	–45	FF47C	–65	FFED9	–85	FFFE3
–6	BFD92	–26	F995B	–46	FF5BC	–66	FFEF9	–86	FFFE6
–7	C6D31	–27	FA485	–47	FF6DA	–67	FFF16	–87	FFFE9
–8	CD0AD	–28	FAE78	–48	FF7D9	–68	FFF2F	–88	FFFEB
–9	D2958	–29	FB756	–49	FF8BC	–69	FFF46	–89	FFFED
–10	D785E	–30	FBF3D	–50	FF986	–70	FFF5A	–90	FFFEF
–11	DBECC	–31	FC648	–51	FFA3A	–71	FFF6C	–91	FFFF1
–12	DFD91	–32	FCC8E	–52	FFADB	–72	FFF7C	–92	FFFF3
–13	E3583	–33	FD227	–53	FFB6A	–73	FFF8B	–93	FFFF4
–14	E675F	–34	FD723	–54	FFBEA	–74	FFF97	–94	FFFF6
–15	E93CF	–35	FDB95	–55	FFC5C	–75	FFFA3	–95	FFFF7
–16	EBB6A	–36	FDF8B	–56	FFCC1	–76	FFFAD	–96	FFFF8
–17	EDEB6	–37	FE312	–57	FFD1B	–77	FFFB6	–97	FFFF9
–18	EFE2C	–38	FE638	–58	FFD6C	–78	FFFBE	–98	FFFF9
–19	F1A36	–39	FE905	–59	FFDB4	–79	FFFC5	–99	FFFFA

Table 3–21 contains the converted gain values as used in the 'write D1 memory' command

4. Specifications

4.1. Outline Dimensions

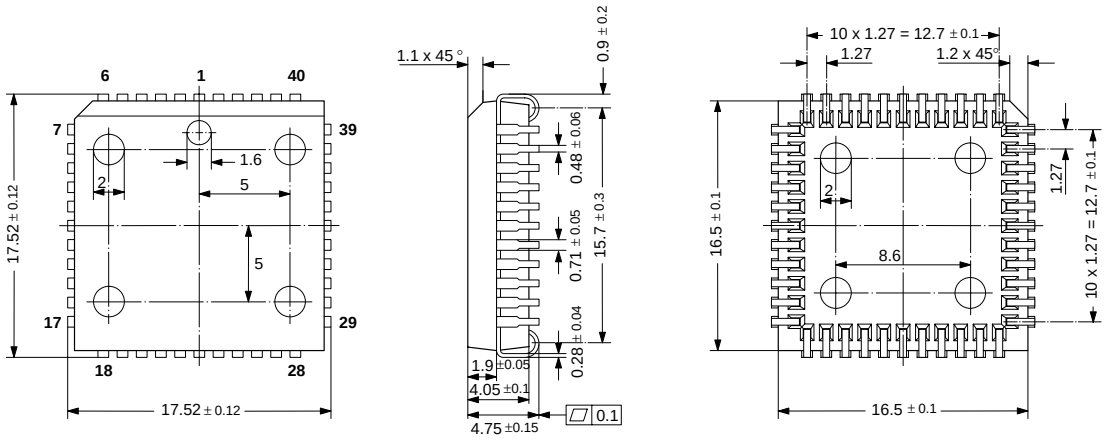


Fig. 4–1:
44-Pin Plastic Leaded Chip Carrier Package
(PLCC44)
Weight approximately 2.5 g
Dimensions in mm

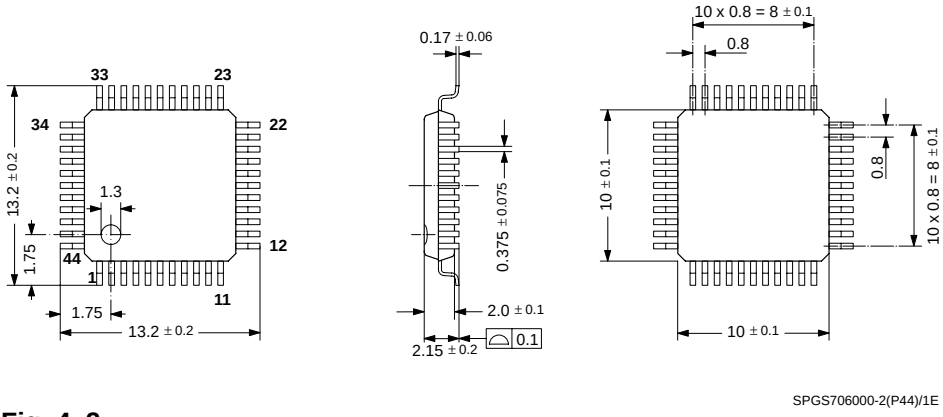


Fig. 4–2:
44-Pin Plastic Quad Flat Package
(PMQFP44)
Weight approximately 0.4 g
Dimensions in mm

Note: Start pin and orientation of pin numbering is different for PLCC and PMQFP packages!

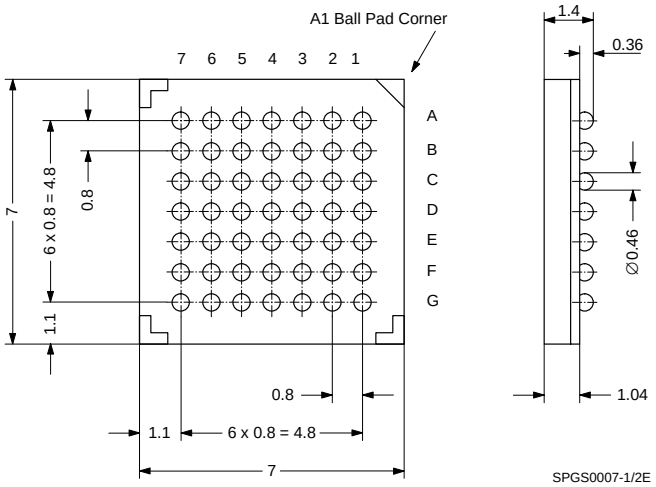


Fig. 4–3:
49-Ball Plastic Ball Grid Array
(PBGA49)
Weight approximately 0.13 g
Dimensions in mm

4.2. Pin Connections and Short Descriptions

NC not connected, leave vacant
LV If not used, leave vacant
X obligatory, pin must be connected as described in application information

VDD connect to positive supply
VSS connect to ground

Pin No. PMQFP 44-pin	Pin No. PLCC 44-pin	Pin No. PBGA 49-ball	Pin Name Test Alias in ()	Type	Connection (If not used)	Short Description
1	6	C3	TE	IN	VSS	Test Enable
2	5	C2	$\overline{\text{POR}}$	IN	VDD	Reset, Active Low
3	4	B1	I2CC	IN/OUT	X	I^2C Clock Line
4	3	D2	I2CD	IN/OUT	X	I^2C Data Line
5	2	C1	VDD	SUPPLY	X	Positive Supply for Digital Parts
6	1	D1	VSS	SUPPLY	X	Ground Supply for Digital Parts
7	44	E2	DCEN	IN	VSS	Enable DC/DC Converter
8	43	E1	$\overline{\text{EOD}}$	OUT	LV	PIO End of DMA, Active Low
9	42	F2	$\overline{\text{RTR}}$	OUT	LV	PIO Ready to Read, Active Low
10	41	F1	$\overline{\text{RTW}}$	OUT	LV	PIO Ready to Write, Active Low
11	40	G1	DCSG	SUPPLY	VSS	DC Converter Transistor Ground
12	39	E3	DCSO	OUT	VSS	DC Converter Transistor Open Drain
13	38	F3	VSENS	IN	VDD	DC Converter Voltage Sense
14	37	G2	PR	IN	X	PIO-DMA Request or Read/$\overline{\text{Write}}$

Pin No. PMQFP 44-pin	Pin No. PLCC 44-pin	Pin No. PBGA 49-ball	Pin Name Test Alias in ()	Type	Connection (If not used)	Short Description
15	36	F4	$\overline{PCS}$	IN	X	PIO Chip Select, Active Low
16	35	G3	PI19	IN/OUT	LV	PIO Data [19] 1. Demand Pin in SDI mode 2. data bit [7], MSB (PIO-DMA input mode)
17	34	E4	PI18	IN/OUT	LV	PIO Data [18] 1. MPEG header bit 11 – MPEG ID (SDI mode) 2. data bit [6] (PIO-DMA input mode)
18	33	G4	PI17	IN/OUT	LV	PIO Data [17] 1. MPEG header bit 12 – MPEG ID (SDI mode) 2. data bit [5] (PIO-DMA input mode)
19	32	F5	PI16	IN/OUT	LV	PIO Data [16] 1. SIC*, alternative input for SIC (SDI mode) 2. data bit [4] (PIO-DMA input mode)
20	31	G5	PI15	IN/OUT	LV	PIO Data [15] 1. SII*, alternative input for SII (SDI mode) 2. data bit [3] (PIO-DMA input mode)
21	30	F6	PI14	IN/OUT	LV	PIO Data [14] 1. SID*, alternative input for SID (SDI mode) 2. data bit [2] (PIO-DMA input mode)
22	29	G6	PI13	IN/OUT	LV	PIO Data [13] 1. MPEG header bit 13 – Layer ID (SDI mode) 2. data bit [1] (PIO-DMA input mode)
23	28	E5	PI12	IN/OUT	LV	PIO Data [12] 1. MPEG header bit 14 – Layer ID (SDI mode) 2. data bit [0] (PIO-DMA input mode)
24	27	E6	SOD (PI11)	OUT	LV	Serial Output Data
25	26	F7	SOI (PI10)	OUT	LV	Serial Output Frame Identification
26	25	D6	SOC (PI9)	OUT	LV	Serial Output Clock
27	24	E7	PI8	IN	X	Start-up[1]: Clock output scaler on / off
				OUT		Operation[2]: MPEG CRC error
28	23	D7	XVDD	SUPPLY	X	Positive Supply of Output Buffers
29	22	C6	XVSS	SUPPLY	X	Ground of Output Buffers
30	21	C7	SID (PI7)	IN	X	Serial Input Data
31	20	B6	SII (PI6)	IN	VSS	Serial Input Frame Identification

Pin No. PMQFP 44-pin	Pin No. PLCC 44-pin	Pin No. PBGA 49-ball	Pin Name Test Alias in ()	Type	Connection (If not used)	Short Description
32	19	B7	SIC (PI5)	IN	X	Serial Input Clock
33	18	A7	PI4	IN	X	Start-up[1]: Select SDI / PIO-DMA input mode
				OUT		Operation[2]: MPEG-Frame Sync
34	17	B5	PI3	IN	X	Start-up[1]: Enable Layer 3 / Disable Layer 3 decoding
				OUT		Operation[2]: MPEG header bit 20 (Sampling frequency)
35	16	A6	PI2	IN	X	Start-up[1]: Enable Layer 2 / Disable Layer 2 decoding
				OUT		Operation[2]: MPEG header bit 21 (Sampling frequency)
36	15	B4	PI1	IN	X	Start-up[1]: SDO: Select 32-bit mode / 16-bit I^2S mode
				OUT		Operation[2]: MPEG header bit 30 (Emphasis)
37	14	A5	PI0	IN	X	Start-up[1]: Select Multimedia mode / Broadcast mode
				OUT		Operation[2]: MPEG header bit 31 (Emphasis)
38	13	C4	CLKO	OUT	LV	Clock Output for the D/A converter
39	12	A4	PUP	OUT	LV	Power Up, i.e. status of voltage supervision
40	11	B3	WSEN	IN	X	Enable DSP and Start DC/DC Converter
41	10	A3	WRDY	OUT	LV	If WSEN = 0: valid clock input at CLKI If WSEN = 1: clock synthesizer PLL locked
42	9	B2	AVDD	SUPPLY	VDD	Supply for analog circuits
43	8	A2	CLKI	IN	X	Clock input
44	7	A1	AVSS	SUPPLY	VSS	Ground supply for analog circuits

[1] Start-up configuration see Section 2.8.
[2] Not available in PIO-DMA mode, see Section 2.8.1.

4.2.1. Pin Descriptions

4.2.1.1. Power Supply Pins

Connection of all power supply pins is mandatory for the function of the MAS 3507D.

VDD **SUPPLY**
VSS **SUPPLY**

The VDD/VSS pair is internally connected with all digital modules of the MAS 3507D.

XVDD **SUPPLY**
XVSS **SUPPLY**

The XVDD/XVSS pins are internally connected with the pin output buffers.

AVDD **SUPPLY**
AVSS **SUPPLY**

The AVDD/AVSS pair is connected internally with the analog blocks of the MAS 3507D, i.e. clock synthesizer and supply voltage supervision circuits.

4.2.1.2. DC/DC Converter Pins

DCEN **IN**

The DCEN input signal enables the DC/DC converter operation.

DCSG **SUPPLY**

The DC converter Signal Ground pin is used as a basepoint for the internal switching transistor of the DC/DC converter. It must always be connected to ground.

DCSO **OUT**

DCSO is an open drain output and should be connected with external circuitry (inductor/diode) to start the DC/DC converter. When the DC/DC converter is not used, it has to be connected to VSS.

VSENS **IN**

The VSENS pin is the input for the DC/DC converter feedback loop. It must be connected directly with the Schottky diode and the capacitor as shown in Fig. 2–3. When the DC/DC converter is not used, it has to be connected to VDD.

4.2.1.3. Control Lines

I2CC **SCL** **IN/OUT**
I2CD **SDA** **IN/OUT**

Standard I^2C control lines. Normally there are Pullup-resistors tied from each line to VDD.

4.2.1.4. Parallel Interface Lines

4.2.1.4.1. PIO Handshake Lines

PIO handshake lines are not used during start-up but in operation mode. Read out of the status information and the demand mode work in µP-mode: set $\overline{PCS}$ = '0' and PR = '1'. Usage of PIO-DMA mode is possible with input mode via PIO.

$\overline{PCS}$ **IN**

The PIO chip select must be set to '0' to activate the PIO as Output in operation mode (e.g. PI19 = demand signal in mutimedia mode & SDI input mode).

PR **IN**

The PIO PR must be set to '1' to validate data output from MAS 3507D.

$\overline{RTW}$ **OUT**

$\overline{RTW}$ is not supported by the built-in firmware.

$\overline{RTR}$ **OUT**

$\overline{RTR}$ is only supported by the built-in firmware in PIO-DMA input mode.

$\overline{EOD}$ **OUT**

End of DMA ($\overline{EOD}$) is only supported by the built-in firmware in PIO-DMA input mode.

4.2.1.4.2. PIO Data Lines

The function of the parallel interface is separated into two parts. During start-up, the PIO will read the start-up configuration (independent from the PIO handshake lines). This is done to define the environment for the MAS 3507D (see Section 2.8.1. for details).

After start-up, the PIO will be switched to µP-mode. With the PR = '1' and the $\overline{PCS}$ = '0', the PIO interface is defined as output and displays some status information of the MPEG decoder. The PIO can be connected to an external controller or to a display unit (e.g. LED). The internal MPEG decoder firmware attaches specific functions to the following pins:

PI19 DEMAND PIN OUT

When MAS 3507D is in multimedia mode it demands with PI19 = ’1’ for new input data.

PI18 MPEG-IDEX OUT
PI17 MPEG-ID OUT

These pins mirror the according bits of the MPEG header (see Table 2–9 for details).

PI16 (SIC*) IN
PI15 (SII*) IN
PI14 (SID* IN

The SIC*, SID*, and SII* may be configured as alternative serial input lines in order to support alternative serial digital inputs.

PI13 LAYER ID OUT
PI12 LAYER ID OUT

These pins mirror the according bits of the MPEG header (see Table 2–9 for details).

PI8 MPEG-CRC-ERROR OUT/IN

The MPEG-CRC-ERROR pin is activated if no successful MPEG decoding is possible. The reason might be that the CRC check of the MPEG Frame header has detected an error or that no valid bit stream is available. The error signal will stay active for the entire duration of one MPEG frame.

During start-up, this pin is an input for enabling/disabling the CLKO+divider (see Section 3.6.).

PI4 MPEG-FRAME-SYNC OUT/IN

The MPEG-FRAME-SYNC signal indicates that a MPEG header has been decoded properly and the internal MPEG decoder is in a synched state. The MPEG-FRAME-SYNC signal is inactive after Power On Reset and will be activated if a valid MPEG Layer 2 or 3 header has been recognized. The signal will be cleared if the ancillary data information is read out by the controller via I^2C interface.

During start-up, this pin sets either SDI- or PIO-DMA-input mode (see Section 3.6.).

PI3 SAMPLING FREQUENCY OUT
PI2 SAMPLING FREQUENCY OUT
PI1 EMPHASIS OUT
PI0 EMPHASIS OUT

These pins mirror the according bits of the MPEG header (see Table 2–9 for details).

During start-up, these pins are input pins (see Section 3.6.).

4.2.1.5. Voltage Supervision And Other Functions

CLKI IN

This is the clock input of the MAS 3507D. CLKI should be a buffered output of a crystal oscillator. Standard clock frequency is 14.725. Others can be used, if PLL_offset register is changed by I^2C.

CLKO OUT

The CLKO is an oversampling clock that is synchronized to the digital audio data (SOD) and the frame identification (SOI).

PUP OUT

The PUP output indicates that the power supply voltage exceeds its minimal level (software adjustable).

WSEN IN

WSEN enables DSP operation and starts DC/DC-converter.

WRDY OUT

WRDY has two functions depending on the state of the WSEN signal.

If WSEN = ’0’, it indicates that a valid clock has been recognized at the CLKI clock input.

If WSEN = ’1’, the WRDY output will be set to ‘0’ until the internal clock synthesizer has locked to the incoming audio data stream, and thus, the CLKO clock output signal is valid.

4.2.1.6. Serial Input Interface

SID IN
SII IN
SIC IN

Data, Frame Indication, and Clock line of the serial input interface. The SII line should be connected with VSS in the standard mode.

4.2.1.7. Serial Output Interface

SOD OUT
SOI OUT
SOC OUT

Data, Frame Indication, and Clock line of the serial output interface. The SOI indicates whether the left or the right audio sample is transmitted. Besides the two modes (selected by the PI1 during start-up), it is possible to reconfigure the interface.

4.2.1.8. Miscellaneous

$\overline{\text{POR}}$ **IN**

The Power On Reset pin is used to reset the digital parts of the MAS 3507D. $\overline{\text{POR}}$ is a low active signal.

TE **IN**

The TE pin is for production test only and must be connected with VSS in all applications.

4.2.2. Pin Configurations

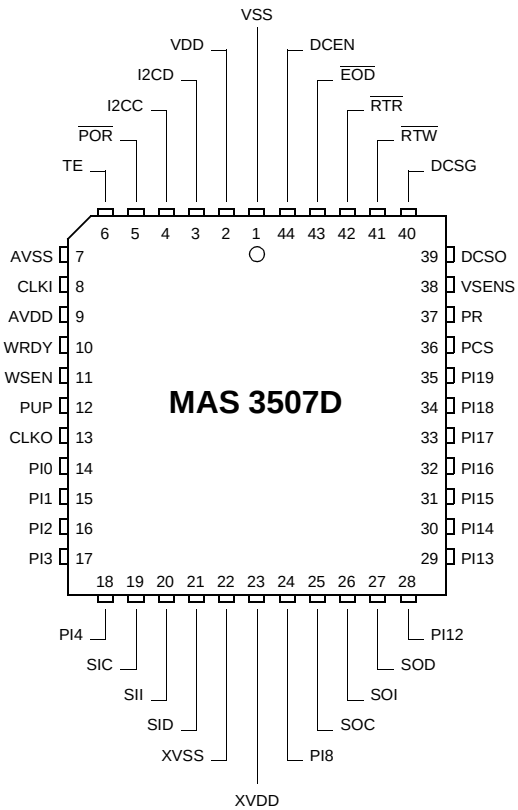


Fig. 4–4: 44-pin PLCC package

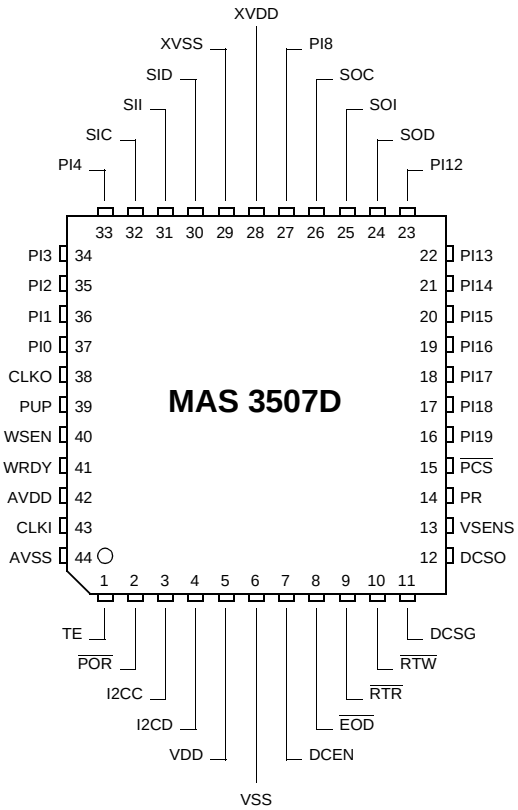


Fig. 4–5: 44-pin PMQFP package

4.2.3. Internal Pin Circuits

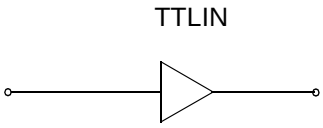


Fig. 4–6: Input pins $\overline{\text{PCS}}$, PR

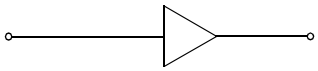


Fig. 4–7: Input pin TE, DCEN

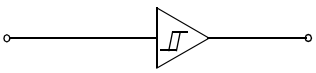


Fig. 4–8: Input pins WSEN, $\overline{\text{POR}}$

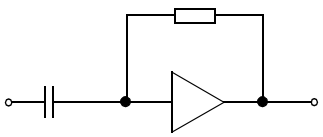


Fig. 4–9: Input pin CLKI

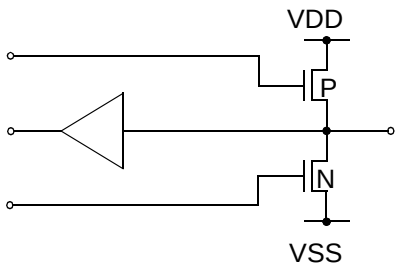


Fig. 4–10: Input/Output pins PI0...PI4, PI8, SOC, SOI, SOD, PI12...PI19

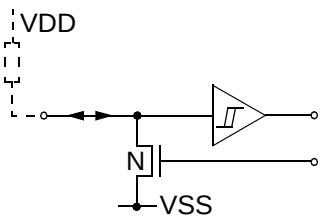


Fig. 4–11: Input/Output pins I2CC, I2CD

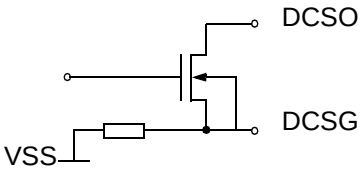


Fig. 4–12: Input/Output pins DCSO, DCSG

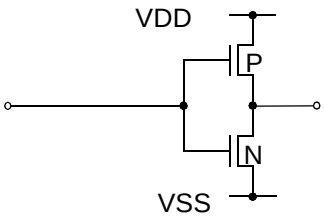


Fig. 4–13: Output pins WRDY, $\overline{\text{RTW}}$, $\overline{\text{EOD}}$, $\overline{\text{RTR}}$, CLKO, PUP

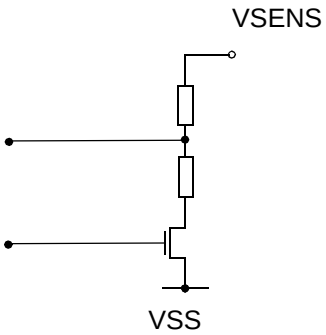


Fig. 4–14: Input pin VSENS

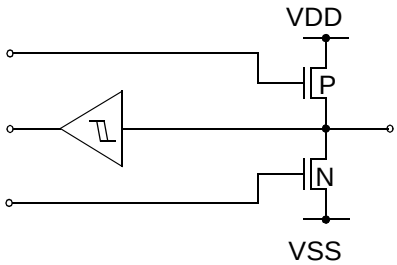


Fig. 4–15: Input/Output pins SIC, SII, SID

4.2.4. Electrical Characteristics

4.2.4.1. Absolute Maximum Ratings

Symbol	Parameter	Pin Name	Min.	Max.	Unit
T_A	Ambient Operating Temperature		–30	85	°C
T_S	Storage Temperature		–40	125	°C
P_{MAX}	Power dissipation	VDD, XVDD, AVDD		600 400 (PBGA)	mW
V_{SUP}	Supply voltage	VDD, XVDD, AVDD		5.5	V
V_{Idig}	Input voltage, all digital inputs		–0.3	V_{SUP} +0.3	V
I_{Idig}	Input current, all digital inputs		–20	+20	mA
I_{Out}	Current, all digital output			0.5	A
I_{OutDC}	Current	DCSO		1.5	A

Stresses beyond those listed in the “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only. Functional operation of the device at these or any other conditions beyond those indicated in the “Recommended Operating Conditions/Characteristics” of this specification is not implied. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.

4.2.4.2. Recommended Operating Conditions

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit
T_A	Ambient temperature range		–30		85	°C
V_{SUP}	Supply voltage	VDD, XVDD, AVDD	2.5	2.7	3.6	V
Reference Frequency Generation						
CLK_F	Clock Frequency[1)]	CLKI		14.725		MHz
CLK_{I_V}	Clock Input Voltage		0		V_{SUP}	V
CLK_{Amp}	Clock Amplitude		0.5			V_{pp}
[1)] range acc. to Section 3.7.2.1.						

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit
Levels						
I_{IL27}	Input Low Voltage @V_{SUP} = 2.5 V ... 3.6 V	$\overline{POR}$ I2CC, I2CD, DCEN, WSEN			0.4	V
I_{IH36}	Input High Voltage @V_{SUP} = 2.5 V ... 3.6 V		1.8			V
I_{IH33}	Input High Voltage @V_{SUP} = 2.5 V ... 3.3 V		1.7			V
I_{IH30}	Input High Voltage @V_{SUP} = 2.5 V ... 3.0 V		1.6			V
I_{ILD}	Input Low Voltage	PI<i>[2], SII, SIC, SID, PR, PCS, TE,			0.4	V
I_{IHD}	Input High Voltage		V_{SUP} – 0.5			V
T_{rf}	Rise / Fall time of digital inputs	PI<i>, SII, SIC, SID, PR, PCS, CLKI			10	ns
D_{cycle}	Duty cycle of digital clock inputs	SIC, CLKI	40	50	60	%
DC-DC converter external circuitry						
C_1	Blocking Capacitor (25 mΩ ESR)[3]	VSENS, DCSG		330		µF
V_F	Schottky Diode Forward voltage[4]	DCSO, VSENS	0.35		0.45	V
L	Inductance of Ferrite ring core coil[5] (50 mΩ),VAC 616/103	DCSO		20		µH

[2] i = 0 to 4, 8 , 12 to 19
[3] Sanyo Oscon 6SA330M
(distributed by Endrich Bauelemente, D-72202 Nagold-lselshausen, www.endrich.com)
[4] ZETEX ZMCS1000
(distributed by ZETEX, D-81673 München, europe.sales@zetex.com), standard Schottky 1N5817
[5] C8 R/4L, SDS0604 (distributed by Endrich Bauelemente, see above)

4.2.4.3. Characteristics

at T_A = –30 to 85 °C, V_{SUP} = 2.5 to 3.6 V, typ. values at T_A = 27°C, V_{SUP} = 2.7 V, CLK_F = 14.725 MHz, duty cycle = 50%

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
Supply Voltage							
I_{SUP}	Current consumption	VDD, XVDD, AVDD		32		mA	2.7 V, sampling frequency ≥ 32kHz
				17		mA	2.7 V, sampling frequency ≤ 24 kHz
				11		mA	2.7 V, sampling frequency ≤ 12 kHz
Digital Outputs and Inputs							
V_{DOL}	Output Low Voltage	SOI[1], SOC[1], SOD[1], $\overline{EOD}$, $\overline{RTR}$, $\overline{RTW}$, WRDY, PUP, CLKO PI<i>			0.3	V	I_{load} = 6mA
V_{DIH}	Output High Voltage		V_{SUP}– 0.3			V	I_{load} = 6mA
Z_{DigI}	Input Impedance	PI<i>, SII, SIC, SID, PR, PCS, CLKI			7	pF	
I_{DLeak}	Digital Input Leakage Current		–1		1	µA	0 V < V_{pin} < V_{SUP}
[1] in low inpedance mode							

4.2.4.3.1. I²C Characteristics

at T_A = –30 to 85 °C, V_{SUP} =2.5 to 3.6 V, typ. values at T_A = 27°C, V_{SUP} = 2.7 V, CLK_F = 14.725 MHz, duty cycle = 50 %

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
R_{ON}	Output resistance	I2CC, I2CD			60	Ω	I_{load} = 5 mA, V_{SUP} = 2.7 V
f_{I2C}	I²C Bus Frequency	I2CC			400	kHz	
t_{I2C1}	I²C START Condition Setup Time	I2CC, I2CD	300			ns	
t_{I2C2}	I²C STOP Condition Setup Time	I2CC, I2CD	300			ns	
t_{I2C3}	I²C Clock Low Pulse Time	I2CC	1250			ns	
t_{I2C4}	I²C Clock High Pulse Time	I2CC	1250			ns	
t_{I2C5}	I²C Data Hold Time before rising edge of clock	I2CC	80			ns	
t_{I2C6}	I²C Data Hold Time after falling edge of clock	I2CC	80			ns	
V_{I2COL}	I²C Output Low Voltage	I2CC, I2CD			0.3	V	I_{LOAD} = 5 mA
I_{I2COH}	I²C Output high leakage current	I2CC, I2CD			1	uA	V_{I2CH} = 3.6 V
t_{I2COL1}	I²C Data Output Hold Time after falling edge of clock	I2CC, I2CD	20			ns	
t_{I2COL2}	I²C Data Output Setup Time before rising edge of clock	I2CC, I2CD	250			ns	f_{I2C} = 400kHz

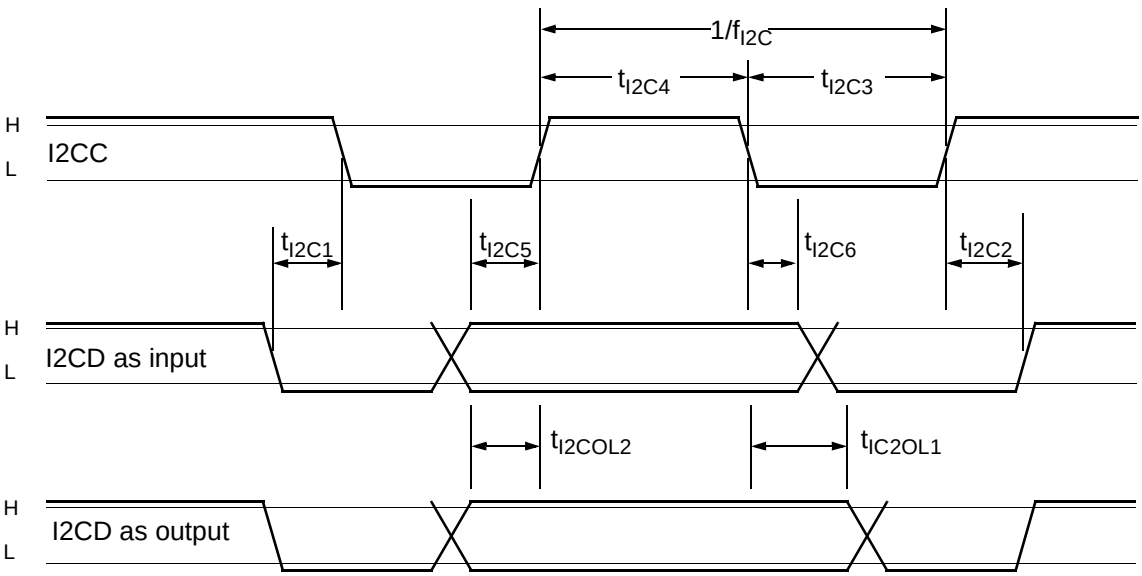


Fig. 4–16: I²C timing diagram

4.2.4.3.2. I²S Bus Characteristics – SDI

at T_A = –30 to 85 °C, V_{SUP} =2.5 to 3.6 V, typ. values at T_A = 27°C, V_{SUP} = 2.7 V, CLK_F = 14.725 MHz, duty cycle = 50 %

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
t_{SICLK}	I²S Clock Input Clockperiod	SIC	960			ns	multimedia mode, mean data rate < 150 kbit/s
t_{SIIDS}	I²S Data SetupTime before falling edge of clock	SIC, SID	50		t_{SICLK}-100	ns	
t_{SIIDH}	I²S data hold time	SID	50			ns	
t_{bw}	Burst wait time	SIC, SID	480				

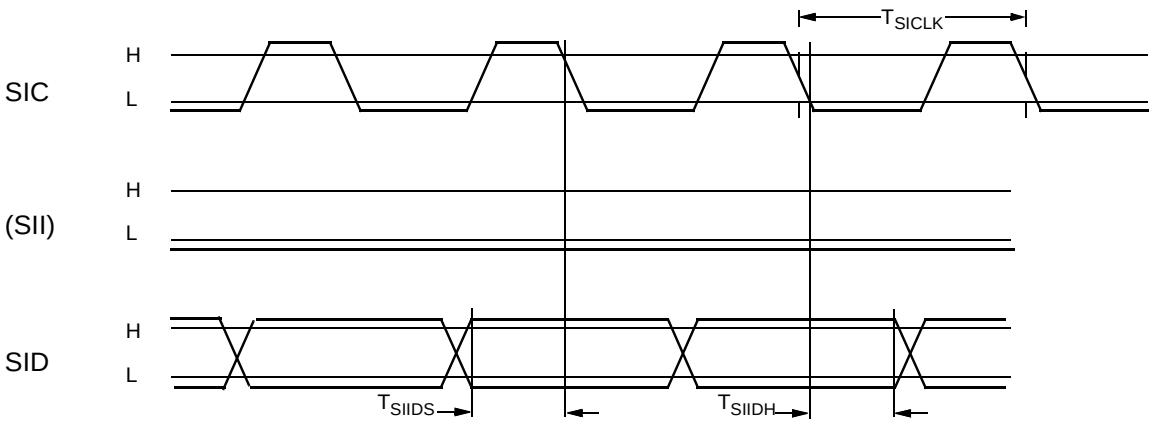


Fig. 4–17: Serial input

4.2.4.3.3. I²S Characteristics – SDO

at T_A = –30 to 85 °C, V_{SUP} = 2.5 to 3.6 V, typ. values at T_A = 27°C, V_{SUP} = 2.7 V, CLK_F = 14.725 MHz, duty cycle = 50 %

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
t_{SOCLK}	I²S Clock Output Period	SOC		325		ns	48 kHz Stereo 32 bit/sample
t_{SOISS}	I²S Wordstrobe Hold Time after falling edge of clock	SOC, SOI	10		t_{SOCLK}/ 2	ns	
t_{SOODC}	I²S Data Hold Time after falling edge of clock	SOC, SOD	10		t_{SOCLK}/ 2	ns	

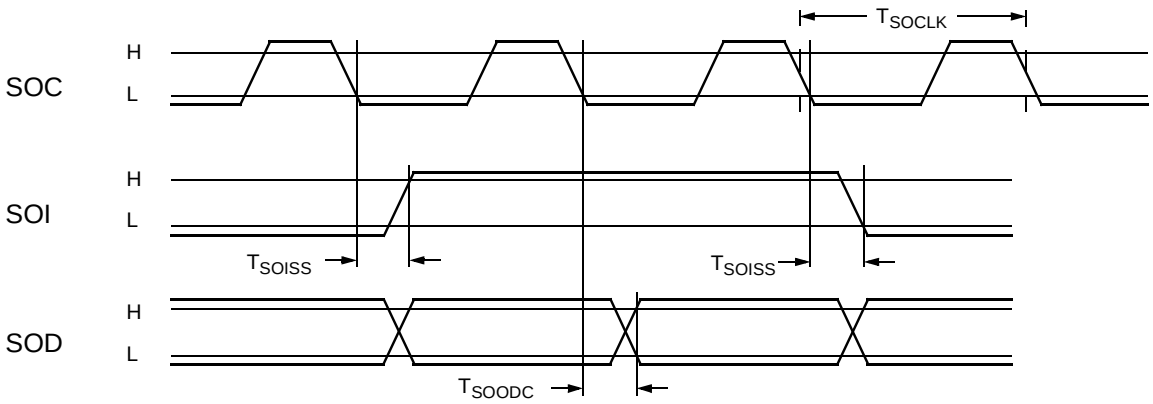


Fig. 4–18: Serial output

4.2.4.4. Firmware Characteristics

at T_A = –30 to 85 °C, V_{SUP} = 2.5 to 3.6 V, typ. values at T_A = 27°C, V_{SUP} = 2.7 V, CLK_F = 14.725 MHz, duty cycle = 50 %

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
Synchronization Times						
$t_{mpgsync}$	Synchronization on MPEG Bit Streams		12...36	72	ms	f_S = 32 kHz, MPEG 2.5
Ranges						
PLLRange	Tracking range of sampling clock recovery PLL	–200		200	ppm	Broadcast mode

4.2.4.4.1. Input Timing Parameters of the MultimediaMode

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
$T_{sdstart}$	Reaction time for data source	PI19	3.1		5.7	ms	f_S = 48 kHz, 320...64 kbit/s
$T_{sdstart}$	Reaction time for data source		4.2		9.2	ms	f_S = 24 kHz, 320...32 kbit/s
T_{sdstar}	Reaction time for data source		23.1		25.6	ms	f_S = 12 kHz, 64...16 kbit/s
T_{sdstar}	Reaction time for data source		34.8		38.4	ms	f_S = 8 kHz, 64...8 kbit/s
T_{sdstop}	Reaction time for data source				1.3	ms	

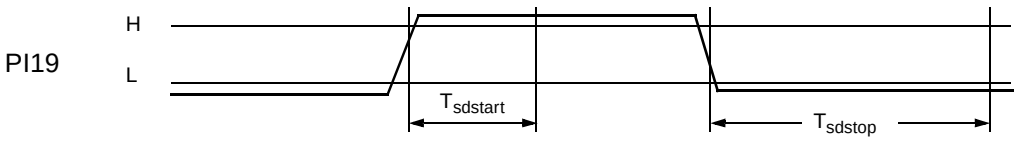


Fig. 4–19: Demand mode

$T_{sdstart}$ refers to the maximal response time for a serial data source to start data transmission with respect to the rising edge of the demand signal at the pin PI19.

T_{sdstop} refers to the maximal response time for a serial data source to stop data transmission with respect to the falling edge of the demand signal at the pin PI19.

4.2.4.5. DC/DC Converter Characteristics

at T_A = –30 to 85 °C, V_{SUP} = 3.0 V, CLK_F = 14.725 MHz, f_{sw} = 230 kHz, typ. values at T_A = +27 °C

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
V_{IN1}	Minimum Start-Up Input Voltage			0.9	1.0	V	I_{LOAD} = 0 mA DCCF = $08000 (Reset)
V_{IN2}	Minimum Operating Voltage			0.6	0.8	V	I_{LOAD} = 55 mA, DCCF = $08000 (Reset)
				1.3	1.8	V	I_{LOAD} = 250 mA, DCCF = $08000 (Reset)
V_{OUT}	Output Voltage		2.0 [1)]		3.5	V	see Section 4.2.4.6.
$dV_{OUT}/dV_{IN}/V_{OUT}$	Line Regulation			1		%	V_{IN} = 1.0...3.0 V, I_{LOAD} = 55 mA
$dV_{OUT}/dI_{LOAD}/V_{OUT}$	Load Regulation			0.6		%	V_{IN} = 1.2 V, I_{LOAD} = 0...55 mA, f_{SW} = 230 kHz
$dV_{OUT}/dI_{LOAD}/V_{OUT}$	Load Regulation			1.2		%	V_{IN} = 1.2 V, I_{LOAD} = 0...55 mA, f_{SW} = 165 kHz
h_{max}	Maximum Efficiency			90		%	
I_{SUPPLY}	Supply Current			1.1	5	mA	V_{IN} = 3.0 V, I_{LOAD} = 0, includ. switch current
$I_{L,MAX}$	Inductor Current Limit	DCSO, DCSG		1.0	1.4	A	
R_{ON}	Switch On-Resistance	DCSO, DCSG		0.2	0.4	Ω	T_j = 25 °C
I_{LEAK}	Switch Leakage Current	DCSO, DCSG		0.1	1	µA	T_j = 25 °C
f_{SW}	Switch Frequency	DCSO, DCSG	156	230	460	kHz	Depending on DCCF
t_{START}	Start Up Time to PUP-Enable	DCEN, PUP		8		ms	V_{IN} = 1.0 V, I_{LOAD} = 1 mA, PUPLIM = 010 (Reset)
$V_{STARTTRAN}$	Start-Up to Normal Mode Transition Voltage	VSENSE		1.9		V	

1) see Section 4.2.4.2.

All measurements are made with a C8 R/4L 20 µH, 25 mΩ ferrite ring-core coil, Zetex ZLMCS1000 Schottky diode, and Sanyo/Oscon 6SA330M 330 µF, 25 mΩ ESR capacitors at input and output (see Section 4.2.4. on page 47).

4.2.4.6. Typical Performance Characteristics

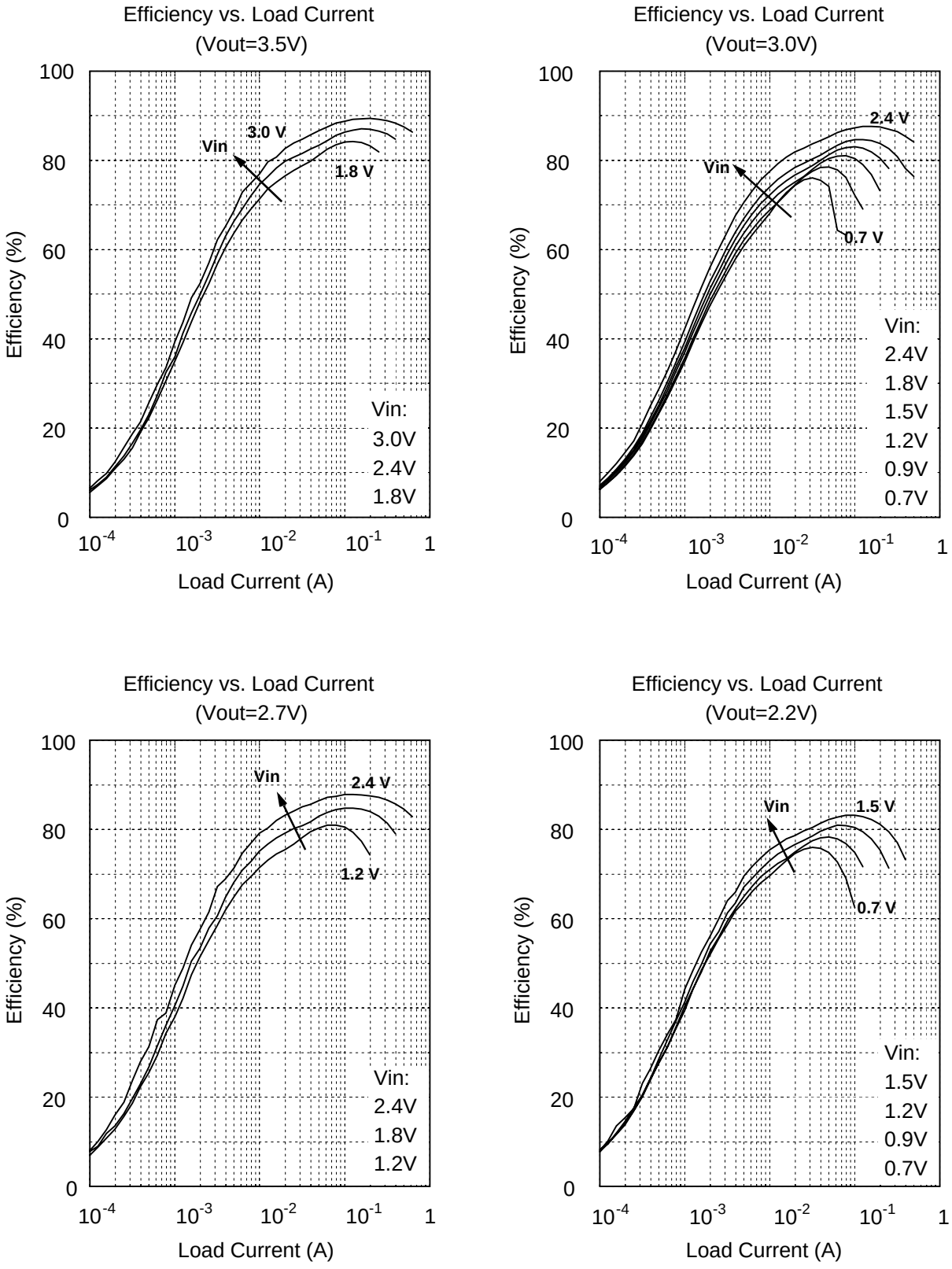


Fig. 4–20: Efficiency vs. Load Current

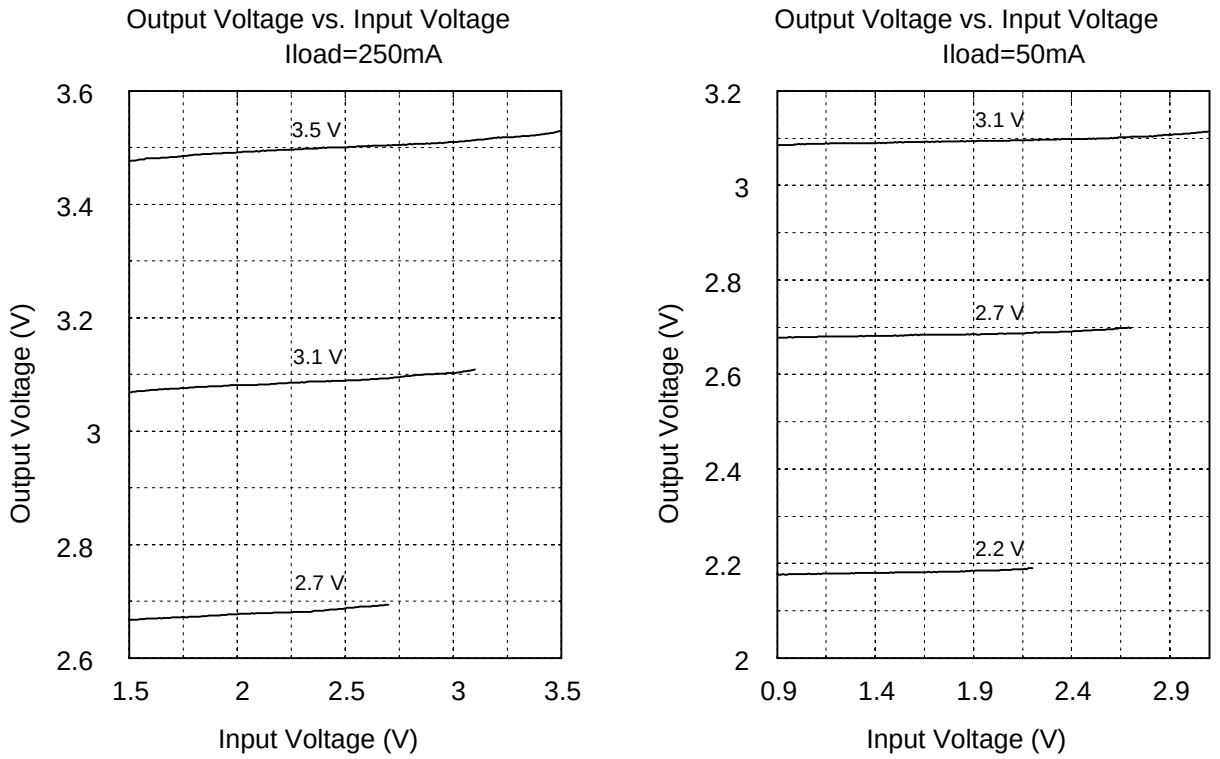


Fig. 4–21: Output Voltage vs. Input Voltage

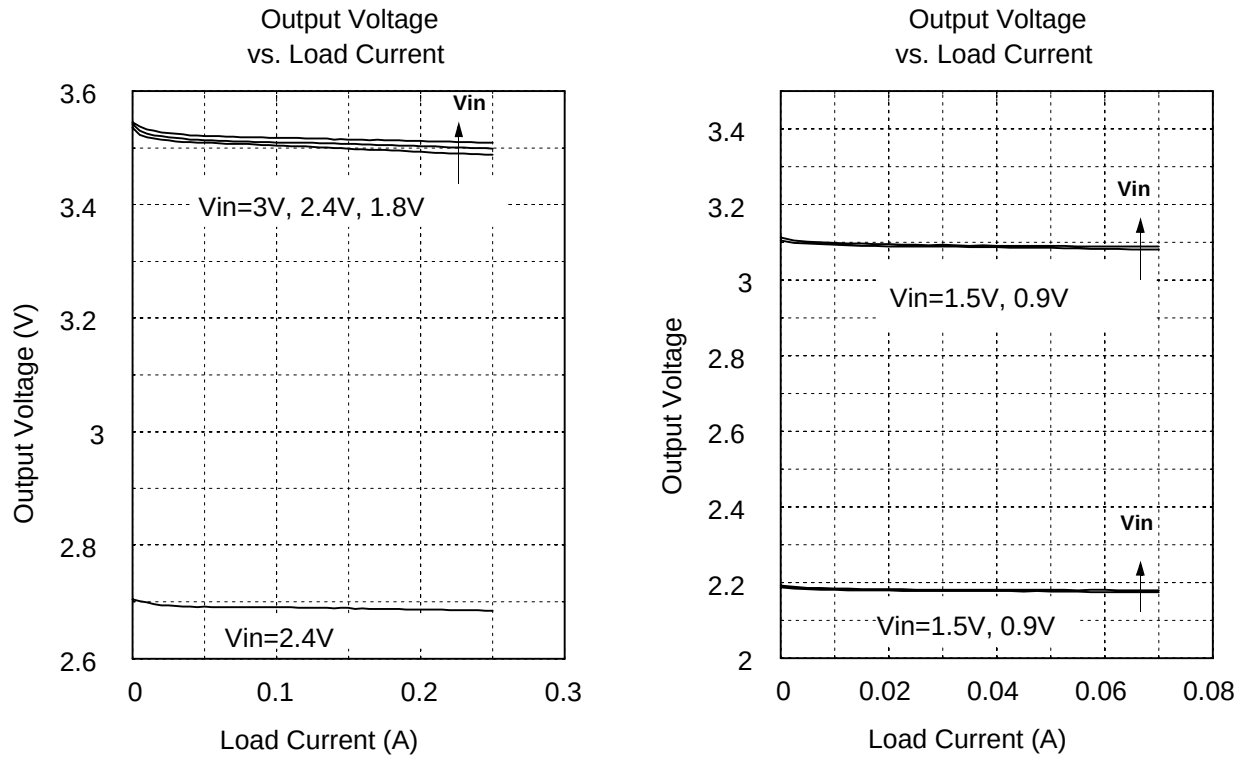


Fig. 4–22: Output Voltage vs. Load Current

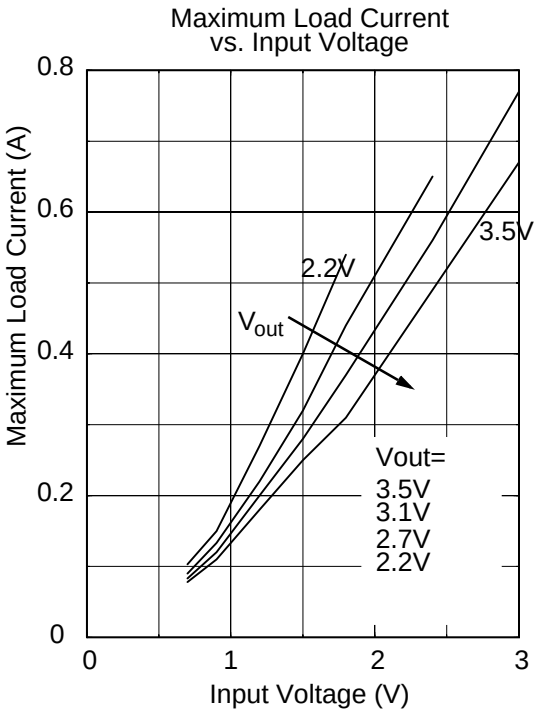


Fig. 4–23: Maximum Load Current vs. Input Voltage

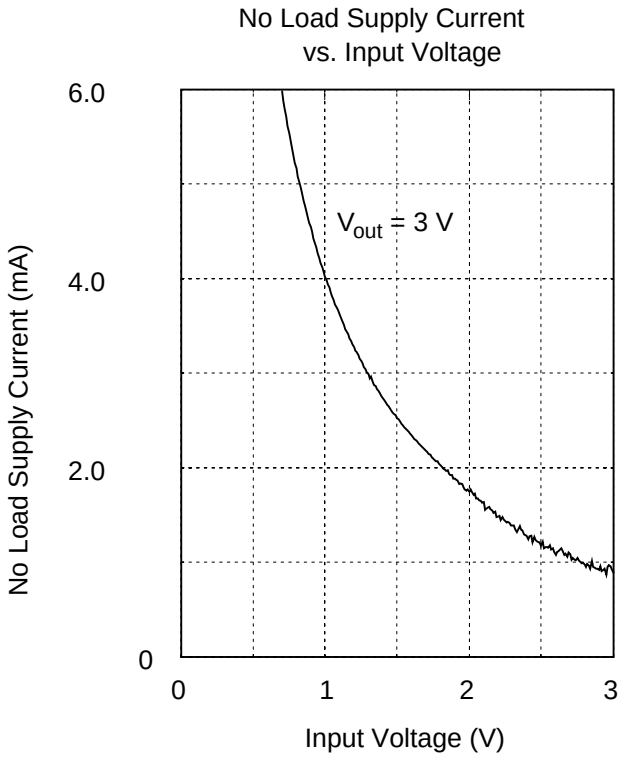
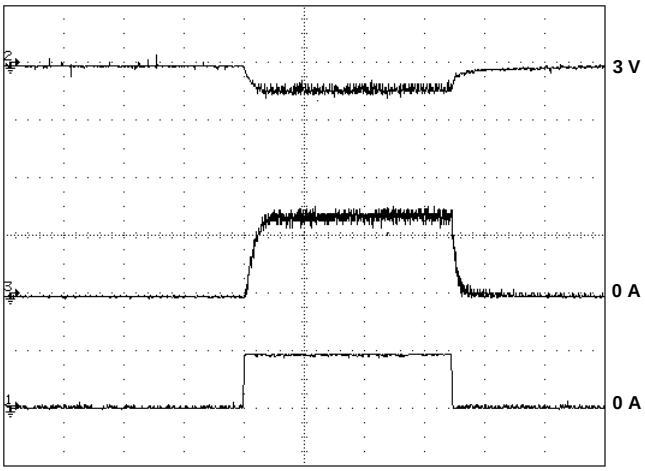


Fig. 4–24: No Load Supply Current vs. Input Voltage

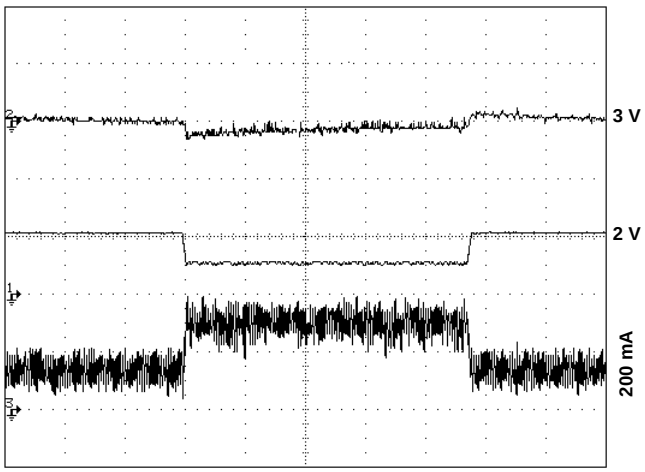


500.00 µs/Div

V_{in} = 1.2 V; V_{out} = 3 V

1	Load Current	200.0 mA/Div
2	Output Voltage	100.0 mV/Div / AC-coupled
3	Inductor Current	500.0 mA/Div

Fig. 4–25: Load Transient-Response

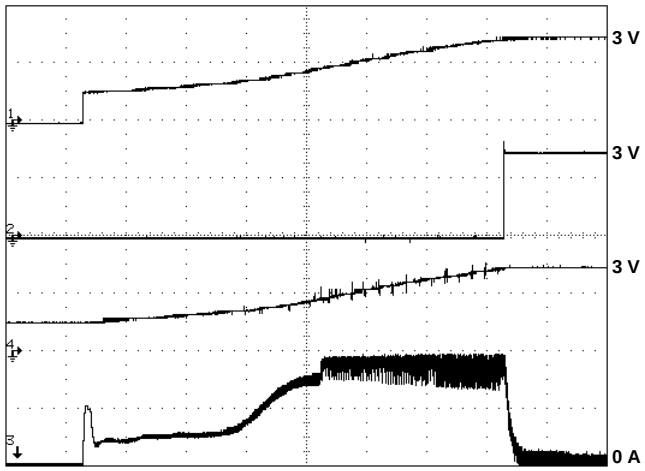


5.00 ms/Div

I_{load} = 100 mA; V_{out} = 3 V

1	V_{in}	2.000 V/Div
2	Output Voltage	50.00 mV/Div / AC-coupled
3	Inductor Current	200.0 mA/Div

Fig. 4–26: Line Transient-Response



500 µs/Div

V_{in} = 1 V; I_{load} = 0 mA

1	V (DCEN)	2.000 V/Div
2	V (PUP)	2.000 V/Div
3	Inductor Current	500.0 mA/Div
4	Output Voltage	2.000 V/Div

Fig. 4–27: Startup Waveform

5. Data Sheet History

1. Preliminary data sheet: “MAS 3507D MPEG 1/2 Layer2/3 Audio Decoder”, Feb. 25, 1998, 6251-459-1PD. First release of the preliminary data sheet.

2. Preliminary data sheet: “MAS 3507D MPEG 1/2 Layer 2/3 Audio Decoder”, Oct. 21, 1998, 6251-459-2PD. Second release of the preliminary data sheet. Major changes:

– Table 3–20: Volume matrix conversion added

– Address for Prefactor register corrected

– Definition for register $aa changed

– Fig. 4–1: Outline Dimension for PLCC44 changed

– Fig. 4–2: PQFP44 package diagram changed

– Fig. 4–3 and Fig. 4–4: Pin configurations added

3. Preliminary data sheet: “MAS 3507D MPEG 1/2 Layer 2/3 Audio Decoder, March 16, 2000, 6251-459-3PD. Third release of the preliminary data sheet.

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