DALLAS SEMICONDUCTOR

DS1385/DS1387
RAMified Real Time Clock 4K x 8

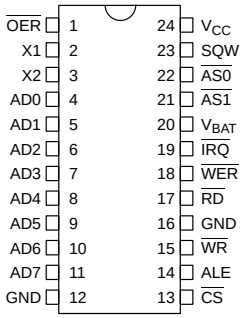
FEATURES

- Upgraded IBM AT computer clock/calendar with 4K x 8 extended RAM
- Totally nonvolatile with over 10 years of operation in the absence of power
- Counts seconds, minutes, hours, day of the week, date, month and year with leap year compensation
- Binary or BCD representations of time, calendar and alarm
- 12– or 24–hour clock with AM and PM in 12–hour mode
- Daylight Savings Time option
- Multiplex bus for pin efficiency
- Interfaced with software as 64 user RAM locations plus 4K x 8 of static RAM
  - 14–bytes of clock and control registers
  - 50–bytes of general purpose RAM
  - 4K x 8 SRAM accessible by using separate control pins
- Programmable square wave output signal
- Bus–compatible interrupt signals ($\overline{IRQ}$)
- Three interrupts are separately software–maskable and testable:
  - Time–of–day alarm once/second to once/day
  - Periodic rates from 122 µs to 500 ms
  - End–of–clock update cycle
- Available as chip (DS1385 or DS1385S) or stand alone module with embedded lithium battery and crystal (DS1387)

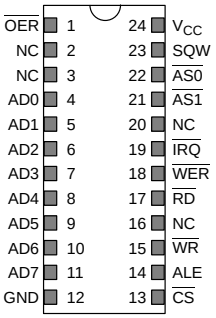
ORDERING INFORMATION

DS1385	RTC Chip; 24–pin DIP
DS1385S	RTC Chip; 28–pin SOIC
DS1387	RTC Module; 24–pin DIP

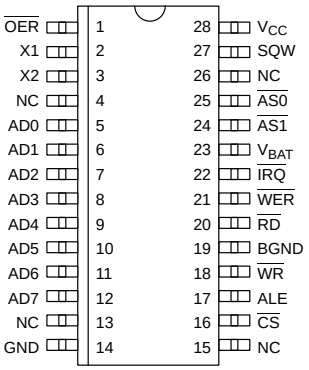
PIN ASSIGNMENT



DS1385 24–PIN DIP
(600 MIL)



DS1387 24–PIN
ENCAPSULATED PACKAGE
(740 MIL FLUSH)



DS1385S 28–PIN SOIC
(330 MIL)

PIN DESCRIPTION

$\overline{OER}$	–	RAM Output Enable
X1	–	Crystal Input
X2	–	Crystal Output
AD0-AD7	–	Mux'ed Address/Data Bus
$\overline{CS}$	–	RTC Chip Select Input
ALE	–	RTC Address Strobe
$\overline{WR}$	–	RTC Write Data Strobe
$\overline{RD}$	–	RTC Read Data Strobe
$\overline{WER}$	–	RAM Write Data Strobe
$\overline{IRQ}$	–	Interrupt Request Output (open drain)
$\overline{AS1}$	–	RAM Upper Address Strobe
$\overline{AS0}$	–	RAM Lower Address Strobe
SQW	–	Square Wave Output
V_{CC}	–	+5V Supply
GND	–	Ground
V_{BAT}	–	Battery + Supply
BGND	–	Battery Ground
NC	–	No Connection

DESCRIPTION

The DS1385/DS1387 RAMified Real Time Clocks (RTCs) are upward–compatible successors to the industry standard DS1285/DS1287 RTC's for PC applications. In addition to the basic DS1285/DS1287 RTC functions, 4K bytes of on–chip nonvolatile RAM have been added.

The RTC functions include a time–of–day clock, a one-hundred year calendar, time–of–day interrupt, periodic interrupts, and an end–of–clock update cycle interrupt. In addition, 50–bytes of user NV RAM are provided within this basic RTC function which can be used to store configuration data. The clock and user RAM are maintained in the absence of system V_{CC} by a lithium battery.

The 4K x 8 additional NV RAM is provided to store a much larger amount of system configuration data than is possible within the original 50–byte area. This RAM is accessed via control signals separate from the RTC, and is also maintained as nonvolatile storage from the lithium battery.

OPERATION

The block diagram in Figure 1 shows the pin connections with the major internal functions of the DS1385/DS1387. The following paragraphs describe the function of each pin.

SIGNAL DESCRIPTIONS

GND, V_{CC} – DC power is provided to the device on these pins. V_{CC} is the +5 volt input. When 5 volts are applied within normal limits, the device is fully accessible and data can be written and read. When V_{CC} is below 4.25 volts typical, reads and writes are inhibited. However, the timekeeping function continues unaffected by the lower input voltage. As V_{CC} falls below 3 volts typical, the RAM and timekeeper are switched over to the energy source connected to the V_{BAT} pin in the case of the DS1385, or to the internal battery in the case of the DS1387. The timekeeping function maintains an accuracy of ±1 minute per month at 25°C regardless of the voltage input on the V_{CC} pin.

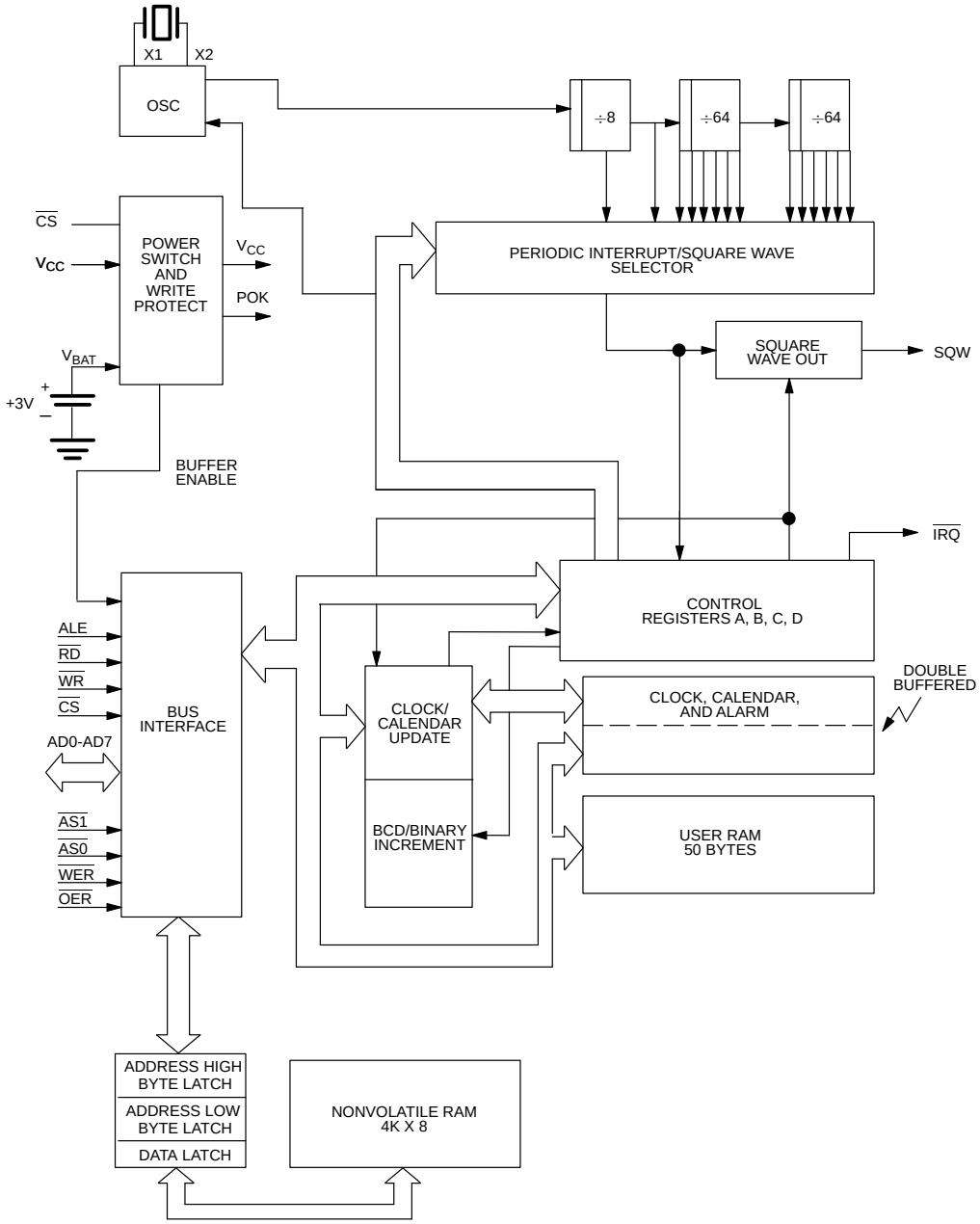
SQW (Square Wave Output) – The SQW pin can output a signal from one of 13 taps provided by the 15 internal divider stages of the real time clock. The frequency of the SQW pin can be changed by programming Register A as shown in Table 2. The SQW signal can be turned on and off using the SQWE bit in Register B. The SQW signal is not available when V_{CC} is less than 4.25 volts typical.

AD0–AD7 (Multiplexed Bi–directional Address/Data Bus) – Multiplexed buses save pins because address information and data information time share the same signal paths. The addresses are present during the first portion of the bus cycle and the same pins and signal paths are used for data in the second portion of the cycle. Address/data multiplexing does not slow the access time of the DS1385/DS1387 since the bus change from address to data occurs during the internal RAM access time. Addresses must be valid prior to the latter portion of ALE, $\overline{AS0}$, or $\overline{AS1}$, at which time the DS1385/DS1387 latches the address from AD0 to AD7. Valid write data must be present and held stable during the latter portion of the $\overline{WR}$ or $\overline{WER}$ pulses. In a read cycle, the DS1385/DS1387 outputs eight bits of data during the latter portion of the $\overline{RD}$ or $\overline{OER}$ pulses. The read cycle is terminated and the bus returns to a high impedance state as $\overline{RD}$ or $\overline{OER}$ transitions high.

ALE (RTC Address Strobe Input) – A positive going address strobe pulse serves to demultiplex the bus. The falling edge of ALE causes the RTC address to be latched within the DS1385/DS1387.

$\overline{RD}$ (RTC Read Input) – $\overline{RD}$ identifies the time period when the DS1385/DS1387 drives the bus with RTC read data. The $\overline{RD}$ signal is an enable signal for the output buffers of the clock.

DS1385/DS1387 BLOCK DIAGRAM Figure 1



$\overline{WR}$ (RTC Write Input) –The $\overline{WR}$ signal is an active low signal. The $\overline{WR}$ signal defines the time period during which data is written to the addressed clock register.

$\overline{CS}$ (RTC Chip Select Input) – The Chip Select signal must be asserted low during a bus cycle for the RTC portion of the DS1385/DS1387 to be accessed. $\overline{CS}$ must be kept in the active state during $\overline{RD}$ and $\overline{WR}$ timing. Bus cycles which take place without asserting $\overline{CS}$ will latch addresses but no access will occur.

$\overline{IRQ}$ (Interrupt Request Output) – The $\overline{IRQ}$ pin is an active low output of the DS1385/DS1387 that can be tied to an interrupt input on a processor. The $\overline{IRQ}$ output remains low as long as the status bit causing the interrupt is present and the corresponding interrupt–enable bit is set. To clear the $\overline{IRQ}$ pin, the application program normally reads the C register.

When no interrupt conditions are present, the $\overline{IRQ}$ level is in the high impedance state. Multiple interrupting devices can be connected to an $\overline{IRQ}$ bus. The $\overline{IRQ}$ bus is an open drain output and requires an external pull–up resistor.

$\overline{AS0}$ (RAM Address Strobe Zero) – The rising edge of $\overline{AS0}$ latches the lower eight bits of the 4K x 8 RAM address.

$\overline{AS1}$ (RAM Address Strobe One) – The rising edge of $\overline{AS1}$ latches the upper four bits of the 4K x 8 RAM address.

$\overline{OER}$ (RAM Output Enable) – $\overline{OER}$ is active low and identifies the time period when the DS1385/DS1387 drives the bus with RAM read data.

$\overline{WER}$ (RAM Write Enable) – $\overline{WER}$ is an active low signal and is used to perform writes to the 4K x 8 RAM portion of the DS1385/DS1387.

(DS1385 ONLY)
X1, X2 – Connections for a standard 32.768 KHz quartz crystal. When ordering, request a load capacitance of 6 pF. The internal oscillator circuitry is designed for operation with a crystal having a specified load capacitance (CL) of 6 pF. The crystal is connected directly to the X1 and X2 pins. There is no need for external capacitors or resistors. Note: X1 and X2 are very high impedance nodes. It is recommended that they and the crystal be guard–ringed with ground and that high frequency signals be kept away from the crystal area. For more information on crystal selection and crystal layout considerations, please consult Application Note 58, “Crystal Considerations with Dallas Real Time Clocks”.

V_{BAT}, BGND – Battery input for any standard 3 volt lithium cell or other energy source. Battery voltage must be held between 2.5 and 3.7 volts for proper operation. The nominal write protect trip point voltage is set by the internal circuitry and is 4.25 volts typical. A maximum load of 1 µA at 25°C and 3.0V on V_{BAT} should in the absence of power be used to size the external energy source.

The battery should be connected directly to the V_{BAT} pin. A diode must not be placed in series with the battery to the V_{BAT} pin. Furthermore, a diode is not necessary because reverse charging current protection circuitry is provided internal to the device and has passed the requirements of Underwriters Laboratories for UL listing (E99151).

ADDRESS MAP

The address map of the DS1385/DS1387 is shown in Figure 2. The address map consists of the RTC and the 4K X 8 NV SRAM section. The RTC section contains 50–bytes of user RAM, 10–bytes of RAM that contain the RTC time, calendar, and alarm data, and 4–bytes which are used for control and status. All 64–bytes can be directly written or read except for the following:

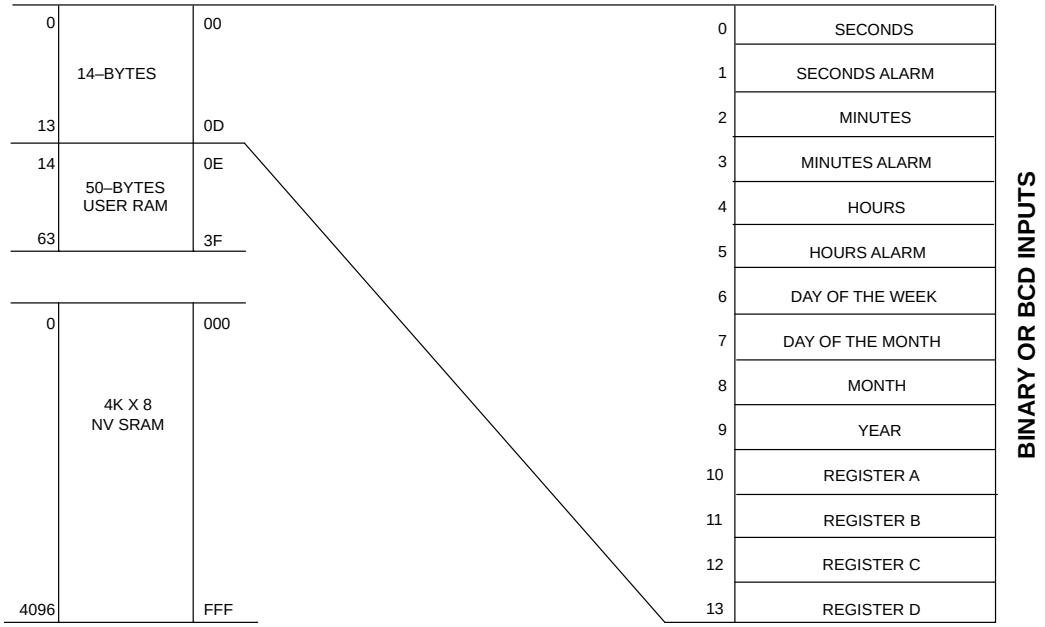
1. Registers C and D are read-only.
2. Bit–7 of Register A is read-only.
3. The high order bit of the seconds byte is read-only.

RTC (REAL TIME CLOCK)

The RTC function is the same as the DS1287 Real Time Clock. Access to the RTC is accomplished with four controls: ALE, $\overline{RD}$, $\overline{WR}$ and $\overline{CS}$. The RTC is the same in the DS1287 with the following exceptions:

1. The MOT pin on the DS1285/DS1287 is not present on the DS1385/DS1387. The bus selection capability of the DS1285/DS1287 has been eliminated. Only the Intel bus interface timing is applicable.
2. The $\overline{RESET}$ pin on the DS1285/DS1287 is not present on the DS1385/DS1387. The DS1385/DS1387 will operate the same as the DS1285/DS1287 with $\overline{RESET}$ tied to V_{CC}.

ADDRESS MAP DS1385/DS1387 Figure 2



TIME, CALENDAR AND ALARM LOCATIONS

The time and calendar information is obtained by reading the appropriate register bytes shown in Table 1. The time, calendar and alarm are set or initialized by writing the appropriate register bytes. The contents of the time, calendar and alarm registers can be either Binary or Binary–Coded Decimal (BCD) format. Table 1 shows the binary and BCD formats of the twelve time, calendar and alarm locations.

Before writing the internal time, calendar and alarm registers, the SET bit in Register B should be written to a logic one to prevent updates from occurring while access is being attempted. Also at this time, the data format (binary or BCD), should be set via the data mode bit (DM) of Register B. All time, calendar and alarm registers must use the same data mode. The set bit in Register B should be cleared after the data mode bit has been written to allow the real–time clock to update the time and calendar bytes.

Once initialized, the real–time clock makes all updates in the selected mode. The data mode cannot be changed without reinitializing the ten data bytes. The 24/12 bit cannot be changed without reinitializing the hour locations. When the 12–hour format is selected, the high order bit of the hours byte represents PM when it is a logic one. The time, calendar and alarm bytes are always accessible because they are double buffered. Once per second the 10–bytes are advanced by one second and checked for an alarm condition. If a read of the time and calendar data occurs during an update, a problem exists where seconds, minutes, hours, etc. may not correlate. The probability of reading incorrect time and calendar data is low. Several methods of avoiding any possible incorrect time and calendar reads are covered later in this text.

The three alarm bytes can be used in two ways. First, when the alarm time is written in the appropriate hours, minutes and seconds alarm locations, the alarm interrupt is initiated at the specified time each day if the alarm enable bit is high. The second method is to insert a “don’t care” state in one or more of the three alarm bytes. The “don’t care” code is any hexadecimal value from C0 to FF. The two most significant bits of each byte set the “don’t care” condition when at logic 1. An alarm will be generated each hour when the “don’t care” bits are set in the hours byte. Similarly, an alarm is generated every minute with “don’t care” codes in the hours and minute alarm bytes. The “don’t care” codes in all three alarm bytes create an interrupt every second.

TIME, CALENDAR AND ALARM DATA MODES Table 1

ADDRESS LOCATION	FUNCTION	DECIMAL RANGE	RANGE	
			BINARY DATA MODE	BCD DATA MODE
0	Seconds	0–59	00–3B	00–59
1	Seconds Alarm	0–59	00–3B	00–59
2	Minutes	0–59	00–3B	00–59
3	Minutes Alarm	0–59	00–3B	00–59
4	Hours–12–hr Mode	1–12	01–0C AM, 81–8C PM	01–12AM, 81–92PM
	Hours–24–hr Mode	0–23	00–17	00–23
5	Hours Alarm–12–hr	1–12	01–0C AM, 81–8C PM	01–12AM, 81–92PM
	Hours Alarm–24–hr	0–23	00–17	00–23
6	Day of the Week Sunday = 1	1–7	01–07	01–07
7	Date of the Month	1–31	01–1F	01–31
8	Month	1–12	01–0C	01–12
9	Year	0–99	00–63	00–99

USER NONVOLATILE RAM – RTC

The 50 user nonvolatile RAM bytes are not dedicated to any special function within the DS1385/DS1387. They can be used by the application program as nonvolatile memory and are fully available during the update cycle. This memory is directly accessible in the RTC section.

INTERRUPTS

The RTC plus RAM includes three separate, fully automatic sources of interrupt for a processor. The alarm interrupt can be programmed to occur at rates from once per second to once per day. The periodic interrupt can be selected for rates from 500 ms to 122 µs. The update–ended interrupt can be used to indicate to the program that an update cycle is complete. Each of these independent interrupt conditions is described in greater detail in other sections of this text.

The application program can select which interrupts, if any, are going to be used. Three bits in Register B enable the interrupts. Writing a logic 1 to an interrupt–enable bit permits that interrupt to be initiated when the event occurs. A logic 0 in an interrupt–enable bit prohibits the $\overline{IRQ}$ pin from being asserted from that interrupt condition. If an interrupt flag is already set when an interrupt is enabled, $\overline{IRQ}$ is immediately set at an active level, although the interrupt initiating the event may have occurred much earlier. As a result, there are cases where the program should clear such earlier initiated interrupts before first enabling new interrupts.

When an interrupt event occurs, the relating flag bit is set to logic 1 in Register C. These flag bits are set independent of the state of the corresponding enable bit in Register B. The flag bit can be used in a polling mode without enabling the corresponding enable bits. When a flag is set, an indication is given to software that an interrupt event has occurred since the flag bit was last read. However, care should be taken when using the flag bits as they are cleared each time Register C is read. Double latching is included with Register C so that bits which are set remain stable throughout the read cycle. All bits which are set (high) are cleared when read and new interrupts which are pending during the read cycle are held until after the cycle is completed. One, two or three bits can be set when reading Register C. Each utilized flag bit should be examined when read to ensure that no interrupts are lost.

The alternative flag bit usage method is with fully enabled interrupts. When an interrupt flag bit is set and the corresponding interrupt enable bit is also set, the $\overline{IRQ}$ pin is asserted low. $\overline{IRQ}$ is asserted as long as at least one of the three interrupt sources has its flag and enable bits both set. The IRQF bit in Register C is a one whenever the $\overline{IRQ}$ pin is being driven low. Determination that the RTC initiated an interrupt is accomplished by reading Register C. A logic one in bit–7 (IRQF bit) indicates that one or more interrupts have been initiated. The act of reading Register C clears all active flag bits and the IRQF bit.

OSCILLATOR CONTROL BITS

When the DS1385/DS1387 is shipped from the factory, the internal oscillator is turned off. This feature prevents the lithium battery from being used until it is installed in a system. A pattern of 010 in bits 6 through 4 of Register A will turn the oscillator on and enable the countdown chain. A pattern of 11X will turn the oscillator on, but holds the countdown chain of the oscillator in reset. All other combinations of bits 6 through 4 keep the oscillator off.

SQUARE WAVE OUTPUT SELECTION

Thirteen of the 15 divider taps are made available to a 1–of–15 selector, as shown in the block diagram of Figure 1. The first purpose of selecting a divider tap is to generate a square wave output signal on the SQW pin. The RS3–RS0 bits in Register A establish the square wave output frequency. These frequencies are listed in Table 2. The SQW frequency selection shares its 1–of–15 selector with the periodic interrupt generator. Once the frequency is selected, the output of the SQW pin can be turned on and off under program control with the square wave enable bit (SQWE).

PERIODIC INTERRUPT RATE AND SQUARE WAVE OUTPUT FREQUENCY Table 2

SELECT BITS REGISTER A				t_{PI} PERIODIC INTERRUPT RATE	SQW OUTPUT FREQUENCY
RS3	RS2	RS1	RS0		
0	0	0	0	None	None
0	0	0	1	3.90625 ms	256 Hz
0	0	1	0	7.8125 ms	128 Hz
0	0	1	1	122.070 µs	8.192 KHz
0	1	0	0	244.141 µs	4.096 KHz
0	1	0	1	488.281 µs	2.048 KHz
0	1	1	0	976.5625 µs	1.024 KHz
0	1	1	1	1.953125 ms	512 Hz
1	0	0	0	3.90625 ms	256 Hz
1	0	0	1	7.8125 ms	128 Hz
1	0	1	0	15.625 ms	64 Hz
1	0	1	1	31.25 ms	32 Hz
1	1	0	0	62.5 ms	16 Hz
1	1	0	1	125 ms	8 Hz
1	1	1	0	250 ms	4 Hz
1	1	1	1	500 ms	2 Hz

PERIODIC INTERRUPT SELECTION

The periodic interrupt will cause the $\overline{IRQ}$ pin to go to an active state from once every 500 ms to once every 122 µs. This function is separate from the alarm interrupt which can be output from once per second to once per day. The periodic interrupt rate is selected using the same Register A bits which select the square wave frequency (see Table 1). Changing the Register A bits affects both the square wave frequency and the periodic interrupt output. However, each function has a separate enable bit in Register B. The SQWE bit controls the square wave output. Similarly, the periodic interrupt is enabled by the PIE bit in Register B. The periodic interrupt can be used with software counters to measure inputs, create output intervals or await the next needed software function.

UPDATE CYCLE

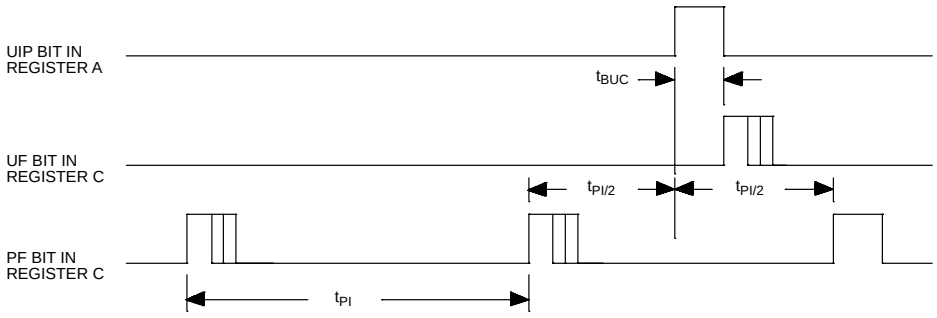
The DS1385/DS1387 executes an update cycle once per second regardless of the SET bit in Register B. When the SET bit in Register B is set to one, the user copy of the double buffered time, calendar and alarm bytes is frozen and will not update as the time increments. However, the time countdown chain continues to update the internal copy of the buffer. This feature allows time to maintain accuracy independent of reading or writing the time, calendar and alarm buffers and also guarantees that time and calendar information is consistent. The update cycle also compares each alarm byte with the corresponding time byte and issues an alarm if a match or if a “don’t care” code is present in all three positions.

There are three methods that can handle access of the real–time clock that avoid any possibility of accessing inconsistent time and calendar data. The first method uses the update–ended interrupt. If enabled, an interrupt occurs after every up date cycle that indicates that over 999 ms are available to read valid time and date information. If this interrupt is used, the IRQF bit in Register C should be cleared before leaving the interrupt routine.

A second method uses the update–in–progress bit (UIP) in Register A to determine if the update cycle is in progress. The UIP bit will pulse once per second. After the UIP bit goes high, the update transfer occurs 244 µs later. If a low is read on the UIP bit, the user has at least 244 µs before the time/calendar data will be changed. Therefore, the user should avoid interrupt service routines that would cause the time needed to read valid time/calendar data to exceed 244 µs.

The third method uses a periodic interrupt to determine if an update cycle is in progress. The UIP bit in Register A is set high between the setting of the PF bit in Register C (see Figure 3). Periodic interrupts that occur at a rate of greater than t_{BUC} allow valid time and date information to be reached at each occurrence of the periodic interrupt. The reads should be complete within ($t_{PI}/2+t_{BUC}$) to ensure that data is not read during the update cycle.

UPDATE–ENDED AND PERIODIC INTERRUPT RELATIONSHIP Figure 3



t_{PI} = Periodic interrupt time interval per Table 1.
t_{BUC} = Delay time before update cycle = 244 µs.

REGISTERS

The DS1385/DS1387 has four control registers which are accessible at all times, even during the update cycle.

REGISTER A

MSB							LSB
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
UIP	DV2	DV1	DV0	RS3	RS2	RS1	RS0

UIP – The Update In Progress (UIP) bit is a status flag that can be monitored. When the UIP bit is a one, the update transfer will soon occur. When UIP is a zero, the update transfer will not occur for at least 244 µs. The time, calendar and alarm information in RAM is fully available for access when the UIP bit is zero. The UIP bit is read only. Writing the SET bit in Register B to a one inhibits any update transfer and clears the UIP status bit.

DV2, DV1, DV0 – These three bits are used to turn the oscillator on or off and to reset the countdown chain. A pattern of 010 is the only combination of bits that will turn the oscillator on and allow the RTC to keep time. A pattern of 11X will enable the oscillator but holds the countdown chain in reset. The next update will occur at 500 ms after a pattern of 010 is written to DV2, DV1, and DV0.

RS3, RS2, RS1, RS0 – These four rate–selection bits select one of the 13 taps on the 15–stage divider or disable the divider output. The tap selected can be used to generate an output square wave (SQW pin) and/or a periodic interrupt. The user can do one of the following:

1. Enable the interrupt with the PIE bit;
2. Enable the SQW output pin with the SQWE bit;
3. Enable both at the same time and the same rate; or
4. Enable neither.

Table 2 lists the periodic interrupt rates and the square wave frequencies that can be chosen with the RS bits.

REGISTER B

MSB							LSB
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SET	PIE	AIE	UIE	SQWE	DM	24/12	DSE

SET – When the SET bit is a zero, the update transfer functions normally by advancing the counts once per second. When the SET bit is written to a one, any update transfer is inhibited and the program can initialize the time and calendar bytes without an update occurring in the midst of initializing. Read cycles can be executed in a similar manner. SET is a read/write bit that is not modified by internal functions of the DS1385/DS1387.

PIE – The Periodic Interrupt Enable bit is a read/write bit which allows the Periodic Interrupt Flag (PF) bit in Register C to drive the $\overline{IRQ}$ pin low. When the PIE bit is set to one, periodic interrupts are generated by driving the $\overline{IRQ}$ pin low at a rate specified by the RS3-RS0 bits of Register A. A zero in the PIE bit blocks the $\overline{IRQ}$ output from being driven by a periodic interrupt, but the Periodic Flag (PF) bit is still set at the periodic rate. PIE is not modified by any internal DS1385/DS1387 functions.

AIE – The Alarm Interrupt Enable (AIE) bit is a read/write bit which, when set to a one, permits the Alarm Flag (AF) bit in register C to assert $\overline{IRQ}$. An alarm interrupt occurs for each second that the three time bytes equal the three alarm bytes including a don't care alarm code of binary 11XXXXXX. When the AIE bit is set to zero, the AF bit does not initiate the $\overline{IRQ}$ signal. The internal functions of the DS1385/DS1387 do not affect the AIE bit.

UIE – The Update Ended Interrupt Enable (UIE) bit is a read/write bit that enables the Update End Flag (UF) bit in Register C to assert $\overline{IRQ}$. The SET bit going high clears the UIE bit.

SQWE – When the Square Wave Enable (SQWE) bit is set to a one, a square wave signal at the frequency set by the rate–selection bits RS3 through RS0 is driven out on a SQW pin. When the SQWE bit is set to zero, the SQW pin is held low. SQWE is a read/write bit.

DM – The Data Mode (DM) bit indicates whether time and calendar information is in binary or BCD format. The DM bit is set by the program to the appropriate format and can be read as required. This bit is not modified by internal functions. A one in DM signifies binary data while a zero in DM specifies Binary Coded Decimal (BCD) data.

24/12 – The 24/12 control bit establishes the format of the hours byte. A one indicates the 24–hour mode and a zero indicates the 12–hour mode. This bit is read/write.

DSE – The Daylight Savings Enable (DSE) bit is a read/write bit which enables two special updates when DSE is set to one. On the first Sunday in April the time increments from 1:59:59 AM to 3:00:00 AM. On the last Sunday in October when the time first reaches 1:59:59

AM it changes to 1:00:00 AM. These special updates do not occur when the DSE bit is a zero. This bit is not affected by internal functions.

REGISTER C

MSB							LSB
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
IRQF	PF	AF	UF	0	0	0	0

IRQF - The Interrupt Request Flag (IRQF) bit is set to a one when one or more of the following are true:

PF = PIE = 1
AF = AIE = 1
UF = UIE = 1
i.e., IRQF = (PF • PIE) + (AF • AIE) + (UF • UIE)
Any time the IRQF bit is a one, the $\overline{IRQ}$ pin is driven low. All flag bits are cleared after Register C is read by the program.

PF – The Periodic Interrupt Flag (PF) is a read–only bit which is set to a one when an edge is detected on the selected tap of the divider chain. The RS3 through RS0 bits establish the periodic rate. PF is set to a one independent of the state of the PIE bit. When both PF and PIE are ones, the $\overline{IRQ}$ signal is active and will set the IRQF bit. The PF bit is cleared by a software read of Register C.

AF – A one in the Alarm Interrupt Flag (AF) bit indicates that the current time has matched the alarm time. If the AIE bit is also a one, the $\overline{IRQ}$ pin will go low and a one will appear in the IRQF bit. A read of Register C will clear AF.

UF – The Update Ended Interrupt Flag (UF) bit is set after each update cycle. When the UIE bit is set to one, the one in UF causes the IRQF bit to be a one which will assert the $\overline{IRQ}$ pin. UF is cleared by reading Register C.

BIT 3 THROUGH BIT 0 – These are reserved bits of the status Register C. These bits always read zero and cannot be written.

REGISTER D

MSB							LSB
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
VRT	0	0	0	0	0	0	0

VRT – The Valid RAM and Time (VRT) bit is set to the one state by Dallas Semiconductor Corporation prior to shipment. This bit is not writable and should always be a one when read. If a zero is ever present, an exhausted internal lithium energy source is indicated and both the contents of the RTC data and RAM data are questionable.

BIT 6 THROUGH BIT 0 – The remaining bits of Register D are reserved and not usable. They cannot be written and, when read, they will always read zero.

4K X 8 RAM

The DS1385/DS1387 provides 4K x 8 of on–chip SRAM which is controlled as nonvolatile storage sustained from a lithium battery. On power–up, the RAM is taken out of write–protect status by the internal power OK signal (POK) generated from the write protect circuitry. The POK signal becomes active at 4.25 volts (typical).

The on–chip 4K x 8 nonvolatile SRAM is accessed via the eight multiplexed address/data lines AD7–AD0. Access to the SRAM is controlled by three on–chip latch registers. Two registers are used to hold the SRAM address and the third register is used to hold read/write data. The SRAM address space is from 000H to FFFH.

Four control signals, $\overline{AS0}$, $\overline{AS1}$, $\overline{OER}$, and $\overline{WER}$, are used to access the 4K x 8 SRAM. The address latches are loaded from the address/data bus in response to rising edge signals applied to the Address Strobe 0 ($\overline{AS0}$) and Address Strobe 1 ($\overline{AS1}$) signals. $\overline{AS0}$ is used to latch the lower 8–bits of address, and $\overline{AS1}$ is used to latch the upper 4–bits of address. It is necessary to meet the setup and hold times given in the Electrical Specifications with valid address information in order to properly latch the address. If the upper or lower order address is correct from a prior cycle, it is not necessary to repeat the address latching sequence.

A write operation requires valid data to be placed on the bus (AD7–AD0) followed by the activation of the Write Enable RAM ($\overline{WER}$) line. Data on the bus will be written to the RAM provided that the write timing specifications are met. During a read cycle, the Output Enable RAM ($\overline{OER}$) signal is driven active. Data from the RAM will become valid on the bus provided that the RAM read access timing specifications are met. The $\overline{WER}$ and $\overline{OER}$ signals should never be active at the same time. In addition, access to the clock/calendar registers and user RAM (via $\overline{CS}$) must not be attempted when the 4K x 8 RAM is being accessed. The RAM is enabled when either $\overline{WER}$ or $\overline{OER}$ is active. $\overline{CS}$ is only used for the access of the clock calendar registers (including the extended Dallas registers) and the 50–bytes of user RAM.

ABSOLUTE MAXIMUM RATINGS*

Voltage on any Pin Relative to Ground	–0.3V to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	DS1387: –40°C to +70°C DS1385: –55°C to +125°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Power Supply Voltage	V_{CC}	4.5	5.0	5.5	V	1
Input Logic 1	V_{IH}	2.2		V_{CC}+0.3	V	1
Input Logic 0	V_{IL}	–0.3		+0.8	V	1
Battery Voltage	V_{BAT}	2.5		3.7	V	9

DC ELECTRICAL CHARACTERISTICS

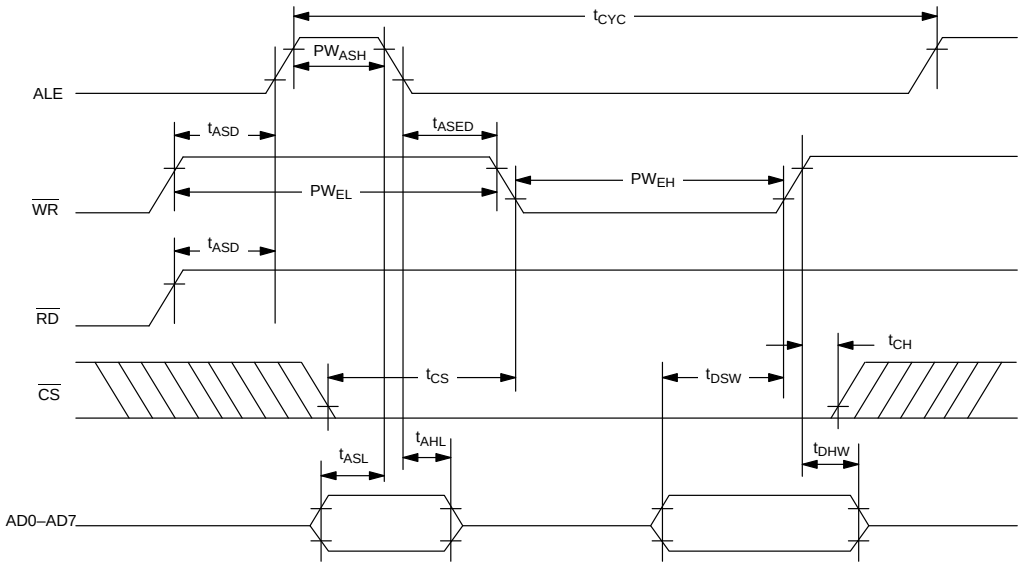
(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Power Supply Current	I_{CC1}		35	50	mA	2
Standby Current $\overline{CS}$, $\overline{OER}$ and $\overline{WER}$ = V_{CC} –0.3 volt	I_{CC2}		1	5.0	mA	6
Input Leakage	I_{IL}	–1.0		+1.0	µA	3
I/O Leakage	I_{LO}	–1.0		+1.0	µA	3
Output @ 2.4 volts	I_{OH}	–1.0			mA	1, 4
Output @ 0.4 volts	I_{OL}			2.0	mA	1

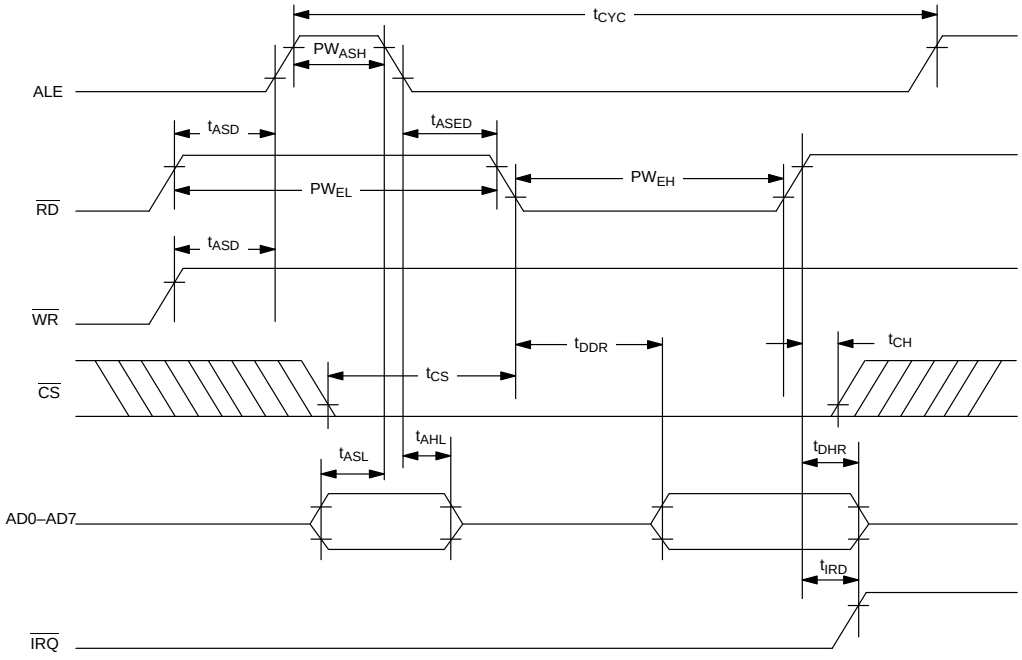
RTC AC TIMING CHARACTERISTICS (0°C to 70°C; V_{CC} = 4.5V to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Cycle Time	t_{CYC}	305		DC	ns	
Pulse Width, $\overline{RD}$/$\overline{WR}$ Low	PW_{EH}	125			ns	
Pulse Width, $\overline{RD}$/$\overline{WR}$ High	PW_{EL}	150			ns	
Input Rise and Fall Time	t_R, t_F			30	ns	
Chip Select Setup Time Before $\overline{WR}$ or $\overline{RD}$	t_{CS}	20			ns	
Chip Select Hold Time	t_{CH}	0			ns	
Read Data Hold Time	t_{DHR}	10		80	ns	
Write Data Hold Time	t_{DHW}	0			ns	
Muxed Address Valid Time to ALE Fall	t_{ASL}	30			ns	
Muxed Address Hold Time from ALE Fall	t_{AHL}	10			ns	
$\overline{RD}$ or $\overline{WR}$ High Setup to ALE Rise	t_{ASD}	25			ns	
Pulse Width ALE High	PW_{ASH}	60			ns	
ALE Low Setup to $\overline{RD}$ or $\overline{WR}$ Fall	t_{ASED}	40			ns	
Output Data Delay Time from $\overline{RD}$	t_{DDR}	20		120	ns	5
Data Setup Time to Write	t_{DSW}	100			ns	
$\overline{IRQ}$ Release from $\overline{RD}$	t_{IRD}			2	µs	

DS1385/DS1387 BUS TIMING FOR WRITE CYCLE TO RTC



DS1385/DS1387 BUS TIMING FOR READ CYCLE TO RTC

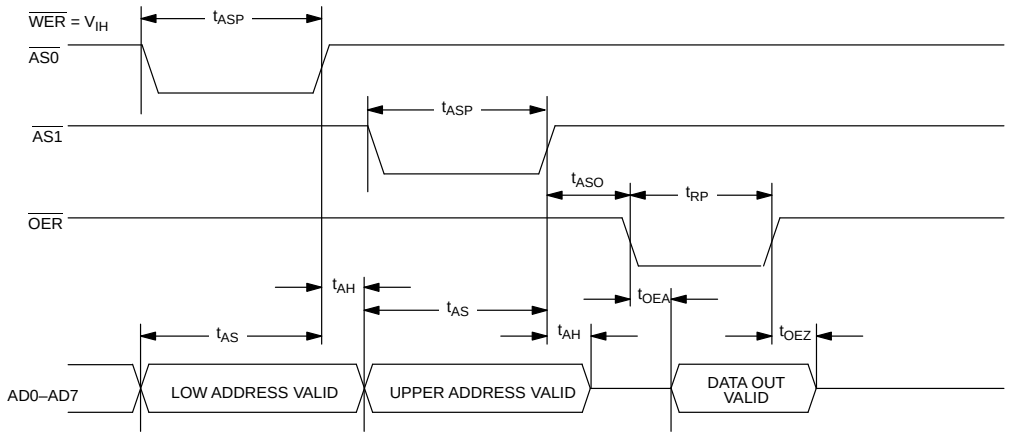


4K X 8 AC TIMING CHARACTERISTICS

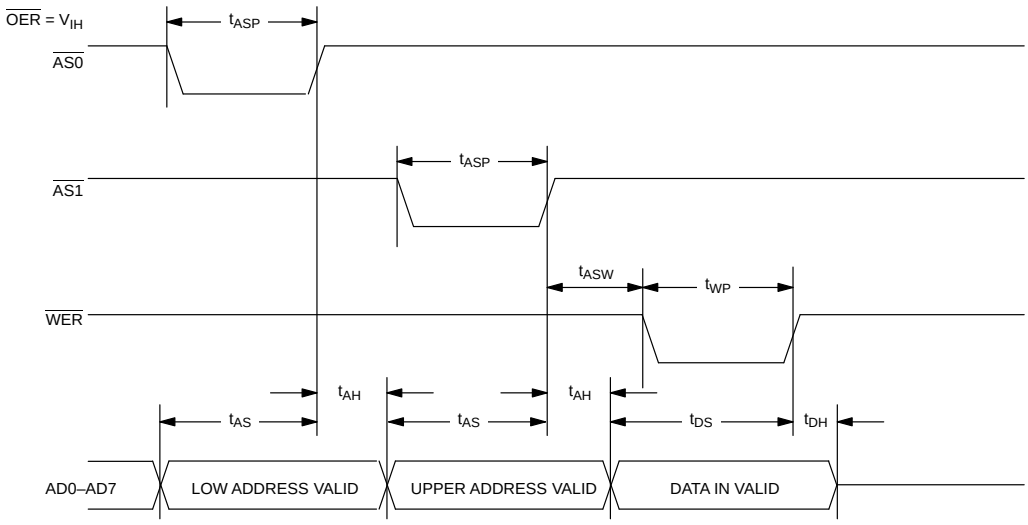
(0°C to 70°C; V_{CC} = 5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Address Setup Time	t_{AS}	55			ns	
Address Hold Time	t_{AH}	0			ns	
Data Setup Time	t_{DS}	75			ns	
Data Hold Time	t_{DH}	0			ns	
Output Enable Access Time	t_{OEA}			200	ns	7
Write Pulse Width	t_{WP}	200			ns	
$\overline{OER}$ Pulse Width	t_{RP}	200			ns	
$\overline{OER}$ to Output in High Z	t_{OEZ}			50	ns	
$\overline{AS0}$, $\overline{AS1}$ Pulse Width	t_{ASP}	75			ns	
$\overline{AS0}$, $\overline{AS1}$ High to $\overline{OER}$ Low	t_{ASO}	20			ns	
$\overline{AS0}$, $\overline{AS1}$ High to $\overline{WER}$ Low	t_{ASW}	20			ns	

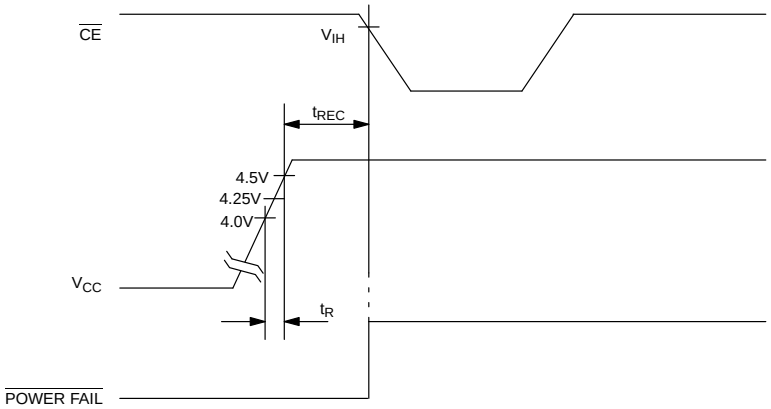
BUS TIMING FOR READ CYCLE TO 4K X 8 NV SRAM



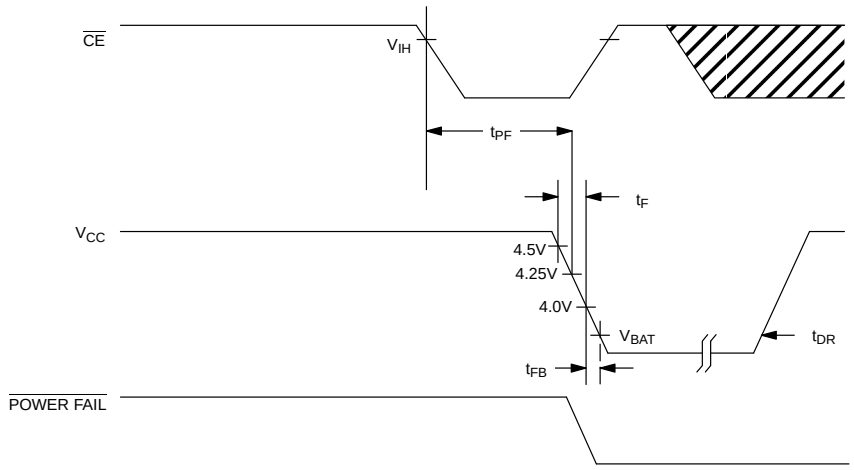
BUS TIMING FOR WRITE CYCLE TO 4K X 8 SRAM



POWER–UP CONDITION



POWER–DOWN CONDITION



POWER–UP POWER–DOWN TIMING

(t_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
$\overline{CE}$ High to Power Fail	t_{PF}			0	ns	
Recovery at Power Up	t_{REC}		150		ms	
V_{CC} Slew Rate Power Down	t_F 4.0 ≤V_{CC} ≤ 4.5V	300			µs	
V_{CC} Slew Rate Power Down	t_{FB} 3.0 ≤V_{CC}≤ 4.0V	10			µs	
V_{CC} Slew Rate Power Up	t_R 4.5V≥V_{CC}≥4.0V	0			µs	
Expected Data Retention	t_{DR}	10			years	8

WARNING:
Under no circumstances are negative undershoots, of any amplitude, allowed when device is in battery back–up mode.

CAPACITANCE

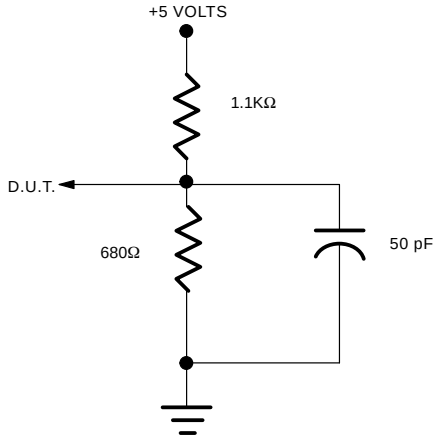
(t_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}			12	pF	
Output Capacitance	C_{OUT}			12	pF	

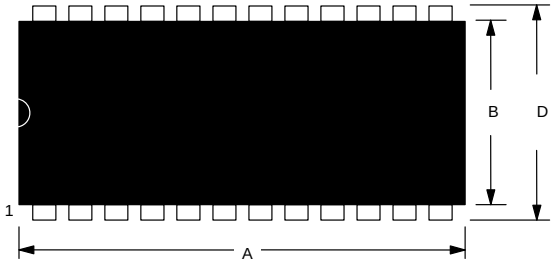
NOTES:

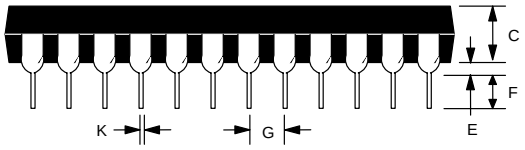
1. All voltages are referenced to ground.
2. All outputs are open.
3. Applies to the AD0–AD7 pins and the SQW pin when each is in the high impedance state.
4. The $\overline{IRQ}$ pin is open drain.
5. Measured with a load as shown in Figure 4.
6. All other inputs at CMOS levels.
7. Measured with a load as shown in Figure 4.
8. The real–time clock will keep time to an accuracy of ±1 minute per month during data retention time for the period of t_{DR}.
9. Applies to DS1385 and DS1385S only.

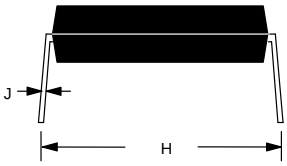
OUTPUT LOAD Figure 4



DS1385 24–PIN DIP

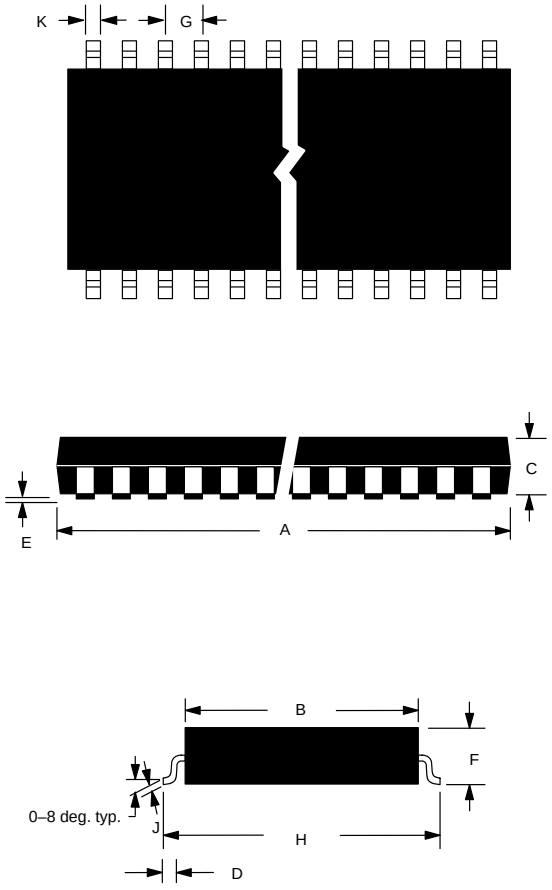






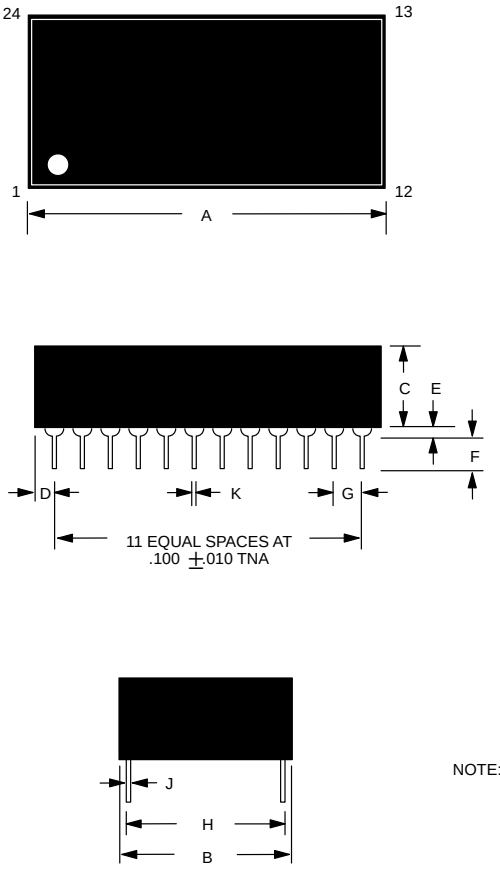
PKG	24–PIN	
DIM	MIN	MAX
A IN. MM	1.245 31.62	1.270 32.26
B IN. MM	0.530 13.46	0.550 13.97
C IN. MM	0.140 3.56	0.160 4.06
D IN. MM	0.600 15.24	0.625 15.88
E IN. MM	0.015 0.38	0.050 1.27
F IN. MM	0.120 3.05	0.145 3.68
G IN. MM	0.090 2.29	0.110 2.79
H IN. MM	0.625 15.88	0.675 17.15
J IN. MM	0.008 0.20	0.012 0.30
K IN. MM	0.015 0.38	0.022 0.56

DS1385S 28–PIN SOIC



PKG	28–PIN	
DIM	MIN	MAX
A IN. MM	0.706 17.93	0.728 18.49
B IN. MM	0.338 8.58	0.350 8.89
C IN. MM	0.086 2.18	0.110 2.79
D IN. MM	0.020 0.58	0.050 1.27
E IN. MM	0.002 0.05	0.014 0.36
F IN. MM	0.090 2.29	0.124 3.15
G IN. MM	0.050 1.27	BSC
H IN. MM	0.460 11.68	0.480 12.19
J IN. MM	0.006 0.15	0.013 0.33
K IN. MM	0.014 0.36	0.020 0.51

DS1387 24–PIN 740 MIL FLUSH ENCAPSULATED



PKG	24–PIN	
DIM	MIN	MAX
A IN. MM	1.320 33.53	1.335 33.91
B IN. MM	0.720 18.29	0.740 18.80
C IN. MM	0.345 8.76	0.370 9.40
D IN. MM	0.100 2.54	0.130 3.30
E IN. MM	0.015 0.38	0.030 0.89
F IN. MM	0.110 2.79	0.140 3.56
G IN. MM	0.090 2.29	0.110 2.79
H IN. MM	0.590 14.99	0.630 16.00
J IN. MM	0.008 0.20	0.012 0.30
K IN. MM	0.015 0.38	0.021 0.53

NOTE: PINS 2, 3, 16, AND 20 ARE MISSING BY DESIGN.