Features

- **Fastest Propagation Speeds in the Industry $T_{PD\ (F\ grade)}$ = 2.5 ns, $T_{PD\ (G\ grade)}$ = 2.0 ns**
- **Maximum Derating for Capacitive Loads 1.5ns/100pF (F grade) and 1.1ns/100pF (G grade)**
- **Very Low Ground Bounce <0.6V @ V_{CC}=5.00 V, T_a=25°C**
- **Excellent Noise Rejection**
- **Typical Output Skew ≤0.25ns**
- **Bus Hold Circuitry to Retain Last Active State During Tri-State™**
- **Available in SSOP and TSSOP Packages**

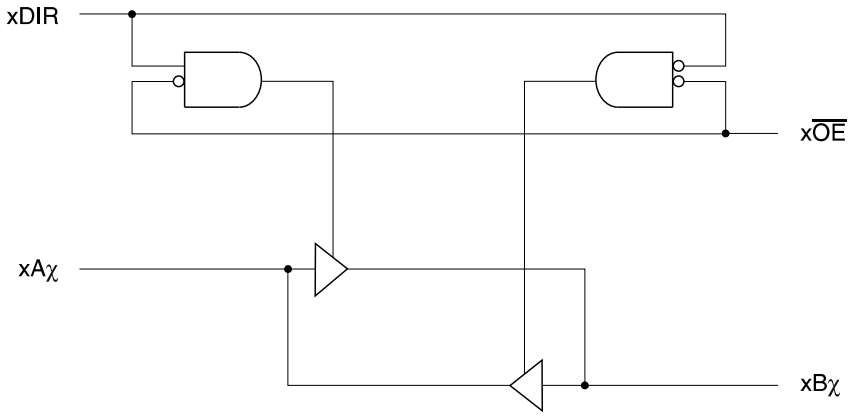
AT16245
Fast Logic™ Bi-Directional Transceiver

AT16245F
AT16245G

Description

Atmel's new family of high speed CMOS transceivers offers the best of all worlds to the user requiring stability and ultra fast speeds. These transceivers, which can function as two 8-bit devices or one 16-bit device, are capable of improving processing efficiency as much as 6% by reducing the number of wait states required during memory access. In addition, this family of parts has been designed to minimize ground bounce on the outputs while rejecting input spikes of up to 1.8V and 1 ns wide. This combination of ultra high speed and low noise is the next step in high speed performance.

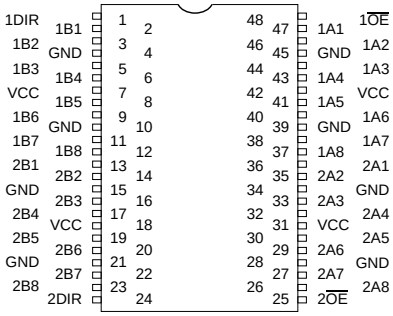
Functional Block Diagram



Pin Configurations

Pin Names	Descriptions
$x\overline{OE}$	Output Enable Input (Active Low)
xDIR	Direction Control Input
xAχ	Side A Inputs or Tri-State Outputs
xBχ	Side B Inputs or Tri-State Outputs

SSOP/TSSOP



Top View

0754B

Function Table

Inputs		Outputs
$x\overline{OE}$	xDIR	
L	L	Bus B Data to Bus A
L	H	Bus A Data to Bus B
H	X(1)	High Z State

Note: 1. X = Don't Care

Absolute Maximum Ratings*

Operating Temperature	0°C to +70°C
Storage Temperature	-65°C to +150°C
Voltage on any Pin with Respect to Ground	-2.0 V to +7.0V(1)
Maximum Operating Voltage	6.0V

NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Notes: 1. Minimum voltage is -0.6V dc which may undershoot to -2.0V for pulses of less than 20 ns. Maximum output pin voltage is VCC +0.75V dc which may overshoot to +7.0V for pulses of less than 20 ns.

5.0 Volt DC Characteristics

Applicable over recommended operating range from T_a=0°C to +70°C, V_{CC}=+5.0V ±5% (unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
ΔI_{CC}	Quiescent Power Supply Current	V_{CC}=Max, V_{IN}=3.4V		0.8	1.2	mA
V_{IH}	Input High Voltage		2.0			V
V_{IL}	Input Low Voltage				0.8	V
I_{IH}	Input High Current (I/O Pins)	V_{IN}=V_{CC}			±15	µA
I_{IL}	Input Low Current (I/O Pins)	V_{IN}= GND			±15	µA
I_{OZ}	Output Leakage Current				±10	µA
V_{OH}(1)	Output High Voltage F Grade only	V_{CC}=4.75 V I_{OH}=-10 mA	2.7			V
V_{OH}(2)	Output High Voltage G Grade only	V_{CC}=4.75 V I_{OH}=-12 mA	2.7			V
V_{OL}	Output Low Voltage (F Grade)	I_{OL}=10 mA			0.55	V
V_{OL}	Output Low Voltage (G Grade)	I_{OL} =12 mA			0.55	V

Note: 1. F grade: At $V_{CC(max),\ the\ value\ of\ VOH(max)}$ = 3.75V and at $V_{CC(min)}$, $V_{OH(max)}$ = 3.25V
2. G grade: At $V_{CC(max),\ the\ value\ of\ VOH(max)}$ = 3.75V and at $V_{CC(min)}$, $V_{OH(max)}$ = 3.35V

AC Characteristics
AT16245F

Applicable over recommended operating range from T_a=0°C to +70°C, V_{CC}=5.0V ±5% (unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
t_{PHL} t_{PLH}	Propagation Delay	CL=50 pF			2.5	ns
t_{PZH} t_{PZL}	Output Enable Time	CL=50 pF			6.0	ns
t_{PHZ} t_{PLZ}	Output Disable Time	CL=50 pF			6.0	ns
t_{SK}(1)	Output Skew	CL=50 pF			0.5	ns
Δt_{PHL}(1) Δt_{PLH}	Propagation Delay vs Output Loading			1.3	1.5	ns/100pF

Note: 1. This parameter is guaranteed but not 100% tested.

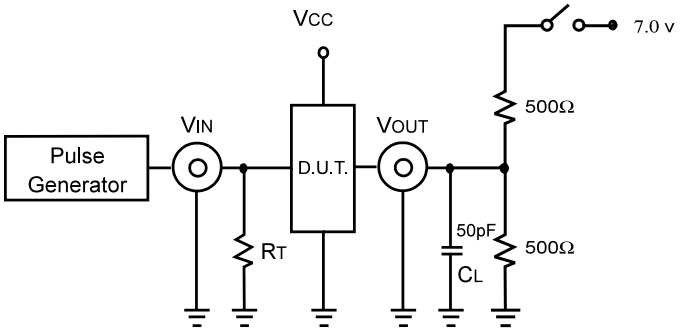
AT16245G

Applicable over recommended operating range from T_a=0°C to +70°C, V_{CC}=5.0V ±5% (unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
T_{PHL} T_{PLH}	Propagation Delay	CL=50 pF			2.0	ns
T_{PZH} T_{PZL}	Output Enable Time	CL=50 pF			6.0	ns
T_{PHZ} T_{PLZ}	Output Disable Time	CL=50 pF			5.0	ns
T_{SK}(1)	Output Skew	CL=50 pF			0.5	ns
Δt_{PHL}(1) Δt_{PLH}	Propagation Delay vs Output Loading			0.9	1.1	ns/100pF

Note: 1. This parameter is guaranteed but not 100% tested.

Test Circuits(1,2)



Note: 1. Pulse Generator: Rate ≤ 1.0 MHz, t_F ≤2.5 ns, t_R ≤ 2.5 ns.
2. AC tests are done with a single bit switching, and timings need to be derated when multiple outputs are switching in the same direction simultaneously. This derating should not exceed 0.5 ns for 16 inputs switching simultaneously.

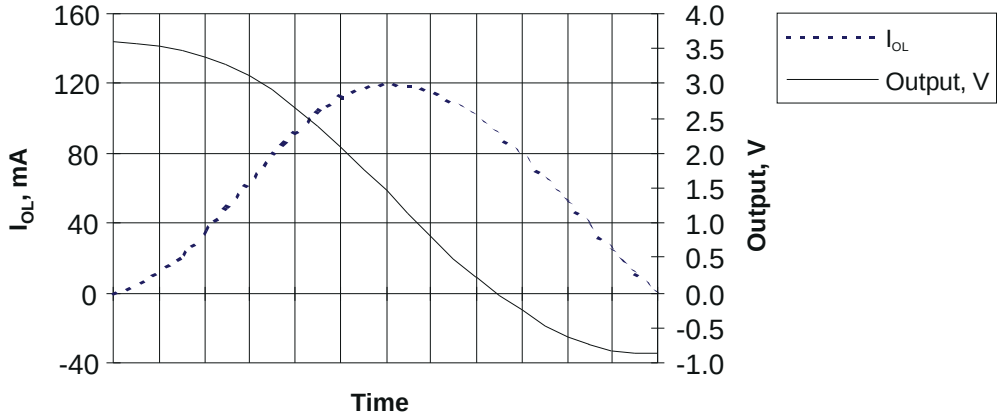
Switch Position

Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

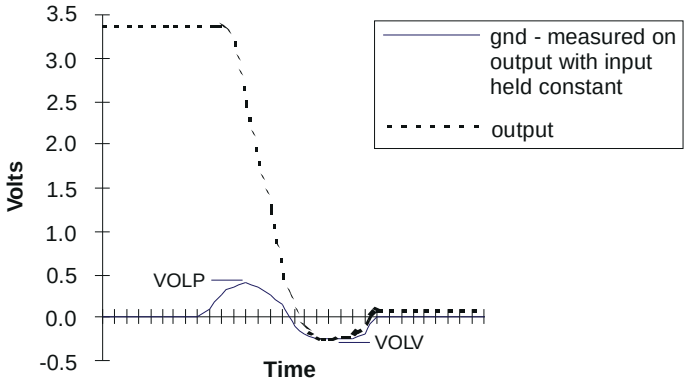
Definitions:

C_L = Load capacitance; Includes jig and probe capacitance.
R_T = Termination resistance; Should be equal to Z_{OUT} of the Pulse Generator.

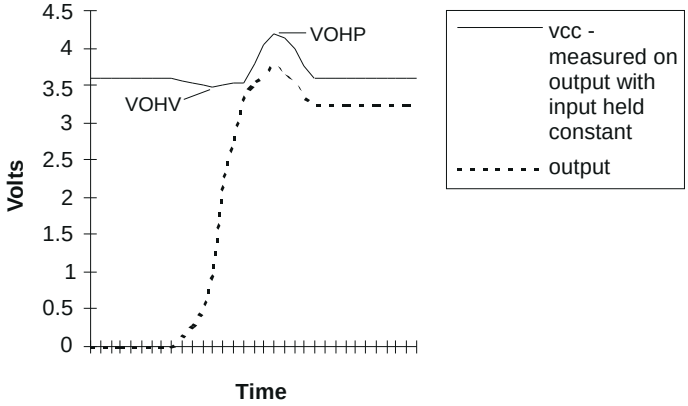
IOL Pull Down Current



Ground Bounce for High to Low Transitions(1)



Supply Bounce for Low to High Transitions(2)



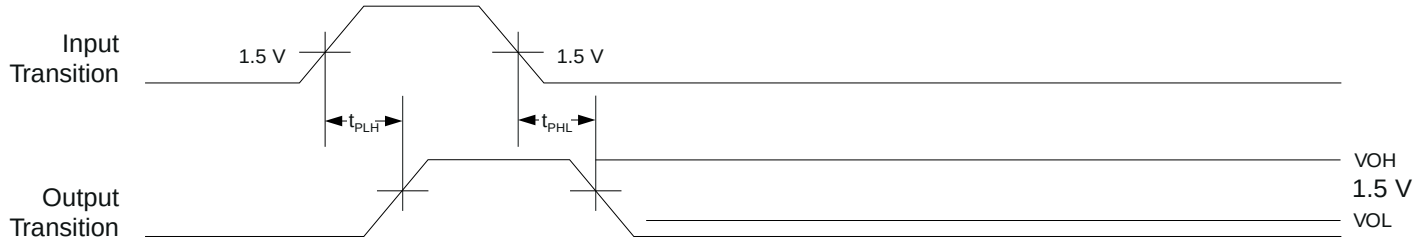
Typical Values

Parameter	Value	Units
V_{OLP}	0.4	V
V_{OLV}	-0.26	V
V_{OHV}	V_{CC} - 0.13	V
V_{OHP}	V_{CC} + 0.6	V

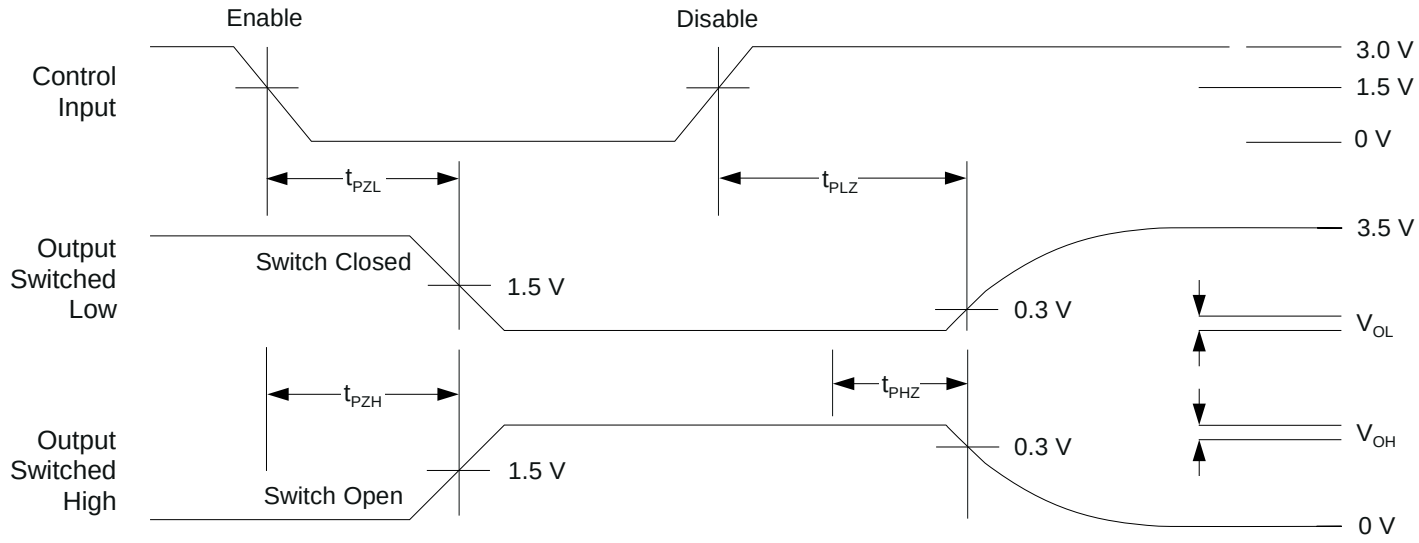
Note: 1. When multiple outputs are switched at the same time, rapidly changing current on the ground and V_{CC} paths cause a voltage to develop across the parasitic inductance of the wire bond and package pins. This occurrence is called simultaneous switching noise. Atmel's AT16245 products have minimized this phenomenon as shown on the graph. Output data is for 15 outputs switching simultaneously at a frequency of 1 MHz. The ground data is measured on the one remaining output, which is set to logic low and will reflect any device ground movement.

2. As on the graph for Ground Bounce, a similar condition occurs for low to high transitions. Output data is for 15 outputs switching simultaneously at a frequency of 1 MHz. V_{CC} droop is measured on the one remaining output pin, which is set to a logic high. This output will reflect any movement on the device V_{CC}.

Propagation Delay Waveforms



Enable and Disable Waveforms(1)



Note: 1. Enable and disable waveforms are the same for both x$\overline{OE}$ and xDIR inputs.

Ordering Information

T_{PD}	Ordering Code	Package	Operation Range
2.5 ns	AT16245F - 25YC AT16245F - 25XC	48Y 48X	Commercial
2.0 ns	AT16245G - 20YC AT16245G - 20XC	48Y 48X	Commercial

Package Type	
48X	48 Pin, Plastic Thin Shrink Small Outline Package (TSSOP)
48Y	48 Pin, Plastic Shrink Small Outline Package (SSOP)