

### P-CHANNEL MOS FIELD EFFECT TRANSISTOR FOR SWITCHING

#### DESCRIPTION

The  $\mu$ PA1811 is a switching device which can be driven directly by a 2.5-V power source.

The  $\mu$ PA1811 features a low on-state resistance and excellent switching characteristics, and is suitable for applications such as power switch of portable machine and so on.

#### FEATURES

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- Can be driven by a 2.5- V power source
- Low on-state resistance  $R_{DS(on)1} = 75 \text{ m}\Omega \text{ MAX.}$  (Vgs = -4.5 V, ID = -2.0 A)  $R_{DS(on)2} = 80 \text{ m}\Omega \text{ MAX.}$  (Vgs = -4.0 V, ID = -2.0 A)  $R_{DS(on)3} = 120 \text{ m}\Omega \text{ MAX.}$  (Vgs = -2.5 V, ID = -2.0 A)

#### **ORDERING INFORMATION**

PART NUMBER	PACKAGE		
μPA1811GR-9JG	Power TSSOP8		

#### ABSOLUTE MAXIMUM RATINGS (TA = 25°C)

Drain to Source Voltage	VDSS	-20	V
Gate to Source Voltage	Vgss	-12/+6	V
Drain Current (DC)	ID(DC)	±4.0	А
Drain Current (pulse) <sup>Note1</sup>	D(pulse)	±16	А
Total Power Dissipation Note2	P⊤	2.0	W
Channel Temperature	Tch	150	°C
Storage Temperature	Tstg	–55 to +150	°C

# 4 :Gate 1.0±0.05

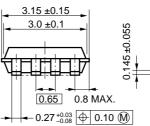
PACKAGE DRAWING (Unit : mm)

1, 5, 8 : Drain

2, 3, 6, 7: Source

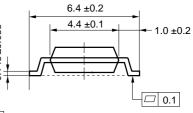


1.2 MAX.

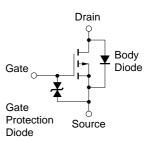


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#### **EQUIVALENT CIRCUIT**



**Notes 1.** PW  $\leq$  10  $\mu$ s, Duty Cycle  $\leq$  1 %

- 2. Mounted on ceramic substrate of 5000 mm<sup>2</sup> x 1.1 mm
- **Remark** The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

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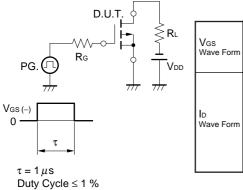
#### ELECTRICAL CHARACTERISTICS (TA = 25 °C)

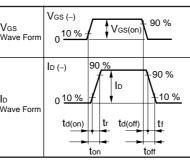
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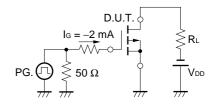
CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	IDSS	$V_{DS} = -20 V$ , $V_{GS} = 0 V$			-10	μA
Gate Leakage Current	lgss	$V_{GS} = \pm 12 V$ , $V_{DS} = 0 V$			±10	μA
Gate Cut-off Voltage	V <sub>GS(off)</sub>	$V_{DS} = -10 V$ , $I_{D} = -1 mA$	-0.5	-0.9	-1.5	V
Forward Transfer Admittance	y <sub>fs</sub>	$V_{DS} = -10 V$ , $I_D = -2.0 A$	2.5	6.8		S
Drain to Source On-state Resistance	RDS(on)1	$V_{GS} = -4.5 V$ , $I_D = -2.0 A$		42	75	mΩ
	RDS(on)2	$V_{GS} = -4.0 \text{ V}, \text{ Id} = -2.0 \text{ A}$		46	80	mΩ
	RDS(on)3	$V_{GS} = -2.5 V$ , $I_D = -2.0 A$		73	120	mΩ
Input Capacitance	Ciss	V <sub>DS</sub> = -10 V		1160		pF
Output Capacitance	Coss	V <sub>GS</sub> = 0 V		680		pF
Reverse Transfer Capacitance	Crss	f = 1 MHz		210		pF
Turn-on Delay Time	td(on)	$V_{DD} = -10 V$		40		ns
Rise Time	tr	ID = -2.0 A		100		ns
Turn-off Delay Time	td(off)	$V_{GS(on)} = -4.0 V$		90		ns
Fall Time	tr	R <sub>G</sub> = 5 Ω		60		ns
Total Gate Charge	Q <sub>G</sub>	$V_{DD} = -10 V$		36		nC
Gate to Source Charge	Q <sub>GS</sub>	ID = -4.0 A		5		nC
Gate to Drain Charge	Qgd	Vgs = -4.0 V		16		nC
Diode Forward Voltage	VF(S-D)	IF = 4.0 A, VGS = 0 V		0.74		V
Reverse Recovery Time	trr	IF = 4.0 A, VGS = 0 V		77		ns
Reverse Recovery Charge	Qrr	di/dt = 100 A/µS		69		nC

#### **TEST CIRCUIT 1 SWITCHING TIME**





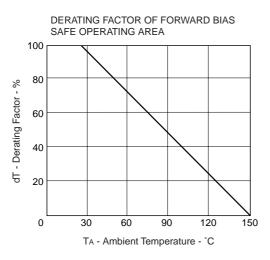
#### **TEST CIRCUIT 2 GATE CHARGE**

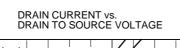


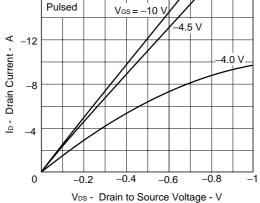


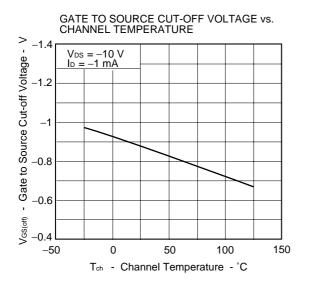
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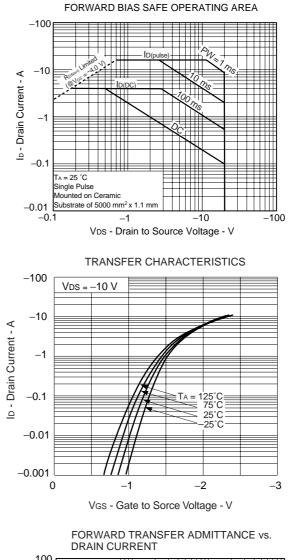


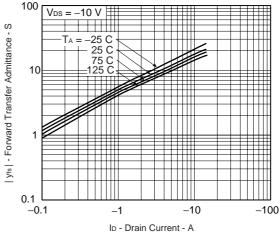


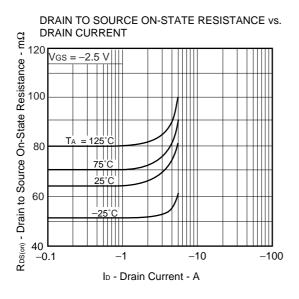


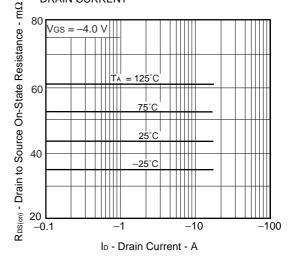








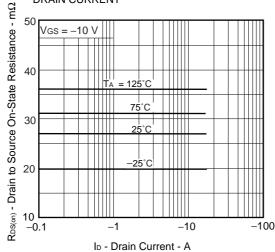


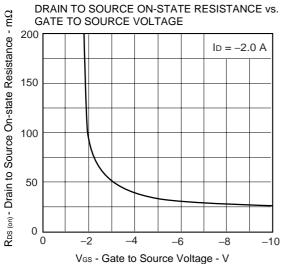


DRAIN TO SOURCE ON-STATE RESISTANCE vs.

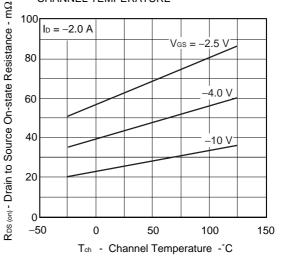
DRAIN CURRENT

DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT

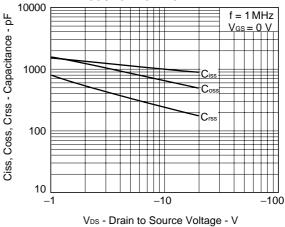




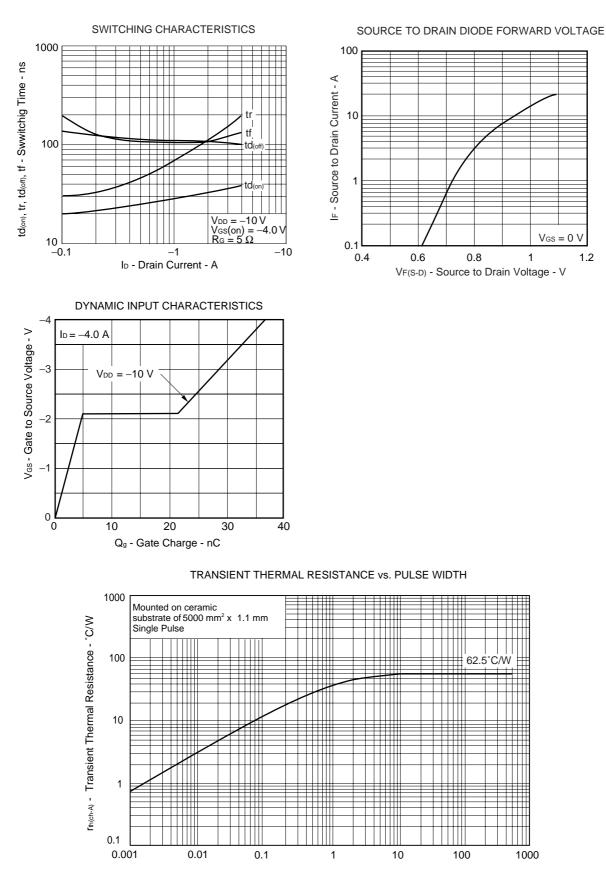




CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



Data Sheet D11820EJ1V0DS00



PW - Pulse Width - s

Data Sheet D11820EJ1V0DS00

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