

# DATA SHEET

## **PCA8550**

4-bit multiplexed/1-bit latched 5-bit I<sup>2</sup>C  
EEPROM

Product specification

1998 Sep 29

4-bit multiplexed/1-bit latched 5-bit I<sup>2</sup>C EEPROM

PCA8550

## FEATURES

- 4-bit 2-to-1 multiplexer, 1-bit latch
- 5-bit internal non-volatile register
- Override input forces all outputs to logic 0
- Internal non-volatile register write/readable via I<sup>2</sup>C bus
- Write-protect pin enables/disables I<sup>2</sup>C writes to register
- 2.5V multiplexed outputs
- 3.3V non-multiplexed output (latched)
- 5V tolerant inputs
- Useful for 'jumperless' configuration of PC motherboards
- Designed for use in Pentium Pro/Pentium II™ systems

Pentium II is a registered trademark of Intel Corporation

## DESCRIPTION

The primary function of the 4-bit 2-to-1 I<sup>2</sup>C multiplexer is to select either a 4-bit input or data from a non-volatile register and drive this value onto the output pins. One additional non-multiplexed register output is also provided. The non-multiplexed output is latched to prevent output value changes during I<sup>2</sup>C writes to the non-volatile register. A write protect input is provided to enable/disable the ability to write to the non-volatile register. An "override" input feature forces all outputs to logic 0.

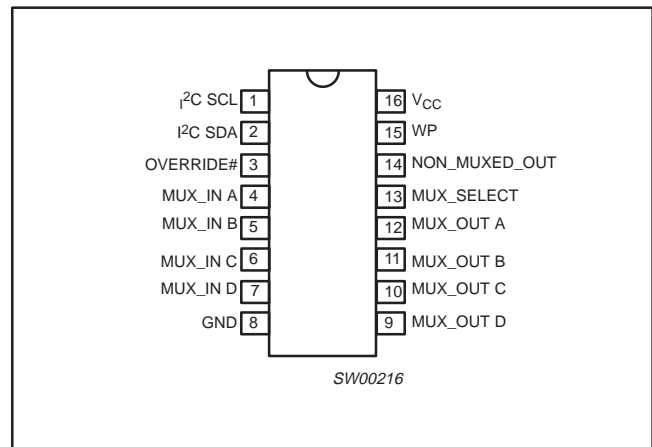
## ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DRAWING NUMBER
16-Pin Plastic SO	0°C to +70°C	PCA8550D	PCA8550D	SOT109-1
16-Pin Plastic SSOP	0°C to +70°C	PCA8550DB	PCA8550DB	SOT338-1
16-Pin Plastic TSSOP	0°C to +70°C	PCA8550PW	PCA8550PW DH	SOT403-1

## FUNCTIONAL DESCRIPTION

When the MUX\_SELECT signal is logic 0, the multiplexer will select the data from the non-volatile register to drive on the MUX\_OUT pins. When the MUX\_SELECT signal is logic 1, the multiplexer will select the MUX\_IN lines to drive on the MUX\_OUT pins. The MUX\_SELECT signal is also used to latch the NON\_MUXED\_OUT signal which outputs data from the non-volatile register. The NON\_MUXED\_OUT signal latch is transparent when MUX\_SELECT is in a logic 0 state, and will latch data when MUX\_SELECT is in a logic 1 state. When the active-LOW OVERRIDE# signal is set to logic 0 and the MUX\_SELECT signal is at a logic 0, all outputs will be driven to logic 0. This information is summarized in Table 1.

## PIN CONFIGURATION



The write protect (WP) input is used to control the ability to write the contents of the 5-bit non-volatile register. If the WP signal is logic 0, the I<sup>2</sup>C bus will be able to write the contents of the non-volatile register. If the WP signal is logic 1, data will not be allowed to be written into the non-volatile register.

The factory default for the contents of the non-volatile register are all logic 0. These stored values can be read or written using the I<sup>2</sup>C bus (described in the next section).

The OVERRIDE#, WP, MUX\_IN, and MUX\_SELECT signals have internal pullup resistors. See the DC and AC Characteristics for hysteresis and signal spike suppression figures.

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## PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1	I <sup>2</sup> C SCL	I <sup>2</sup> C bus clock
2	I <sup>2</sup> C SDA	Bi-directional I <sup>2</sup> C bus data
3	OVERRIDE#	Forces all outputs to logic 0
4	MUX_IN A	External inputs to multiplexer
5	MUX_IN B	
6	MUX_IN C	
7	MUX_IN D	
8	GND	Common ground voltage rail
9	MUX_OUT D	2.5V multiplexed output
10	MUX_OUT C	
11	MUX_OUT B	
12	MUX_OUT A	
13	MUX_SELECT	Selects MUX_IN inputs or register contents for MUX_OUT outputs
14	NON_MUXED_OUT	TTL-level output from non-volatile memory
15	WP	Non-volatile register write-protect
16	V <sub>CC</sub>	Positive voltage rail

## FUNCTION TABLE

Table 1. Function table

OVERRIDE #	MUX_SELECT	MUX_OUT OUTPUTS	NON_MUXED_OUT OUTPUT
0	0	All 0's	All 0's
0	1	MUX_IN inputs	Latched NON_MUXED_OUT <sup>1</sup>
1	0	From non-volatile register	From non-volatile register
1	1	MUX_IN inputs	From non-volatile register

### NOTE

1. Latched NON\_MUXED\_OUT state will be the value present on the NON\_MUXED\_OUT output at the time of the MUX\_SELECT input transitioned from a logic 0 to a logic 1 state.

## I<sup>2</sup>C Interface

Communicating with this device is initiated by sending a valid address on the I<sup>2</sup>C bus. The address format (see Figure 1) is a fixed unique 7-bit value followed by a 1-bit read/write value which determines the direction of the data transfer.

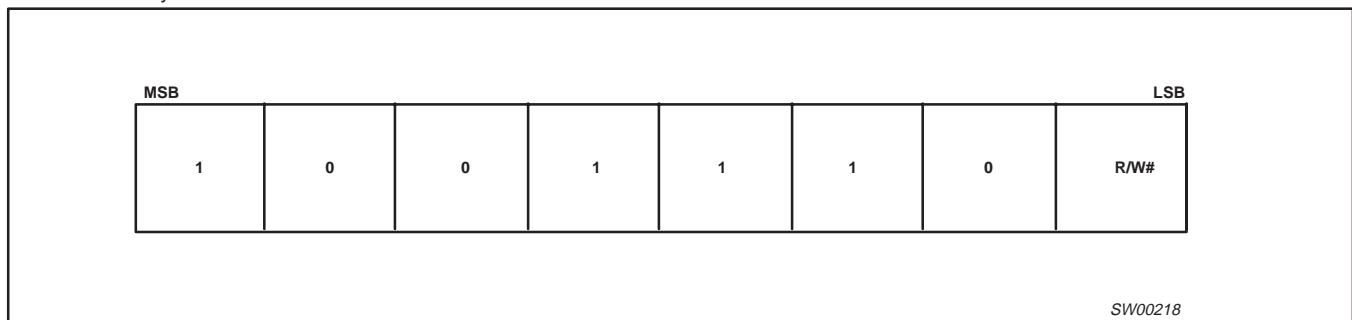


Figure 1. I<sup>2</sup>C Address Byte

Following the address and acknowledge bit are 8 data bits which, depending on the read/write bit in the address, will read data from or write data to the non-volatile register. Data will be written to the register if the read/write bit is logic 0 and the WP input is logic 0. Data will be read from the register if the bit is logic 1. The three high-order bits (see Figure 2) are logic 0. The next bit is data which is non-multiplexed. The low four bits are the data which will be multiplexed. A write with any of the first three bits non-zero will be aborted.

### NOTE:

1. To ensure data integrity, the non-volatile register must be internally write protected when V<sub>CC</sub> to the I<sup>2</sup>C bus is powered down or V<sub>CC</sub> to the component is dropped below normal operating levels.

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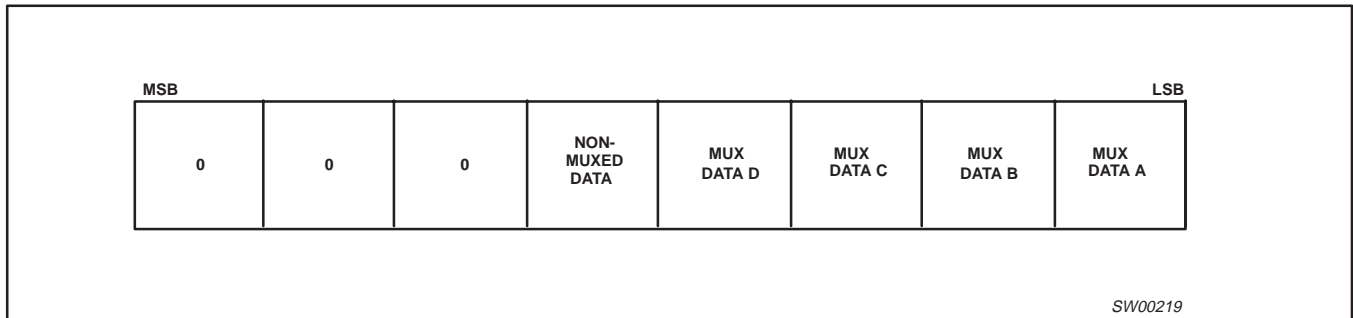
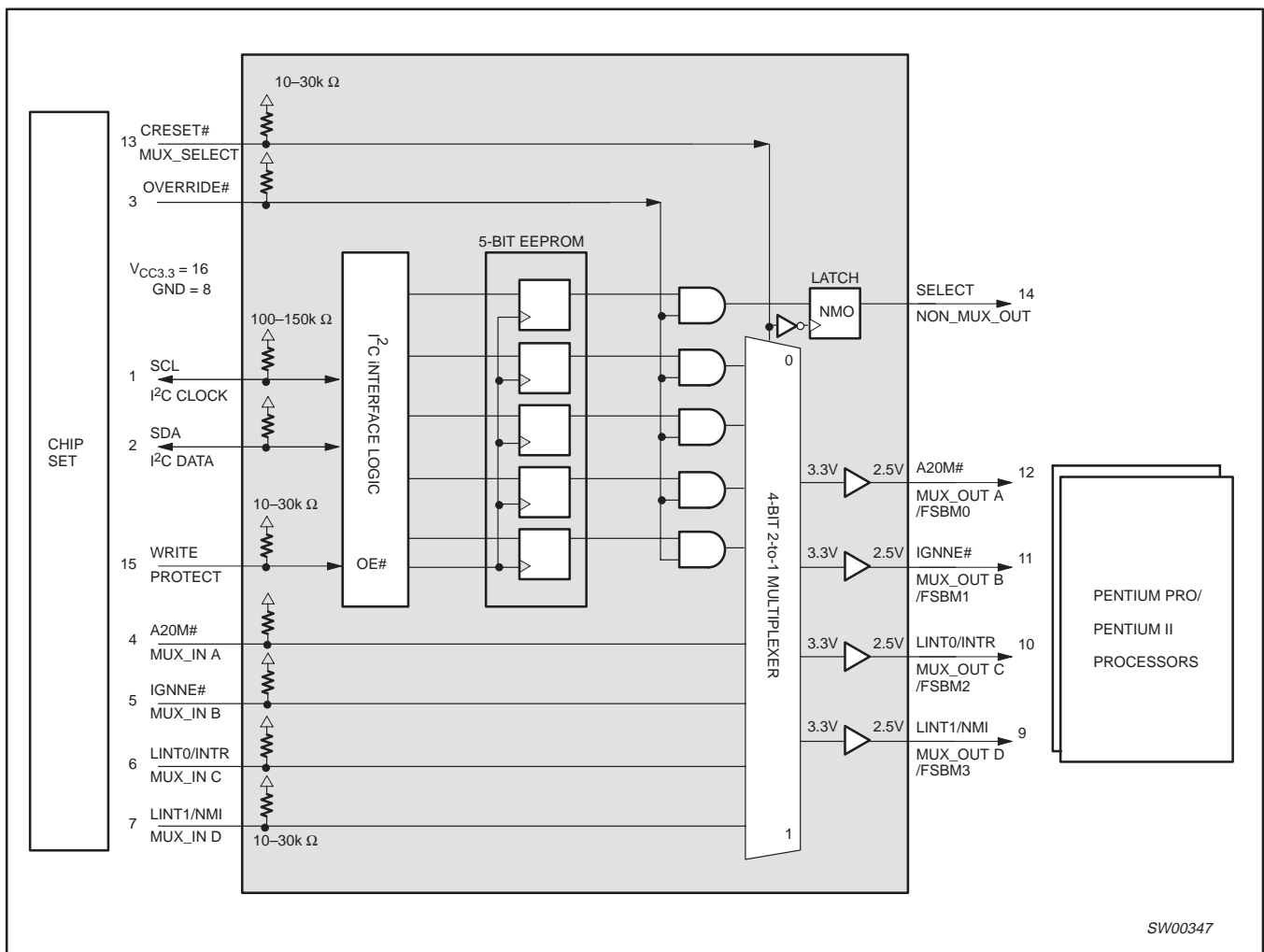


Figure 2. I<sup>2</sup>C Data Byte

## BLOCK DIAGRAM



4-bit multiplexed/1-bit latched 5-bit I<sup>2</sup>C EEPROM

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**ABSOLUTE MAXIMUM RATINGS<sup>1, 2</sup>**

In accordance with the Absolute Maximum Rating System (IEC 134)

Voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V <sub>CC</sub>	DC supply voltage		-0.5 to +4.6	V
V <sub>I</sub>	DC input voltage	Note 3	-1.5 to V <sub>CC</sub> +1.5	V
V <sub>OUT</sub>	DC output voltage	Note 3	-0.5 to V <sub>CC</sub> +0.5	V
T <sub>stg</sub>	Storage temperature range		-60 to +150	°C

**NOTES:**

- Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
- The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

**RECOMMENDED OPERATING CONDITIONS**

SYMBOL	PARAMETER	CONDITIONS	LIMITS		UNIT
			MIN	MAX	
V <sub>CC</sub>	DC supply voltage		3.0	3.6	V
SCL, SDA	V <sub>IL</sub> V <sub>IH</sub> V <sub>OL</sub>	I <sub>OL</sub> = 3mA	-0.5 2.7	0.9 4.0 0.4	V
VERRIDE#, MUX_IN, MUX_SELECT	V <sub>IL</sub> V <sub>IH</sub>		-0.5 2.0	0.8 4.0	V
MUX_OUT, NON_MUXED_OUT	I <sub>OL</sub> I <sub>OH</sub>			2.0 -2.0	mA
dt/dv	Input transition rise or fall time		0	10	ns/V
T <sub>A</sub>	Operating temperature		0	70	°C

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## DC CHARACTERISTICS

SYMBOL	PARAMETER	LIMITS		UNIT
		Temp = 0°C to +70°C 3.0V < V <sub>CC</sub> ≤ 3.6V		
		MIN	MAX	
SCL, SDA	V <sub>OL</sub>	0	0.6	V
	I <sub>OL</sub> (V <sub>OL</sub> = 0.4V)		3.0	mA
	I <sub>OL</sub> (V <sub>OL</sub> = 0.6V)		6.0	mA
	I <sub>IL</sub> (V <sub>IL</sub> = 0.4V)	-7	-32	μA
	I <sub>IH</sub> (V <sub>IH</sub> = 2.4V)	-1.5	-12	μA
	V <sub>HYS</sub> <sup>1</sup>	0.19		V
OVERRIDE#, WP, MUX_SELECT	I <sub>IL</sub>	-86	-267	μA
	I <sub>IH</sub>	-20	-100	μA
MUX A ⇒ D	I <sub>IL</sub> (V <sub>IL</sub> = 0.4V) I <sub>IH</sub> (V <sub>IH</sub> = 2.4V)	-0.72 -0.166	-2.0 -0.75	mA
MUX_OUT	V <sub>OL</sub> (I <sub>OL</sub> = 100μA)	-0.3	0.4	V
	V <sub>OL</sub> (I <sub>OL</sub> = 2.0mA)	-0.3	0.7	
	V <sub>OH</sub> (I <sub>OH</sub> = -100μA)	2.0	2.625	
	V <sub>OH</sub> (I <sub>OH</sub> = -1.0mA)	1.7	2.625	
NON_MUXED_OUT	V <sub>OL</sub> (I <sub>OL</sub> = 100μA)	-0.5	0.4	V
	V <sub>OL</sub> (I <sub>OL</sub> = 2.0mA)	-0.5	0.7	
	V <sub>OH</sub> (I <sub>OH</sub> = -100μA)	2.4	3.6	
	V <sub>OH</sub> (I <sub>OH</sub> = -2.0mA)	2.0	3.6	
I <sub>CC</sub>	Quiescent supply current (V <sub>CC</sub> = 3.3V) V <sub>I</sub> = 0V to V <sub>CC</sub>		10	mA
I <sub>CC</sub>	Quiescent supply current V <sub>I</sub> = V <sub>CC</sub>		500	μA
C <sub>IN</sub>	All inputs		10	pF
	ESD protection	2.0		KV
	Input diode clamp voltage	-1.5		V

## NOTES:

- V<sub>HYS</sub> is the hysteresis of Schmitt-Trigger inputs
- Human body model

## NON-VOLATILE STORAGE SPECIFICATIONS

Parameter	Specification
Memory cell data retention	10 years min
Number of memory cell write cycles	1,000 cycles min

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## AC CHARACTERISTICS

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
T <sub>MPD</sub>	Mux input to output propagation delay		20.0	ns
T <sub>SOV</sub>	MUX_SELECT to output valid		22	ns
T <sub>OVN</sub>	OVERRIDE# to NON_MUX output delay		15.0	ns
T <sub>OVM</sub>	OVERRIDE# to mux output delay		25.0	ns
T <sub>R</sub>	Output rise time	1.0	3.0	ns/V
T <sub>F</sub>	Output fall time	1.0	3.0	ns/V
C <sub>L</sub>	Test load capacitance on Muxed/Non-Muxed outputs		15	pF
	I <sup>2</sup> C BUS			
f <sub>SCL</sub>	I <sup>2</sup> C clock frequency	10	400	KHz
T <sub>SCH</sub>	I <sup>2</sup> C clock high time	600		ns
T <sub>SCL</sub>	I <sup>2</sup> C clock low time	1.3		ns
T <sub>DSP</sub>	I <sup>2</sup> C data spike time	0	50	ns
T <sub>SDS</sub>	I <sup>2</sup> C data setup time	100		ns
T <sub>SDH</sub>	I <sup>2</sup> C data hold time	0		ns
T <sub>ICR</sub>	I <sup>2</sup> C input rise time (10–400pF bus)	20	300	ns
T <sub>ICF</sub>	I <sup>2</sup> C input fall time (10–400pF bus)	20	300	ns
T <sub>BUF</sub>	I <sup>2</sup> C bus free time between start and stop	1.3		ns
T <sub>STS</sub>	I <sup>2</sup> C repeated start condition setup	600		ns
T <sub>STH</sub>	I <sup>2</sup> C repeated start condition hold	600		ns
T <sub>SPS</sub>	I <sup>2</sup> C stop condition setup	600		ns
C <sub>B</sub>	I <sup>2</sup> C bus capacitive load		400	pF
T <sub>W</sub>	Write cycle time <sup>1</sup>	TYPICAL = 15		ms

## NOTE:

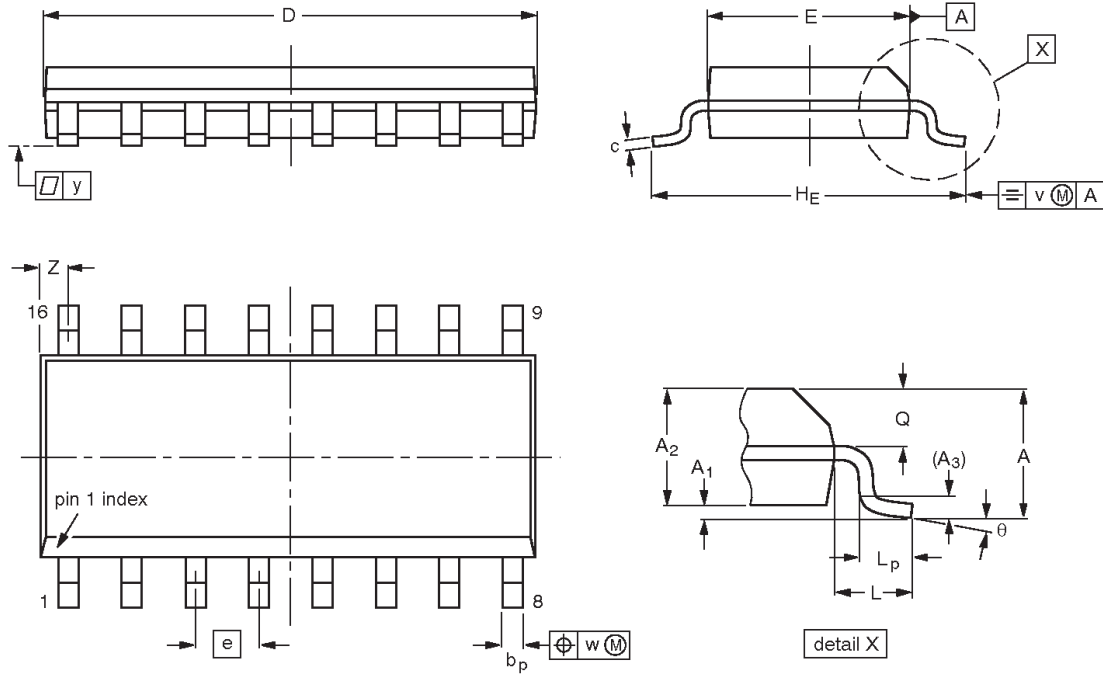
1. WRITE CYCLE time can only be measured indirectly during write cycle. The device will not acknowledge its I<sup>2</sup>C address.

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SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1



**DIMENSIONS (inch dimensions are derived from the original mm dimensions)**

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z <sup>(1)</sup>	θ
mm	1.75 0.10	0.25 1.25	1.45 0.049	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069 0.004	0.010 0.049	0.057 0.014	0.01	0.019 0.014	0.0100 0.0075	0.39 0.38	0.16 0.15	0.050	0.244 0.228	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

**Note**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT109-1	076E07S	MS-012AC				95-01-23 97-05-22

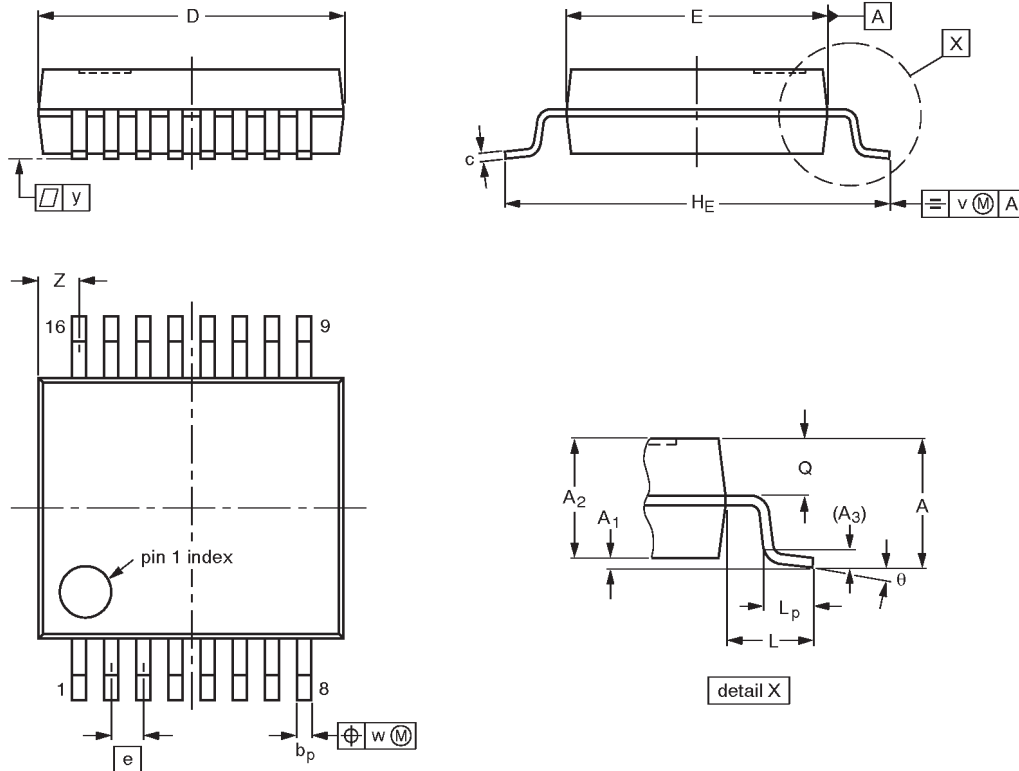


4-bit multiplexed/1-bit latched 5-bit I<sup>2</sup>C EEPROM

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SSOP16: plastic shrink small outline package; 16 leads; body width 5.3 mm

SOT338-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z <sup>(1)</sup>	θ
mm	2.0	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	6.4 6.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.00 0.55	8° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

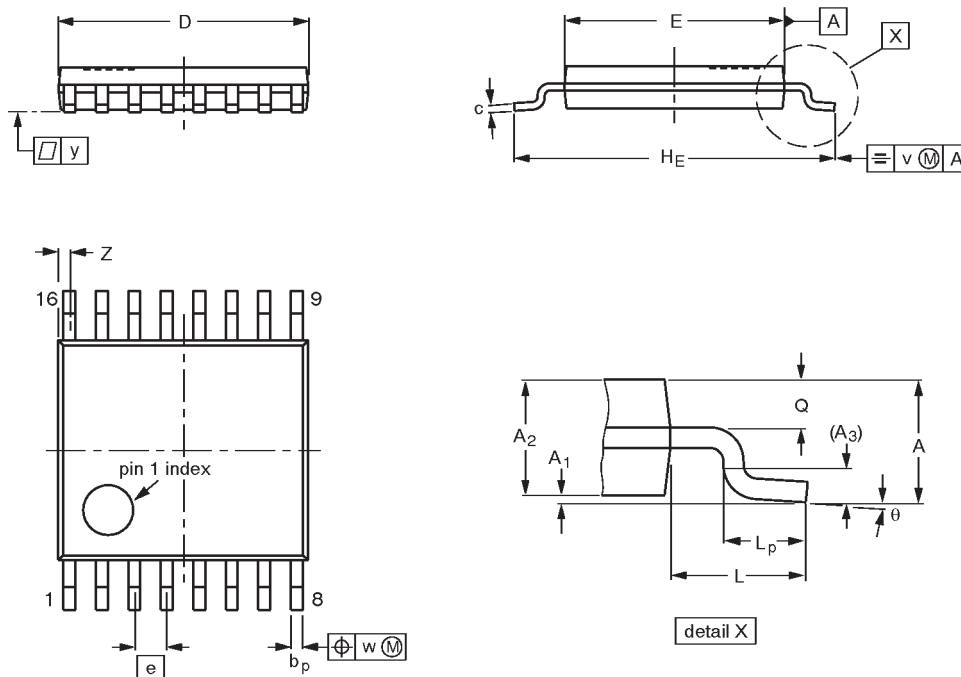
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT338-1		MO-150AC				94-01-14- 95-02-04

4-bit multiplexed/1-bit latched 5-bit I<sup>2</sup>C EEPROM

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TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm

SOT403-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(2)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z <sup>(1)</sup>	θ
mm	1.10	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.40 0.06	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT403-1		MO-153				94-07-12 95-04-04

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**NOTES**

4-bit multiplexed/1-bit latched 5-bit I<sup>2</sup>C EEPROM

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**Data sheet status**

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product specification	Production	This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

[1] Please consult the most recently issued datasheet before initiating or completing a design.

**Definitions**

**Short-form specification** — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

**Limiting values definition** — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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Philips Semiconductors  
811 East Arques Avenue  
P.O. Box 3409  
Sunnyvale, California 94088-3409  
Telephone 800-234-7381

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