



# MX23L1611

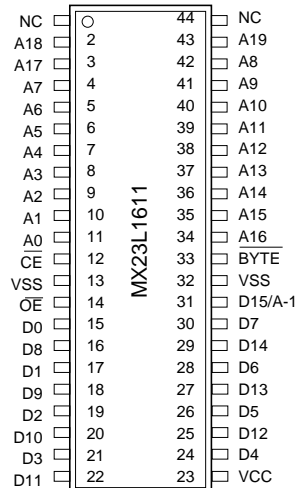
## 3.3 Volt 16-Mbit (2M x 8 / 1M x 16) Mask ROM with Page Mode

### FEATURES

- Bit organization
  - 2M x 8 (byte mode)
  - 1M x 16 (word mode)
- Fast access time
  - Random access: 100ns (max.)
  - Page access: 30ns (max.)
- Page Size
  - 8 words per page
- Current
  - Operating: 40mA
  - Standby: 15uA
- Supply voltage
  - 100ns @ 3.0V ~ 3.6V
  - 120ns @ 2.7V ~ 3.6V
- Package
  - 44 pin SOP (500mil)
  - 48 pin TSOP (12mm x 20mm)

### PIN CONFIGURATION

#### 44 SOP



### ORDER INFORMATION

Part No.	Access Page Access		Package
	Time	Time	
MX23L1611MC-10	100ns	30ns	44 pin SOP
MX23L1611MC-12	120ns	50ns	44 pin SOP
MX23L1611MI-12*	120ns	50ns	44 pin SOP
MX23L1611TC-10	100ns	30ns	48 pin TSOP
MX23L1611TC-12	120ns	50ns	48 pin TSOP
MX23L1611TI-12*	120ns	50ns	48 pin TSOP

\*Note: Industrial grade's temperature is -40°C~85°C

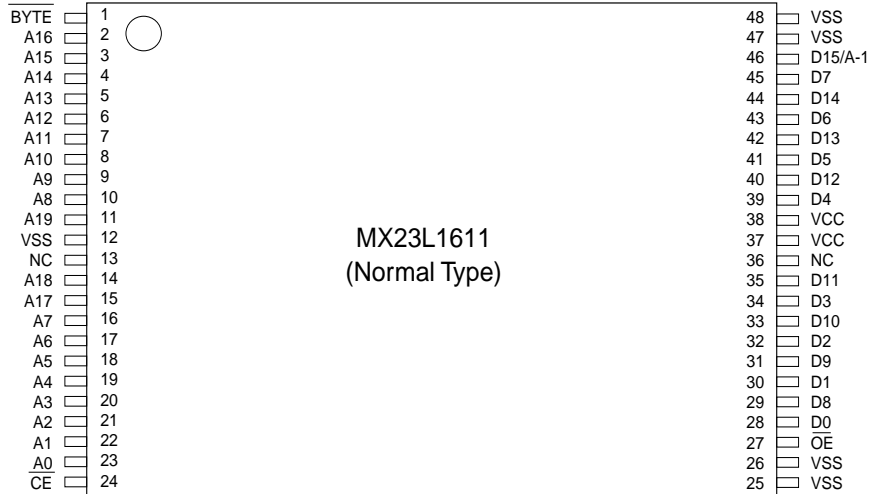
### PIN DESCRIPTION

Symbol	Pin Function
A0~A19	Address Inputs
D0~D14	Data Outputs
D15/A-1	D15 (Word Mode)/ LSB Address (Byte Mode)
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
Byte	Word/ Byte Mode Selection
VCC	Power Supply Pin
VSS	Ground Pin
NC	No Connection

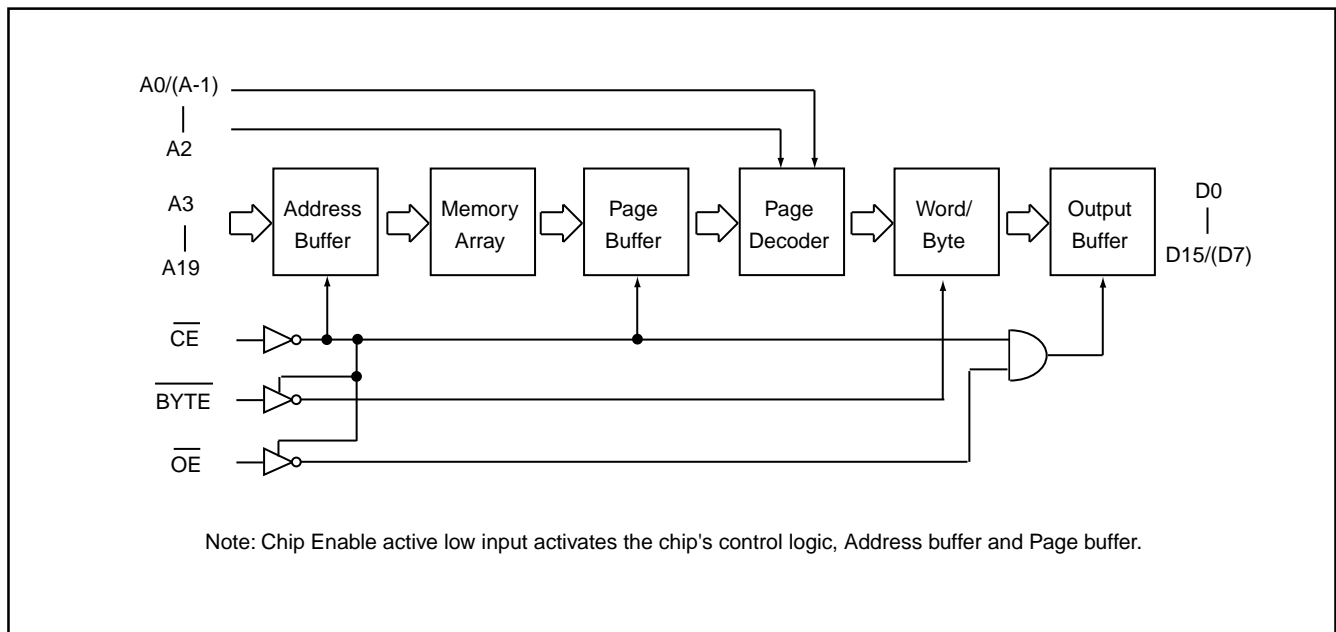
### MODE SELECTION

$\overline{CE}$	$\overline{OE}$	Byte	D15/A-1	D0~D7	D8~D15	Mode	Power
H	X	X	X	High Z	High Z	-	Stand-by
L	H	X	X	High Z	High Z	-	Active
L	L	H	Output	D0~D7	D8~D15	Word	Active
L	L	L	Input	D0~D7	High Z	Byte	Active

### 48 TSOP (Normal Type)



### BLOCK DIAGRAM



**ABSOLUTE MAXIMUM RATINGS**

Item	Symbol	Ratings
Voltage on any Pin Relative to VSS	VIN	-1.3V to VCC+2.0V (Note)
Ambient Operating Temperature	Topr	-40°C to 85°C
Storage Temperature	Tstg	-65°C to 125°C

Note: Minimum DC voltage on input or I/O pins is -0.5V. During voltage transitions, inputs may undershoot VSS to -1.3V for periods of up to 20ns. Maximum DC voltage on input or I/O pins is VCC+0.5V. During voltage transitions, input may overshoot VCC to VCC+2.0V for periods of up to 20ns.

**DC CHARACTERISTICS** (Ta = -10°C ~ 70°C, VCC = 3.0V~3.6V)

Item	Symbol	MIN.	MAX.	Conditions
Output High Voltage	VOH	2.4V	-	IOH = -0.4mA
Output Low Voltage	VOL	-	0.4V	IOL = 1.6mA
Input High Voltage	VIH	2.2V	VCC+0.3V	
Input Low Voltage	VIL	-0.3V	0.2 x VCC	
Input Leakage Current	ILI	-	5uA	0V, VCC
Output Leakage Current	ILO	-	5uA	0V, VCC
Operating Current	ICC1	-	40mA	tRC = 100ns, all output open
Standby Current (TTL)	ISTB1	-	1mA	$\overline{CE} = V_{IH}$
Standby Current (CMOS)	ISTB2	-	15uA	$\overline{CE} > V_{CC} - 0.2V$
Input Capacitance	CIN	-	10pF	Ta = 25°C, f = 1MHZ
Output Capacitance	COUT	-	10pF	Ta = 25°C, f = 1MHZ

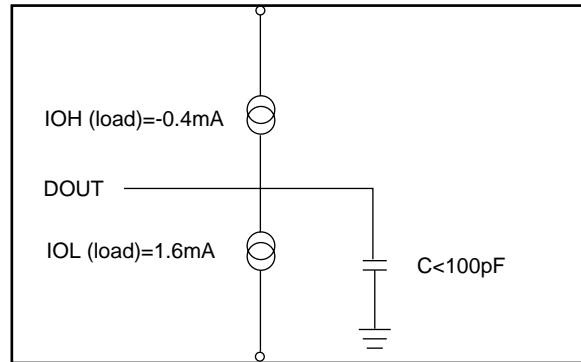
**AC CHARACTERISTICS** (Ta = -10°C ~ 70°C, VCC = 3.0V~3.6V)

Item	Symbol	23L1611-10		23L1611-12	
		MIN.	MAX.	MIN.	MAX.
Read Cycle Time	tRC	100ns	-	120ns	-
Address Access Time	tAA	-	100ns	-	120ns
Chip Enable Access Time	tACE	-	100ns	-	120ns
Page Mode Access Time	tPA	-	30ns	-	50ns
Output Enable Time	tOE	-	30ns	-	50ns
Output Hold After Address	tOH	0ns	-	0ns	-
Output High Z Delay	tHZ	-	20ns	-	20ns

Note: Output high-impedance delay (tHZ) is measured from OE or CE going high, and this parameter guaranteed by design over the full voltage and temperature operating range - not tested.

## AC Test Conditions

Input Pulse Levels	0.4V~ 2.6V
Input Rise and Fall Times	10ns
Input Timing Level	1.4V
Output Timing Level	1.4V
Output Load	See Figure



Note:

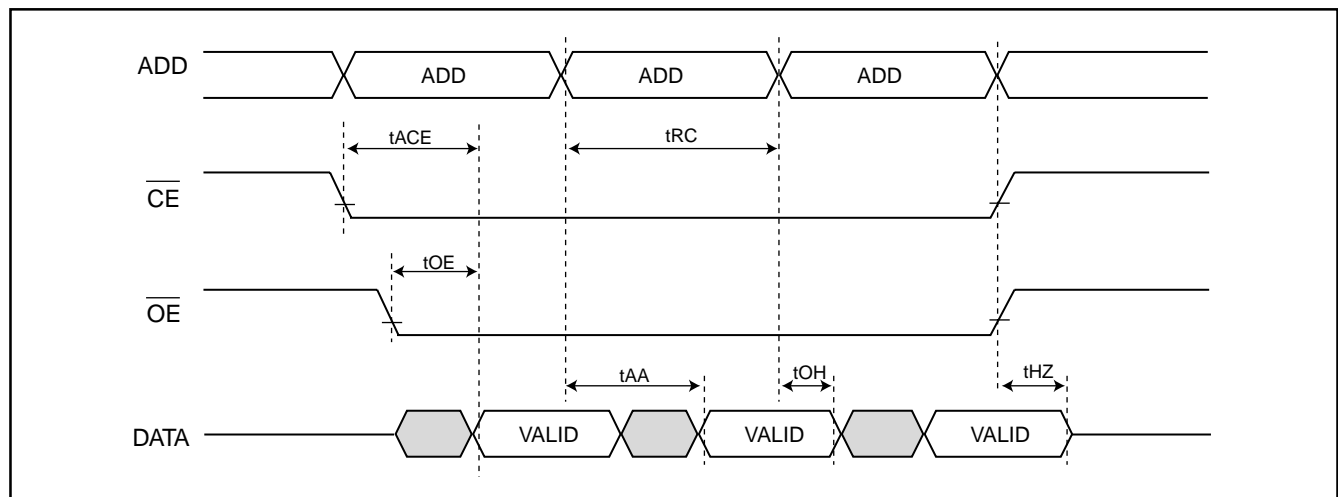
No output loading is present in tester load board.

Active loading is used and under software programming control.

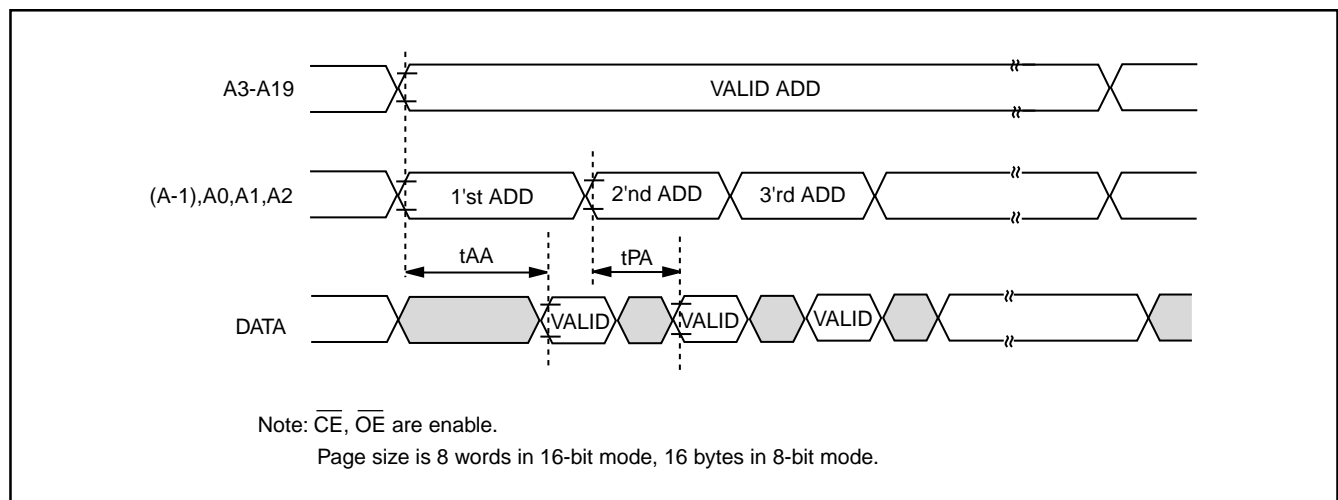
Output loading capacitance includes load board's and all stray capacitance.

## TIMING DIAGRAM

### RANDOM READ

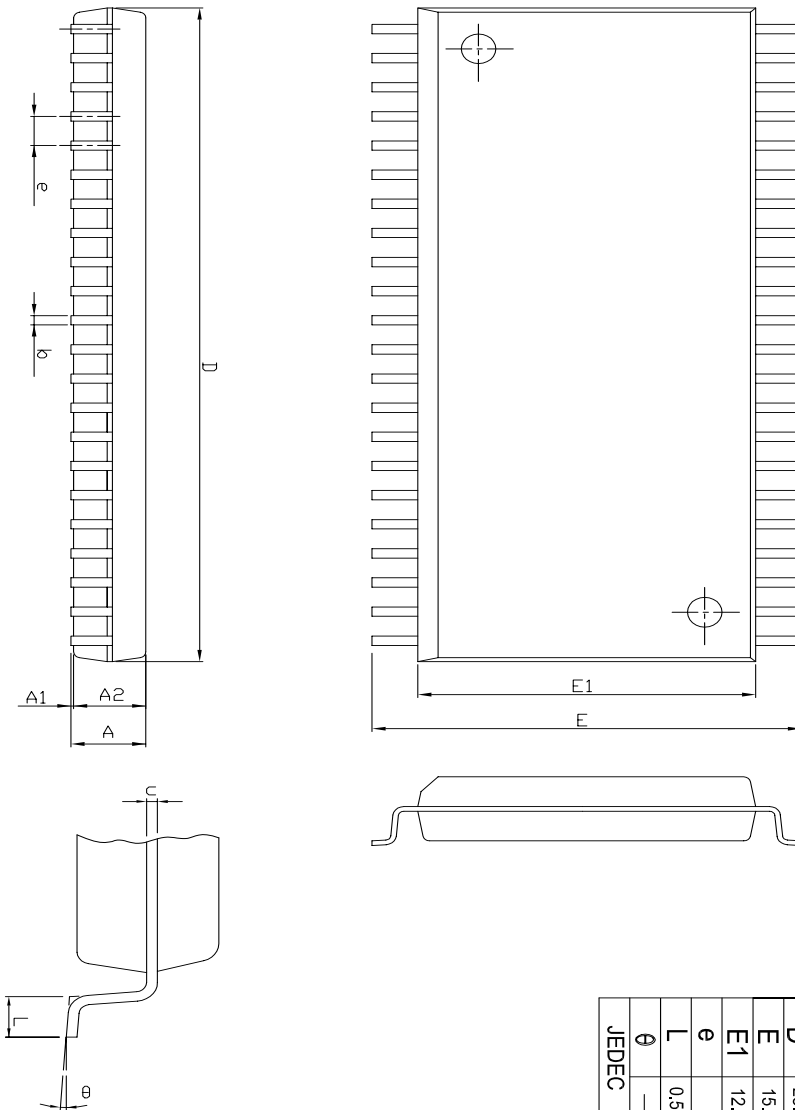


### PAGE READ



## PACKAGE INFORMATION

### 44-PIN PLASTIC SOP

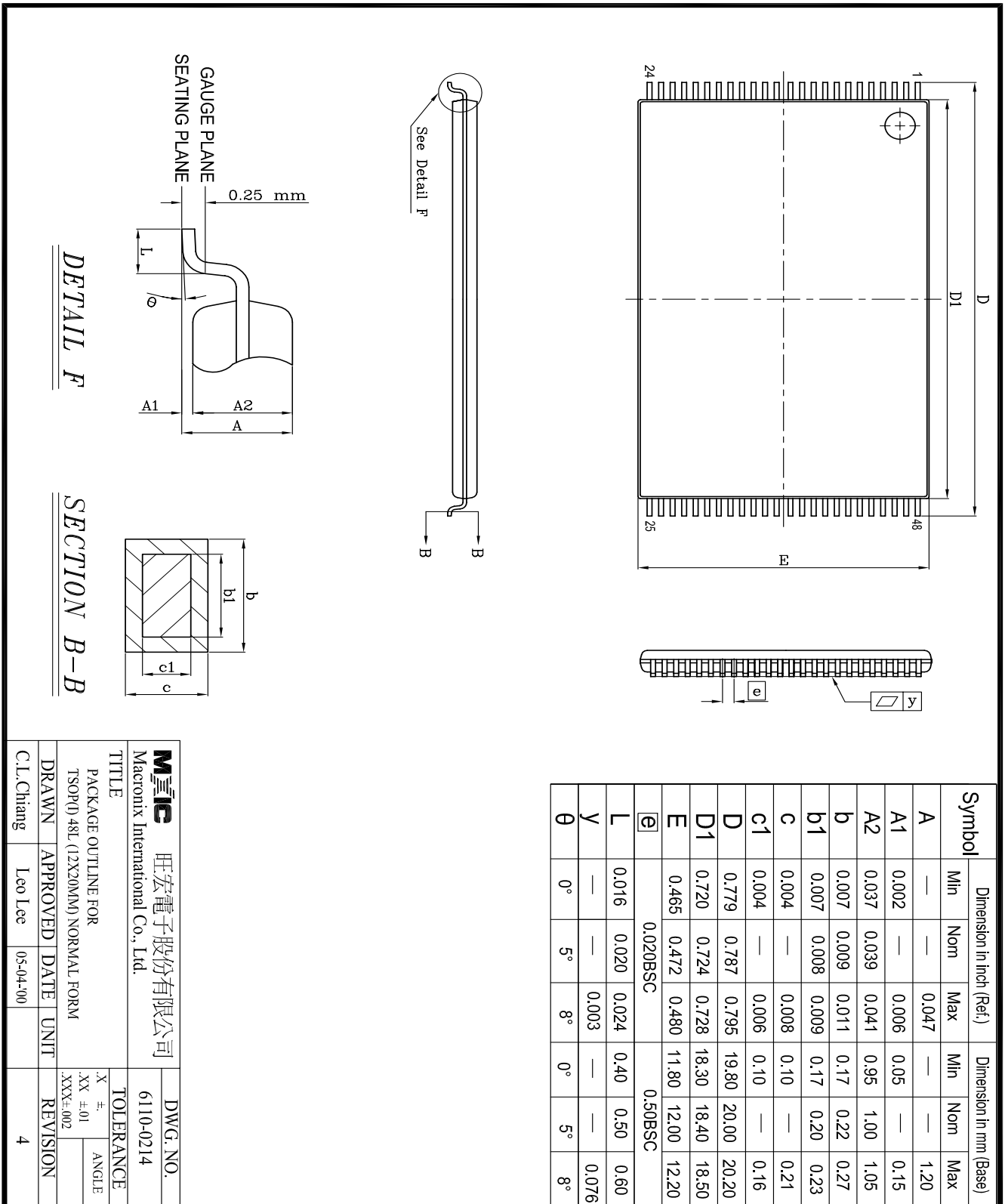


Symbol	Dimension in mm (Base)			Dimension in inch (Ref.)		
	Min	Nom	Max	Min	Nom	Max
A	—	—	3.00	—	—	0.118
A1	0.10	—	—	0.004	—	—
A2	2.57	2.69	2.82	0.101	0.106	0.111
b	—	0.41 REF	—	—	0.016 REF	—
C	—	0.20 REF	—	—	0.008 REF	—
D	28.37	28.50	28.63	1.117	1.122	1.127
E	15.77	16.03	16.28	0.621	0.631	0.641
E1	12.47	12.60	12.73	0.491	0.496	0.501
e	—	1.27 REF	—	—	0.050 REF	—
L	0.58	0.79	0.99	0.023	0.031	0.039
θ	—	5°	—	—	5°	—

JEDEC

<b>Mxic</b> 旺宏電子股份有限公司 Macronix International Co., Ltd.		DWG. NO. 6110-0207	
TITLE PACKAGE OUTLINE FOR SOP 44L (500 MIL)			
DRAWN	APPROVED	DATE	UNIT
C.L.Chang	Dennis Chang	05-03-01	INCH
TOLERANCE		REVISION	
X ±		1	
XX ±01		ANGLE	
.XXX±.002		ROUGNESS	
		2	

## 48-PIN PLASTIC TSOP



<b>Mxic</b> 旺宏電子股份有限公司 Macronix International Co., Ltd.		DWG. NO. 6110-0214	
TITLE PACKAGE OUTLINE FOR TSOP(0) 48L (12X20MM) NORMAL FORM			
DRAWN C.L.Chiang		DATE 05-04-00	
APPROVED Leo Lee		REVISION 4	
TOLERANCE .X ±. .XX ±.01 .XXX ±.002		ANGLE	

**REVISION HISTORY**

<b>REVISION</b>	<b>DESCRIPTION</b>	<b>PAGE</b>	<b>DATE</b>
1.5	Temperature range is revised as -10°C~70°C	P3	NOV/27/1998
1.6	Output hold after address (tOH) spec is revised as 0ns(min.) 120ns speed grade's voltage range is revised as 2.7V~3.6V	P3 P1	JAN/22/1999
1.7	DC characteristics Standby current (ISTB2):5uA-->15uA	P1,3	Dec/30/1999
1.8	Modify Package Information	P5~6	JUL/18/2001



**MX23L1611**

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