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Features

- 2,048 channel non-blocking switch
- Maintains frame integrity on concatenated channels.
- Per-channel selection of minimum or constant throughput delay
- Serial streams at 2.048, 4.096 or 8.192Mb/s
- Frame offset delay measurement
- Programmable frame delay offset
- Per-channel three-state control
- Per-channel message mode
- Control interface compatible to Intel/Motorola CPUs
- Block programming feature for connection memory
- ST-BUS/MVIP and GCI interfaces
- Test Port compatible to IEEE-1149.1 standard

Applications

- Medium and large switching platforms
- C.O. switches
- CTI application
- Voice/data multiplexer
- Digital cross connects
- ST-BUS/HMVIP interface functions

Ordering Information

MT90820AP	84 Pin PLCC
MT90820AL	100 Pin QFP

-40 to +85°C

Description

The Large Digital Switch (LDX) is an advanced digital switch allowing the users to build up to 2048 channel non-blocking switch. The serial interface can be at 2, 4 or 8 Mb/s compatible to ST-BUS/MVIP/ HMVIP or GCI standards. The LDX can be programmed to provide either minimum or constant throughput delay on all its channels. The device also features three-state control and message mode on per-channel basis.

To manage the problem of line delays, each input stream can have an individually programmed input frame offset delay. The offset delay can be calibrated with a dedicated frame measurement facility inside the device.

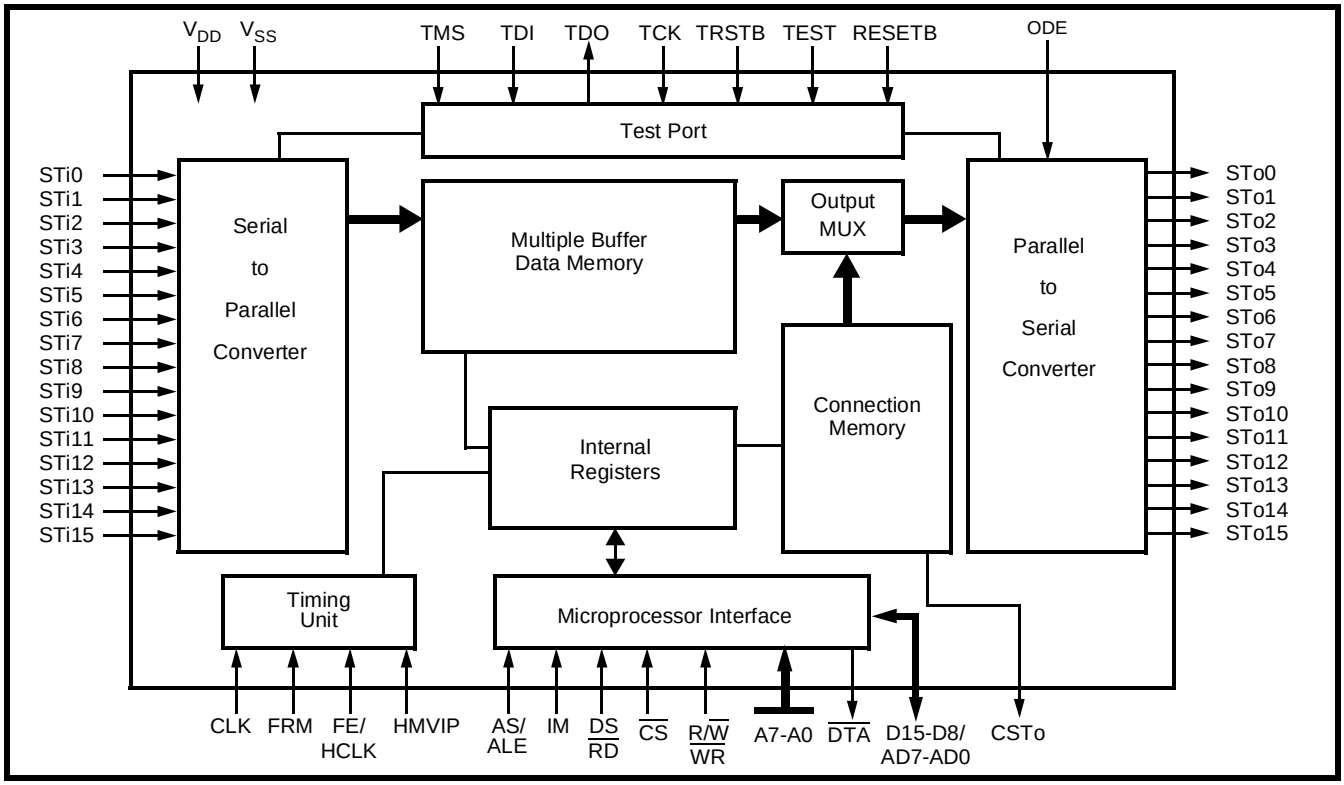

Figure 1 - Functional Block Diagram

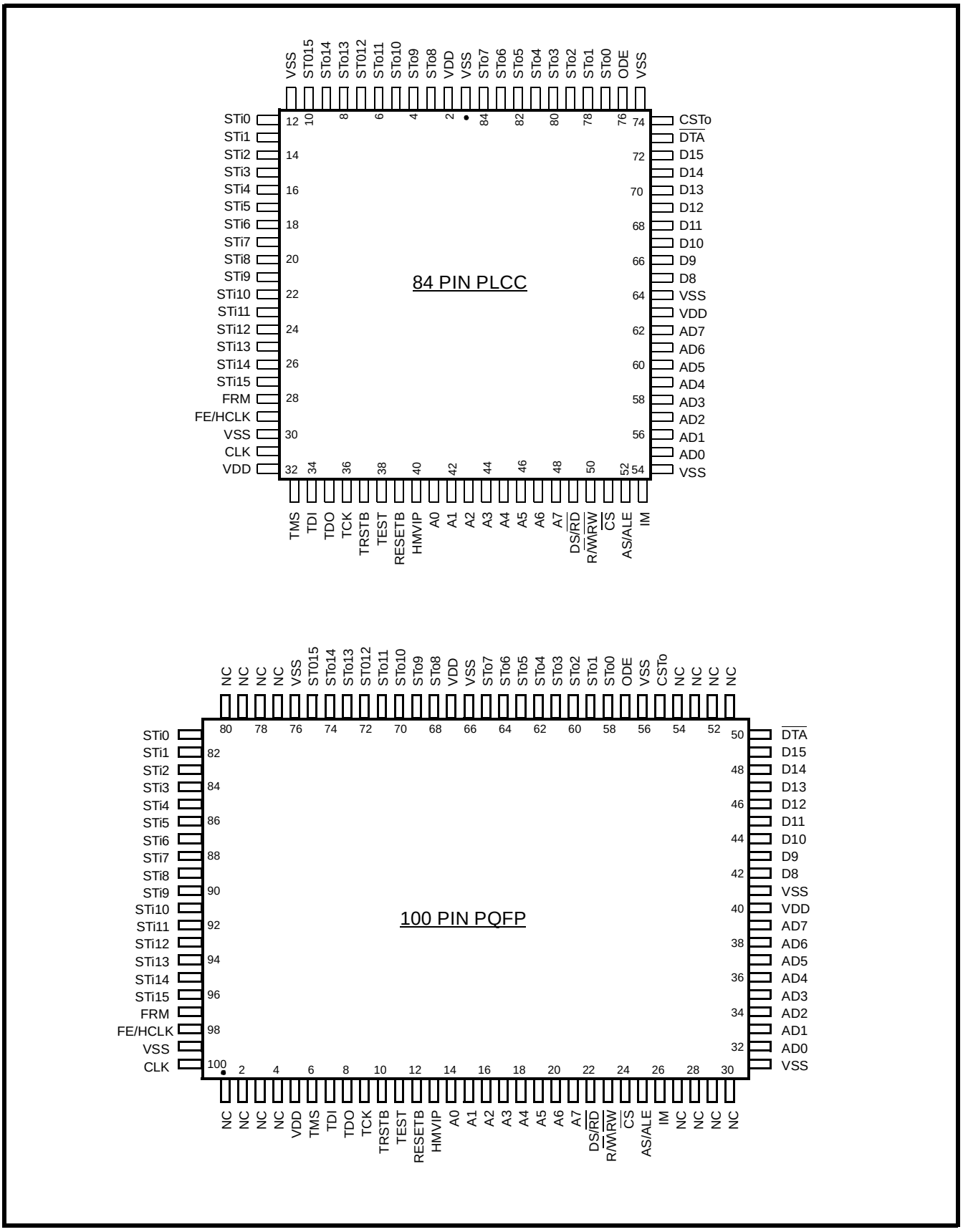

Figure 2 - Pin Connections

Pin Description

Pin #		Name	Description
84	**100**		
1, 11, 30, 54 64, 75	31, 41, 56, 66, 76, 99	V_{SS}	**Ground.**
2, 32, 63	5, 40, 67	V_{DD}	**+5 Volt Power Supply.**
3 - 10	68-75	STo8 - 15	**Data Stream Output 8 to 15: Serial data Output stream.** These stream may have data rates of 2.048, 4.096 or 8.192 Mb/s.
12 - 27	81-96	STi0 - 15	**Data Stream Input 0 to 15: Serial data input stream.** These stream may have data rates of 2.048, 4.096 or 8.192.
28	97	FRM	**Frame Pulse (input):** This input accepts and automatically identifies frame synchronization signals formatted according to ST-BUS and GCI interface specifications, when HMVIP pin =0. When HMVIP pin =1, FRM input accepts a negative frame pulse which conforms to HMVIP formats.
29	98	FE/HCLK	**Frame Measurement input**, when HMVIP pin = 0. **4.096MHz Clock input**, when HMVIP pin = 1.
31	100	CLK	**Clock (input):** Serial clock for shifting data in/out on the serial stream.
33	6	TMS	When 1, enable test mode for production testing.
34	7	TDI	**Test Data Input.**
35	8	TDO	**Test Data Output.**
36	9	TCK	**Test Clock input.**
37	10	TRSTB	**Test Reset Input:** When 0, resets the test circuit.
38	11	IC	**Internal Connection:** keep at 0 for normal operation.
39	12	RESETB	**Device Reset Input:** When 0, resets the device.
40	13	HMVIP	**HMVIP mode input.** When 1, enables HMVIP interface. When 0, the device operates in ST-BUS/GCI mode.
41 - 48	14-21	A0 - A7	**Address 0 - 7(Input):** When non-multiplexed CPU bus is selected, these lines provide the A0 - A7 address lines to internal memories.
49	22	DS/RD	**Data Strobe/Read (input)**: When non-multiplexed CPU bus or Motorola multiplexed bus are selected, this input is DS. This active high input works in conjunction with CSB to enable read and write operation. For Intel multiplexed bus, this input is RDB. This active low input sets the data bus lines (AD0-AD7, D8-D15) as outputs.
50	23	R/W\WR	**Read/Write \ Write (Input):** In case of non-multiplexed and Motorola multiplexed buses, this input is Read/Write. This input controls the direction of the data bus lines (AD0 - AD7, D8-D15) during a microprocessor access.
51	24	CS	**Chip Select (Input):** Active low input enabling a microprocessor access of the device.

Pin Description

Pin #		Name	Description
84	**100**		
52	25	AS/ALE	**Address Strobe or Latch Enable:** This input is only used if multiplexed bus is selected.
53	26	IM	**CPU Interface Mode (input):** If High, this input selects the multiplexed microprocessor bus interface. If this input is not connected or grounded, the device resumes non-multiplexed bus interface.
55 - 62	32-39	AD0 - 7	**Address/Data Bus (Bidirectional):** These are bi-directional data pins on the microprocessor interface. In the multiplexed bus mode, these pins also provide the input address to the internal registers and memories.
65 - 72	42-49	D8 - 15	**Data Bus (Bidirectional):** These are additional bi-directional data pins on the microprocessor interface.
73	50	DTA	**Data Acknowledgement (Open Drain Output):** This active low output indicates that a data bus transfer is complete. A 10 kohm pull-up resistor is required at this output.
74	55	CSTo	**Control Output (output).**
76	57	ODE	**Output Device Enable (input):** This is the output enable control for the STo0 to STo15 serial outputs. When this input is high, the STo0-15 output drivers function normally. If this input is low, Sto0-15 are in high impedance. Note: Even when ODE is high, each channel may still be put into high impedance state by using per channel control bit in the connection memory.
77 - 84	58-65	STo0 - 7	**Data Stream Output 0 to 7:** Serial data Output stream. These streams may have data rates of 2.048, 4.096 or 8.192Mb/s.
-	1 - 4, 27 - 30, 51 - 54 77 - 80	NC	Unused pins.

Device Overview

The LDX is capable of switching 2,048 × 2,048 channels. The device is designed to switch 64 or N x 64 kbit/s data. It can provide frame integrity for data applications and minimum throughput switching delay for voice application on a per channel basis.

The serial input streams of LDX can operate at 2.048, 4.096 and 8.192 Mbit/s and are arranged in 125µs wide frames which contains 32, 64 and 128 channels, respectively. The LDX automatically identifies the polarity of the input frame synchronization signal and configures the serial ports to be compatible to either ST-BUS and GCI formats. The input and output streams accept identical data rates only.

By using Mitel message mode capability, the microprocessor can access input and output time-slots on a per channel basis to control external circuits or other ST-BUS devices. Two different microprocessor bus interface can be selected through an input mode pin (IM): Non-multiplexed or Multiplexed. These interfaces provide compatibility with Intel/National multiplexed and Motorola Multiplexed/Non-multiplexed buses.

The frame offset calibration allows users to measure the frame offset delay using an frame evaluation pin (FE). The input stream offset delay can be individually programmed using internal registers.

Functional Description

A functional Block Diagram of the LDX device is shown in Figure 1. Depending upon the application, the LDX device receives TDM serial data at different rates.

Data and Connect Memory

For all data rates, the received serial data is converted to parallel format by the serial to parallel converters and stored sequentially in a Data Memory. Depending upon the selected operation, the data memory may have up to 2,048 bytes in use. The sequential addressing of the data memory is performed by an internal counter which is reset by the input 8 kHz frame pulse (FRM) marking the frame boundaries of the incoming serial data streams.

Data to be output on the serial streams may come from two sources: Data Memory or Connect Memory. Locations in the connect memory are associated with particular output streams. When a channel is due to be transmitted on an output, the data for the channel can either be switched from an input as in connection mode or it can be from the connect memory as in message mode. Data destined for a particular channel on the serial output stream is read from the data memory or connect memory during the previous channel time-slot. This allows enough time for memory access and parallel to serial conversion.

Connection and Message Modes

In Connection mode, the addresses of the inputs for all output channels are stored in the connect memory. Once the source addresses are programmed by the CPU, the contents of the data memory at the selected address are transferred to the parallel-to-serial inverters. By having the output channel specifying the source channel through the connect memory, the user can route the same input channel to serval output channels, allowing broadcast facility within the switch.

In message mode, the CPU writes data to the connect memory locations corresponding to the output link and channel number. The lower half (8-LSBs) of the connect memory content is transferred directly to the parallel-to-serial converter one channel before it is to be output. The data is transmitted on to the output every frame until it is changed by the CPU with a new data.

The five most significant bits in the connect memory determine individual output channel to be in message or connection mode, select output throughput delay type, enable/disable output drivers and enable/disable the loopback mode. In addition, one of these bits allows the user to control the CSTo output.

If an output channel is set to high-impedance, the TDM serial stream output will be in high impedance during that channel time. In addition to the per-channel control, all channels on the TDM outputs can be placed in high impedance by either pulling the ODE input pin low or programming a particular bit in the control register.

The connect memory data is received via the microprocessor interface through the data I/O bus. The addressing of the LDX internal registers, data and connect memories is performed through address input pins and the Memory Select bit in the control register.

Serial Data Interface

The master clock (CLK) can be either at 4.096, 8.192 or 16.384 MHz allowing serial data link operation at 2.048, 4.096 and 8.192 Mb/s respectively. The master clock frequency is always twice the data rate. The input and output streams accept identical data rate.

The input 8 kHz frame pulse can be in either ST-BUS or GCI format. The LDX automatically detects the presence of an input frame pulse and identifies the type of serial interface. In ST-Bus format, every second falling edge of the master clock marks a bit boundary and the input data is clocked by the rising edge, three quarters of the way into the bit cell. In GCI format, every second rising edge of the master clock marks the bit boundary while data sampling is performed on the falling edge, at three quarters of the bit cell boundary.

Switching Configuration

Switching configurations are determined basically by the data rates selected at the serial inputs and outputs. To specify the switching configuration required, the Interface Mode Selection (IMS) register has to be initialized on system power-up. The switching configuration is selected by two DR bits in the IMS register.

Serial Links with Data Rates at 2.048 Mb/s

When the 2.048Mb/s data rate is selected for input and output streams, the device is configured with 16-input/16-output data streams with 32 64Kbit/s channels each. The modes allows 512 x 512 channel Switch Matrix configuration. The interface clock is 4.096 MHz.

Serial Links with Data Rates at 4.096 Mb/s

When the 4.096 Mb/s data rate is selected for input and output streams, the device is configured with 16-input/16-output data streams with 64 64Kbit/s channels each. The modes allows 1,024 x 1,024 channel Switch Matrix configuration. The interface clock is 8.192MHz.

Serial Links with Data Rates at 8.192 Mb/s

When the 8.192Mb/s data rate is selected for input and output streams, the device is configured with 16-input/16-output data streams with 128 64Kbit/s channels each. The modes allows 2,048 x 2,048 channel Switch Matrix configuration. The interface clock is at 16.384 MHz.

Table 1 summarizes the switching configurations.

Input Frame Offset Selection

The LDX provides a feature called Input Frame Offset allowing users to compensate for the varying delays on the incoming serial inputs while building large switch matrices. Usually, different delays occur on the digital backplanes causing the data and frame pulse signal to be skewed at the input of the switch device. This may result in the system frame pulse to be active at the FRM input before the first bit of the frame is received at the serial input.

The LDX allows users to compensate the input delay offset by programming the Frame Input Offset (FOS) registers. Each input stream can have its own delay offset value. Possible adjustment is up to 4 master clock periods forward with resolution of 1/2 clock period.

Frame Alignment Evaluation

To manage the problem of different data input delays (with respect to the frame pulse), the LDX provides the FE input for the frame alignment evaluation. The evaluation starts when the SFE bit in the IMS register is changed from low to high. Two frames later, the CFE bit of the frame alignment register (FAR) changes from low to high to signal the CPU

Serial Interface Data Rate	Master Clock Required (MHz)	Number of Input x Output Streams	Matrix Channel Capacity	Switch Matrix type	Input/Output Stream used
2 Mb/s	4.096	16 x 16	512 x 512	Non-Blocking	STi0-15/STo0-15
4 Mb/s	8.192	16 x 16	1,024 x 1,024	Non-Blocking	STi0-15/STo0-15
8 Mb/s	16.384	16 x 16	2,048 x 2,048	Non-Blocking	STi0-15/STo0-15

Table 1: Switching Configuration

that a valid offset measurement is ready to be read from the FAR register.

This feature is not available when the HMVIP interface is enabled, i.e. when HMVIP pin is tied to V_{DD}.

Memory Block Programming

The LDX device provides the capability of block programming the connect memory block. By using this feature, the five MSBs of the connect memory belonging to each output channel can be automatically programmed with a fixed pattern defined by the IMS register. This feature reduces the system initialization time.

To enable the block programming mode, user have to set the Memory Block Program (MBP) bit of the control register to HIGH and program the IMS register with the Block Programming Enable (BPE) bit = 1, and the desired pattern. The block programming takes two frames to complete.

Delay Through the LDX

The switching of information from the input serial streams to the output serial streams results in a delay. Depending on the type of information to be switched, the LDX can be programmed to perform time-slot interchange functions with different throughput delay capabilities on the per-channel basis. For voice application, variable throughput delay can be selected ensuring minimum delay between input and output data. In wideband data applications, constant throughput delay can be selected maintaining the frame integrity of the information through the switch.

The delay through the LDX varies according to the type of throughput delay selected in the connect memory.

Microprocessor Port

The LDX provides an microprocessor interface with non-multiplexed and multiplexed bus structures. The LDX microport is compatible to Motorola multiplexed/ non-multiplexed and Intel multiplexed buses. The multiplexed bus structure is selected by the CPU interface Mode (IM) pin.

When the IM pin is not connected (left open) or grounded, the LDX parallel port assumes the default Motorola non-multiplexed bus mode. If IM pin is connected HIGH, the internal parallel microport provides compatibility to MOTEL interface allowing direct connection to Intel, National and Motorola CPUs.

The MOTEL circuit (**MO**torola and in**TEL** compatible bus) automatically identifies the types of CPU Bus connected to the LDX. This circuit uses the level of the DS/$\overline{RD}$ input pin at the rising edge of the AS/ALE to identify the appropriate bus timing connected to the LDX. If DS/$\overline{RD}$ is low at the rising edge of AS/ ALE then Motorola bus timing is selected. If DS/RD is HIGH at the rising edge of AS/ALE, then the Intel bus timing is selected.

The LDX microport provides the access to the internal registers, connect and data memories. All locations can be read or written except for the data memory which can be read only.

Internal Register and Address Memory

To access internal registers, users have to connect the A7 pin to LOW. To access to data and connect memories positions, users have to connect the A7 pin HIGH.

Table 2 summarizes the internal register and address memory mapping.

Initialization of the LDX

On initialization or power up, the contents of the connect memory can be in any states. This is a potentially hazardous condition when multiple LDXs outputs are tied together to form matrices, as these output may conflict each other. The ODE pin should be held low on power up to keep all outputs in the high impedance condition.

A7	A6	A5	A4	A3	A2	A1	A0	Location
0	0	0	0	0	0	0	0	Control Register, CAR.
0	0	0	0	0	0	0	1	Interface Mode Selection register, IMS
0	0	0	0	0	0	1	0	Frame Alignment register, FAR
0	0	0	0	0	0	1	1	Frame Input Offset register 0, FOS0
0	0	0	0	0	1	0	0	Frame Input Offset register 1, FOS1
0	0	0	0	0	1	0	1	Frame Input Offset register 2, FOS2
0	0	0	0	0	1	1	0	Frame Input Offset register 3, FOS3
1 1 1 1 1	0 0 0 0 0	0 0 0 0 0	0 0 . 1 1	0 0 . 1 1	0 0 . 1 1	0 0 . 1 1	0 1 . 0 1	Ch 0* Ch 1* . Ch 30* Ch 31*
1 1 1 1 1	0 0 0 0 0	1 1 1 1 1	0 0 . 1 1	0 0 . 1 1	0 0 . 1 1	0 0 . 1 1	0 1 . 0 1	Ch 32** Ch 33** . Ch 62** Ch 63**
1 1 1 1 1	1 1 1 1 1	0 0 . 1 1	0 0 . 1 1	0 0 . 1 1	0 0 . 1 1	0 0 . 1 1	0 1 . 0 1	Ch 64*** Ch 65*** . Ch 126*** Ch 127***

Note 1: The bit A7 must be retained HIGH for accesses to Data and Connection Memory positions.
The bit A7 must be retained LOW for accesses to Registers.
Note*: Channel 0 to 31 are used in 2Meg mode.
Note**: Channel 0 to 63 are used in 4Meg mode.
Note***: Channel 0 to 127 are used in 8Meg mode.

Table 2 - Internal Register and Address Memory Mapping

Absolute Maximum Ratings*

	Parameter	Symbol	Min	Max	Units
1	Supply Voltage	V_{DD}		6.0	V
2	Voltage on any pin I/O (other than supply pins)	V	V_{SS} - 0.3	V_{DD} + 0.3	V
3	Current at digital outputs	I_O		40	mA
4	Package power dissipation	P_D		2	W
5	Storage temperature	T_{ST}	- 65	150	°C

* Exceeding these figures may cause permanent damage. Functional operation under these conditions is not guaranteed.

Recommended Operating Conditions - Voltages are with respect to ground (V_{SS}) unless otherwise stated.

	Characteristics	Sym	Min	Typ*	Max	Units	Test Conditions
1	Operating Temperature	T_{OP}	4.75	5.0	5.25	°C	
2	Positive Supply	V_{DD}	4.75	5.0	5.25	V	
3	Input Voltage	V_I	0		V_{DD}	V	

* Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing.

DC Electrical Characteristics - Voltages are with respect to ground (V_{SS}) unless otherwise stated.

		Characteristics	Sym	Min	Typ	Max	Units	Test Conditions
1	INPUTS	Supply Current	I_{DD}		50		mA	Output unloaded
2		Input Voltage High	V_{IH}	2.0			V	
3		Input Voltage Low	V_{IL}			0.8	V	
4		Input Leakage (input pins) Input Leakage (I/O pins)	I_{IL}		 34	5 100	µA µA	V_I between V_{SS} and V_{DD}
5		Input Pin Capacitance	C_I		8		pF	
6	OUTPUTS	Output Voltage High	V_{OH}	2.4			V	I_{OH} = 10mA
7		Output Voltage Low	V_{OL}			0.4	V	I_{OL} = 5mA
8		Output High Current	I_{OH}	10			mA	Sourcing. V_{OH}=2.4V
9		Output Low Current	I_{OL}	5			mA	Sinking. V_{OL}=0.4V
10		High Impedance Leakage	I_{OZ}		5		µA	
11		Output Pin Capacitance	C_O		8		pF	

NOTES: