

# The MRFIC Line

## 900 MHz GaAs

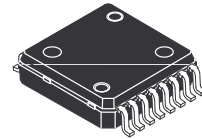
### Integrated Power Amplifier

Designed primarily for use in high efficiency Analog Cellular applications, the MRFIC0912 is a two-stage power amplifier in Motorola's proprietary Power Flat Pack 16-lead package. This integrated circuit requires minimal off-chip matching while allowing for the maximum in flexibility in optimizing gain and efficiency. The design employs Motorola's planar, self-aligned GaAs MESFET IC process to give the highest efficiency possible.

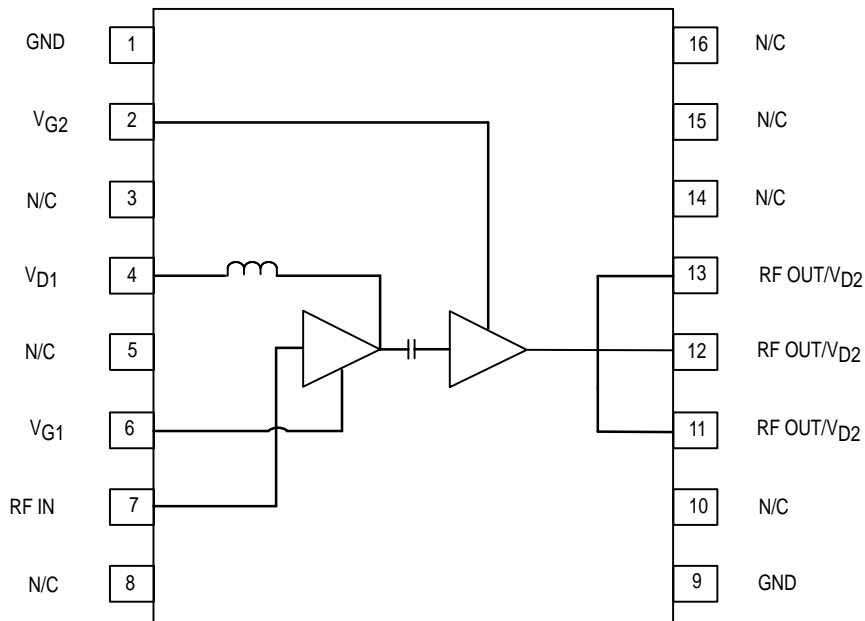
- Usable Frequency Range = 800–1000 MHz, Specified for 824–905 MHz
- 30.8 dBm Minimum Output Power
- 470 mA Maximum Supply Current at 30.8 dBm Output
- 23.8 dB Minimum Gain
- Simple Off-chip Matching for Maximum Power/Efficiency Flexibility
- 4.6 Volt Supply
- 45 dB/Volt Typical Power Output Control
- Order MRFIC0912R2 for Tape and Reel Option.  
R2 Suffix = 1,500 Units per 16 mm, 13 inch Reel.
- Device Marking = M0912

**MRFIC0912**

**900 MHz  
GaAs INTEGRATED  
POWER AMPLIFIER**



**CASE 978-02  
(FPF-16)**



**Pin Connections and Functional Block Diagram**

**MAXIMUM RATINGS** ( $T_A = 25^\circ\text{C}$  unless otherwise noted)

Ratings	Symbol	Limit	Unit
Supply Voltage	$V_{D1}, V_{D2}$	8	Vdc
RF Input Power	$P_{RF}$	20	dBm
Gate Voltage	$V_{G1}, V_{G2}, V_{GG}$	-5	Vdc
Storage Temperature Range	$T_{stg}$	-65 to +150	$^\circ\text{C}$
Operating Case Temperature	$T_C$	-35 to +100	$^\circ\text{C}$
Thermal Resistance, Junction to Case	$R_{\theta JC}$	18	$^\circ\text{C/W}$

**RECOMMENDED OPERATING RANGES**

Parameter	Symbol	Value	Unit
RF Frequency	$f_{RF}$	824–905	MHz
Supply Voltage	$V_{D1}, V_{D2}$	4.0–6.0	Vdc
Gate Voltage	$V_{G1}, V_{G2}$	-2.3 to -1.5	Vdc

**ELECTRICAL CHARACTERISTICS** ( $V_{D1}, V_{D2} = 4.6\text{ V}$ ,  $T_A = 25^\circ\text{C}$ ,  $f_{RF} = 840\text{ MHz}$ ,  $P_{in} = 7\text{ dBm}$ ,  $V_{GG}$  set for  $I_{D2Q} = 200\text{ mA}$ , Tested in Circuit Shown in Figure 1)

Characteristic	Min	Typ	Max	Unit
RF Output Power	30.8	31.2	—	dBm
Power Slump ( $V_{D1}, V_{D2} = 4.0\text{ V}$ , $T_C = 100^\circ\text{C}$ )	28.5	—	—	dBm
Load Mismatch Survival ( $V_{D1}, V_{D2} = 7\text{ V}$ , Load VSWR = 10:1, all phases, 10 sec)	No Degradation			
Spurious Output ( $V_{D1}, V_{D2} = 0\text{ to }7\text{ V}$ , $P_{in} = 5\text{ to }9\text{ dBm}$ , Load VSWR = 10:1)	—	—	-60	dBc
Input Return Loss	—	10	—	dB
Harmonic Output ( $P_{out} = 30.8\text{ dBm}$ )				dBc
$2f_0$	—	—	-25	
$3f_0$	—	—	-40	
$4f_0$	—	—	-40	
Noise Power ( $V_{DD} = 0\text{ to }7\text{ V}$ , 45 MHz Above $f_{RF}$ at 30 kHz BW)	—	—	-93	dBm
Maximum Power Control Voltage Slope (Change in $P_{out}$ for Change on $V_{D1}$ )	—	45	—	dB/V
Total Supply Current ( $V_{D1}$ set for $P_{out} = 30.8\text{ dBm}$ )	—	430	470	mA
$V_{GG}$ Required for $I_{D2Q} = 200\text{ mA}$	-2.3	-2.0	-1.7	Vdc
Gate Current during RF Operation	-2	—	2	mA

**DESIGN AND APPLICATIONS INFORMATION**

The MRFIC0912 has been designed for high efficiency 900 MHz applications such as analog cellular and Industrial, Medical and Scientific (ISM) equipment. The two stage MES-FET design utilizes Motorola's planar refractory gate process to allow high performance GaAs to be applied to consumer applications. The proprietary PFP-16 package assures good grounding and low thermal resistance.

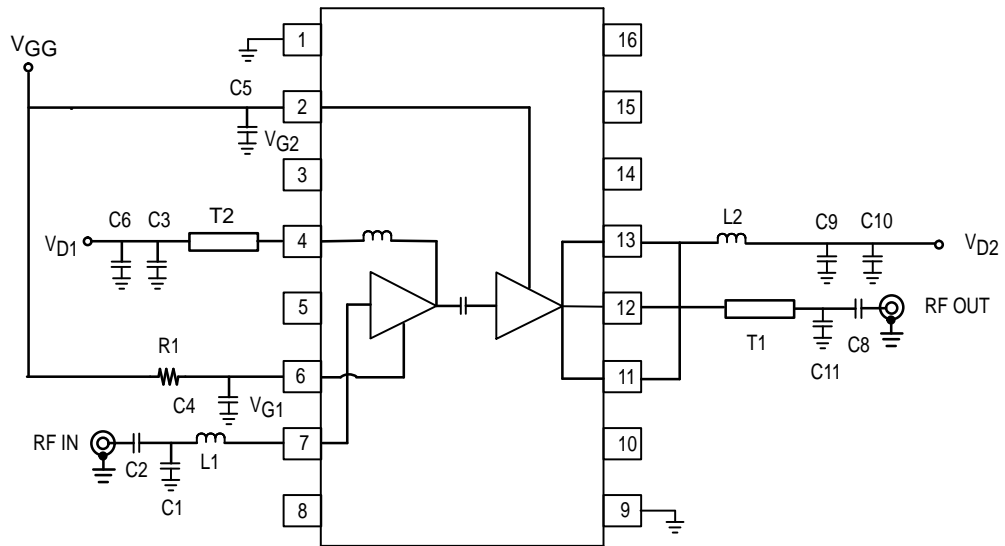
As shown in Figure 1, the gate voltage pins can be ganged together and one voltage applied to both gates to set the quiescent operating current. Alternatively,  $V_{G1}$  and  $V_{G2}$  can be set separately.  $V_{D1}$  can be used as power control with a 45 dB per volt sensitivity. The placement of C3 in the  $V_{D1}$  supply line can be varied to optimize RF performance since T2 is part of a shunt L matching section. On the output, pins

11, 12 and 13, the placement of C11 is adjusted for best RF performance.

Layout is important for amplifier stability and RF performance. Ground vias must be located as close to circuit ground connections as possible. Power supply bypassing C3, C6, C9, and C10 must be included to reduce out-of-band gain and prevent spurious output.

**Evaluation Boards**

Evaluation boards are available for RF Monolithic Integrated Circuits by adding a "TF" suffix to the device type. For a complete list of currently available boards and ones in development for newly introduced product, please contact your local Motorola Distributor or Sales Office.



R1	1 k $\Omega$	C6	0.01 $\mu$ F	L2	22 nH
C1	3.3 pF	C10	1 $\mu$ F	T1	50 $\Omega$ , 13° @ 840 MHz
C2, C3, C8, C9	100 pF	C4, C5	1000 pF	T2	50 $\Omega$ , 8° @ 840 MHz
C11	8.2 pF	L1	10 nH	BOARD MATERIAL — GLASS/EPOXY, $\epsilon_r = 4.45$ , THICKNESS = 18 MIL	

Figure 1. Applications Circuit Configuration

### TYPICAL CHARACTERISTICS

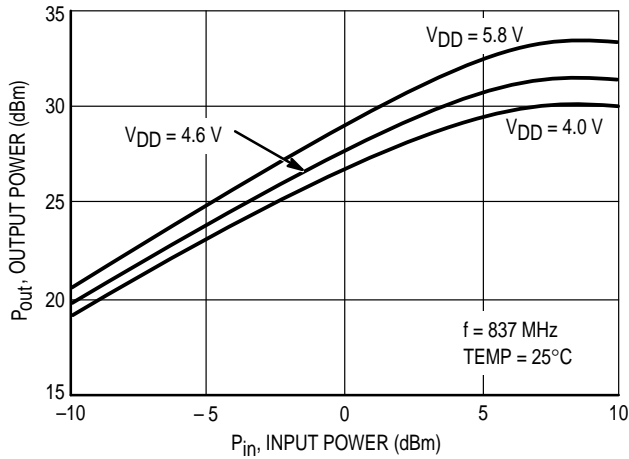


Figure 2. Output Power versus Input Power

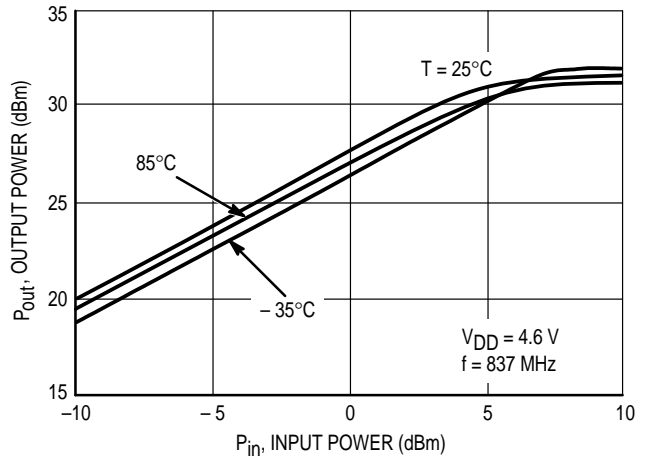
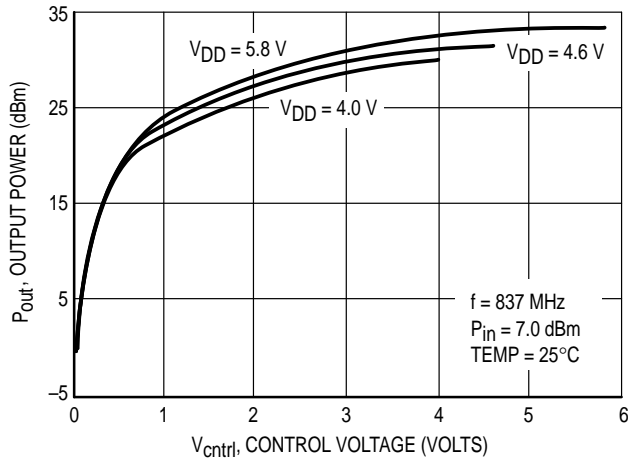
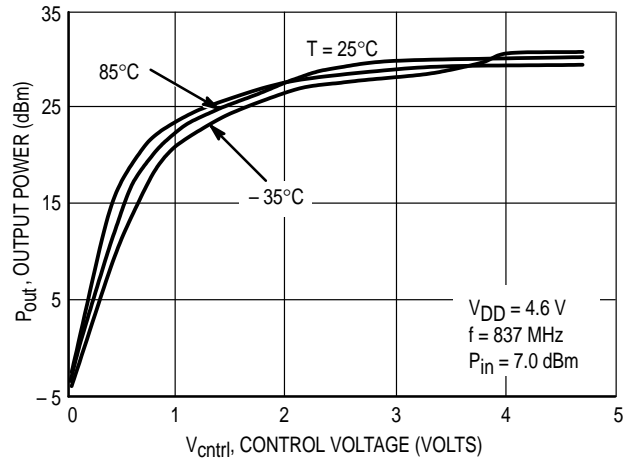


Figure 3. Output Power versus Input Power

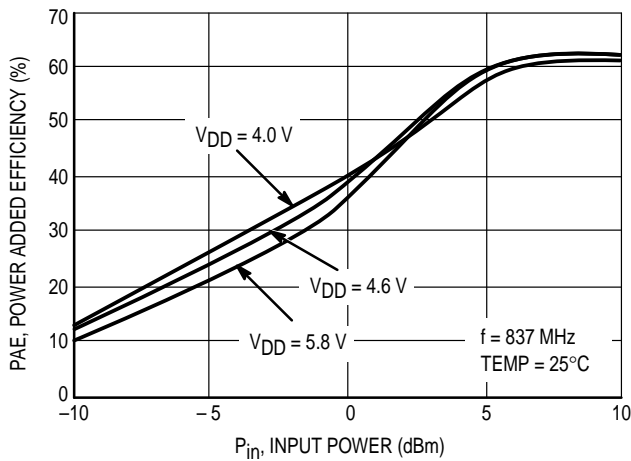
## TYPICAL CHARACTERISTICS



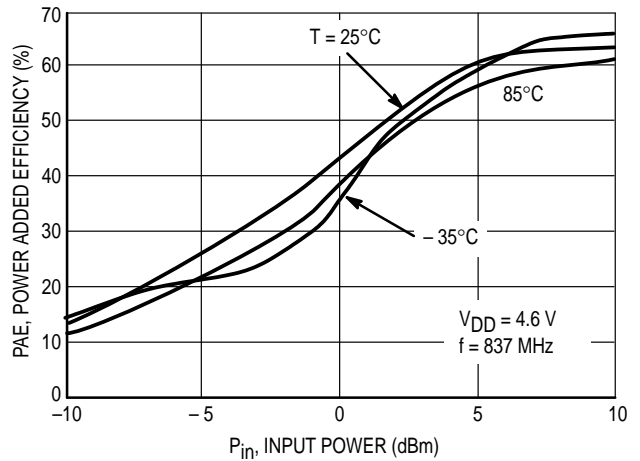
**Figure 4. Output Power versus Control Voltage**



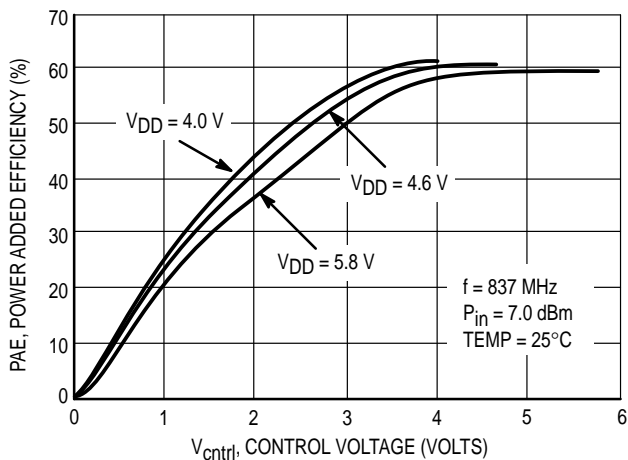
**Figure 5. Output Power versus Control Voltage**



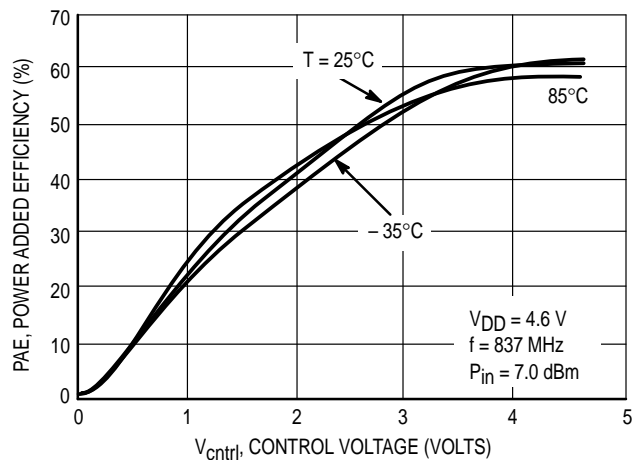
**Figure 6. Power Added Efficiency versus Input Power**



**Figure 7. Power Added Efficiency versus Input Power**



**Figure 8. Power Added Efficiency versus Control Voltage**



**Figure 9. Power Added Efficiency versus Control Voltage**

## TYPICAL CHARACTERISTICS

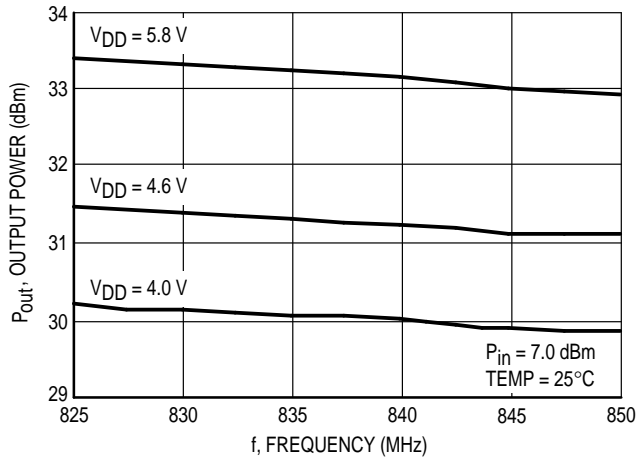


Figure 10. Output Power versus Frequency

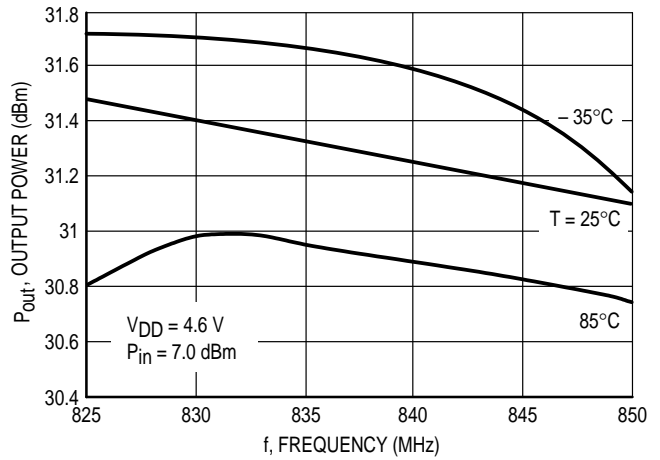


Figure 11. Output Power versus Frequency

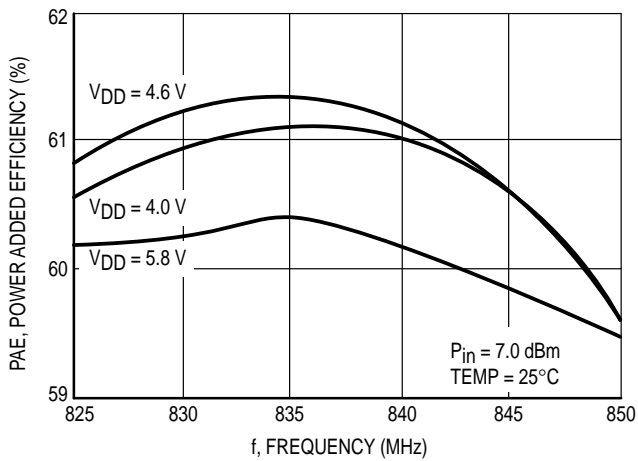


Figure 12. Power Added Efficiency versus Frequency

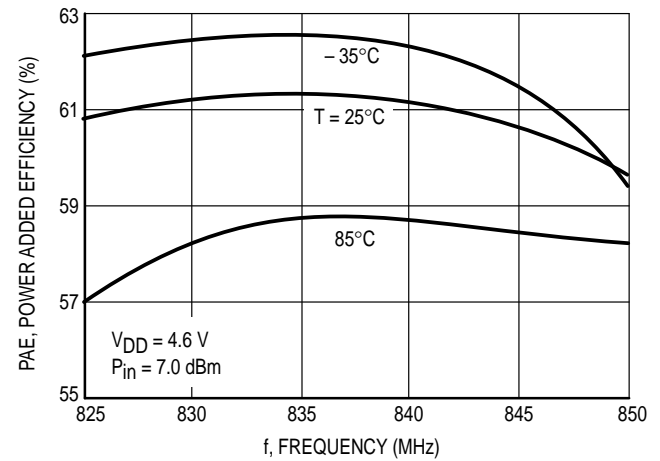


Figure 13. Power Added Efficiency versus Frequency

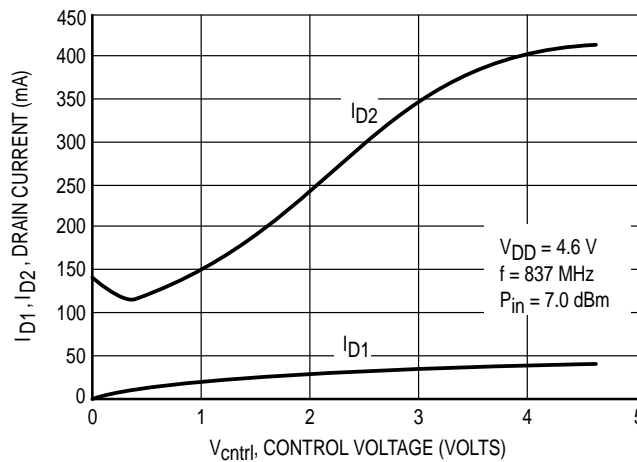
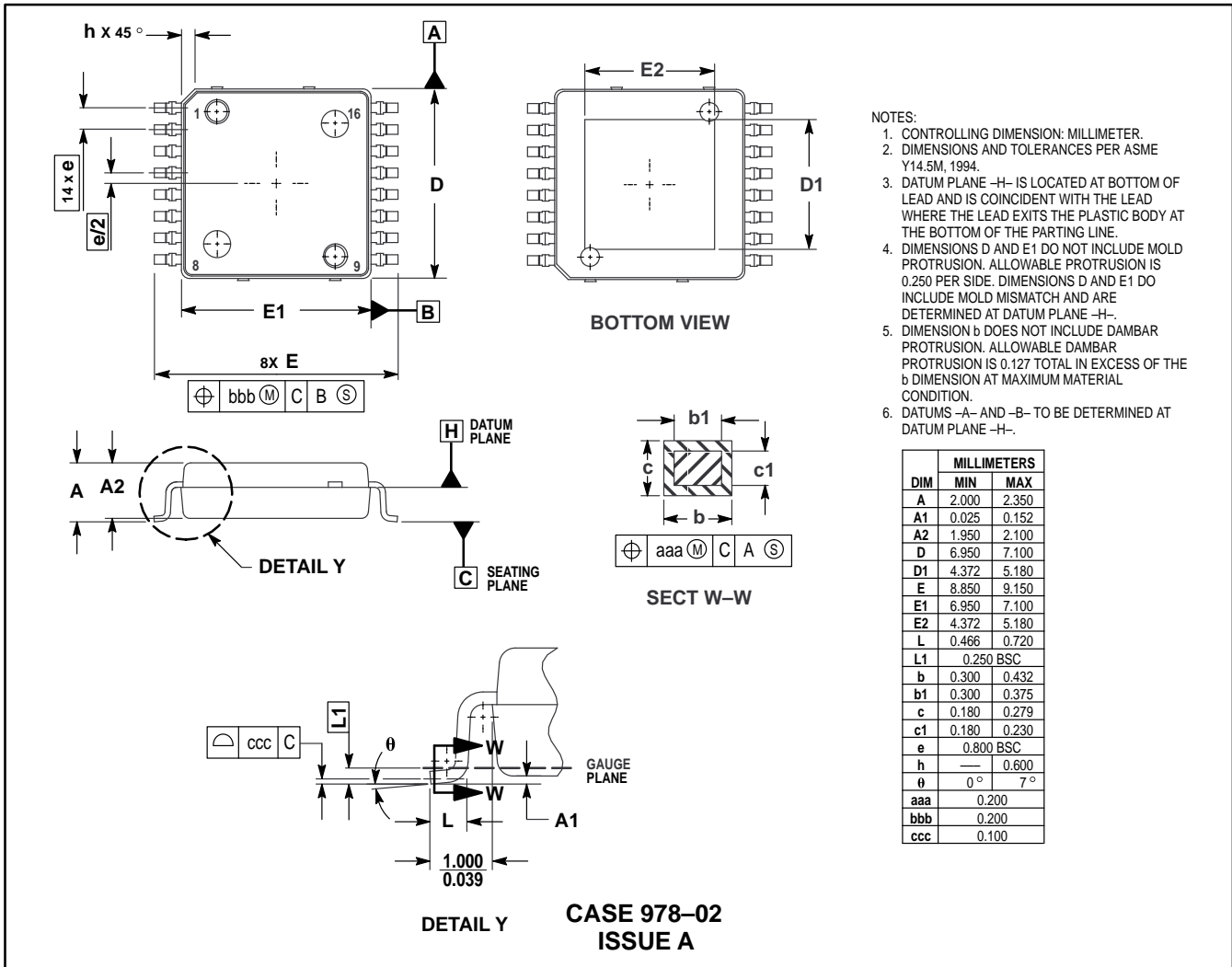


Figure 14. Drain Current versus Control Voltage

## PACKAGE DIMENSIONS



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