

# HD74HC112

Dual J-K Flip-Flops (with Preset and Clear)

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## Description

Each flip-flop has independent J, K, preset, clear and clock inputs and Q and  $\bar{Q}$  outputs. This device is edge sensitive to the clock input and change state on the negative going transition of the clock pulse. Clear and preset are independent of the clock and accomplished by a low logic level on the corresponding input.

## Features

- High Speed Operation:  $t_{pd}$  (Clock to Q) = 17 ns typ ( $C_L = 50$  pF)
- High Output Current: Fanout of 10 LSTTL Loads
- Wide Operating Voltage:  $V_{CC} = 2$  to 6 V
- Low Input Current: 1  $\mu$ A max
- Low Quiescent Supply Current:  $I_{CC}$  (static) = 2  $\mu$ A max ( $T_a = 25^\circ\text{C}$ )

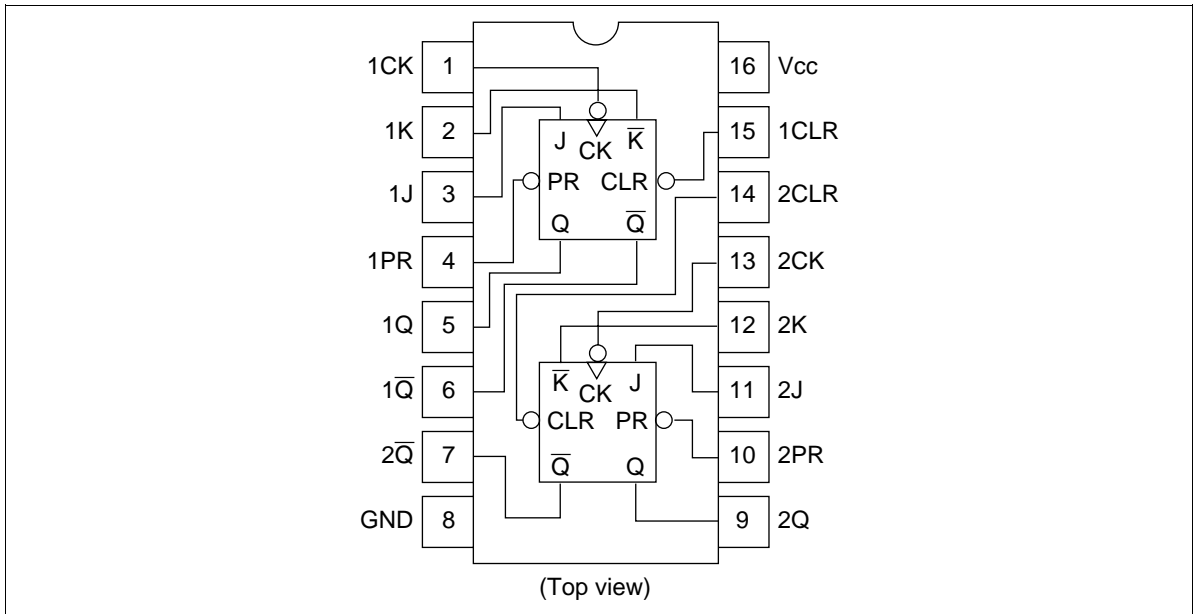
## Function Table

Inputs					Output	
Preset	Clear	Clock	J	K	Q	$\bar{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H* <sup>1</sup>	H* <sup>1</sup>
H	H		L	L	No Change	
H	H		L	H	L	H
H	H		H	L	H	L
H	H		H	H	Toggle	
H	H	L	X	X	No Change	
H	H	H	X	X	No Change	
H	H		X	X	No Change	

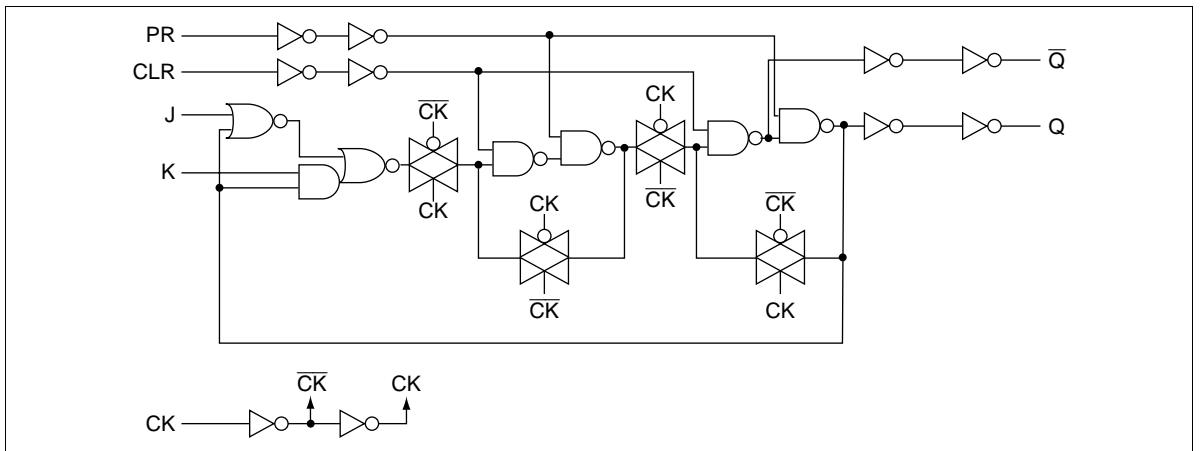
Note: 1. Q and  $\bar{Q}$  will remain HIGH as long as Preset and Clear are Low, but Q and  $\bar{Q}$  are unpredictable, if Preset and Clear go HIGH simultaneously.

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## Pin Arrangement



## Logic Diagram (1/2)



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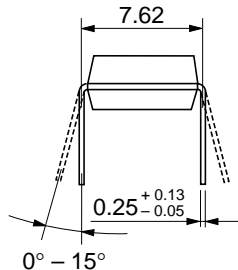
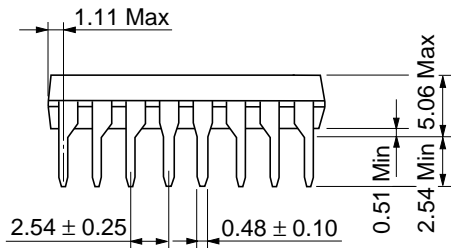
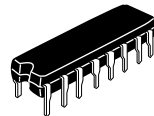
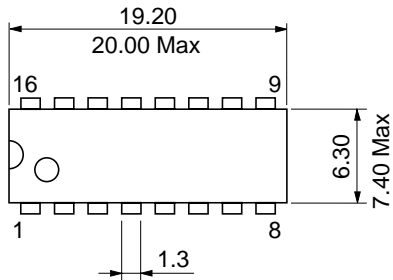
DC Characteristics

Item	Symbol	V <sub>CC</sub> (V)	Ta = 25°C			Ta = -40 to +85°C		Unit	Test Conditions	
			Min	Typ	Max	Min	Max			
Input voltage	V <sub>IH</sub>	2.0	1.5	—	—	1.5	—	V		
		4.5	3.15	—	—	3.15	—			
		6.0	4.2	—	—	4.2	—			
	V <sub>IL</sub>	2.0	—	—	0.5	—	0.5			V
		4.5	—	—	1.35	—	1.35			
		6.0	—	—	1.8	—	1.8			
Output voltage	V <sub>OH</sub>	2.0	1.9	2.0	—	1.9	—	V	Vin = V <sub>IH</sub> or V <sub>IL</sub> I <sub>OH</sub> = -20 μA	
		4.5	4.4	4.5	—	4.4	—			
		6.0	5.9	6.0	—	5.9	—			
		4.5	4.18	—	—	4.13	—			I <sub>OH</sub> = -4 mA
		6.0	5.68	—	—	5.63	—			I <sub>OH</sub> = -5.2 mA
		V <sub>OL</sub>	2.0	—	0.0	0.1	—			0.1
	4.5		—	0.0	0.1	—	0.1			
	6.0		—	0.0	0.1	—	0.1			
	4.5		—	—	0.26	—	0.33	I <sub>OL</sub> = 4 mA		
	6.0	—	—	0.26	—	0.33	I <sub>OL</sub> = 5.2 mA			
Input current	I <sub>in</sub>	6.0	—	—	±0.1	—	±1.0	μA	Vin = V <sub>CC</sub> or GND	
Quiescent supply current	I <sub>CC</sub>	6.0	—	—	2.0	—	20	μA	Vin = V <sub>CC</sub> or GND, I <sub>out</sub> = 0 μA	

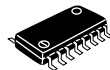
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## AC Characteristics ( $C_L = 50$ pF, Input $t_r = t_f = 6$ ns)

Item	Symbol	$V_{CC}$ (V)	$T_a = 25^\circ\text{C}$			$T_a = -40$ to $+85^\circ\text{C}$		Unit	Test Conditions	
			Min	Typ	Max	Min	Max			
Maximum clock frequency	$f_{max}$	2.0	—	—	6	—	5	MHz		
		4.5	—	—	30	—	24			
		6.0	—	—	35	—	28			
Propagation delay time	$t_{PLH}$	2.0	—	—	150	—	190	ns	Clock to Q or $\bar{Q}$	
		4.5	—	17	30	—	38			
		6.0	—	—	26	—	33			
	$t_{PHL}$	2.0	—	—	140	—	175		Clear to Q or $\bar{Q}$	
		4.5	—	15	28	—	35			
		6.0	—	—	24	—	30			
		2.0	—	—	140	—	175			Preset Q or $\bar{Q}$
		4.5	—	16	28	—	35			
		6.0	—	—	24	—	30			
	Pulse width	$t_w$	2.0	80	—	—	100	—	ns	Clock, Clear
			4.5	16	9	—	20	—		
			6.0	14	—	—	17	—		
Setup time	$t_{su}$	2.0	100	—	—	125	—	ns	Data to Clock	
		4.5	20	3	—	25	—			
		6.0	17	—	—	21	—			
Hold time	$t_h$	2.0	5	—	—	5	—	ns	Clock to Data	
		4.5	5	-2	—	5	—			
		6.0	5	—	—	5	—			
Removal time	$t_{rem}$	2.0	100	—	—	125	—	ns	Clear to Clock	
		4.5	20	2	—	25	—			
		6.0	17	—	—	21	—			
Output rise/fall time	$t_{TLH}$	2.0	—	—	75	—	95	ns		
		4.5	—	5	15	—	19			
	$t_{THL}$	6.0	—	—	13	—	16			
Input capacitance	$C_{in}$	—	—	5	10	—	10	pF		



Hitachi Code	DP-16
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	1.07 g



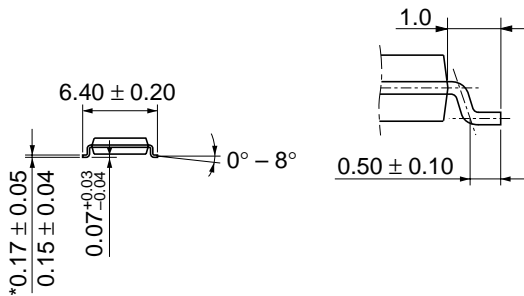
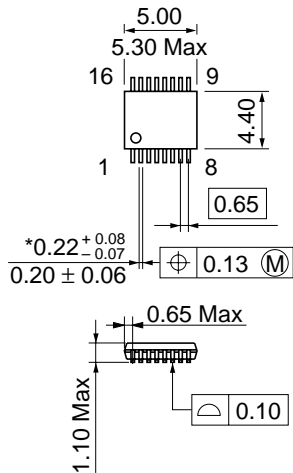
\*Dimension including the plating thickness  
Base material dimension

Hitachi Code	FP-16DA
JEDEC	—
EIAJ	Conforms
Weight (reference value)	0.24 g



\*Dimension including the plating thickness  
Base material dimension

Hitachi Code	FP-16DN
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	0.15 g



\*Dimension including the plating thickness  
 Base material dimension

Hitachi Code	TTP-16DA
JEDEC	—
EIAJ	—
Weight (reference value)	0.05 g



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