

Digital Filter for CD Player

Description

CXD1244S is a digital filter LSI with 4-times/8-times over sampling rate, developed for compact disc player.

Features

- Built-in 4-times/8-times sampling digital filter for 2 channels.
- Ripple within 0.00001dB
- Attenuation within -100dB(24.1k ).
- Noise shaping, Attenuator
- Soft muting, de-emphasis and a wide variety of built-in functions.

Application

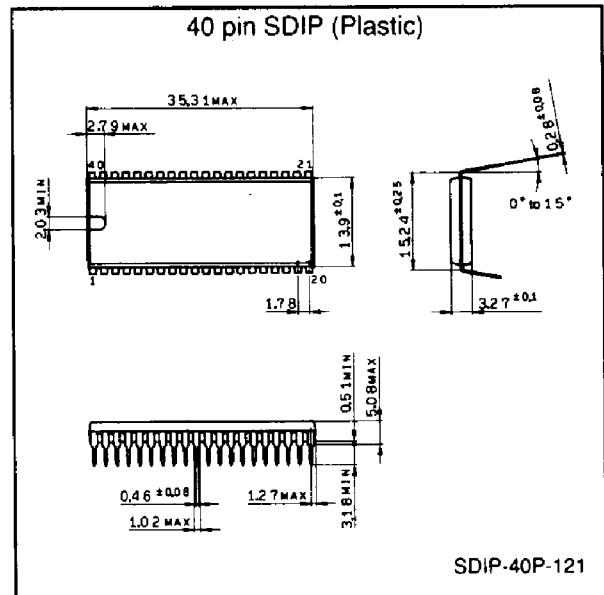
Compact disc player

Structure

Silicon gate CMOS IC

Package Outline

Unit: mm



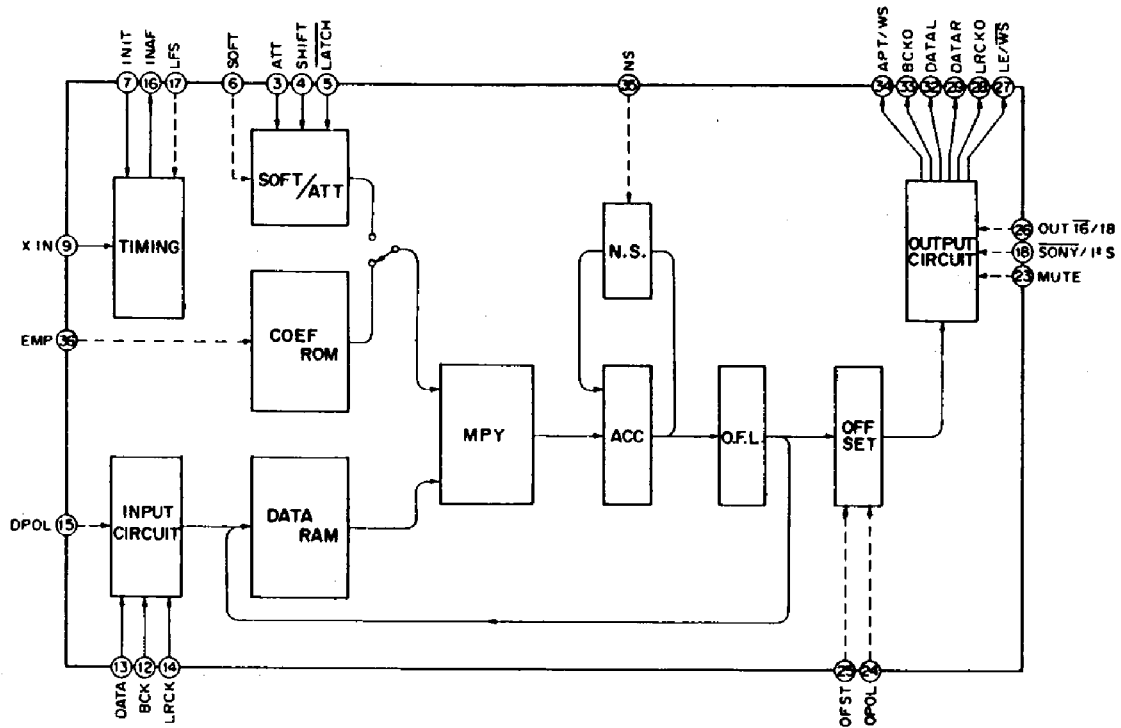
Absolute Maximum Ratings (Ta=25°C)

- Supply voltage  $V_{DD}$  -0.5 to +6.5 V
- Input voltage  $V_i$  -0.5 to  $V_{DD} + 0.5$  V
- Storage temperature  $T_{stg}$  -55 to +150 °C
- Allowable power dissipation  $P_D$  500 mW (Ta=60°C)

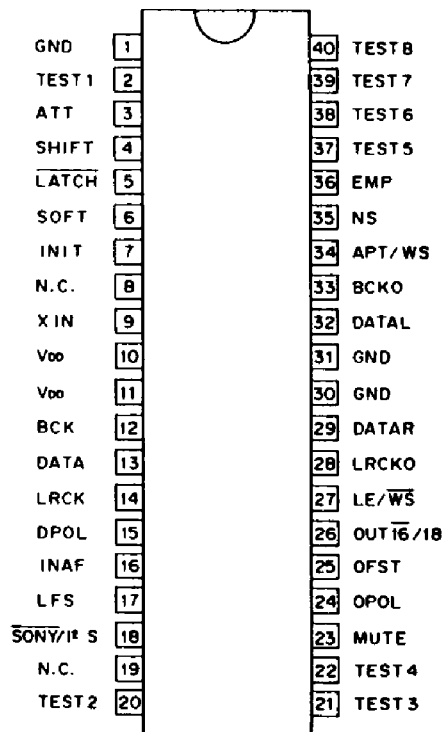
Recommended Operating Conditions

- Supply voltage  $V_{DD}$  4.75 to 5.25 V
- Operating temperature  $T_{opr}$  -10 to +60 °C
- OSC frequency  $f_x$  12.0 to 18.5 MHz

Block Diagram



Pin Configuration (Top View)



## Pin Description

No.	Symbol	I/O	Description
1	GND	—	
2	TEST1	I	Test pin (Normally fixed to "L" level)
3	ATT	I	Attenuate data input
4	SHIFT	I	Attenuate data shift clock input
5	LATCH	I	Attenuate data latch clock input
6	SOFT	I	Soft muting ON/OFF active at "H".
7	INIT	I	Synchronous again with the rising edge of this signal.
8	NC		
9	XIN	I	Master CLK input (f=384 Fs)
10, 11	V <sub>DD</sub>	—	Supply (+5V)
12	BCK	I	BCK input
13	DATA	I	Serial data input (2's complement)
14	LRCK	I	LRCK input
15	DPOL	I	Output data polarity "L" : non inversion "H" : inversion.
16	INAF	O	When I/O sync is missed "H" is output.
17	LFS	I	4Fs mode ON/OFF available at "H" only during I <sup>2</sup> S.
18	SONY/I <sup>2</sup> S	I	Output format specified at "L": Sony, at "H": I <sup>2</sup> S
19	NC	I	
20 to 22	TEST 2 to 4	I	Test pin (Normally fixed to 'L' level)
23	MUTE	I	Turns output to 0 or offset value. Active at 'H'.
24	DPOL	I	Offset polarity 'L': (-) 'H': (+)
25	OFST	I	Offset ON/OFF Active at 'H'
26	OUT16/18	I	Output data word length specified at 'L': 16 bit at 'H': 18 bit
27	LE/WS	O	LE output (Sony format)/WS output (I <sup>2</sup> S format)
28	LRCKO	O	LRCKO output
29	DATAR	O	Rch serial data output (2's complement)
30, 31	GND	—	
32	DATAL	O	Lch serial data output (2's complement)
33	BCKO	O	BCKO output
34	APT/WS	O	APT output (Sony format)/WS output (I <sup>2</sup> S format)
35	NS	I	Noise shaping ON/OFF Active at 'H'
36	EMP	I	Deemphasis ON/OFF Active at 'H'
37 to 40	TEST 5 to 8	I	Test pin (Normally fixed to 'L' level)

**Electrical Characteristics**  
**DC characteristics**

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
'H' input voltage (Except Shift, Latch)	V <sub>IH</sub>	—	0.76 V <sub>DD</sub>			V
'H' input voltage (Shift, Latch)						
'L' input voltage (Except Shift, Latch)	V <sub>IL</sub>	—			0.24 V <sub>DD</sub>	V
'L' input voltage (Shift, Latch)						
Input leak voltage	I <sub>LI</sub>	—			±5	μA
'H' output voltage	V <sub>OH</sub>	I <sub>o</sub> =-2mA	V <sub>DD</sub> -0.5			V
'L' output voltage	V <sub>OL</sub>	I <sub>o</sub> = 2mA			0.4	V

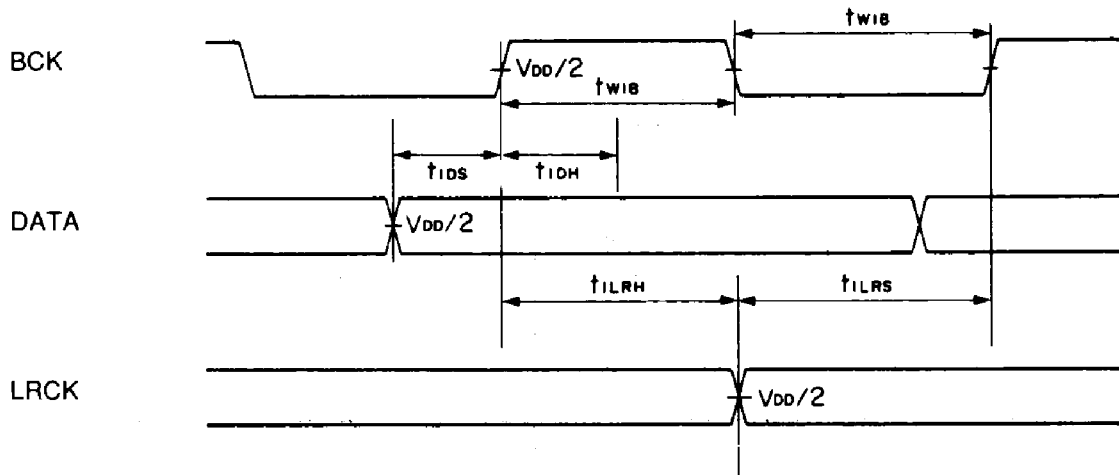
**AC characteristics**

Item	Symbol	Conditions	Min.	Typ.	Min.	Unit
OSC frequency	F <sub>x</sub>		12.0	16.9	18.5	MHz
Input BCK frequency	F <sub>BCK</sub>				2.31	MHz
Input BCK pulse width	t <sub>WIB</sub>	Defined at Duty	40°	50	60	%
Input data set up time	t <sub>IDS</sub>		20			ns
Input data hold time	t <sub>IDH</sub>		20			ns
Input LRCK set up time	t <sub>ILRS</sub>		50			ns
Input LRCK hold time	t <sub>ILRH</sub>		50			ns
Output BCK pulse width	t <sub>WOB</sub>	F <sub>x</sub> =16.9MHz Sony output mode 8Fs. BCK24 CL=50pF	40			ns
Output data set up time	t <sub>ODS</sub>		25			ns
Output data hold time	t <sub>ODH</sub>		25			ns
Output BCK pulse width	t <sub>WOB</sub>	F <sub>x</sub> =16.9MHz I <sup>2</sup> S output mode 8Fs. CL=50pF	60			ns
Output data set up time	t <sub>ODS</sub>		35			ns
Output data hold time	t <sub>ODH</sub>		35			ns
Output BCK pulse width	t <sub>WOB</sub>	F <sub>x</sub> =18.5MHz Sony output mode 8Fs. BCK24 CL=50pF	40			ns
Output data set up time	t <sub>ODS</sub>		20			ns
Output data hold time	t <sub>ODH</sub>		20			ns
Output BCK pulse width	t <sub>WOB</sub>	F <sub>x</sub> =16.9MHz I <sup>2</sup> S output mode 8Fs. CL=50pF	60			ns
Output data set up time	t <sub>ODS</sub>		32			ns
Output data hold time	t <sub>ODH</sub>		32			ns
Output signal Rise/Fall time	t <sub>R</sub> , t <sub>F</sub>	CL=50pF			30	ns

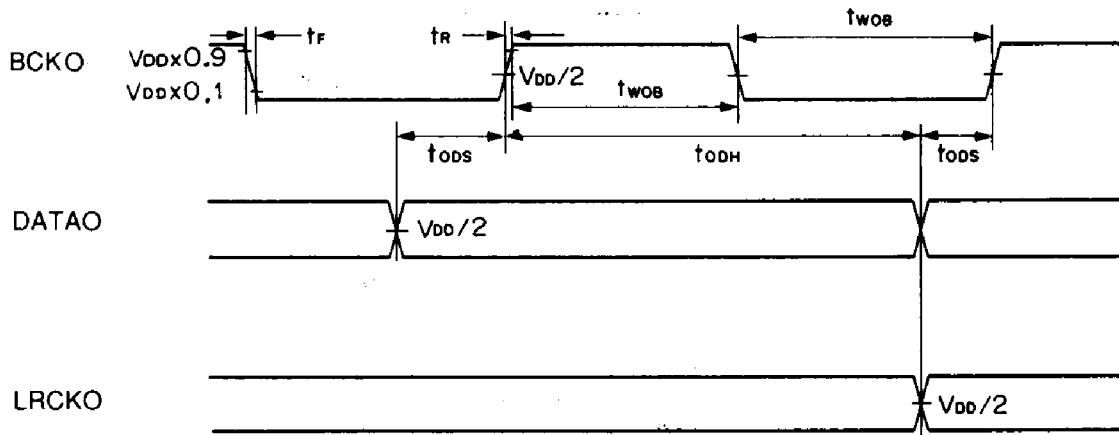
**Note)** Duty defined at 1/2 V<sub>DD</sub>, see the Timing Chart.

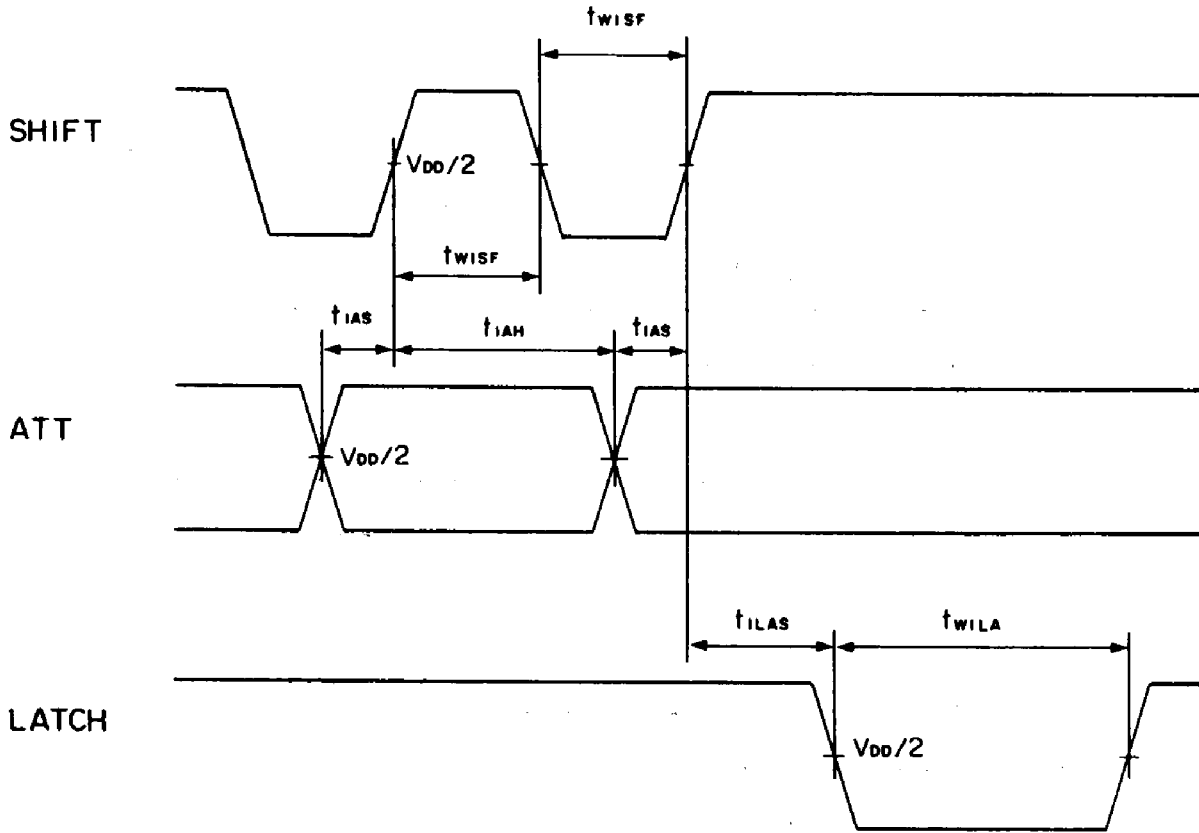
Timing Chart

• Input



• Output





Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Shift pulse width	$T_{WISF}$		600			ns
ATT set up time	$T_{IAS}$		300			ns
ATT hold time	$T_{IAH}$		600			ns
Latch pulse width	$T_{WILA}$		400			ns
Latch set up time	$T_{ILAS}$		500			ns

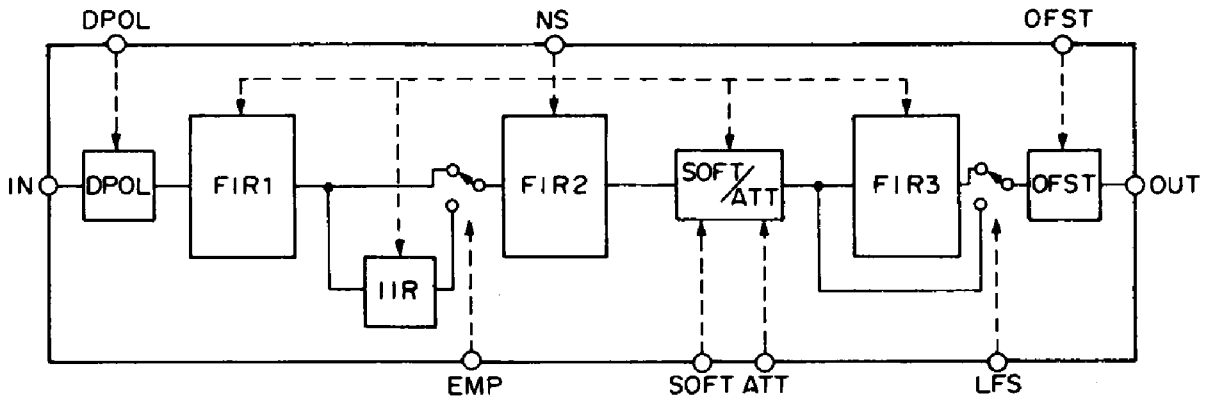
Schmitt input characteristics (SHIFT, LATCH)

	Min.	Typ.	Max.	Unit
$V_{T+}$	$0.54 \times V_{DD}$	3.0	$0.76 \times V_{DD}$	V
$V_{T-}$	$0.24 \times V_{DD}$	2.0	$0.43 \times V_{DD}$	V
HYST	0.52	1.0	—	V

**Functions**

**Conceptual block diagram**

An outline block diagram of this LSI is shown below.

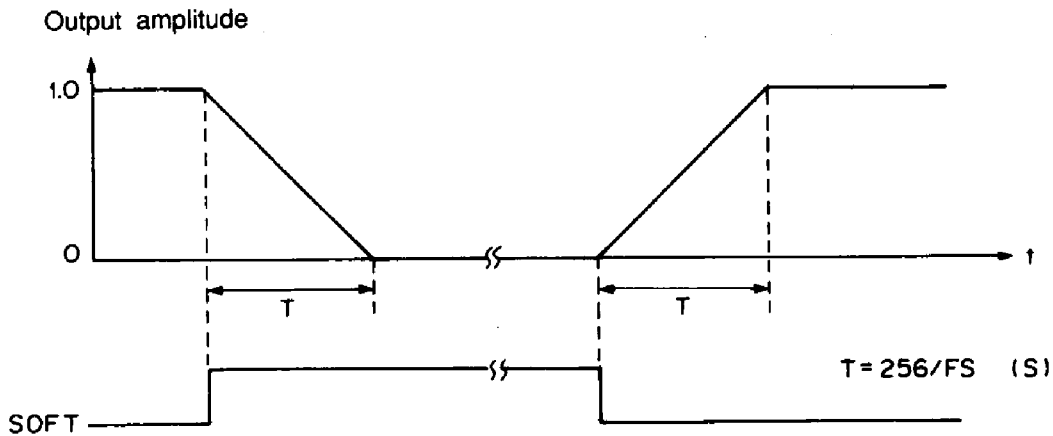


**1. Noise shaping**

For respective outputs FIR 1 to 3, IIR, SOFT/ATT figures are usually rounded off. However, by turning NS to "H" noise shaping can be applied. NS register is cleared when INIT is at "L" or NS at "L".

**2. Soft muting**

By turning SOFT to "H"/"L", data can be smoothly muted or demuted.



**3. Digital attenuator**

Can attenuate output data by means of transfer data from an external microcomputer.

1) Command and Audio output

Attenuate data is in 12 bit and can be set in 1024 steps.

The relationship between command and output is shown in the chart below.

Attenuate data	Audio output
400 (H)	0 dB
3FF (H)	-0.0085 dB
3FE (H)	-0.017 dB
⋮	⋮
001 (H)	-60.206 dB
000 (H)	-∞

The attenuate value from 001 (H) to 3FF (H) can be obtained through the following formula.

$$ATT = 20 \log \left[ \frac{\text{Input data}}{1024} \right] \text{ dB}$$

Example: Attenuate data for 3FA (H)

$$ATT = 20 \log \left[ \frac{1018}{1024} \right] \text{ dB} = -0.051 \text{ dB}$$

2) Attenuator operation

Suppose that there are pieces of attenuator data ATT1, ATT2 and ATT3 and that  $ATT1 > ATT3 > ATT2$  and that the place of attenuator data ATT1 is transferred first and ATT2 transferred next. If ATT2 is transferred before. The value of ATT2 is reached (during the state of A in Fig.1), the attenuation directly approaches the value of ATT2. If ATT3 is transferred before the value of ATT2 is reached (during the state of B or C in Fig.1), the attenuation is carried on from the value at the time (B or C) to approach the value of ATT3. Transition from one piece of attenuator data to another is the same as in the case of softmuting.

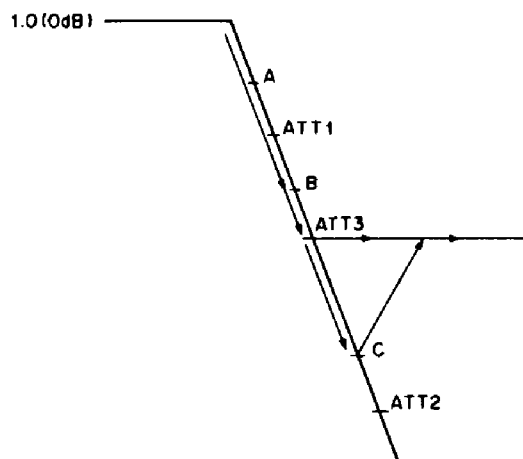
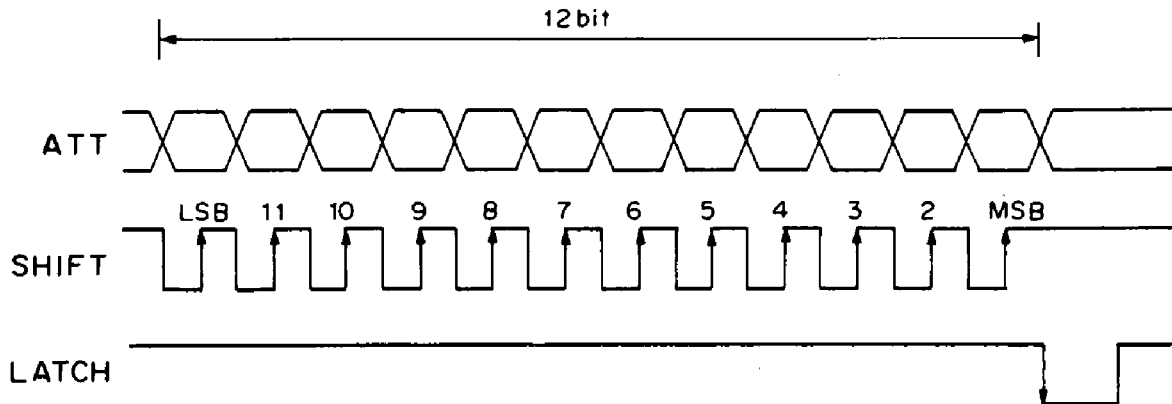


Fig.1 Transition from one attenuator value to another

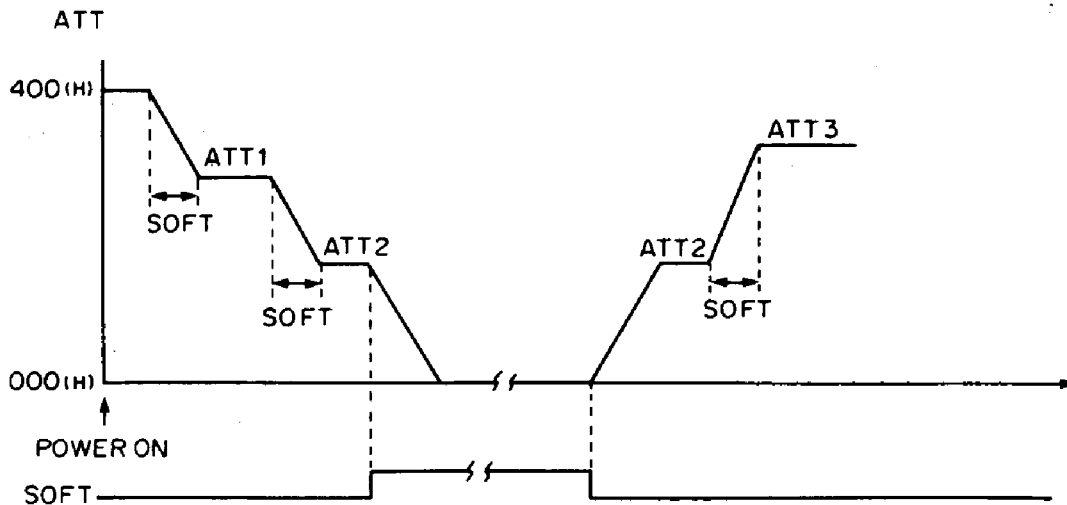


3) Input data timing

Attenuate function can be activated by means of ATT, Shift and Latch.  
Transfer format is indicated as follows.



- (1) ATT data is a 12 bit word length and LSB first transfer ATT data is available 000(H) to 400(H).
- (2) When Latch is at "L", ATT cannot be transferred.
- (3) With INIT at f, 400 (H) is set as ATT data.



- The transition from ATT1 to ATT2 takes place in soft muting operation.
- During attenuate operation SOFT is set to either ON or OFF, it turns back to the original ATT data.
- When ATT data =400 (H) Noise shaping is not applied regardless of NS ON or OFF.  
When ATT data =400 (H) Noise shaping is applied regardless of NS ON or OFF.

4. Digital deemphasis

By turning EMP to "H", deemphasis can be applied by means of IIR filter.  
Time constant of de-emphasis are  $\tau_1=50\mu s$  and  $\tau_2=15\mu s$  at  $f_s=44.1kHz$ .

**5. Offset**

Offset can be applied to the output data by means of OFST and OPOL.  
Pos/Neg selection of the offset value is possible as indicated in the following chart.

OFST	OPOL	OUT $\overline{16/18}$	Offset value
L	X	L	0000 (H)
L	X	H	00000 (H)
H	H	L	02AA (H)
H	H	H	02AA8 (H)
H	L	L	FD55 (H)
H	L	H	FD554 (H)

**6. Muting**

By turning MUTE to "H" or INIT to "L", the output can be muted. Then, the offset value set at the offset is output. When INIT is at "L", 0 data is input to this LSI.

**7. Data polarity**

Inversion and non inversion of the output data can be selected by means of DPOL.

When DPOL is at "H", non inversion.  
when DPOL is at "L", inversion.

**8. I/O synchronizing circuit****1) Principle**

A window featuring 10 internal system clocks (XIN/2) is set. The sync circuit observes whether the rising edge (LRCK $\uparrow$ ) of LRCK that is input, has entered the window or not. When the power supply is turned on, should LRCK $\uparrow$  be out of the window the sync circuit stops the internal processing in timing with the center of the window. Synchronously with the appearance of the next LRCK $\uparrow$  the processing is started. Through this operation synchronization between the exterior system and this LSI is established.

**2) Resynchronization by means of INIT**

Even when LRCK $\uparrow$  is inside the window but located close to one of the 2 edges of the window, the sync may miss with the mingling of external noise or other Re sync operation. To this effect it is necessary to apply resync, without fault, after supply is turned on. ReSync operation is executed with the INIT $\uparrow$  timing. Sync. circuit is initialized and LRCK is located in the center of the window.

Moreover, when the sync falls out of the window, INAF output turns to "H" level.

**3) Non synchronous MUTE**

When INAF is at H, 0 data is output regardless of offset ON/OFF.

**9. Output format**

The output format of this LSI can be selected as shown in the chart below.

	8Fs		4Fs
	SONY	I <sup>2</sup> S	I <sup>2</sup> S
(Control pin)			
SONY/I <sup>2</sup> S	'L'	'H'	←
LEFS	no effect	'L'	'H'
OUT <sup>16/18</sup>	At will	no effect	←
(Output pin)			
8LRCK	8LRCK	4LRCK	←
LRCKO	24BCK	16BCK	←
BCKO	DATAL	} Staggered	MIX data
DATAL	DATAR		DATA
DATAR	APT	WS	←
APT/WS			
LE/WS	LE	WS	←

**10. I/O signal latch timing**

1) Input

DPOL, SOFT, MUTE, OFST, OPOL, INIT,  $\overline{\text{SONY/I}^2\text{S}}$ , LFS, OUT<sup>16/18</sup>, NS, EMP

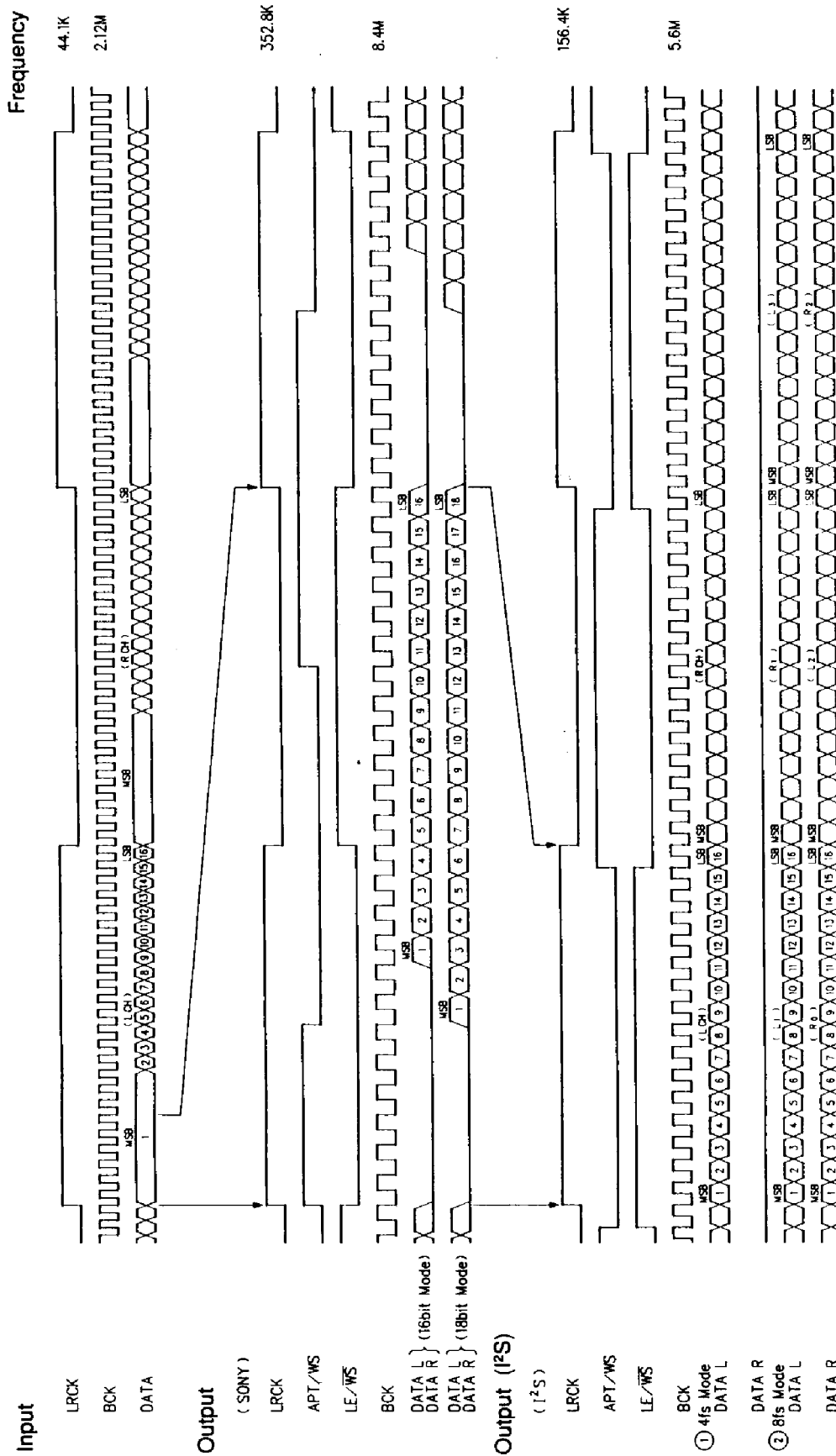
The above indicated input signals are latched by means of internal clocks equivalent to LRCK.

2) Output

LRCKO, DATAL, DATAR, APT.WS, LE/WS

The above indicated output signals are latched by means of internal clocks equivalent to BCKO.

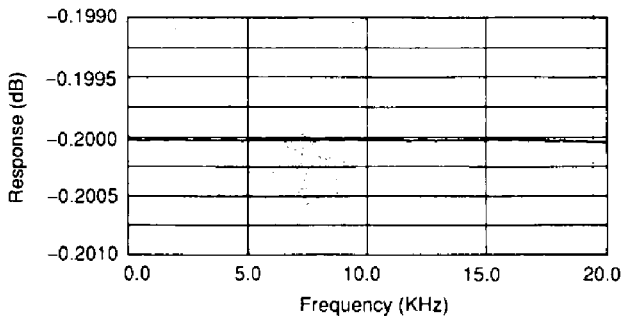
I/O Timing Chart



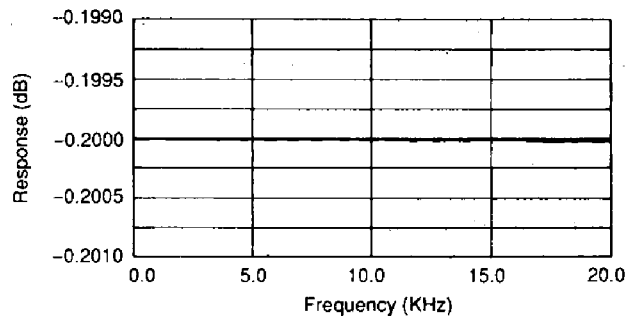
Filter characteristics (for 4Fs)

Filter characteristics (for 8Fs)

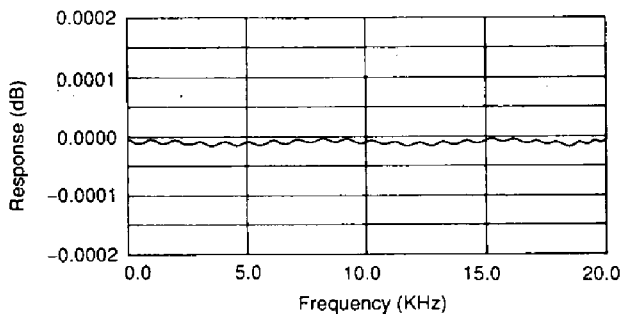
Frequency characteristics



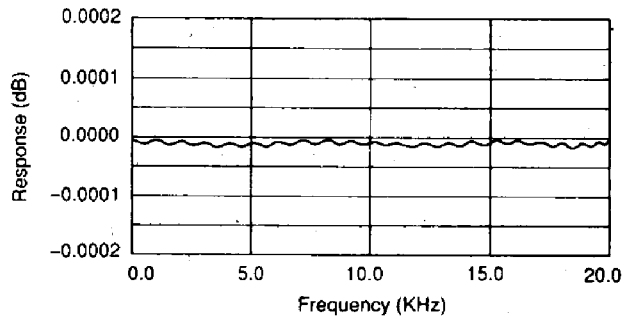
Frequency characteristics



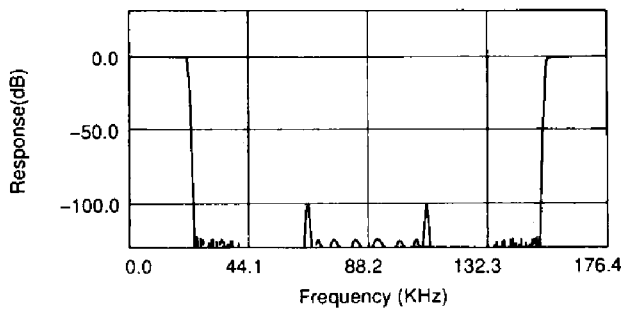
Ripple characteristics



Ripple characteristics



Attenuate



Attenuate

