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Power SEMiconductors Italian COrporation

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PHASE CONTROL THYRISTOR

AT503

Repetitive voltage up to **1600 V**
Mean on-state current **445 A**
Surge current **6.4 kA**

FINAL SPECIFICATION

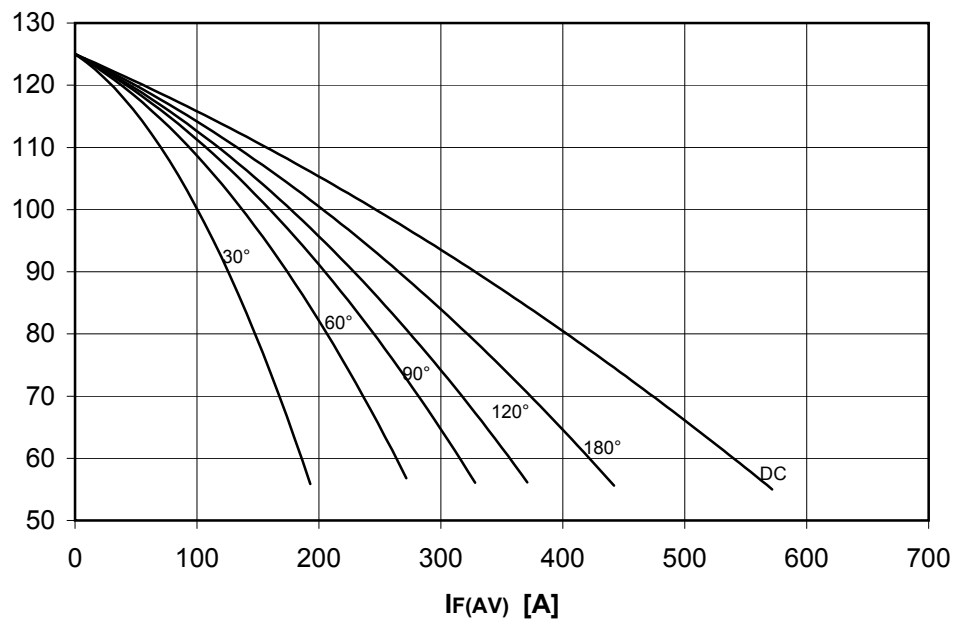
gen 03 - ISSUE : 03

Symbol	Characteristic	Conditions	T _j [°C]	Value	Unit
BLOCKING					
V _{RRM}	Repetitive peak reverse voltage		125	1600	V
V _{RSM}	Non-repetitive peak reverse voltage		125	1700	V
V _{DRM}	Repetitive peak off-state voltage		125	1600	V
I _{RRM}	Repetitive peak reverse current	V=V _{RRM}	125	30	mA
I _{DRM}	Repetitive peak off-state current	V=V _{DRM}	125	30	mA
CONDUCTING					
I _{T (AV)}	Mean on-state current	180° sin, 50 Hz, Th=55°C, double side cooled		445	A
I _{T (AV)}	Mean on-state current	180° sin, 50 Hz, Tc=85°C, double side cooled		355	A
I _{TSM}	Surge on-state current	sine wave, 10 ms	125	6.4	kA
I ² t	I ² t	without reverse voltage		205 x1E3	A²s
V _T	On-state voltage	On-state current = 800 A	25	1.45	V
V _{T(TO)}	Threshold voltage		125	0.9	V
r _T	On-state slope resistance		125	0.680	mohm
SWITCHING					
di/dt	Critical rate of rise of on-state current, min.	From 75% V _{DRM} up to 500 A, gate 10V 5ohm	125	200	A/μs
dv/dt	Critical rate of rise of off-state voltage, min.	Linear ramp up to 70% of V _{DRM}	125	500	V/μs
t _d	Gate controlled delay time, typical	V _D =100V, gate source 10V, 10 ohm, tr=.5 μs	25	1.6	μs
t _q	Circuit commutated turn-off time, typical	dV/dt = 20 V/μs linear up to 75% V _{DRM}	125	200	μs
Q _{rr}	Reverse recovery charge	di/dt=-20 A/μs, I= 330A			μC
I _{rr}	Peak reverse recovery current	V _R = 50 V			A
I _H	Holding current, typical	V _D =5V, gate open circuit	25	300	mA
I _L	Latching current, typical	V _D =5V, tp=30μs	25	700	mA
GATE					
V _{GT}	Gate trigger voltage	V _D =5V	25	3.5	V
I _{GT}	Gate trigger current	V _D =5V	25	200	mA
V _{GD}	Non-trigger gate voltage, min.	V _D =V _{DRM}	125	0.25	V
V _{FGM}	Peak gate voltage (forward)			20	V
I _{FGM}	Peak gate current			8	A
V _{RGM}	Peak gate voltage (reverse)			5	V
P _{GM}	Peak gate power dissipation	Pulse width 100 μs		75	W
P _G	Average gate power dissipation			1	W
MOUNTING					
R _{th(j-h)}	Thermal impedance, DC	Junction to heatsink, double side cooled		95	°C/kW
R _{th(c-h)}	Thermal impedance	Case to heatsink, double side cooled		20	°C/kW
T _j	Operating junction temperature			-30 / 125	°C
F	Mounting force			4.9 / 5.9	kN
	Mass			55	g
ORDERING INFORMATION : AT503 S 16 standard specification ☐ VDRM&VRRM/100 ☐					

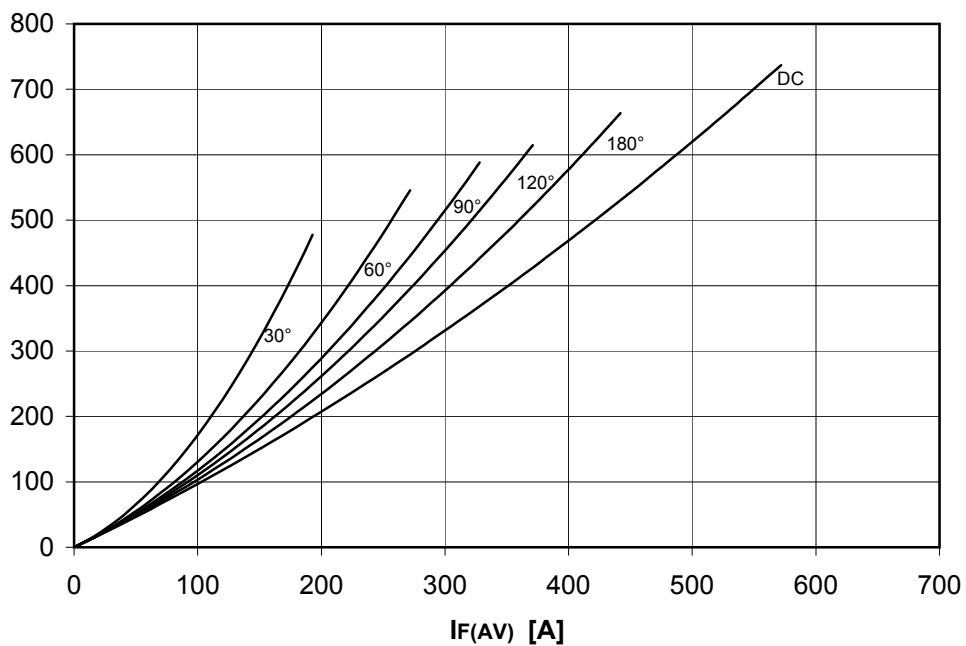
DISSIPATION CHARACTERISTICS

SQUARE WAVE

Th [°C]



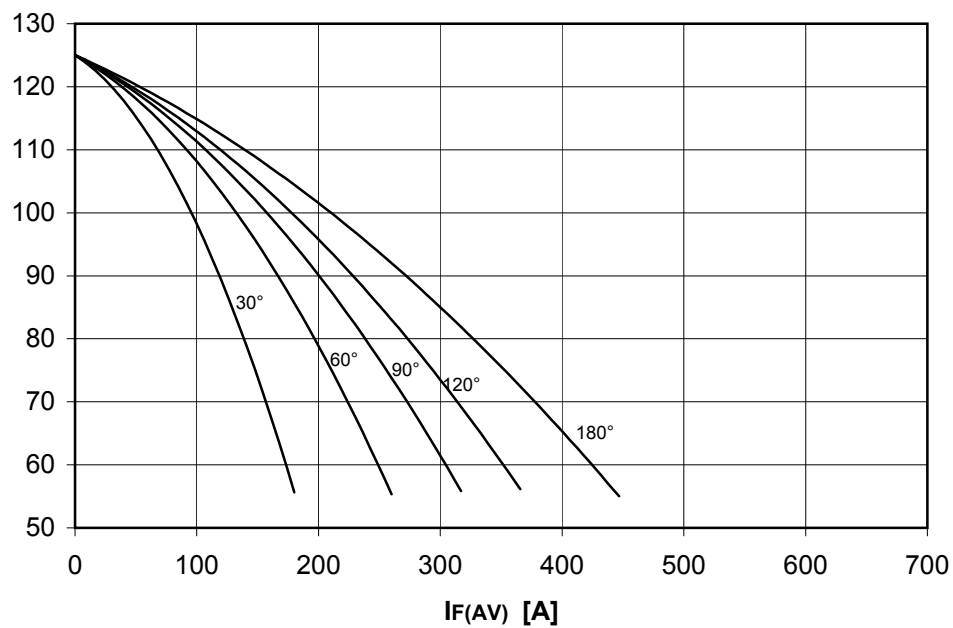
PF(AV) [W]



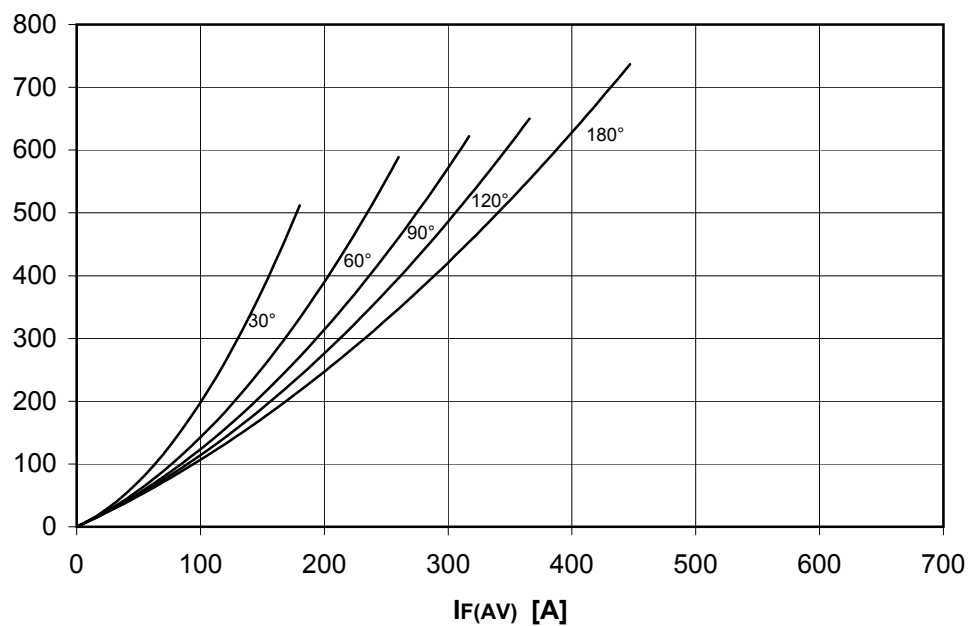
DISSIPATION CHARACTERISTICS

SINE WAVE

Th [°C]



PF(AV) [W]

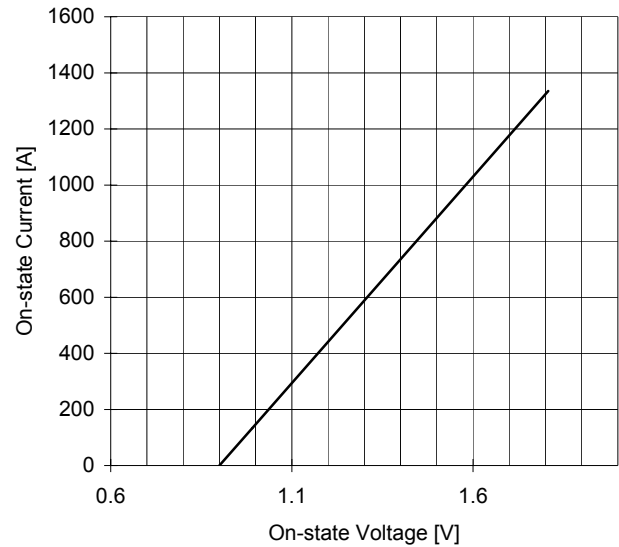


AT503 PHASE CONTROL THYRISTOR

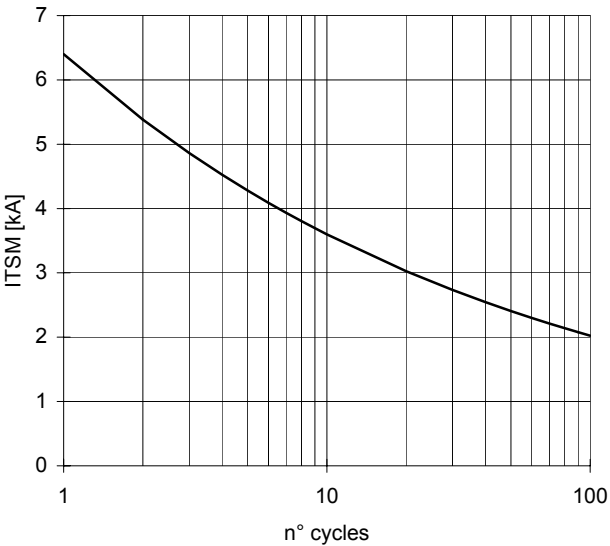


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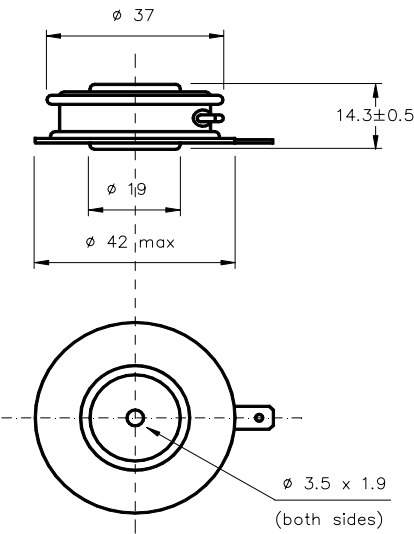
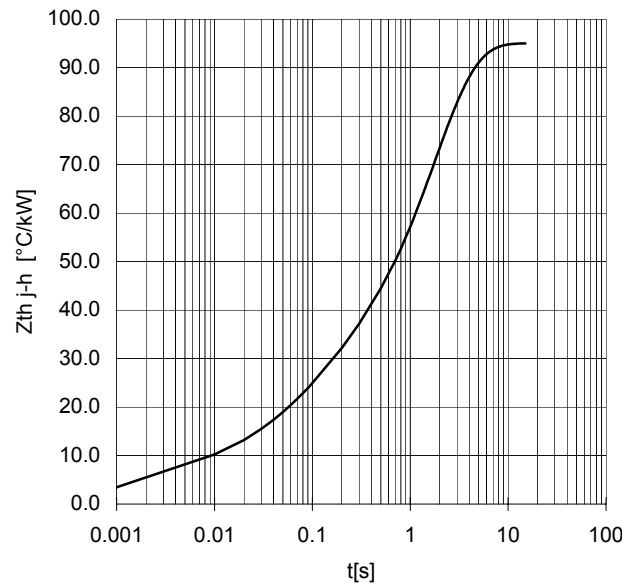
ON-STATE CHARACTERISTIC
Tj = 125 °C



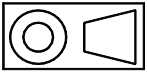
SURGE CHARACTERISTIC
Tj = 125 °C



TRANSIENT THERMAL IMPEDANCE
DOUBLE SIDE COOLED



Dimensions
in mm



Cathode terminal type DIN 46244 - A 4.8 - 0.8

Gate terminal type AMP 60598 - 1

All the characteristics given in this data sheet are guaranteed only with uniform clamping force, cleaned and lubricated heatsink, surfaces with flatness < .03 mm and roughness < 2 µm.
In the interest of product improvement POSEICO S.p.A. reserves the right to change any data given in this data sheet at any time without previous notice.
If not stated otherwise the maximum value of ratings (symbols over shaded background) and characteristics is reported.

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