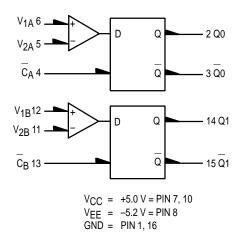
Dual A/D Converter

The MC1650 and the MC1651 are very high speed comparators utilizing differential amplifier inputs to sense analog signals above or below a reference level. An output latch provides a unique sample-hold feature. The MC1650 provides high impedance Darlington inputs, while the MC1651 is a lower impedance option, with higher input slew rate and higher speed capability.

The clock <u>inputs</u> (C_a and C_b) operate from MECL III or MECL 10,000 digital levels. When C_a is at a logic high level, Q0 <u>will</u> be at a logic high level provided that $V_1 > V_2$ (V_1 is more positive than V_2). Q0 is the logic complement of Q0. When the clock input goes to a low logic level, the outputs are latched in their present state.

Assessment of the performance differences between the MC1650 and the MC1651 may be based upon the relative behaviors shown in Figures 4 and 7.

LOGIC DIAGRAM



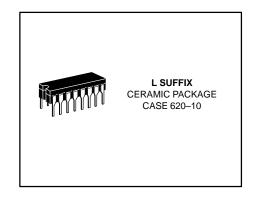
- P_D = 330 mW typ/pkg (No Load)
- $t_{pd} = 3.5 \text{ ns typ (MC1650)}$
- = 3.0 ns typ (MC1651)
- Input Slew Rate = 350 V/μs (MC1650) = 500 V/μs (MC1651)
- Differential Input Voltage: 5.0 V (-30°C to +85°C)
- Common Mode Range:
 - -3.0 V to +2.5 V (-30°C to +85°C) (MC1651)
 - -2.5 V to +3.0 V (-30°C to +85°C) (MC1650)
- Resolution: ≤ 20 mV (-30°C to +85°C)
- Drives 50 Ω lines

Number at end of terminal denotes pin number for L package (Case 620).

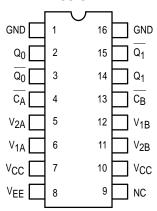
TRUTH TABLE

C	V ₁ , V ₂	Q0 _{n + 1}	Q0 _{n + 1}
Н	$V_1 > V_2$	Н	L
Н	V ₁ < V ₂	L	Н
L	х х	Q0 _n	Q0 _n

MC1650 MC1651



PIN ASSIGNMENT





ELECTRICAL CHARACTERISTICS

			Test Limits						
			-30)°C	+25°C		+85°C		
Characteristic		Symbol	Min	Max	Min	Max	Min	Max	Unit
Power Supply Drain Current	Positive Negative	ICC IE				25* 55*			mAdc
Input Current	MC1650 MC1651	l _{in}				10 40			μAdc
Input Leakage Current	MC1650 MC1651	IR				7.0 10.0			μAdc
Clock Input Current		linH				350			
Output Voltage	Logic 1	VOH	-1.045	-0.875	-0.960	-0.810	-0.890	-0.700	Vdc
Output Voltage	Logic 0	V _{OL}	-1.890	-1.650	-1.850	-1.620	-1.830	-1.575	Vdc
Threshold Voltage (Note 2.)	Logic 1	VOHA	-1.065		-0.980		-0.910		Vdc
Threshold Voltage (Note 2.)	Logic 0	VOLA		-1.630		-1.600		-1.555	Vdc

All data is for 1/2 MC1650 or MC1651, except data marked (*) which refers to the entire package.
 These tests are done in order indicated. See Figure 5.
 Maximum Power Supply Voltages (beyond which device life may be impaired): |V_{EE}| + |V_{CC}| ≥ 12 Vdc.

4.	All Temperature	V _{A3}	V _{A4}	V _{A5}	V _{A6}
	MC1650	+3.0	+2.98	-2.5	-2.48
	MC1651	+2.5	+2.48	-3.0	-2.98

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ELECTRICAL CHARACTERISTICS (continued)

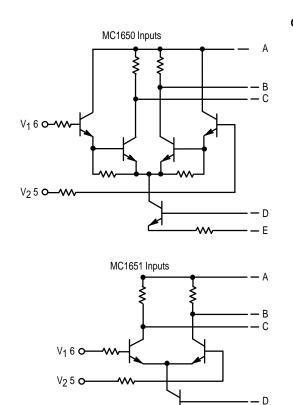
					TES	ST VOLTA	AGE VAL	UES (Vo	lts)				
@ Test Tem	perature	V _{IHmax}	V _{ILmin}	V _{IHAmin}	V _{ILAmax}	V _{A1}	V _{A2}	V _{A3}	V _{A4}	V _{A5}	V _{A6}	V _{CC} 3.	VEE3.
	-30°C	-0.875	-1.890	-1.180	-1.515	+0.02	+0.02					+5.0	-5.2
	+25°C	-0.810	-1.850	-1.095	-1.485	+0.02	+0.02]	See N	lote 4.		+5.0	-5.2
	+85°C	-0.700	-1.830	-1.025	-1.440	+0.02	+0.02]				+5.0	-5.2
				TEST VOL	TAGE APPL	IED TO F	PINS LIST	ED BEL	ow				
Characteristic	Symbol	V _{IHmax}	V _{ILmin}	V _{IHAmin}	V _{ILAmax}	V _{A1}	V _{A2}	V _{A3}	V _{A4}	V _{A5}	V _{A6}	(V _C	CC) nd
Power Supply Pos Drain Current Neg	ICC IE	4,13	4,13			6,12 6,12							1,16 1,16
Input Current MC1650 MC1651	l _{in}	4	13			12		6				1,5,1	11,16
Input Leakage MC1650 Current MC1651	IR	4	13			12				6		1,5,1	11,16
Clock Input Current	l _{in} H	4	13			6,12						1,5,1	11,16
Output Voltage Logic 1	Voн	4,13				6,12	5,11 6,12	6,12	5,11	5,11	6,12	1,6,1 1, 1,	11,16 12,16 16 16 11,16
						5,11	·	5,11	6,12	6,12	5,11	1,6,1 1,	12,16 16 16
Output Voltage Logic 0	VOL	4,13				5,11 6,12	6,12	5,11	6,12	6,12	5,11	1,6,1 1, 1,	11,16 12,16 16 16 11,16
						0,12	5,11	6,12	5,11	5,11	6,12	1,6,1 1,	12,16 12,16 16 16
Threshold Logic 1 Voltage Note 2.	VOHA		13	4	4	6	6 6					1,5	,16
Threshold Logic 0 Voltage Note 2.	VOLA		13	4	4	6	6 6					1,5	,16

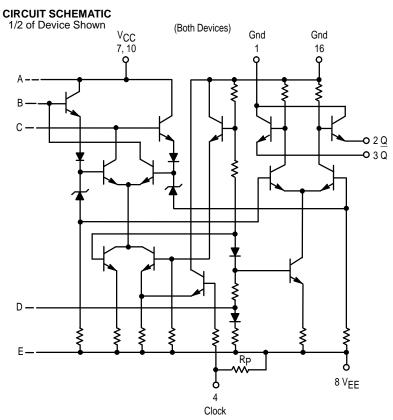
- All data is for 1/2 MC1650 or MC1651, except data marked (*) which refers to the entire package.
 These tests are done in order indicated. See Figure 5.
- 3. Maximum Power Supply Voltages (beyond which device life may be impaired): |V_{EE}| + |V_{CC}| ≥ 12 Vdc.

4.	All Temperature	V _{A3}	V _{A4}	V _{A5}	V _{A6}
	MC1650	+3.0	+2.98	-2.5	-2.48
	MC1651	+2.5	+2.48	-3.0	-2.98

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.

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	SWITCHING TEST VOLTAGE VALUES										
@ Test		(Volts)									
Temperature	V _{R1}	V _{R2}	V _{R3}	٧χ	V _{XX}	v _{CC} 1	ν _{EE} 1				
−30°C	+2.0			+1.04	+2.0	+7.0	-3.2				
+25°C	+2.0	See N	Note 4	+1.11	+2.0	+7.0	-3.2				
+85°C	+2.0			+1.19	+2.0	+7.0	-3.2				

		-30	0°C	+2	5°C	+85	5°C		Conditions	
Characteristic	Symbol	Min	Max	Min	Max	Min	Max	Unit	(See Figures 1–3)	
Switching Times Propagation Delay	^t pd	2.0	5.0	2.0	5.0	2.0	5.7	ns	V_{R1} to V_2 , V_X to Clock, P_1 to V_1 , or, V_{R2} to V_2 , V_X to Clock, P_2 to V_1 , or,	
(50% to 50%) V-Input									V _{R3} to V ₂ , V _X to Clock, P ₃ to V ₁ .	
Clock ²		2.0	4.7	2.0	4.7	2.0	5.2		V_{R1} to V_2 , P_1 to V_1 and P_4 to Clock, or, V_{R1} to V_1 , P_1 to V_2 and P_4 to Clock.	
Clock Enable ³	tsetup	_	_	2.5	_	_	_	ns	V= - to V= B - to V - B - to Clock	
Clock Aperture ³	tap	_	_	1.5	_	١		ns	V _{R1} to V ₂ , P ₁ to V ₁ , P ₄ to Clock	
Rise Time (10% to 90%)	t+	1.0	3.5	1.0	3.5	1.0	3.8	ns	Ve to V. Ve to Clock B. to V.	
Fall Time (10% to 90%)	t-	1.0	3.0	1.0	3.0	1.0	3.3	ns	V_R to V_2 , V_X to Clock, P_1 to V_1 .	

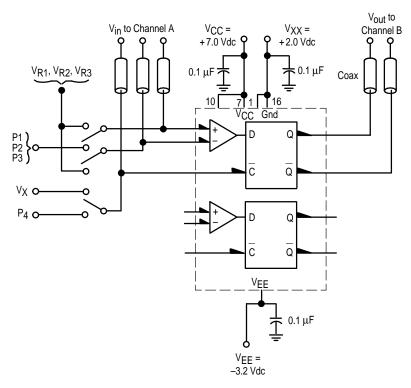
NOTES:

- 1. Maximum Power Supply Voltages (beyond which device life may be impaired:
- V_{CC}|+ |V_{EE}| ≥ 12 Vdc. 2. Unused clock inputs may be tied to ground.
- 3. See Figure 3.

4.	All Temperatures	V _{R2}	V _{R3}
	MC1650	+4.9	-0.4
	MC1651	+4.4	-0.9

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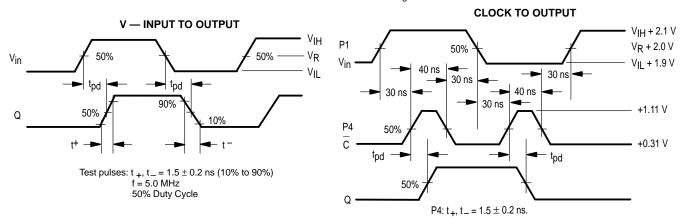
FIGURE 1 — SWITCHING TIME TEST CIRCUIT @ 25°C



Note: All power supply and logic levels are shown shifted 2.0 volts positive.
50 ohm termination to ground located in each scope channel input.
All input and output cables to the scope are equal lengths of 50 ohm coaxial cable.

FIGURE 2 — SWITCHING AND PROPAGATION WAVEFORMS @ 25°C

The pulse levels shown are used to check ac parameters over the full common-mode range.

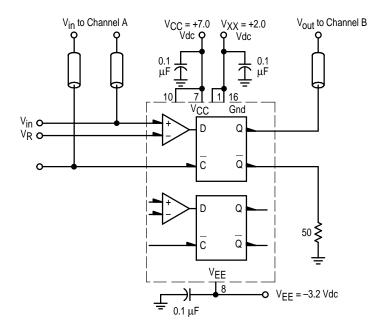


TEST PULSE LEVELS

	Р	1	P	22	P3		
	MC1650	MC1651	MC1650	MC1651	MC1650	MC1651	
VIH	+2.1 V	+2.1 V	+5.0 V	+4.5 V	-0.3 V	-0.8 V	
٧R	+2.0 V	+2.0 V	+4.9 V	+4.4 V	-0.4 V	-0.9 V	
V_{IL}	+1.9 V	+1.9 V	+4.8 V	+4.3 V	–0.5 V	-1.0 V	

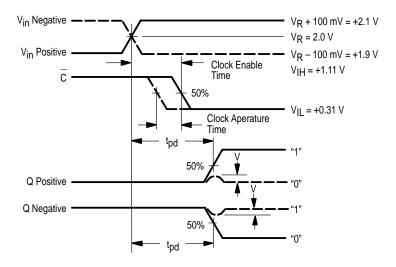
MOTOROLA 4–338

FIGURE 3 — CLOCK ENABLE AND APERTURE TIME TEST CIRCUIT AND WAVEFORMS @ 25°C



50 ohm termination to ground located in each scope channel input. All input and output cables to the scope are equal lengths of 50 ohms coaxial cable.

ANALOG SIGNAL POSITIVE AND NEGATIVE SLEW CASE



Clock enable time = minimum time between analog and clock signal such that output switches, and tpd (analog to Q) is not degraded by more than 200 ps.

Clock aperture time = time difference between clock enable time and time that output does not switch and
V is less than 150 mV.

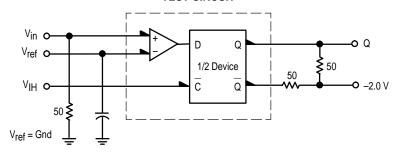
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Note: All power supply and logic levels are shown shifted 2.0 volts positive.

MOTOROLA

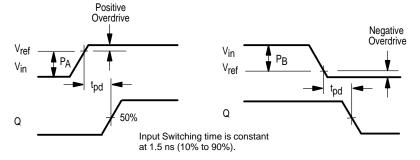
FIGURE 4 — PROPAGATION DELAY (t_{pd}) versus INPUT PULSE AMPLITUDE AND CONSTANT OVERDRIVE

TEST CIRCUIT

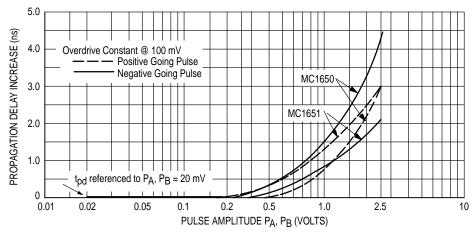


POSITIVE PULSE DIAGRAM

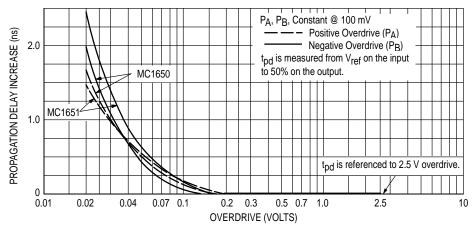
NEGATIVE PULSE DIAGRAM



PROPAGATION DELAY versus PULSE AMPLITUDE



PROPAGATION DELAY versus OVERDRIVE



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FIGURE 5 — LOGIC THRESHOLD TESTS (WAVEFORM SEQUENCE DIAGRAM)

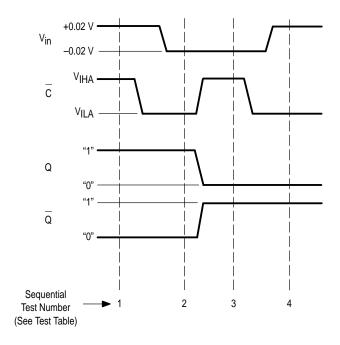
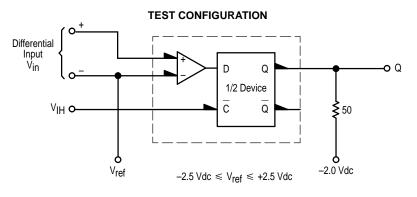
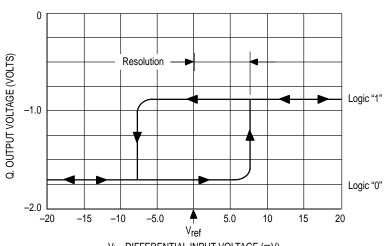


FIGURE 6 — TRANSFER CHARACTERISTICS (Q versus Vin)



TYPICAL TRANSFER CURVES



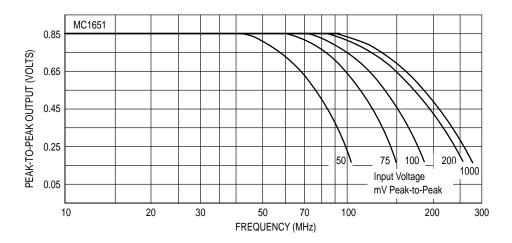
 $V_{\mbox{\scriptsize in,}} \mbox{ DIFFERENTIAL INPUT VOLTAGE (mV)}$

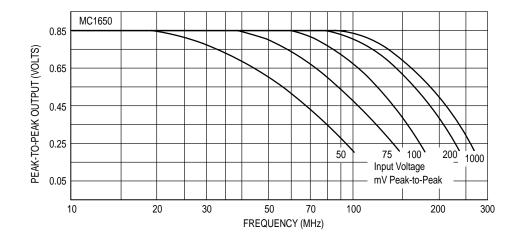
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FIGURE 7 — OUTPUT VOLTAGE SWING versus FREQUENCY

(A) TEST CIRCUIT V1 V2 1/2 Device C Q 1/2 Device C Q -2.0 Vdc

(B) TYPICAL OUTPUT LOGIC SWING versus FREQUENCY

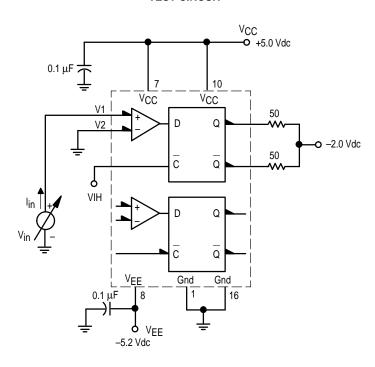


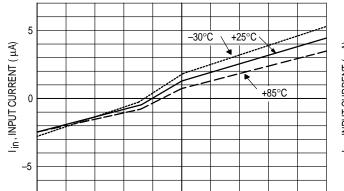


MOTOROLA 4–342

FIGURE 8 — INPUT CURRENT versus INPUT VOLTAGE

TEST CIRCUIT





V_{in}, INPUT VOLTAGE (VOLTS)

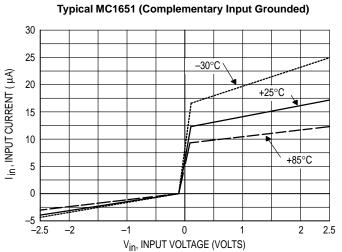
+2

+2.5

-2.5

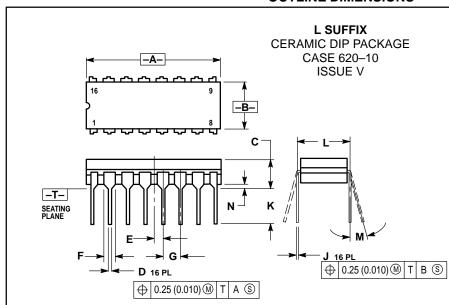
-2

Typical MC1650 (Complementary Input Grounded)



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OUTLINE DIMENSIONS



NOTES:

- DIMENSIONING AND TOLERANCING PER
 ANSI Y14 5M 1982
- ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.
- 3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
- DIMENSION F MAY NARROW TO 0.76 (0.030)
 WHERE THE LEAD ENTERS THE CERAMIC
 RODY

	INC	HES	MILLIN	IETERS
DIM	MIN	MAX	MIN	MAX
Α	0.750	0.785	19.05	19.93
В	0.240	0.295	6.10	7.49
С		0.200		5.08
D	0.015	0.020	0.39	0.50
Е	0.050	BSC	1.27	BSC
F	0.055	0.065	1.40	1.65
G	0.100	BSC	2.54	BSC
Н	0.008	0.015	0.21	0.38
K	0.125	0.170	3.18	4.31
L	0.300	BSC	7.62	BSC
М	0°	15°	0 °	15°
N	0.020	0.040	0.51	1.01

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MC1650/D