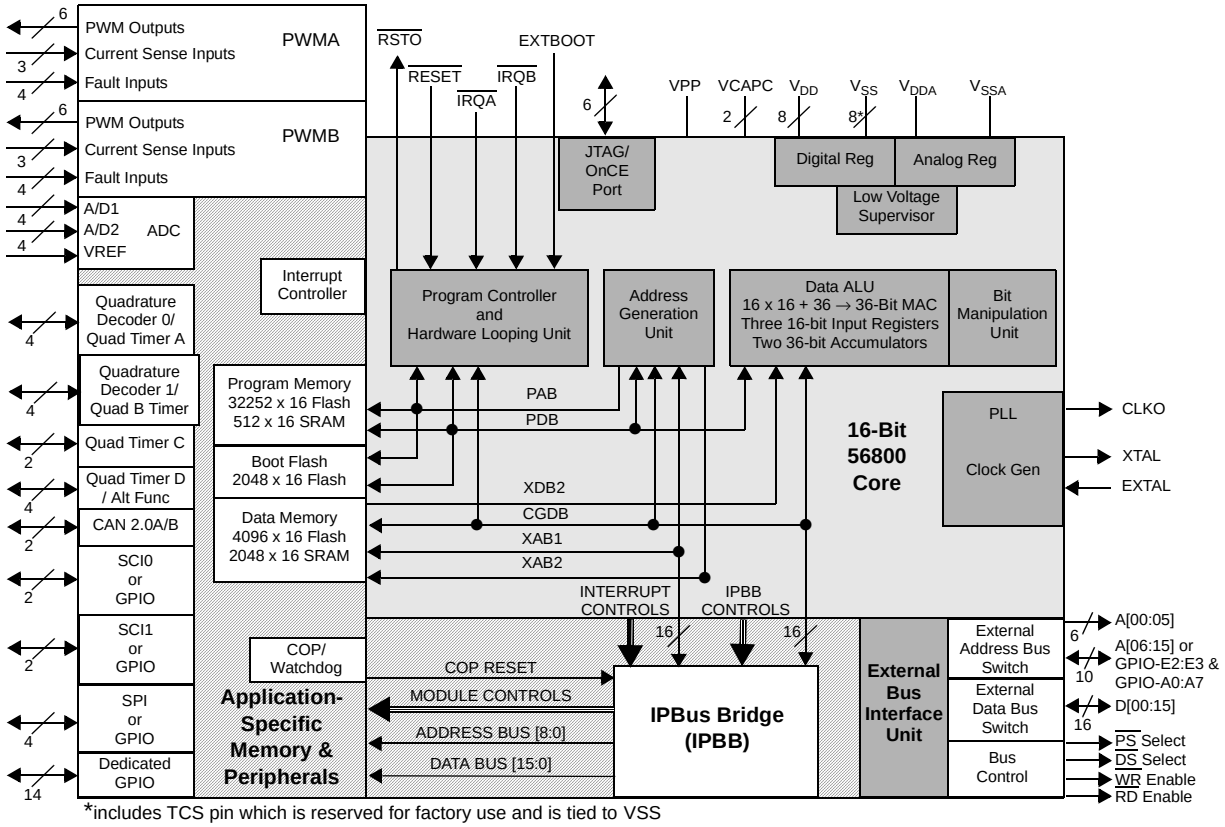
DSP56F805/D
Rev. 12.0, 02/2004

56F805

Technical Data

56F805 16-bit Hybrid Controller

- Up to 40 MIPS at 80MHz core frequency
- DSP and MCU functionality in a unified, C-efficient architecture
- Hardware DO and REP loops
- MCU-friendly instruction set supports both DSP and controller functions: MAC, bit manipulation unit, 14 addressing modes
- 31.5K × 16-bit words Program Flash
- 512 × 16-bit words Program RAM
- 4K × 16-bit words Data Flash
- 2K × 16-bit words Data RAM
- 2K × 16-bit words Boot Flash
- Up to 64K × 16-bit words each of external Program and Data memory
- Two 6-channel PWM Modules
- Two 4-channel, 12-bit ADCs
- Two Quadrature Decoders
- CAN 2.0 B Module
- Two Serial Communication Interfaces (SCIs)
- Serial Peripheral Interface (SPI)
- Up to four General Purpose Quad Timers
- JTAG/OnCE^{TM} port for debugging
- 14 Dedicated and 18 Shared GPIO lines
- 144-pin LQFP Package



*includes TCS pin which is reserved for factory use and is tied to VSS

Figure 1. 56F805 Block Diagram

Part 1 Overview

1.1 56F805 Features

1.1.1 Digital Signal Processing Core

- Efficient 16-bit 56800 family hybrid controller engine with dual Harvard architecture
- As many as 40 Million Instructions Per Second (MIPS) at 80MHz core frequency
- Single-cycle 16 × 16-bit parallel Multiplier-Accumulator (MAC)
- Two 36-bit accumulators, including extension bits
- 16-bit bidirectional barrel shifter
- Parallel instruction set with unique DSP addressing modes
- Hardware DO and REP loops
- Three internal address buses and one external address bus
- Four internal data buses and one external data bus
- Instruction set supports both DSP and controller functions
- Controller style addressing modes and instructions for compact code
- Efficient C compiler and local variable support
- Software subroutine and interrupt stack with depth limited only by memory
- JTAG/OnCE debug programming interface

1.1.2 Memory

- Harvard architecture permits as many as three simultaneous accesses to Program and Data memory
- On-chip memory including a low-cost, high-volume Flash solution
  - 31.5K × 16 bit words of Program Flash
  - 512 × 16-bit words of Program RAM
  - 4K× 16-bit words of Data Flash
  - 2K × 16-bit words of Data RAM
  - 2K × 16-bit words of Boot Flash
- Off-chip memory expansion capabilities programmable for 0, 4, 8, or 12 wait states
  - As much as 64K × 16 bits of Data memory
  - As much as 64K × 16 bits of Program memory

1.1.3 Peripheral Circuits for 56F805

- Two Pulse Width Modulator modules each with six PWM outputs, three Current Sense inputs, and four Fault inputs, fault tolerant design with dead time insertion; supports both center- and edge-aligned modes
- Two 12-bit Analog-to-Digital Converters (ADC) which support two simultaneous conversions; ADC and PWM modules can be synchronized
- Two Quadrature Decoders each with four inputs or two additional Quad Timers

- Two General Purpose Quad Timers totaling six pins: Timer C with two pins and Timer D with four pins
- CAN 2.0 B Module with 2-pin port for transmit and receive
- Two Serial Communication Interfaces, each with two pins (or four additional GPIO lines)
- Serial Peripheral Interface (SPI) with configurable four-pin port (or four additional GPIO lines)
- 14 dedicated General Purpose I/O (GPIO) pins, 18 multiplexed GPIO pins
- Computer Operating Properly (COP) watchdog timer
- Two dedicated external interrupt pins
- External reset input pin for hardware reset
- External reset output pin for system reset
- JTAG/On-Chip Emulation (OnCE™) module for unobtrusive, processor speed-independent debugging
- Software-programmable, Phase Locked Loop-based frequency synthesizer for the hybrid controller core clock

1.1.4 Energy Information

- Fabricated in high-density CMOS with 5V-tolerant, TTL-compatible digital inputs
- Uses a single 3.3V power supply
- On-chip regulators for digital and analog circuitry to lower cost and reduce noise
- Wait and Stop modes available

1.2 56F805 Description

The 56F805 is a member of the 56800 core-based family of hybrid controllers. It combines, on a single chip, the processing power of a DSP and the functionality of a microcontroller with a flexible set of peripherals to create an extremely cost-effective solution. Because of its low cost, configuration flexibility, and compact program code, the 56F805 is well-suited for many applications. The 56F805 includes many peripherals that are especially useful for applications such as motion control, smart appliances, steppers, encoders, tachometers, limit switches, power supply and control, automotive control, engine management, noise suppression, remote utility metering, and industrial control for power, lighting, and automation.

The 56800 core is based on a Harvard-style architecture consisting of three execution units operating in parallel, allowing as many as six operations per instruction cycle. The microprocessor-style programming model and optimized instruction set allow straightforward generation of efficient, compact code for both MCU and DSP applications. The instruction set is also highly efficient for C compilers to enable rapid development of optimized control applications.

The 56F805 supports program execution from either internal or external memories. Two data operands can be accessed from the on-chip Data RAM per instruction cycle. The 56F805 also provides two external dedicated interrupt lines, and up to 32 General Purpose Input/Output (GPIO) lines, depending on peripheral configuration.

The 56F805 controller includes 31.5K words (16-bit) of Program Flash and 4K words of Data Flash (each programmable through the JTAG port) with 512 words of Program RAM and 2K words of Data RAM. It also supports program execution from external memory (64K).

The 56F805 incorporates a total of 2K words of Boot Flash for easy customer-inclusion of field-programmable software routines that can be used to program the main Program and Data Flash memory areas. Both Program and Data Flash memories can be independently bulk-erased or erased in page sizes of 256 words. The Boot Flash memory can also be either bulk- or page-erased.

Key application-specific features of the 56F805 include the two Pulse Width Modulator (PWM) modules. These modules each incorporate three complementary, individually programmable PWM signal outputs (each module is also capable of supporting six independent PWM functions for a total of 12 PWM outputs) to enhance motor control functionality. Complementary operation permits programmable dead time insertion, distortion correction via current sensing by software, and separate top and bottom output polarity control. The up-counter value is programmable to support a continuously variable PWM frequency. Edge- and center-aligned synchronous pulse width control (0% to 100% modulation) is supported. The device is capable of controlling most motor types: ACIM (AC Induction Motors), both BDC and BLDC (Brush and Brushless DC motors), SRM and VRM (Switched and Variable Reluctance Motors), and stepper motors. The PWMs incorporate fault protection and cycle-by-cycle current limiting with sufficient output drive capability to directly drive standard opto-isolators. A “smoke-inhibit”, write-once protection feature for key parameters and a patented PWM waveform distortion correction circuit are also provided. Each PWM is double-buffered and includes interrupt controls to permit integral reload rates to be programmable from 1 to 16. The PWM modules provide a reference output to synchronize the ADCs.

The 56F805 incorporates two separate Quadrature Decoders capable of capturing all four transitions on the two-phase inputs, permitting generation of a number proportional to actual position. Speed computation capabilities accommodate both fast and slow moving shafts. The integrated watchdog timer in the Quadrature Decoder can be programmed with a time-out value to alarm when no shaft motion is detected. Each input is filtered to ensure only true transitions are recorded.

This controller also provides a full set of standard programmable peripherals that include two Serial Communications Interfaces (SCI), one Serial Peripheral Interface (SPI), and four Quad Timers. Any of these interfaces can be used as General Purpose Input/Outputs (GPIOs) if that function is not required. A Controller Area Network interface (CAN Version 2.0 A/B-compliant), an internal interrupt controller and 14 dedicated GPIO are also included on the 56F805.

1.3 State of the Art Development Environment

- Processor Expert™ (PE) provides a Rapid Application Design (RAD) tool that combines easy-to-use component-based software application creation with an expert knowledge system.
- The Code Warrior Integrated Development Environment is a sophisticated tool for code navigation, compiling, and debugging. A complete set of evaluation modules (EVMs) and development system cards will support concurrent engineering. Together, PE, Code Warrior and EVMs create a complete, scalable tools solution for easy, fast, and efficient development.

1.4 Product Documentation

The four documents listed in **Table 2** are required for a complete description and proper design with the 56F805. Documentation is available from local Motorola distributors, Motorola semiconductor sales offices, Motorola Literature Distribution Centers, or online at **www.motorola.com/semiconductors**.

Table 1. 56F805 Chip Documentation

Topic	Description	Order Number
DSP56800 Family Manual	Detailed description of the 56800 family architecture, and 16-bit core processor and the instruction set	DSP56800FM/D
DSP56F801/803/805/ 807 User's Manual	Detailed description of memory, peripherals, and interfaces of the 56F801, 56F803, 56F805, and 56F807	DSP56F801-7UM/D
56F805 Technical Data Sheet	Electrical and timing specifications, pin descriptions, and package descriptions (this document)	DSP56F805/D
56F805 Product Brief	Summary description and block diagram of the 56F805 core, memory, peripherals and interfaces	DSP56F805PB/D
56F805 Errata	Details any chip issues that might be present	DSP56F805E/D

1.5 Data Sheet Conventions

This data sheet uses the following conventions:

$\overline{\text{OVERBAR}}$	This is used to indicate a signal that is active when pulled low. For example, the $\overline{\text{RESET}}$ pin is active when low.
"asserted"	A high true (active high) signal is high or a low true (active low) signal is low.
"deasserted"	A high true (active high) signal is low or a low true (active low) signal is high.

Examples:	Signal/Symbol	Logic State	Signal State	Voltage[1]
	$\overline{\text{PIN}}$	True	Asserted	V_{IL}/V_{OL}
	$\overline{\text{PIN}}$	False	Deasserted	V_{IH}/V_{OH}
	PIN	True	Asserted	V_{IH}/V_{OH}
	PIN	False	Deasserted	V_{IL}/V_{OL}

1. Values for V_{IL}, V_{OL}, V_{IH}, and V_{OH} are defined by individual product specifications.

Part 2 Signal/Connection Descriptions

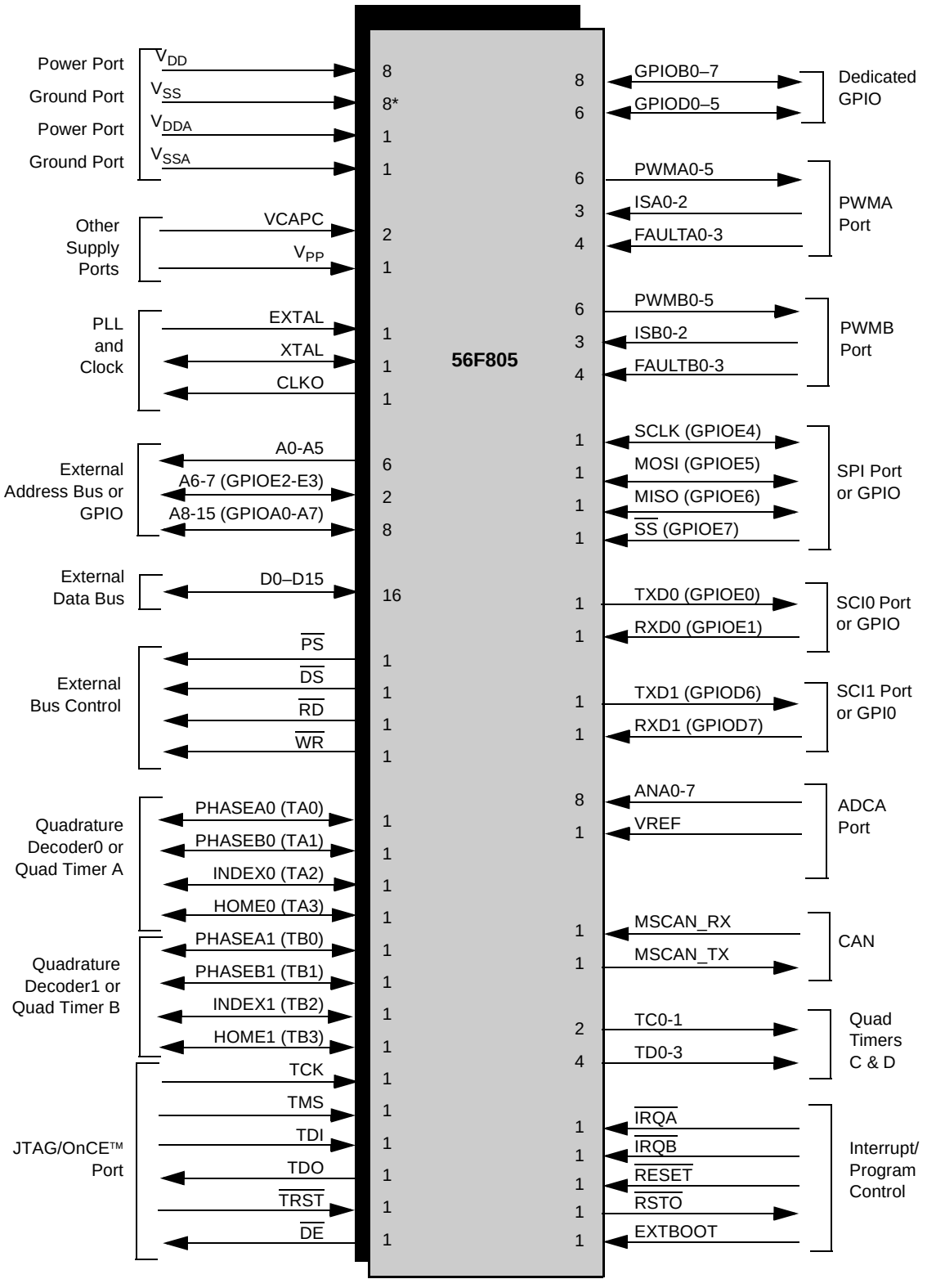
2.1 Introduction

The input and output signals of the 56F805 are organized into functional groups, as shown in **Table 2** and as illustrated in **Figure 2**. In **Table 3** through **Table 19**, each table row describes the signal or signals present on a pin.

Table 2. Functional Group Pin Allocations

Functional Group	Number of Pins	Detailed Description
Power (V_{DD} or V_{DDA})	9	Table 3
Ground (V_{SS} or V_{SSA})	9	Table 4
Supply Capacitors and V_{PP}	3	Table 5
PLL and Clock	3	Table 2.3
Address Bus[1]	16	Table 7
Data Bus	16	Table 8
Bus Control	4	Table 9
Interrupt and Program Control	5	Table 10
Dedicated General Purpose Input/Output	14	Table 11
Pulse Width Modulator (PWM) Port	26	Table 12
Serial Peripheral Interface (SPI) Port[1]	4	Table 13
Quadrature Decoder Port[2]	8	Table 14
Serial Communications Interface (SCI) Port[1]	4	Table 15
CAN Port	2	Table 16
Analog to Digital Converter (ADC) Port	9	Table 17
Quad Timer Module Ports	6	Table 18
JTAG/On-Chip Emulation (OnCE)	6	Table 19

1. Alternately, GPIO pins
2. Alternately, Quad Timer pins



*includes TCS pin which is reserved for factory use and is tied to VSS

Figure 2. 56F805 Signals Identified by Functional Group[1]

1. Alternate pin functionality is shown in parenthesis.

2.2 Power and Ground Signals

Table 3. Power Inputs

No. of Pins	Signal Name	Signal Description
8	V_{DD}	**Power**—These pins provide power to the internal structures of the chip, and should all be attached to V_{DD}.
1	V_{DDA}	**Analog Power**—This pin is a dedicated power pin for the analog portion of the chip and should be connected to a low noise 3.3V supply.

Table 4. Grounds

No. of Pins	Signal Name	Signal Description
7	V_{SS}	**GND**—These pins provide grounding for the internal structures of the chip, and should all be attached to V_{SS}.
1	V_{SSA}	**Analog Ground**—This pin supplies an analog ground.
1	**TCS**	**TCS**—This Schmitt pin is reserved for factory use and must be tied to V_{SS} for normal use. In block diagrams, this pin is considered an additional V_{SS}.

Table 5. Supply Capacitors and VPP

No. of Pins	Signal Name	Signal Type	State During Reset	Signal Description
2	**VCAPC**	Supply	Supply	**VCAPC**—Connect each pin to a 2.2µF or greater bypass capacitor in order to bypass the core logic voltage regulator, required for proper chip operation. For more information, please refer to **Section 5.2**.
1	**VPP**	Input	Input	**VPP**—This pin should be left unconnected as an open circuit for normal functionality.

2.3 Clock and Phase Locked Loop Signals

Table 6. PLL and Clock

No. of Pins	Signal Name	Signal Type	State During Reset	Signal Description
1	**EXTAL**	Input	Input	**External Crystal Oscillator Input**—This input should be connected to an 8MHz external crystal or ceramic resonator. For more information, please refer to **Section 3.5**.
1	**XTAL**	Input/ Output	Chip-driven	**Crystal Oscillator Output**—This output should be connected to an 8MHz external crystal or ceramic resonator. For more information, please refer to **Section 3.5**. This pin can also be connected to an external clock source. For more information, please refer to **Section 3.5.3**.

Table 6. PLL and Clock (Continued)

No. of Pins	Signal Name	Signal Type	State During Reset	Signal Description
1	**CLKO**	Output	Chip-driven	**Clock Output**—This pin outputs a buffered clock signal. By programming the CLKOSEL[4:0] bits in the CLKO Select Register (CLKOSR), the user can select between outputting a version of the signal applied to XTAL and a version of the device's master clock at the output of the PLL. The clock frequency on this pin can also be disabled by programming the CLKOSEL[4:0] bits in CLKOSR.

2.4 Address, Data, and Bus Control Signals

Table 7. Address Bus Signals

No. of Pins	Signal Name	Signal Type	State During Reset	Signal Description
6	**A0–A5**	Output	Tri-stated	**Address Bus**—A0–A5 specify the address for external Program or Data memory accesses.
2	**A6–A7** **GPIOE2–GPIOE3**	Output Input/ Output	Tri-stated Input	**Address Bus**—A6–A7 specify the address for external Program or Data memory accesses. **Port E GPIO**—These two General Purpose I/O (GPIO) pins can be individually programmed as input or output pins. After reset, the default state is Address Bus.
8	**A8–A15** **GPIOA0–GPIOA7**	Output Input/ Output	Tri-stated Input	**Address Bus**—A8–A15 specify the address for external Program or Data memory accesses. **Port A GPIO**—These eight General Purpose I/O (GPIO) pins can be individually be programmed as input or output pins. After reset, the default state is Address Bus.

Table 8. Data Bus Signals

No. of Pins	Signal Name	Signal Type	State During Reset	Signal Description
16	**D0–D15**	Input/ Output	Tri-stated	**Data Bus**— D0–D15 specify the data for external Program or Data memory accesses. D0–D15 are tri-stated when the external bus is inactive. Internal pullups may be active.

Table 9. Bus Control Signals

No. of Pins	Signal Name	Signal Type	State During Reset	Signal Description
1	**PS**	Output	Tri-stated	**Program Memory Select**—PS is asserted low for external Program memory access.
1	**DS**	Output	Tri-stated	**Data Memory Select**—DS is asserted low for external Data memory access.
1	**WR**	Output	Tri-stated	**Write Enable**—WR is asserted during external memory write cycles. When WR is asserted low, pins D0–D15 become outputs and the device puts data on the bus. When WR is deasserted high, the external data is latched inside the external device. When WR is asserted, it qualifies the A0–A15, PS, and DS pins. WR can be connected directly to the WE pin of a Static RAM.
1	**RD**	Output	Tri-stated	**Read Enable**—RD is asserted during external memory read cycles. When RD is asserted low, pins D0–D15 become inputs and an external device is enabled onto the device's data bus. When RD is deasserted high, the external data is latched inside the device. When RD is asserted, it qualifies the A0–A15, PS, and DS pins. RD can be connected directly to the OE pin of a Static RAM or ROM.

2.5 Interrupt and Program Control Signals

Table 10. Interrupt and Program Control Signals

No. of Pins	Signal Name	Signal Type	State During Reset	Signal Description
1	**IRQA**	Input (Schmitt)	Input	**External Interrupt Request A**—The IRQA input is a synchronized external interrupt request indicating an external device is requesting service. It can be programmed to be level-sensitive or negative-edge-triggered.
1	**IRQB**	Input (Schmitt)	Input	**External Interrupt Request B**—The IRQB input is an external interrupt request indicating an external device is requesting service. It can be programmed to be level-sensitive or negative-edge-triggered.
1	**RESET**	Input (Schmitt)	Input	**Reset**—This input is a direct hardware reset on the processor. When RESET is asserted low, the device is initialized and placed in the Reset state. A Schmitt trigger input is used for noise immunity. When the RESET pin is deasserted, the initial chip operating mode is latched from the EXTBOOT pin. The internal reset signal will be deasserted synchronous with the internal clocks, after a fixed number of internal clocks. To ensure complete hardware reset, RESET and TRST should be asserted together. The only exception occurs in a debugging environment when a hardware device reset is required and it is necessary not to reset the OnCE/JTAG module. In this case, assert RESET, but do not assert TRST.

Table 10. Interrupt and Program Control Signals (Continued)

No. of Pins	Signal Name	Signal Type	State During Reset	Signal Description
1	**$\overline{\text{RSTO}}$**	Output	Output	**Reset Output**—This output reflects the internal reset state of the chip.
1	**EXTBOOT**	Input (Schmitt)	Input	**External Boot**—This input is tied to V_{DD} to force device to boot from off-chip memory. Otherwise, it is tied to V_{SS}.

2.6 GPIO Signals

Table 11. Dedicated General Purpose Input/Output (GPIO) Signals

No. of Pins	Signal Name	Signal Type	State During Reset	Signal Description
8	**GPIOB0–GPIOB7**	Input or Output	Input	**Port B GPIO**—These eight dedicated General Purpose I/O (GPIO) pins can be individually programmed as input or output pins. After reset, the default state is GPIO input.
6	**GPIOD0–GPIOD5**	Input or Output	Input	**Port D GPIO**—These six dedicated General Purpose I/O (GPIO) pins can be individually programmed as input or output pins. After reset, the default state is GPIO input.

2.7 Pulse Width Modulator (PWM) Signals

Table 12. Pulse Width Modulator (PWMA and PWMB) Signals

No. of Pins	Signal Name	Signal Type	State During Reset	Signal Description
6	**PWMA0–5**	Output	Tri- stated	**PWMA0–5**—These are six PWMA output pins.
3	**ISA0–2**	Input (Schmitt)	Input	**ISA0–2**—These three input current status pins are used for top/bottom pulse width correction in complementary channel operation for PWMA.
4	**FAULTA0–3**	Input (Schmitt)	Input	**FAULTA0–3**—These four Fault input pins are used for disabling selected PWMA outputs in cases where fault conditions originate off-chip.
6	**PWMB0–5**	Output	Output	**PWMB0–5**—These are six PWMB output pins.
3	**ISB0–2**	Input (Schmitt)	Input	**ISB0–2**— These three input current status pins are used for top/bottom pulse width correction in complementary channel operation for PWMB.
4	**FAULTB0–3**	Input (Schmitt)	Input	**FAULTB0–3**—These four Fault input pins are used for disabling selected PWMB outputs in cases where fault conditions originate off-chip.

2.8 Serial Peripheral Interface (SPI) Signals

Table 13. Serial Peripheral Interface (SPI) Signals

No. of Pins	Signal Name	Signal Type	State During Reset	Signal Description
1	**MISO**	Input/ Output	Input	**SPI Master In/Slave Out (MISO)**—This serial data pin is an input to a master device and an output from a slave device. The MISO line of a slave device is placed in the high-impedance state if the slave device is not selected.
	GPIOE6	Input/ Output	Input	**Port E GPIO**—This pin is a General Purpose I/O (GPIO) pin that can individually be programmed as an input or output pin. After reset, the default state is MISO.
1	**MOSI**	Input/ Output	Input	**SPI Master Out/Slave In (MOSI)**—This serial data pin is an output from a master device and an input to a slave device. The master device places data on the MOSI line a half-cycle before the clock edge that the slave device uses to latch the data.
	GPIOE5	Input/ Output	Input	**Port E GPIO**—This General Purpose I/O (GPIO) pin can be individually programmed as an input or output pin. After reset, the default state is MOSI.
1	**SCLK**	Input/ Output	Input	**SPI Serial Clock**—In master mode, this pin serves as an output, clocking slaved listeners. In slave mode, this pin serves as the data clock input.
	GPIOE4	Input/ Output	Input	**Port E GPIO**—This General Purpose I/O (GPIO) pin can be individually programmed as an input or output pin. After reset, the default state is SCLK.
1	**$\overline{SS}$**	Input	Input	**SPI Slave Select**—In master mode, this pin is used to arbitrate multiple masters. In slave mode, this pin is used to select the slave.
	GPIOE7	Input/ Output	Input	**Port E GPIO**—This General Purpose I/O (GPIO) pin can be individually programmed as an input or output pin. After reset, the default state is $\overline{SS}$.

2.9 Quadrature Decoder Signals

Table 14. Quadrature Decoder (Quad Dec0 and Quad Dec1) Signals

No. of Pins	Signal Name	Signal Type	State During Reset	Signal Description
1	**PHASEA0**	Input	Input	**Phase A**—Quadrature Decoder #0 PHASEA input
	TA0	Input/Output	Input	**TA0**—Timer A Channel 0
1	**PHASEB0**	Input	Input	**Phase B**—Quadrature Decoder #0 PHASEB input
	TA1	Input/Output	Input	**TA1**—Timer A Channel 1
1	**INDEX0**	Input	Input	**Index**—Quadrature Decoder #0 INDEX input
	TA2	Input/Output	Input	**TA2**—Timer A Channel 2
1	**HOME0**	Input	Input	**Home**—Quadrature Decoder #0 HOME input
	TA3	Input/Output	Input	**TA3**—Timer A Channel 3
1	**PHASEA1**	Input	Input	**Phase A**—Quadrature Decoder #1 PHASEA input
	TB0	Input/Output	Input	**TB0**—Timer B Channel 0
1	**PHASEB1**	Input	Input	**Phase B**—Quadrature Decoder #1 PHASEB input
	TB1	Input/Output	Input	**TB1**—Timer B Channel 1
1	**INDEX1**	Input	Input	**Index**—Quadrature Decoder #1 INDEX input
	TB2	Input/Output	Input	**TB2**—Timer B Channel 2
1	**HOME1**	Input	Input	**Home**—Quadrature Decoder #1 HOME input
	TB3	Input/Output	Input	**TB3**—Timer B Channel 3

2.10 Serial Communications Interface (SCI) Signals

Table 15. Serial Communications Interface (SCI0 and SCI1) Signals

No. of Pins	Signal Name	Signal Type	State During Reset	Signal Description
1	**TXD0**	Output	Input	**Transmit Data (TXD0)**—SCI0 transmit data output
	GPIOE0	Input/ Output	Input	**Port E GPIO**—This pin is a General Purpose I/O (GPIO) pin that can individually be programmed as input or output pin. After reset, the default state is SCI output.

Table 15. Serial Communications Interface (SCI0 and SCI1) Signals (Continued)

No. of Pins	Signal Name	Signal Type	State During Reset	Signal Description
1	**RXD0** **GPIOE1**	Input Input/ Output	Input Input	**Receive Data (RXD0)**— SCI0 receive data input **Port E GPIO**—This pin is a General Purpose I/O (GPIO) pin that can individually be programmed as input or output pin. After reset, the default state is SCI input.
1	**TXD1** **GPIOD6**	Output Input/ Output	Input Input	**Transmit Data (TXD1)**—SCI1 transmit data output **Port D GPIO**—This pin is a General Purpose I/O (GPIO) pin that can individually be programmed as an input or output pin. After reset, the default state is SCI output.
1	**RXD1** **GPIOD7**	Input Input/ Output	Input Input	**Receive Data (RXD1)**—SCI1 receive data input **Port D GPIO**—This pin is a General Purpose I/O (GPIO) pin that can individually be programmed as an input or output pin. After reset, the default state is SCI input.

2.11 CAN Signals

Table 16. CAN Module Signals

No. of Pins	Signal Name	Signal Type	State During Reset	Signal Description
1	**MSCAN_ RX**	Input (Schmitt)	Input	**MSCAN Receive Data**—This is the MSCAN input. This pin has an internal pull-up resistor.
1	**MSCAN_ TX**	Output	Output	**MSCAN Transmit Data**—MSCAN output. CAN output is open-drain output and a pull-up resistor is needed.

2.12 Analog-to-Digital Converter (ADC) Signals

Table 17. Analog to Digital Converter Signals

No. of Pins	Signal Name	Signal Type	State During Reset	Signal Description
4	**ANA0–3**	Input	Input	**ANA0–3**—Analog inputs to ADC channel 1
4	**ANA4–7**	Input	Input	**ANA4–7**—Analog inputs to ADC channel 2
1	**VREF**	Input	Input	**VREF**—Analog reference voltage for ADC. Must be set to V_{DDA} - 0.3V for optimal performance.

2.13 Quad Timer Module Signals

Table 18. Quad Timer Module Signals

No. of Pins	Signal Name	Signal Type	State During Reset	Signal Description
2	**TC0-1**	Input/ Output	Input	**TC0–1**—Timer C Channels 0 and 1
4	**TD0-3**	Input/ Output	Input	**TD0–3**—Timer D Channels 0, 1, 2, and 3

2.14 JTAG/OnCE

Table 19. JTAG/On-Chip Emulation (OnCE) Signals

No. of Pins	Signal Name	Signal Type	State During Reset	Signal Description
1	**TCK**	Input (Schmitt)	Input, pulled low internally	**Test Clock Input**—This input pin provides a gated clock to synchronize the test logic and shift serial data to the JTAG/OnCE port. The pin is connected internally to a pull-down resistor.
1	**TMS**	Input (Schmitt)	Input, pulled high internally	**Test Mode Select Input**—This input pin is used to sequence the JTAG TAP controller's state machine. It is sampled on the rising edge of TCK and has an on-chip pull-up resistor.
1	**TDI**	Input (Schmitt)	Input, pulled high internally	**Test Data Input**—This input pin provides a serial input data stream to the JTAG/OnCE port. It is sampled on the rising edge of TCK and has an on-chip pull-up resistor.
1	**TDO**	Output	Tri-stated	**Test Data Output**—This tri-statable output pin provides a serial output data stream from the JTAG/OnCE port. It is driven in the Shift-IR and Shift-DR controller states, and changes on the falling edge of TCK.
1	**$\overline{\text{TRST}}$**	Input (Schmitt)	Input, pulled high internally	**Test Reset**—As an input, a low signal on this pin provides a reset signal to the JTAG TAP controller. To ensure complete hardware reset, $\overline{\text{TRST}}$ should be asserted at power-up and whenever $\overline{\text{RESET}}$ is asserted. The only exception occurs in a debugging environment when a hardware device reset is required and it is necessary not to reset the OnCE/JTAG module. In this case, assert $\overline{\text{RESET}}$, but do not assert $\overline{\text{TRST}}$.
1	**$\overline{\text{DE}}$**	Output	Output	**Debug Event**—$\overline{\text{DE}}$ provides a low pulse on recognized debug events.

Part 3 Specifications

3.1 General Characteristics

The 56F805 is fabricated in high-density CMOS with 5V-tolerant TTL-compatible digital inputs. The term "5V-tolerant" refers to the capability of an I/O pin, built on a 3.3V-compatible process technology, to withstand a voltage up to 5.5V without damaging the device. Many systems have a mixture of devices designed for 3.3V and 5V power supplies. In such systems, a bus may carry both 3.3V and 5V-compatible I/O voltage levels (a standard 3.3V I/O is designed to receive a maximum voltage of 3.3V ± 10% during normal operation without causing damage). This 5V-tolerant capability therefore offers the power savings of 3.3V I/O levels while being able to receive 5V levels without being damaged.

Absolute maximum ratings given in **Table 20** are stress ratings only, and functional operation at the maximum is not guaranteed. Stress beyond these ratings may affect device reliability or cause permanent damage to the device.

The 56F805 DC/AC electrical specifications are preliminary and are from design simulations. These specifications may not be fully tested or guaranteed at this early stage of the product life cycle. Finalized specifications will be published after complete characterization and device qualifications have been completed.

CAUTION

This device contains protective circuitry to guard against damage due to high static voltage or electrical fields. However, normal precautions are advised to avoid application of any voltages higher than maximum rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate voltage level.

Table 20. Absolute Maximum Ratings

Characteristic	Symbol	Min	Max	Unit
Supply voltage	V_{DD}	V_{SS} – 0.3	V_{SS} + 4.0	V
All other input voltages, excluding Analog inputs, EXTAL and XTAL	V_{IN}	V_{SS} – 0.3	V_{SS} + 5.5V	V
Analog inputs, ANA0-7 and VREF	V_{IN}	V_{SSA} – 0.3	V_{DDA} + 0.3	V
Analog inputs EXTAL and XTAL	V_{IN}	V_{SSA}– 0.3	V_{SSA}+ 3.0	V
Current drain per pin excluding V_{DD}, V_{SS}, PWM outputs, TCS, V_{PP}, V_{DDA}, V_{SSA}	I	—	10	mA

Table 21. Recommended Operating Conditions

Characteristic	Symbol	Min	Typ	Max	Unit
Supply voltage, digital	V_{DD}	3.0	3.3	3.6	V
Supply Voltage, analog	V_{DDA}	3.0	3.3	3.6	V
ADC reference voltage	VREF	2.7	–	V_{DDA}	V
Ambient operating temperature	T_A	–40	–	85	°C

Table 22. Thermal Characteristics[6]

Characteristic	Comments	Symbol	Value	Unit	Notes
			144-pin LQFP		
Junction to ambient Natural convection		$R_{\theta JA}$	47.1	°C/W	2
Junction to ambient (@1m/sec)		$R_{\theta JMA}$	43.8	°C/W	2
Junction to ambient Natural convection	Four layer board (2s2p)	$R_{\theta JMA}$ (2s2p)	40.8	°C/W	1,2
Junction to ambient (@1m/sec)	Four layer board (2s2p)	$R_{\theta JMA}$	39.2	°C/W	1,2
Junction to case		$R_{\theta JC}$	11.8	°C/W	3
Junction to center of case		Ψ_{JT}	1	°C/W	4, 5
I/O pin power dissipation		$P_{I/O}$	User Determined	W	
Power dissipation		P_D	$P_D = (I_{DD} \times V_{DD} + P_{I/O})$	W	
Junction to center of case		P_{DMAX}	(TJ - TA) /θJA	°C	

Notes:

1. Theta-JA determined on 2s2p test boards is frequently lower than would be observed in an application. Determined on 2s2p thermal test board.
2. Junction to ambient thermal resistance, Theta-JA ($R_{\theta JA}$) was simulated to be equivalent to the JEDEC specification JESD51-2 in a horizontal configuration in natural convection. Theta-JA was also simulated on a thermal test board with two internal planes (2s2p where "s" is the number of signal layers and "p" is the number of planes) per JESD51-6 and JESD51-7. The correct name for Theta-JA for forced convection or with the non-single layer boards is Theta-JMA.
3. Junction to case thermal resistance, Theta-JC ($R_{\theta JC}$), was simulated to be equivalent to the measured values using the cold plate technique with the cold plate temperature used as the "case" temperature. The basic cold plate measurement technique is described by MIL-STD 883D, Method 1012.1. This is the correct thermal metric to use to calculate thermal performance when the package is being used with a heat sink.
4. Thermal Characterization Parameter, Psi-JT (Ψ_{JT}), is the "resistance" from junction to reference point thermocouple on top center of case as defined in JESD51-2. Ψ_{JT} is a useful value to use to estimate junction temperature in steady-state customer environments.

5. Junction temperature is a function of on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
6. See Section 5.1 from more details on thermal design considerations.

3.2 DC Electrical Characteristics

Table 23. DC Electrical Characteristics

Operating Conditions: $V_{SS} = V_{SSA} = 0$ V, $V_{DD} = V_{DDA} = 3.0–3.6$ V, $T_A = –40°$ to $+85°C$, $C_L \leq 50$pF, $f_{op} = 80$MHz

Characteristic	Symbol	Min	Typ	Max	Unit
Input high voltage (XTAL/EXTAL)	V_{IHC}	2.25	—	2.75	V
Input low voltage (XTAL/EXTAL)	V_{ILC}	0	—	0.5	V
Input high voltage (Schmitt trigger inputs)[1]	V_{IHS}	2.2	—	5.5	V
Input low voltage (Schmitt trigger inputs)[1]	V_{ILS}	-0.3	—	0.8	V
Input high voltage (all other digital inputs)	V_{IH}	2.0	—	5.5	V
Input low voltage (all other digital inputs)	V_{IL}	-0.3	—	0.8	V
Input current high (pullup/pulldown resistors disabled, $V_{IN}=V_{DD}$)	I_{IH}	-1	—	1	µA
Input current low (pullup/pulldown resistors disabled, $V_{IN}=V_{SS}$)	I_{IL}	-1	—	1	µA
Input current high (with pullup resistor, $V_{IN}=V_{DD}$)	I_{IHPU}	-1	—	1	µA
Input current low (with pullup resistor, $V_{IN}=V_{SS}$)	I_{ILPU}	-210	—	-50	µA
Input current high (with pulldown resistor, $V_{IN}=V_{DD}$)	I_{IHPD}	20	—	180	µA
Input current low (with pulldown resistor, $V_{IN}=V_{SS}$)	I_{ILPD}	-1	—	1	µA
Nominal pullup or pulldown resistor value	R_{PU}, R_{PD}		30		KΩ
Output tri-state current low	I_{OZL}	-10	—	10	µA
Output tri-state current high	I_{OZH}	-10	—	10	µA
Input current high (analog inputs, $V_{IN}=V_{DDA}$)[2]	I_{IHA}	-15	—	15	µA
Input current low (analog inputs, $V_{IN}=V_{SSA}$)[3]	I_{ILA}	-15	—	15	µA
Output High Voltage (at IOH)	V_{OH}	$V_{DD} – 0.7$	—	—	V
Output Low Voltage (at IOL)	V_{OL}	—	—	0.4	V
Output source current	I_{OH}	4	—	—	mA
Output sink current	I_{OL}	4	—	—	mA

Table 23. DC Electrical Characteristics (Continued)

Operating Conditions: $V_{SS} = V_{SSA} = 0$ V, $V_{DD} = V_{DDA} = 3.0–3.6$ V, $T_A = –40°$ to +85°C, $C_L \leq 50$pF, $f_{op} = 80$MHz

Characteristic	Symbol	Min	Typ	Max	Unit
PWM pin output source current[3]	I_{OHP}	10	—	—	mA
PWM pin output sink current[4]	I_{OLP}	16	—	—	mA
Input capacitance	C_{IN}	—	8	—	pF
Output capacitance	C_{OUT}	—	12	—	pF
V_{DD} supply current	I_{DDT}[5]				
Run [6]		—	126	152	mA
Wait[7]		—	105	129	mA
Stop		—	60	84	mA
Low Voltage Interrupt, external power supply[8]	V_{EIO}	2.4	2.7	3.0	V
Low Voltage Interrupt, internal power supply[9]	V_{EIC}	2.0	2.2	2.4	V
Power on Reset[10]	V_{POR}	—	1.7	2.0	V

1. Schmitt Trigger inputs are: EXTBOOT, $\overline{\text{IRQA}}$, $\overline{\text{IRQB}}$, $\overline{\text{RESET}}$, ISA0-2, FAULTA0-3, ISB0-2, FAULT0B-3, TCS, TCK, $\overline{\text{TRST}}$, TMS, TDI, and MSCAN_RX
2. Analog inputs are: ANA[0:7], XTAL and EXTAL. Specification assumes ADC is not sampling.
3. PWM pin output source current measured with 50% duty cycle.
4. PWM pin output sink current measured with 50% duty cycle.
5. $I_{DDT} = I_{DD} + I_{DDA}$ (Total supply current for $V_{DD} + V_{DDA}$)
6. Run (operating) I_{DD} measured using 8MHz clock source. All inputs 0.2V from rail; outputs unloaded. All ports configured as inputs; measured with all modules enabled.
7. Wait I_{DD} measured using external square wave clock source ($f_{osc} = 8$MHz) into XTAL; all inputs 0.2V from rail; no DC loads; less than 50pF on all outputs. $C_L = 20$pF on EXTAL; all ports configured as inputs; EXTAL capacitance linearly affects wait I_{DD}; measured with PLL enabled.
8. This low voltage interrupt monitors the V_{DDA} external power supply. V_{DDA} is generally connected to the same potential as V_{DD} via separate traces. If V_{DDA} drops below V_{EIO}, an interrupt is generated. Functionality of the device is guaranteed under transient conditions when $V_{DDA} \geq V_{EIO}$ (between the minimum specified V_{DD} and the point when the V_{EIO} interrupt is generated).
9. This low voltage interrupt monitors the internally regulated core power supply. If the output from the internal voltage is regulator drops below V_{EIC}, an interrupt is generated. Since the core logic supply is internally regulated, this interrupt will not be generated unless the external power supply drops below the minimum specified value (3.0V).
10. Power–on reset occurs whenever the internally regulated 2.5V digital supply drops below 1.5V typical. While power is ramping up, this signal remains active as long as the internal 2.5V is below 1.5V typical, no matter how long the ramp-up rate is. The internally regulated voltage is typically 100mV less than V_{DD} during ramp-up until 2.5V is reached, at which time it self-regulates.

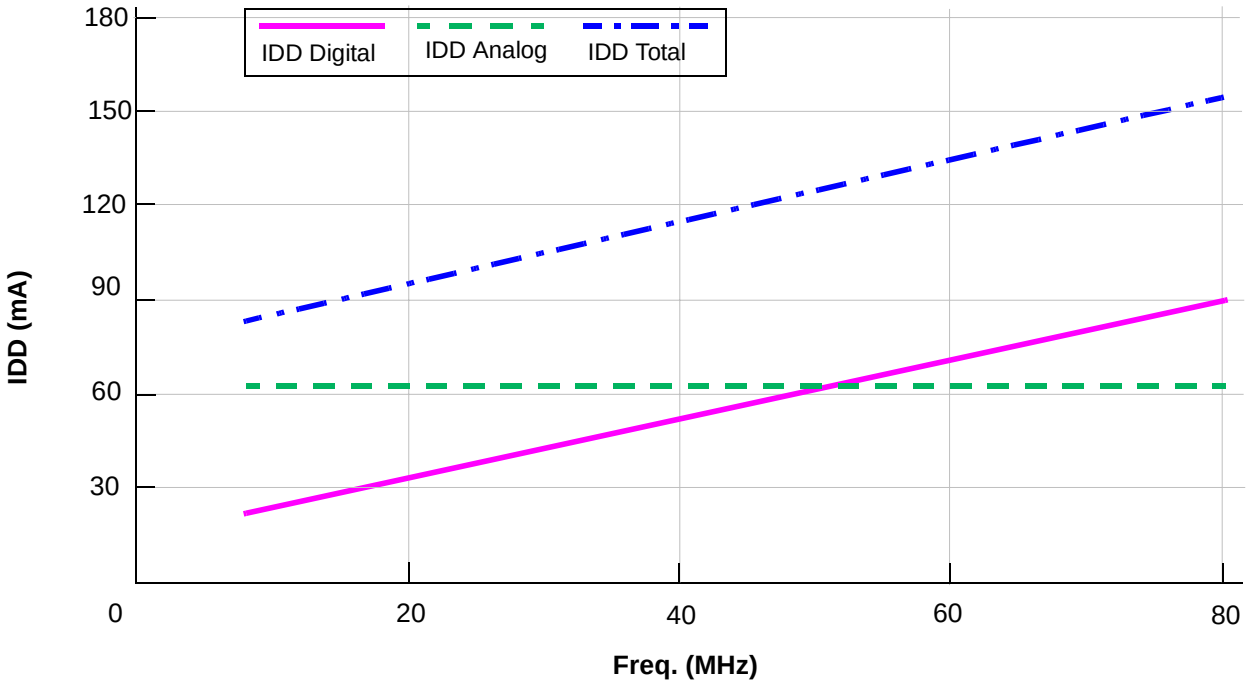
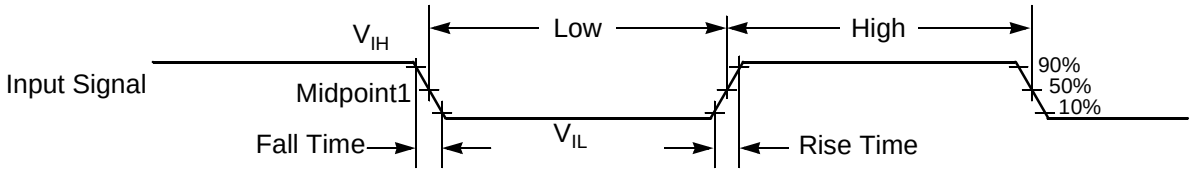


Figure 3. Maximum Run IDD vs. Frequency (see Note 6. in Table 16)

3.3 AC Electrical Characteristics

Timing waveforms in **Section 3.3** are tested using the V_{IL} and V_{IH} levels specified in the DC Characteristics table. In **Figure 4** the levels of V_{IH} and V_{IL} for an input signal are shown.



Note: The midpoint is $V_{IL} + (V_{IH} - V_{IL})/2$.

Figure 4. Input Signal Measurement References

Figure 5 shows the definitions of the following signal states:

- Active state, when a bus or signal is driven, and enters a low impedance state.
- Tri-stated, when a bus or signal is placed in a high impedance state.
- Data Valid state, when a signal level has reached V_{OL} or V_{OH}.
- Data Invalid state, when a signal level is in transition between V_{OL} and V_{OH}.

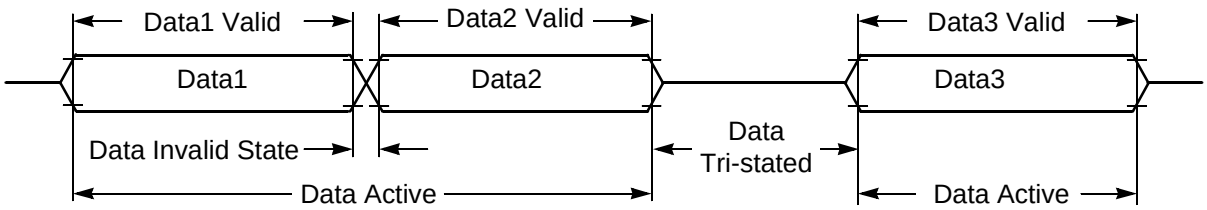


Figure 5. Signal States

3.4 Flash Memory Characteristics

Table 24. Flash Memory Truth Table

Mode	XE[1]	YE[2]	SE[3]	OE[4]	PROG[5]	ERASE[6]	MAS1[7]	NVSTR[8]
Standby	L	L	L	L	L	L	L	L
Read	H	H	H	H	L	L	L	L
Word Program	H	H	L	L	H	L	L	H
Page Erase	H	L	L	L	L	H	L	H
Mass Erase	H	L	L	L	L	H	H	H

1. X address enable, all rows are disabled when XE = 0
2. Y address enable, YMUX is disabled when YE = 0
3. Sense amplifier enable
4. Output enable, tri-state Flash data out bus when OE = 0
5. Defines program cycle
6. Defines erase cycle
7. Defines mass erase cycle, erase whole block
8. Defines non-volatile store cycle

Table 25. IFREN Truth Table

Mode	IFREN = 1	IFREN = 0
Read	Read information block	Read main memory block
Word program	Program information block	Program main memory block
Page erase	Erase information block	Erase main memory block
Mass erase	Erase both block	Erase main memory block

Table 26. Flash Timing Parameters

Operating Conditions: $V_{SS} = V_{SSA} = 0$ V, $V_{DD} = V_{DDA} = 3.0–3.6$V, $T_A = –40°$ to $+85°$C, $C_L \leq 50$pF

Characteristic	Symbol	Min	Typ	Max	Unit	Figure
Program time	T_{prog}*	20	–	–	us	Figure 6
Erase time	T_{erase}*	20	–	–	ms	Figure 7
Mass erase time	T_{me}*	100	–	–	ms	Figure 8
Endurance[1]	E_{CYC}	10,000	20,000	–	cycles	
Data Retention[1] @ 5000 cycles	D_{RET}	10	30	–	years	
The following parameters should only be used in the Manual Word Programming Mode						
PROG/ERASE to NVSTR set up time	T_{nvs}*	–	5	–	us	Figure 6, Figure 7, Figure 8
NVSTR hold time	T_{nvh}*	–	5	–	us	Figure 6, Figure 7
NVSTR hold time (mass erase)	T_{nvh1}*	–	100	–	us	Figure 8
NVSTR to program set up time	T_{pgs}*	–	10	–	us	Figure 6
Recovery time	T_{rcv}*	–	1	–	us	Figure 6, Figure 7, Figure 8
Cumulative program HV period[2]	T_{hv}	–	3	–	ms	Figure 6
Program hold time[3]	T_{pgh}	–	–	–		Figure 6
Address/data set up time[3]	T_{ads}	–	–	–		Figure 6
Address/data hold time[3]	T_{adh}	–	–	–		Figure 6

1. One cycle is equal to an erase program and read.
2. Thv is the cumulative high voltage programming time to the same row before next erase. The same address cannot be programmed twice before next erase.
3. Parameters are guaranteed by design in smart programming mode and must be one cycle or greater.

*The Flash interface unit provides registers for the control of these parameters.

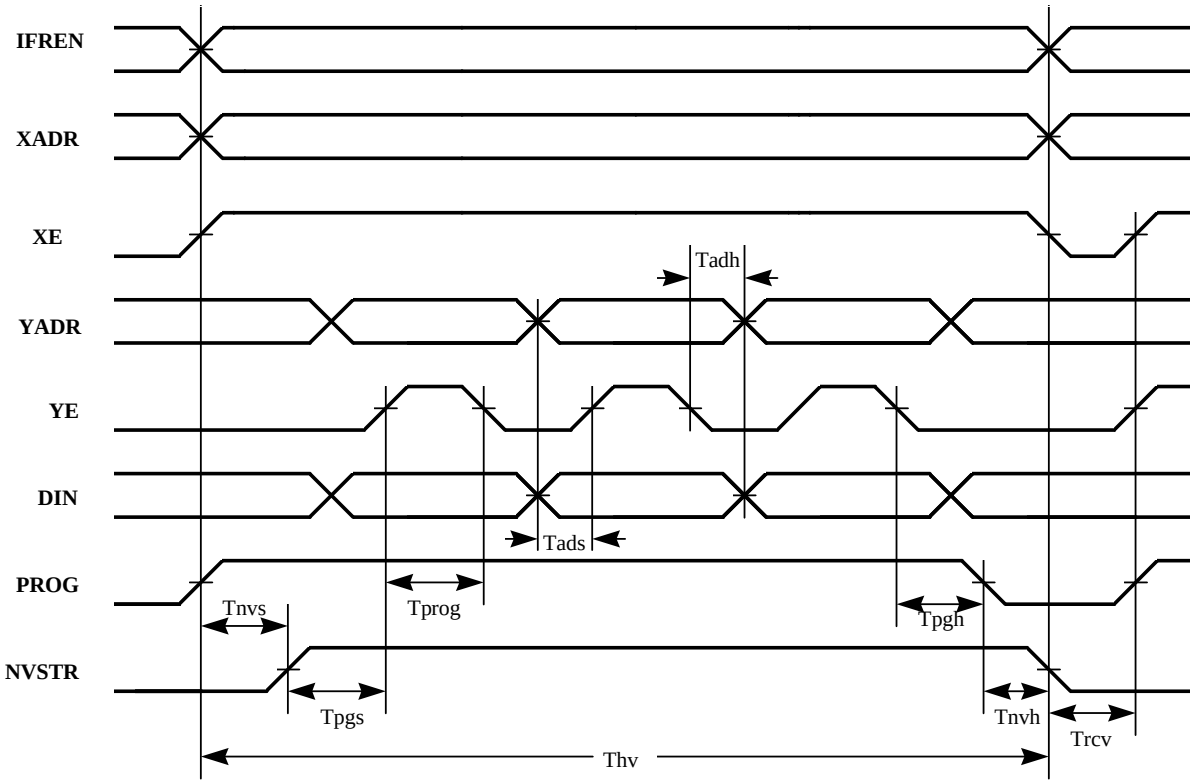


Figure 6. Flash Program Cycle

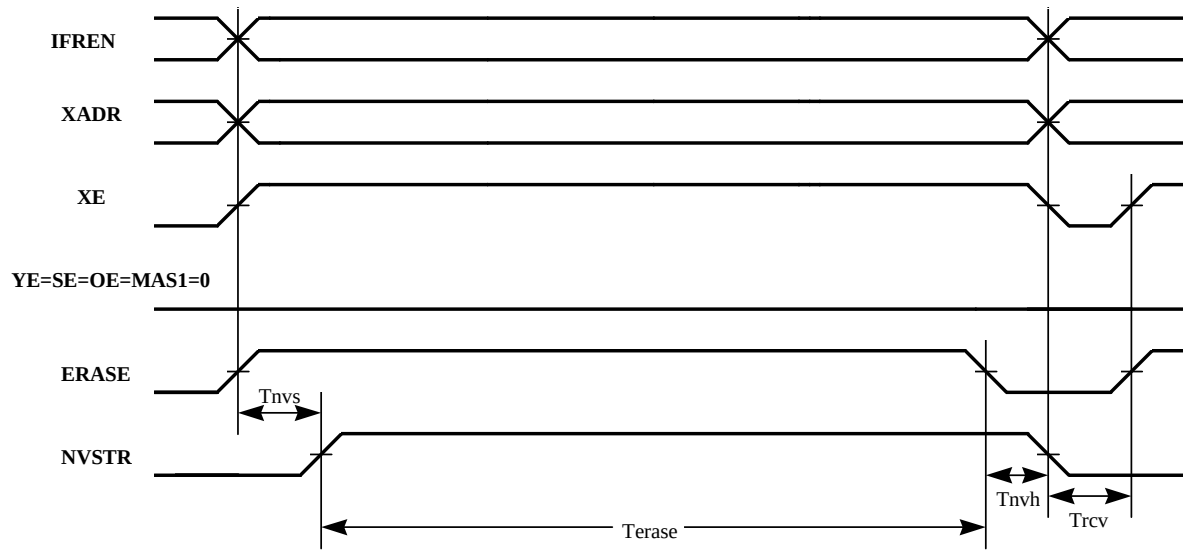


Figure 7. Flash Erase Cycle

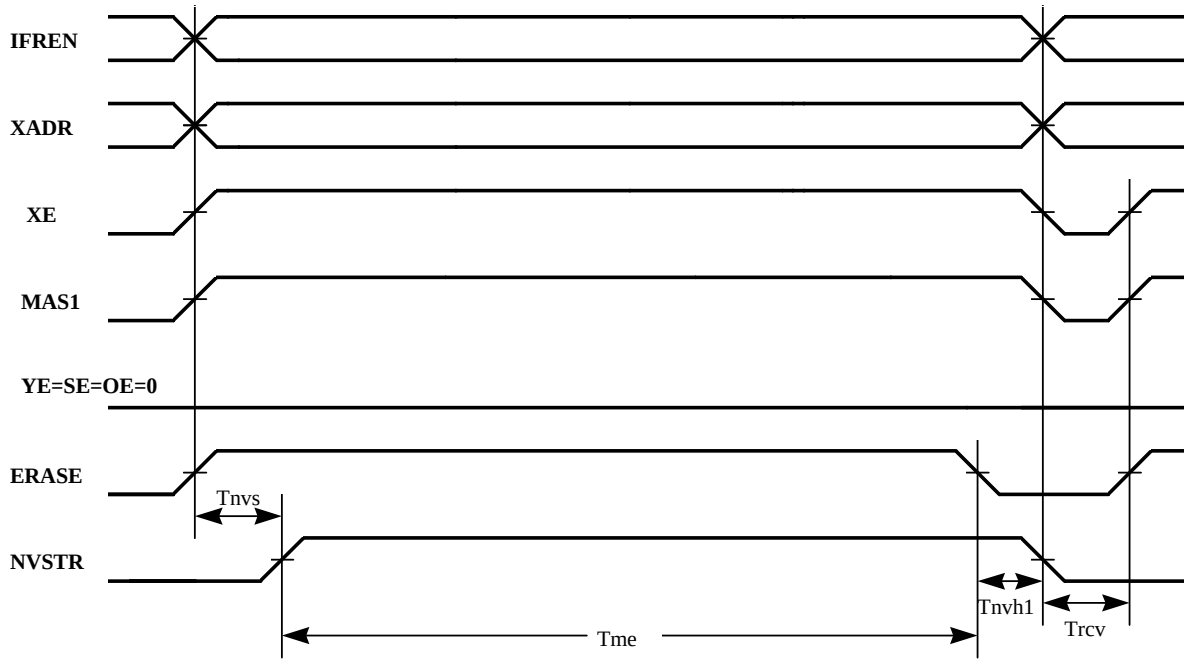


Figure 8. Flash Mass Erase Cycle

3.5 External Clock Operation

The 56F805 system clock can be derived from a crystal or an external system clock signal. To generate a reference frequency using the internal oscillator, a reference crystal must be connected between the EXTAL and XTAL pins.

3.5.1 Crystal Oscillator

The internal oscillator is also designed to interface with a parallel-resonant crystal resonator in the frequency range specified for the external crystal in **Table 28**. In **Figure 9** a recommended crystal oscillator circuit is shown. Follow the crystal supplier's recommendations when selecting a crystal, because crystal parameters determine the component values required to provide maximum stability and reliable start-up. The crystal and associated components should be mounted as close as possible to the EXTAL and XTAL pins to minimize output distortion and start-up stabilization time. The internal 56F80x oscillator circuitry is designed to have no external load capacitors present. As shown in **Figure 10** no external load capacitors should be used.

The 56F80x components internally are modeled as a parallel resonant oscillator circuit to provide a capacitive load on each of the oscillator pins (XTAL and EXTAL) of 10pF to 13pF over temperature and process variations. Using a typical value of internal capacitance on these pins of 12pF and a value of 3pF as a typical circuit board trace capacitance the parallel load capacitance presented to the crystal is 9pF as determined by the following equation:

$$CL = \frac{CL1 * CL2}{CL1 + CL2} + Cs = \frac{12 * 12}{12 + 12} + 3 = 6 + 3 = 9pF$$

This is the value load capacitance that should be used when selecting a crystal and determining the actual frequency of operation of the crystal oscillator circuit.

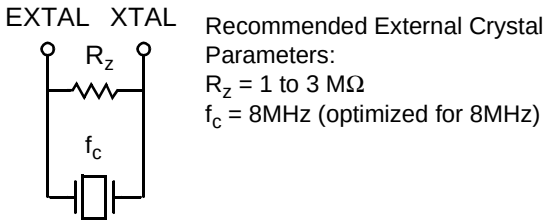


Figure 9. Connecting to a Crystal Oscillator

3.5.2 Ceramic Resonator

It is also possible to drive the internal oscillator with a ceramic resonator, assuming the overall system design can tolerate the reduced signal integrity. In **Figure 10**, a typical ceramic resonator circuit is shown. Refer to supplier's recommendations when selecting a ceramic resonator and associated components. The resonator and components should be mounted as close as possible to the EXTAL and XTAL pins. The internal 56F80x oscillator circuitry is designed to have no external load capacitors present. As shown in **Figure 9** no external load capacitors should be used.

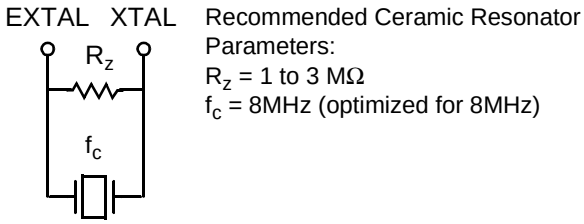


Figure 10. Connecting a Ceramic Resonator

Note: Motorola recommends only two terminal ceramic resonators vs. three terminal resonators (which contain an internal bypass capacitor to ground).

3.5.3 External Clock Source

The recommended method of connecting an external clock is given in **Figure 11**. The external clock source is connected to XTAL and the EXTAL pin is grounded.

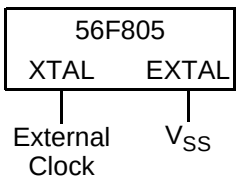


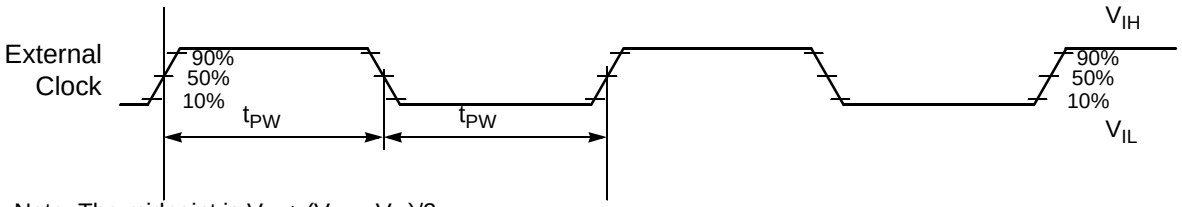
Figure 11. Connecting an External Clock Signal

Table 27. External Clock Operation Timing Requirements[3]

Operating Conditions: $V_{SS} = V_{SSA} = 0$ V, $V_{DD} = V_{DDA} = 3.0–3.6$V, $T_A = –40°$ to $+85°C$

Characteristic	Symbol	Min	Typ	Max	Unit
Frequency of operation (external clock driver)[1]	f_{osc}	0	—	80	MHz
Clock Pulse Width[2, 5]	t_{PW}	6.25	—	—	ns

1. See **Figure 11** for details on using the recommended connection of an external clock driver.
2. The high or low pulse width must be no smaller than 6.25ns or the chip will not function.
3. Parameters listed are guaranteed by design.



Note: The midpoint is $V_{IL} + (V_{IH} – V_{IL})/2$.

Figure 12. External Clock Timing

3.5.4 Phase Locked Loop Timing

Table 28. PLL Timing

Operating Conditions: $V_{SS} = V_{SSA} = 0$ V, $V_{DD} = V_{DDA} = 3.0–3.6$V, $T_A = –40°$ to $+85°C$

Characteristic	Symbol	Min	Typ	Max	Unit
External reference crystal frequency for the PLL[1]	f_{osc}	4	8	10	MHz
PLL output frequency[2]	$f_{out}/2$	40	—	110	MHz
PLL stabilization time [3] 0^o to $+85^oC$	t_{plls}	—	1	10	ms
PLL stabilization time[3] -40^o to 0^oC	t_{plls}	—	100	200	ms

1. An externally supplied reference clock should be as free as possible from any phase jitter for the PLL to work correctly. The PLL is optimized for 8MHz input crystal.
2. ZCLK may not exceed 80MHz. For additional information on ZCLK and $f_{out}/2$, please refer to the OCCS chapter in the User Manual. ZCLK = f_{op}
3. This is the minimum time required after the PLL set-up is changed to ensure reliable operation.

3.6 External Bus Asynchronous Timing

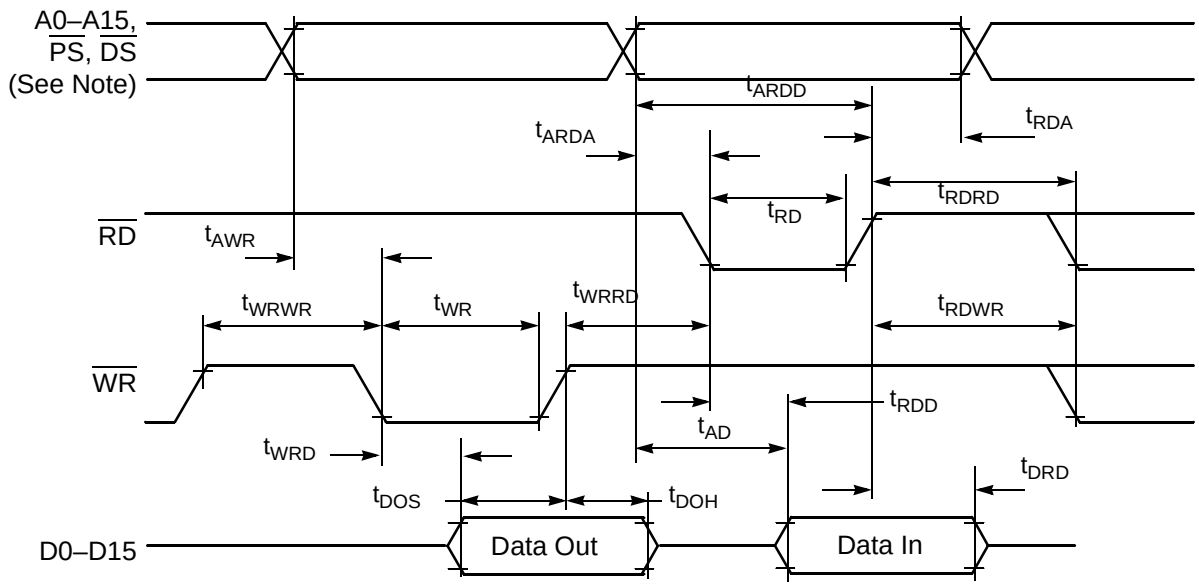
Table 29. External Bus Asynchronous Timing [1, 2]

Operating Conditions: $V_{SS} = V_{SSA} = 0$ V, $V_{DD} = V_{DDA} = 3.0–3.6$ V, $T_A = –40°$ to $+85°C$, $C_L \leq 50$pF, $f_{op} = 80$MHz

Characteristic	Symbol	Min	Max	Unit
Address Valid to $\overline{WR}$ Asserted	t_{AWR}	6.5	—	ns
$\overline{WR}$ Width Asserted Wait states = 0 Wait states > 0	t_{WR}	 7.5 (T*WS)+7.5	 — —	 ns ns
$\overline{WR}$ Asserted to D0–D15 Out Valid	t_{WRD}	—	T + 4.2	ns
Data Out Hold Time from $\overline{WR}$ Deasserted	t_{DOH}	4.8	—	ns
Data Out Set Up Time to $\overline{WR}$ Deasserted Wait states = 0 Wait states > 0	t_{DOS}	 2.2 (T*WS)+6.4	 — —	 ns ns
$\overline{RD}$ Deasserted to Address Not Valid	t_{RDA}	0	—	ns
Address Valid to $\overline{RD}$ Deasserted Wait states = 0 Wait states > 0	t_{ARDD}	 18.7 (T*WS) + 18.7	—	 ns ns
Input Data Hold to $\overline{RD}$ Deasserted	t_{DRD}	0	—	ns
$\overline{RD}$ Assertion Width Wait states = 0 Wait states > 0	t_{RD}	 19 (T*WS)+19	 — —	 ns ns
Address Valid to Input Data Valid Wait states = 0 Wait states > 0	t_{AD}	 — —	 1 (T*WS)+1	 ns ns
Address Valid to $\overline{RD}$ Asserted	t_{ARDA}	-4.4	—	ns
$\overline{RD}$ Asserted to Input Data Valid Wait states = 0 Wait states > 0	t_{RDD}	 — —	 2.4 (T*WS) + 2.4	 ns ns
$\overline{WR}$ Deasserted to $\overline{RD}$ Asserted	t_{WRRD}	6.8	—	ns
$\overline{RD}$ Deasserted to $\overline{RD}$ Asserted	t_{RDRD}	0	—	ns
$\overline{WR}$ Deasserted to $\overline{WR}$ Asserted	t_{WRWR}	14.1	—	ns
$\overline{RD}$ Deasserted to $\overline{WR}$ Asserted	t_{RDWR}	12.8	—	ns

1. Timing is both wait state- and frequency-dependent. In the formulas listed, WS = the number of wait states and T = Clock Period. For 80MHz operation, T = 12.5ns.
2. Parameters listed are guaranteed by design.

To calculate the required access time for an external memory for any frequency < 80Mhz, use this formula:
Top = Clock period @ desired operating frequency
WS = Number of wait states
Memory Access Time = (Top*WS) + (Top- 11.5)



Note: During read-modify-write instructions and internal instructions, the address lines do not change state.

Figure 13. External Bus Asynchronous Timing

3.7 Reset, Stop, Wait, Mode Select, and Interrupt Timing

Table 30. Reset, Stop, Wait, Mode Select, and Interrupt Timing[1, 6]

Operating Conditions: $V_{SS} = V_{SSA} = 0$ V, $V_{DD} = V_{DDA} = 3.0$–3.6 V, $T_A = -40°$ to $+85°C$, $C_L \leq 50$pF

Characteristic	Symbol	Min	Max	Unit	See Figure
$\overline{\text{RESET}}$ Assertion to Address, Data and Control Signals High Impedance	t_{RAZ}	—	21	ns	Figure 14
Minimum $\overline{\text{RESET}}$ Assertion Duration[2] OMR Bit 6 = 0 OMR Bit 6 = 1	t_{RA}	 275,000T 128T	 — —	 ns ns	Figure 14
$\overline{\text{RESET}}$ Deassertion to First External Address Output	t_{RDA}	33T	34T	ns	Figure 14
Edge-sensitive Interrupt Request Width	t_{IRW}	1.5T	—	ns	Figure 15
$\overline{\text{IRQA}}$, $\overline{\text{IRQB}}$ Assertion to External Data Memory Access Out Valid, caused by first instruction execution in the interrupt service routine	t_{IDM}	15T	—	ns	Figure 16
$\overline{\text{IRQA}}$, $\overline{\text{IRQB}}$ Assertion to General Purpose Output Valid, caused by first instruction execution in the interrupt service routine	t_{IG}	16T	—	ns	Figure 16
$\overline{\text{IRQA}}$ Low to First Valid Interrupt Vector Address Out recovery from Wait State[3]	t_{IRI}	13T	—	ns	Figure 17
$\overline{\text{IRQA}}$ Width Assertion to Recover from Stop State[4]	t_{IW}	2T	—	ns	Figure 18

Table 30. Reset, Stop, Wait, Mode Select, and Interrupt Timing[1, 6] (Continued)

Operating Conditions: $V_{SS} = V_{SSA} = 0$ V, $V_{DD} = V_{DDA} = 3.0–3.6$ V, $T_A = –40°$ to $+85°C$, $C_L \leq 50$pF

Characteristic	Symbol	Min	Max	Unit	See Figure
Delay from $\overline{\text{IRQA}}$ Assertion to Fetch of first instruction (exiting Stop) OMR Bit 6 = 0 OMR Bit 6 = 1	t_{IF}	 — —	 275,000T 12T	 ns ns	Figure 18
Duration for Level Sensitive $\overline{\text{IRQA}}$ Assertion to Cause the Fetch of First $\overline{\text{IRQA}}$ Interrupt Instruction (exiting Stop) OMR Bit 6 = 0 OMR Bit 6 = 1	t_{IRQ}	 — —	 275,000T 12T	 ns ns	Figure 19
Delay from Level Sensitive $\overline{\text{IRQA}}$ Assertion to First Interrupt Vector Address Out Valid (exiting Stop) OMR Bit 6 = 0 OMR Bit 6 = 1	t_{II}	 — —	 275,000T 12T	 ns ns	Figure 19
$\overline{\text{RSTO}}$ pulse width[5] normal operation internal reset mode	t_{RSTO}	 63ET 2,097,151ET		 ns ns	Figure 20

1. In the formulas, T = clock cycle. For an operating frequency of 80MHz, T = 12.5ns.
2. Circuit stabilization delay is required during reset when using an external clock or crystal oscillator in two cases:
   • After power-on reset
   • When recovering from Stop state
3. The minimum is specified for the duration of an edge-sensitive IRQA interrupt required to recover from the Stop state. This is not the minimum required so that the IRQA interrupt is accepted.
4. The interrupt instruction fetch is visible on the pins only in Mode 3.
5. ET = External Clock period, For an external crystal frequency of 8MHz, ET=125ns.
6. Parameters listed are guaranteed by design.

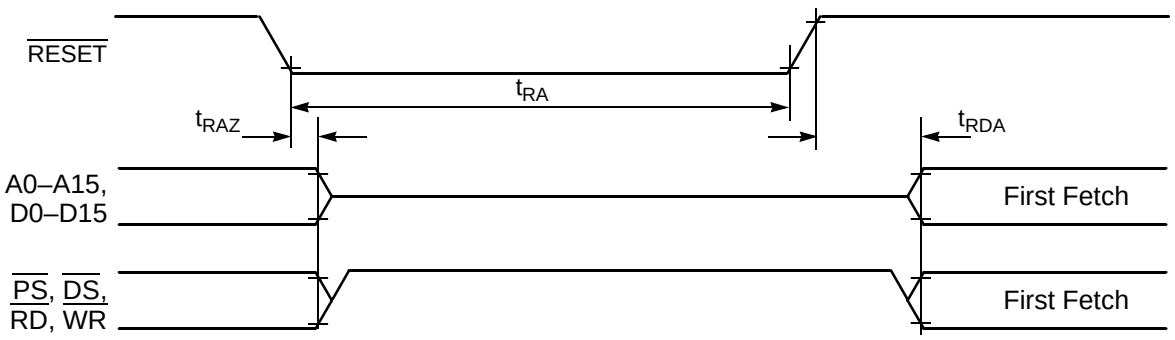


Figure 14. Asynchronous Reset Timing

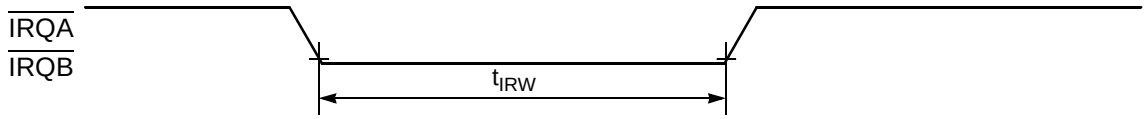


Figure 15. External Interrupt Timing (Negative-Edge-Sensitive)

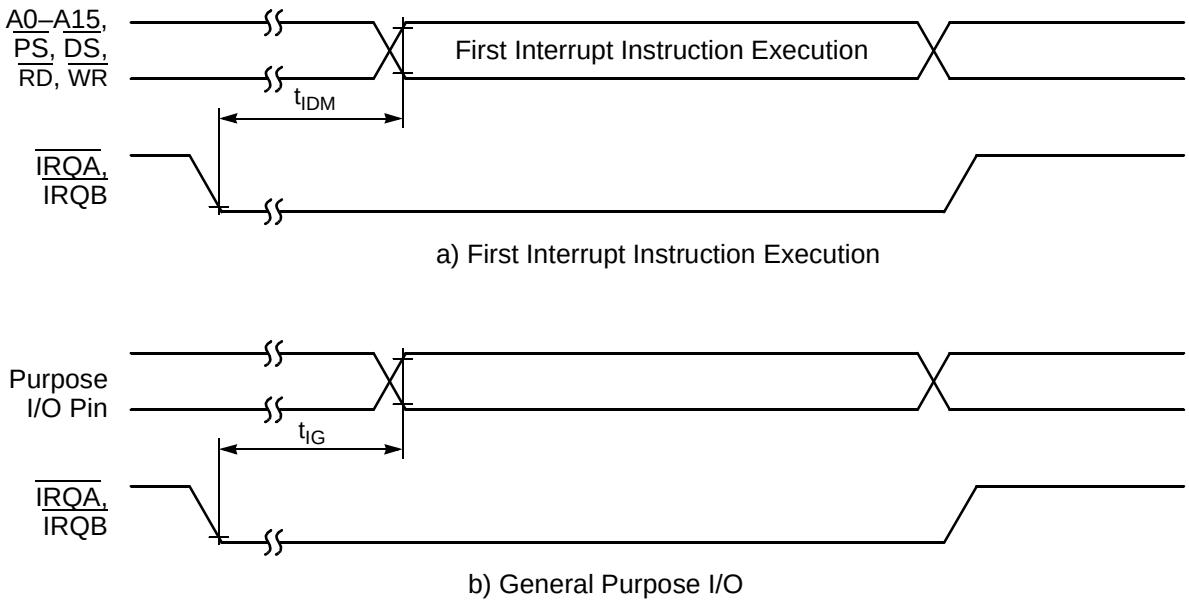


Figure 16. External Level-Sensitive Interrupt Timing

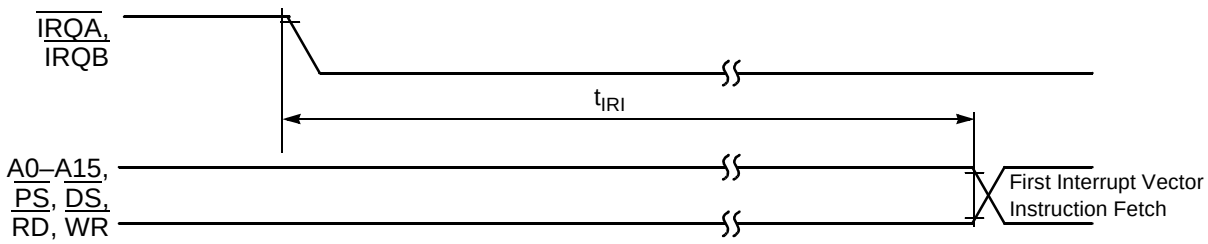


Figure 17. Interrupt from Wait State Timing

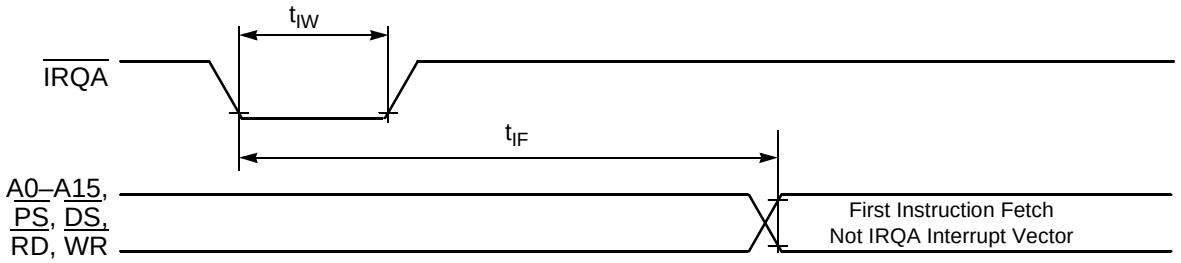


Figure 18. Recovery from Stop State Using Asynchronous Interrupt Timing

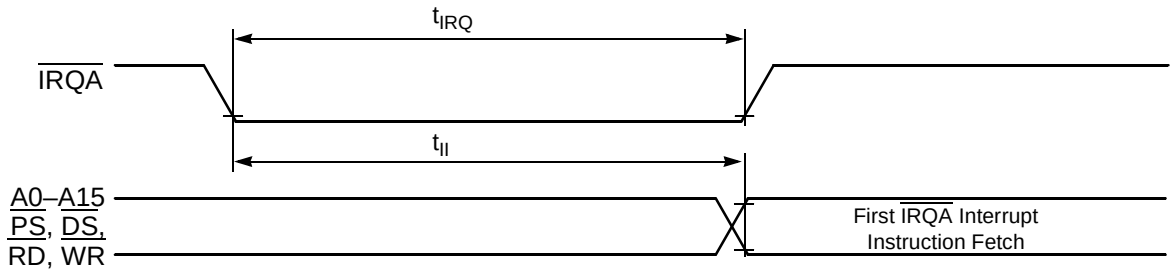


Figure 19. Recovery from Stop State Using IRQA Interrupt Service

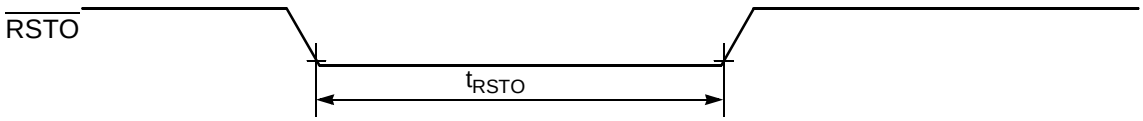


Figure 20. Reset Output Timing

3.8 Serial Peripheral Interface (SPI) Timing

Table 31. SPI Timing[1]

Operating Conditions: $V_{SS} = V_{SSA} = 0$ V, $V_{DD} = V_{DDA} = 3.0–3.6$ V, $T_A = –40°$ to $+85°C$, $C_L \leq 50$pF, $f_{OP} = 80$MHz

Characteristic	Symbol	Min	Max	Unit	See Figure
Cycle time Master Slave	t_C	 50 25	 — —	 ns ns	Figures 21, 22, 23, 24
Enable lead time Master Slave	t_{ELD}	 — 25	 — —	 ns ns	Figure 24
Enable lag time Master Slave	t_{ELG}	 — 100	 — —	 ns ns	Figure 24
Clock (SCLK) high time Master Slave	t_{CH}	 17.6 12.5	 — —	 ns ns	Figures 21, 22, 23, 24
Clock (SCLK) low time Master Slave	t_{CL}	 24.1 25	 — —	 ns ns	Figure 24
Data set-up time required for inputs Master Slave	t_{DS}	 20 0	 — —	 ns ns	Figures 21, 22, 23, 24
Data hold time required for inputs Master Slave	t_{DH}	 0 2	 — —	 ns ns	Figures 21, 22, 23, 24
Access time (time to data active from high-impedance state) Slave	t_A	4.8	15	ns	Figure 24
Disable time (hold time to high-impedance state) Slave	t_D	3.7	15.2	ns	Figure 24
Data Valid for outputs Master Slave (after enable edge)	t_{DV}	 — —	 4.5 20.4	 ns ns	Figures 21, 22, 23, 24
Data invalid Master Slave	t_{DI}	 0 0	 — —	 ns ns	Figures 21, 22, 23, 24
Rise time Master Slave	t_R	 — —	 11.5 10.0	 ns ns	Figures 21, 22, 23, 24
Fall time Master Slave	t_F	 — —	 9.7 9.0	 ns ns	Figures 21, 22, 23, 24

1. Parameters listed are guaranteed by design.

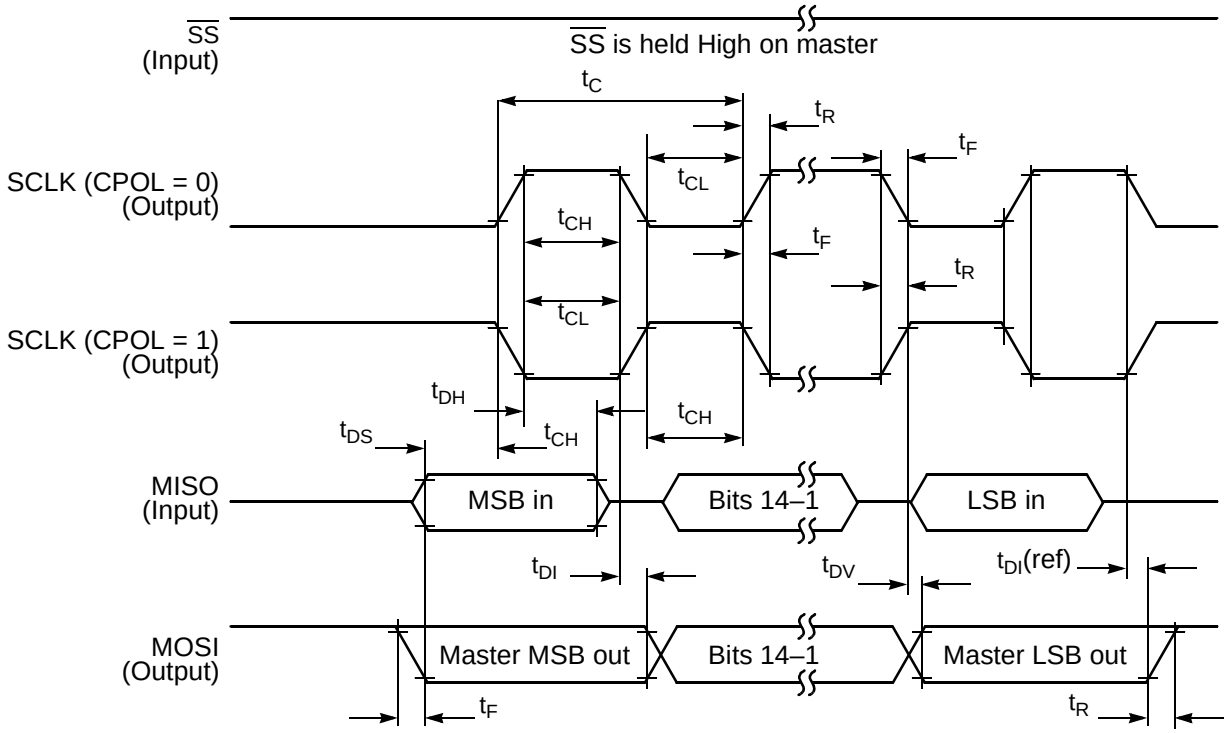


Figure 21. SPI Master Timing (CPHA = 0)

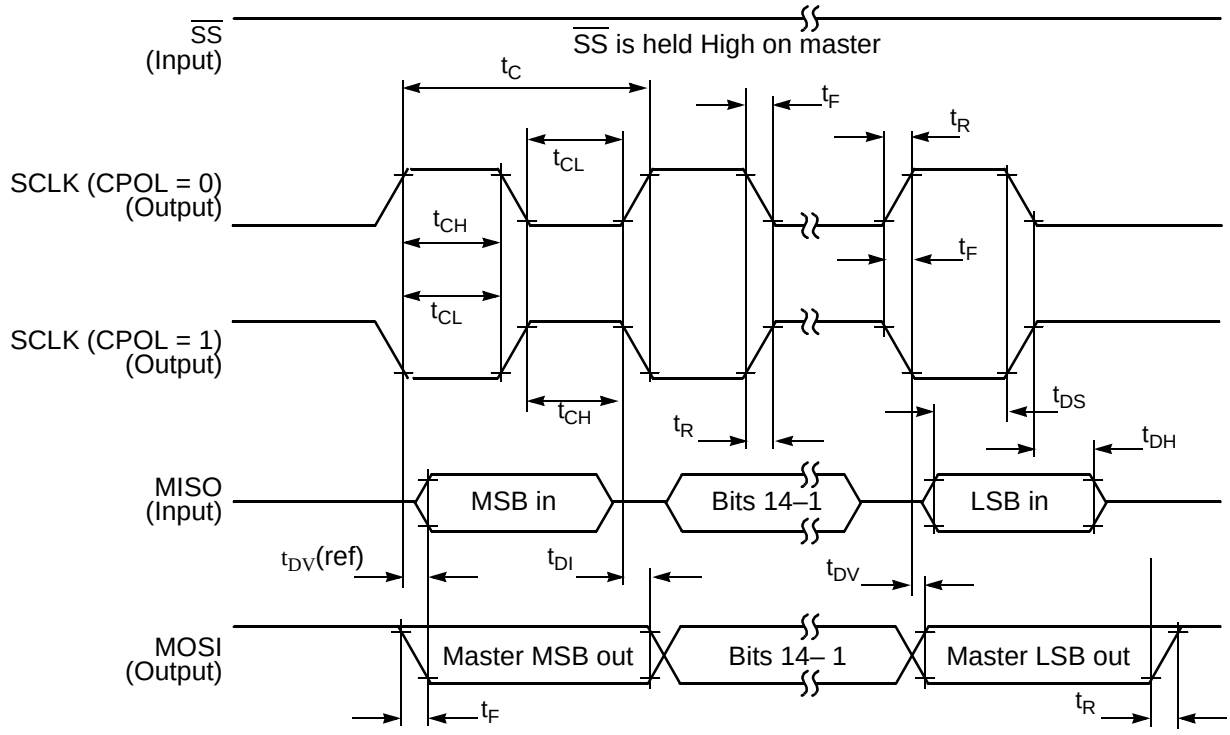


Figure 22. SPI Master Timing (CPHA = 1)

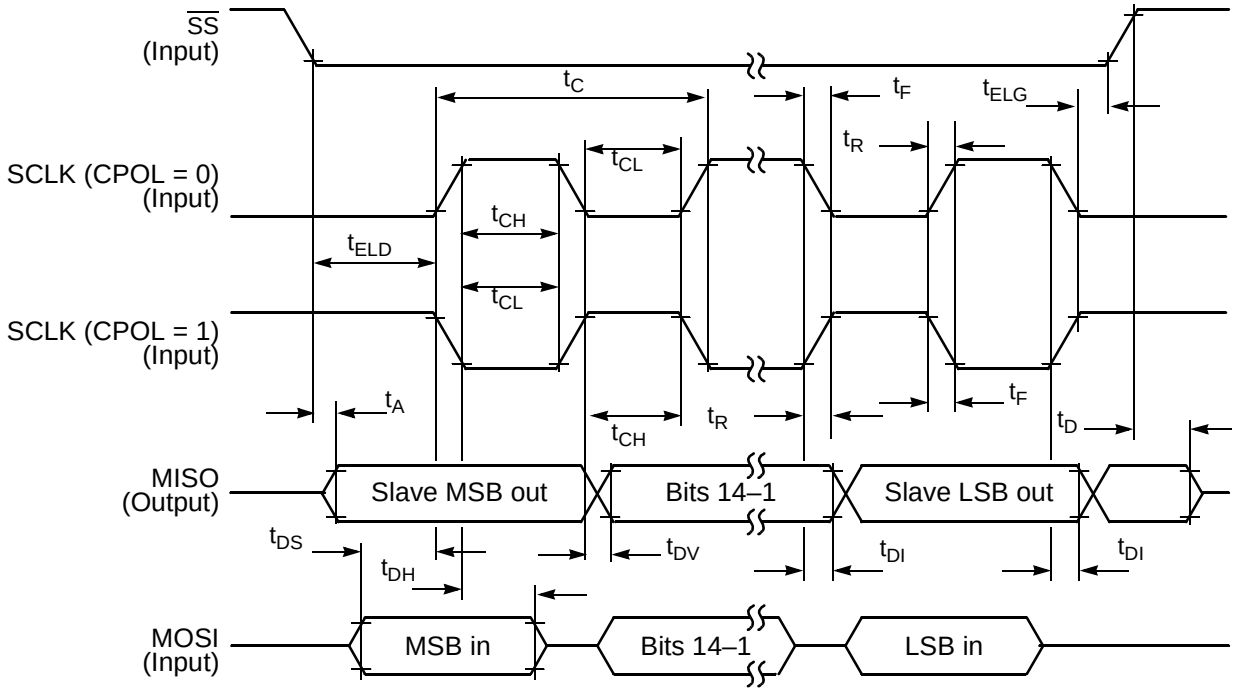


Figure 23. SPI Slave Timing (CPHA = 0)

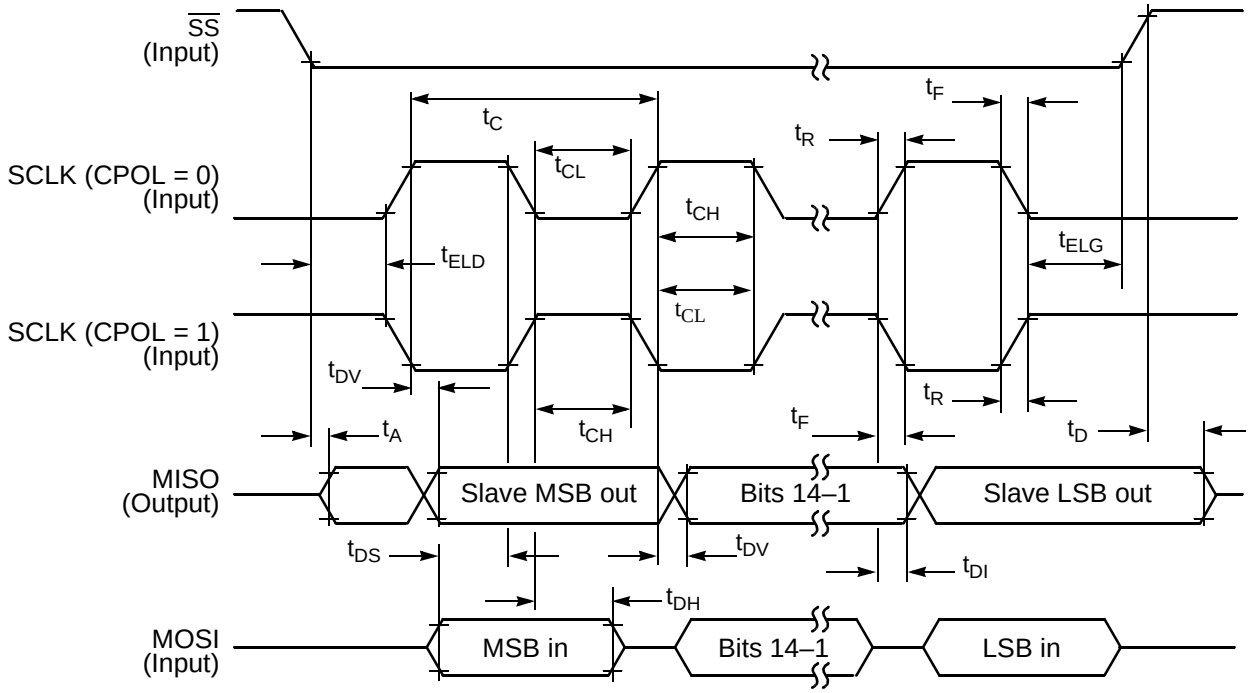


Figure 24. SPI Slave Timing (CPHA = 1)

3.9 Quad Timer Timing

Table 32. Timer Timing[1, 2]

Operating Conditions: $V_{SS} = V_{SSA} = 0$ V, $V_{DD} = V_{DDA} = 3.0–3.6$V, $T_A = –40°$ to $+85°$C, $C_L \leq 50$pF, $f_{OP} = 80$MHz

Characteristic	Symbol	Min	Max	Unit
Timer input period	P_{IN}	4T+6	—	ns
Timer input high/low period	P_{INHL}	2T+3	—	ns
Timer output period	P_{OUT}	2T	—	ns
Timer output high/low period	P_{OUTHL}	1T	—	ns

1. In the formulas listed, T = clock cycle. For 80MHz operation, T = 12.5ns.
2. Parameters listed are guaranteed by design.

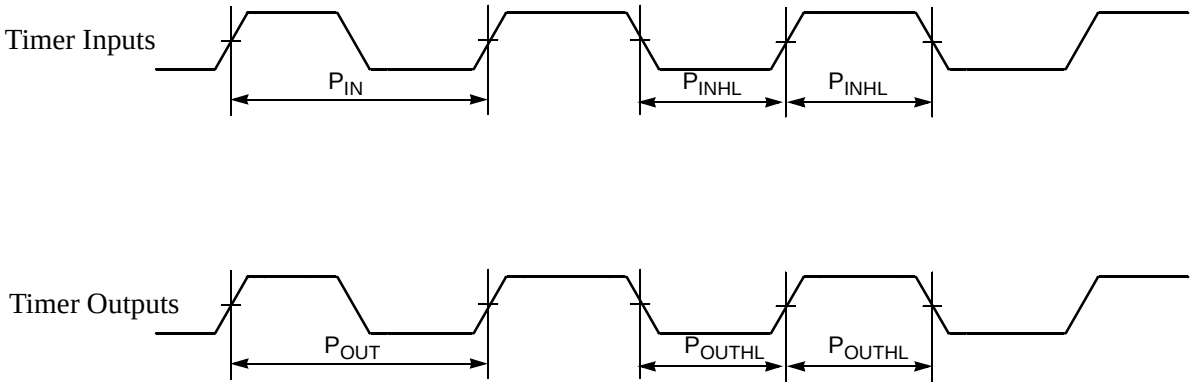


Figure 25. Timer Timing

3.10 Quadrature Decoder Timing

Table 33. Quadrature Decoder Timing[1, 2]

Operating Conditions: $V_{SS} = V_{SSA} = 0$ V, $V_{DD} = V_{DDA} = 3.0–3.6$V, $T_A = –40°$ to $+85°$C, $C_L \leq 50$pF, $f_{OP} = 80$MHz

Characteristic	Symbol	Min	Max	Unit
Quadrature input period	P_{IN}	8T+12	—	ns
Quadrature input high/low period	P_{HL}	4T+6	—	ns
Quadrature phase period	P_{PH}	2T+3	—	ns

1. In the formulas listed, T = clock cycle. For 80MHz operation, T = 12.5ns. $V_{SS} = 0$V, $V_{DD} = 3.0–3.6$V, $T_A = –40°$ to $+85°$C, $C_L \leq 50$pF.
2. Parameters listed are guaranteed by design.

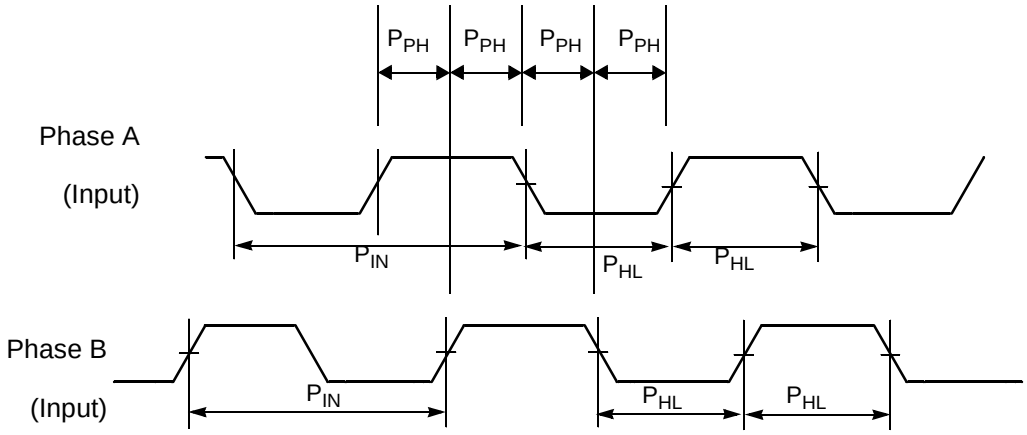


Figure 26. Quadrature Decoder Timing

3.11 Serial Communication Interface (SCI) Timing

Table 34. SCI Timing[4]

Operating Conditions: $V_{SS} = V_{SSA} = 0$ V, $V_{DD} = V_{DDA} = 3.0–3.6$V, $T_A = –40°$ to $+85°$C, $C_L \leq 50$pF, $f_{OP} = 80$MHz

Characteristic	Symbol	Min	Max	Unit
Baud Rate[1]	BR	—	$(f_{MAX}*2.5)/(80)$	Mbps
RXD[2] Pulse Width	RXD_{PW}	0.965/BR	1.04/BR	ns
TXD[3] Pulse Width	TXD_{PW}	0.965/BR	1.04/BR	ns

1. f_{MAX} is the frequency of operation of the system clock in MHz.
2. The RXD pin in SCI0 is named RXD0 and the RXD pin in SCI1 is named RXD1.
3. The TXD pin in SCI0 is named TXD0 and the TXD pin in SCI1 is named TXD1.
4. Parameters listed are guaranteed by design.

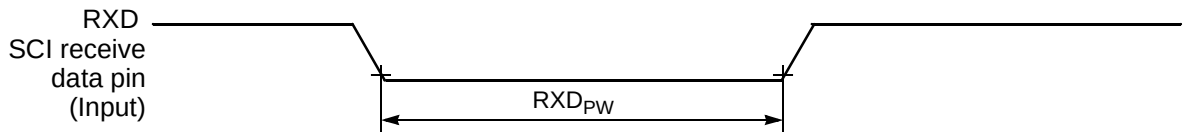


Figure 27. RXD Pulse Width

Figure 28. TXD Pulse Width

3.12 Analog-to-Digital Converter (ADC) Characteristics

Table 35. ADC Characteristics

Operating Conditions: V_{SS} = V_{SSA} = 0 V, V_{DD} = V_{DDA} = 3.0–3.6 V, V_{REF} = V_{DD}-0.3V, ADCDIV = 4, 9, or 14, (for optimal performance), ADC clock = 4MHz, 3.0–3.6 V, T_A = –40° to +85°C, $C_L \leq$ 50pF, f_{OP} = 80MHz

Characteristic	Symbol	Min	Typ	Max	Unit
ADC input voltages	V_{ADCIN}	0[1]	—	V_{REF}[2]	V
Resolution	R_{ES}	12	—	12	Bits
Integral Non-Linearity[3]	INL	—	+/-2.5	+/-4	LSB[4]
Differential Non-Linearity	DNL	—	+/- 0.9	+/-1	LSB[4]
Monotonicity	GUARANTEED				
ADC internal clock[5]	f_{ADIC}	0.5	—	5	MHz
Conversion range	R_{AD}	V_{SSA}	—	V_{DDA}	V
Conversion time	t_{ADC}	—	6	—	t_{AIC} cycles[6]
Sample time	t_{ADS}	—	1	—	t_{AIC} cycles[6]
Input capacitance	C_{ADI}	—	5	—	pF[6]
Gain Error (transfer gain)[5]	E_{GAIN}	.95	1.00	1.10	—
Offset Voltage[5]	V_{OFFSET}	-80	-15	+20	mV
Total Harmonic Distortion[5]	THD	60	64	—	dB
Signal-to-Noise plus Distortion[5]	SINAD	55	60	—	dB
Effective Number Of Bits[5]	ENOB	9	10	—	bit
Spurious Free Dynamic Range[5]	SFDR	65	70	—	dB
Bandwidth	BW	—	100	—	KHz
ADC Quiescent Current (both ADCs)	I_{ADC}	—	50	—	mA
V_{REF} Quiescent Current (both ADCs)	I_{VREF}	—	12	16.5	mA

1. For optimum ADC performance, keep the minimum V_{ADCIN} value $\geq$ 25mV. Inputs less than 25mV may convert to a digital output code of 0.
2. V_{REF} must be equal to or less than V_{DDA} and must be greater than 2.7V. For optimal ADC performance, set V_{REF} to V_{DDA}-0.3V.
3. Measured in 10-90% range.
4. LSB = Least Significant Bit.
5. Guaranteed by characterization.
6. $t_{AIC} = 1/f_{ADIC}$

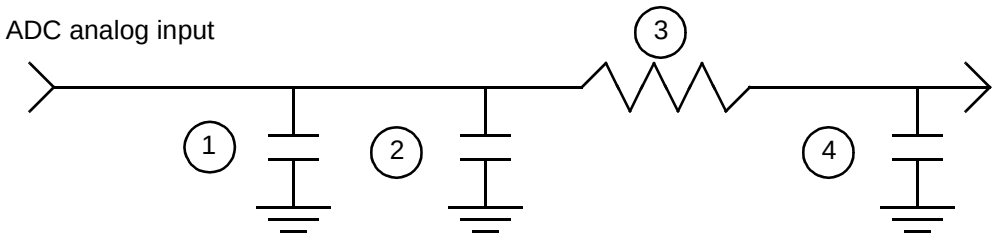


Figure 29. Equivalent Analog Input Circuit

1. Parasitic capacitance due to package, pin to pin, and pin to package base coupling. (1.8pf)
2. Parasitic capacitance due to the chip bond pad, ESD protection devices and signal routing. (2.04pf)
3. Equivalent resistance for the ESD isolation resistor and the channel select mux. (500 ohms)
4. Sampling capacitor at the sample and hold circuit. (1pf)

3.13 Controller Area Network (CAN) Timing

Table 36. CAN Timing[2]

Operating Conditions: $V_{SS} = V_{SSA} = 0$ V, $V_{DD} = V_{DDA} = 3.0–3.6$ V, $T_A = –40°$ to +85°C, $C_L \leq 50$pF, MSCAN Clock = 30MHz

Characteristic	Symbol	Min	Max	Unit
Baud Rate	BR_{CAN}	—	1	Mbps
Bus Wakeup detection [1]	T_{WAKEUP}	5	—	us

1. If Wakeup glitch filter is enabled during the design initialization and also CAN is put into Sleep mode then, any bus event (on MSCAN_RX pin) whose duration is less than 5 microseconds is filtered away. However, a valid CAN bus wakeup detection takes place for a wakeup pulse equal to or greater than 5 microseconds. The number 5 microseconds originates from the fact that the CAN wakeup message consists of 5 dominant bits at the highest possible baud rate of 1Mbps.
2. Parameters listed are guaranteed by design.

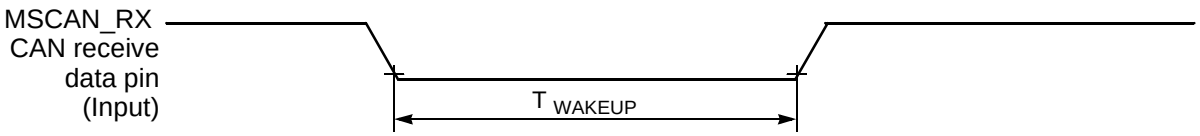


Figure 30. Bus Wakeup Detection

3.14 JTAG Timing

Table 37. JTAG Timing[1, 3]

Operating Conditions: $V_{SS} = V_{SSA} = 0$ V, $V_{DD} = V_{DDA} = 3.0–3.6$ V, $T_A = –40°$ to +85°C, $C_L \leq 50$pF, $f_{OP} = 80$MHz

Characteristic	Symbol	Min	Max	Unit
TCK frequency of operation[2]	f_{OP}	DC	10	MHz
TCK cycle time	t_{CY}	100	—	ns
TCK clock pulse width	t_{PW}	50	—	ns
TMS, TDI data set-up time	t_{DS}	0.4	—	ns
TMS, TDI data hold time	t_{DH}	1.2	—	ns
TCK low to TDO data valid	t_{DV}	—	26.6	ns
TCK low to TDO tri-state	t_{TS}	—	23.5	ns
$\overline{\text{TRST}}$ assertion time	t_{TRST}	50	—	ns
$\overline{\text{DE}}$ assertion time	t_{DE}	4T	—	ns

1. Timing is both wait state- and frequency-dependent. For the values listed, T = clock cycle. For 80MHz operation, T = 12.5ns.
2. TCK frequency of operation must be less than 1/8 the processor rate.
3. Parameters listed are guaranteed by design.

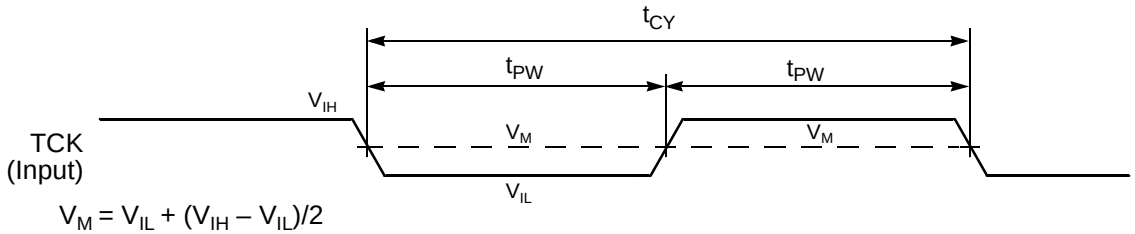


Figure 31. Test Clock Input Timing Diagram

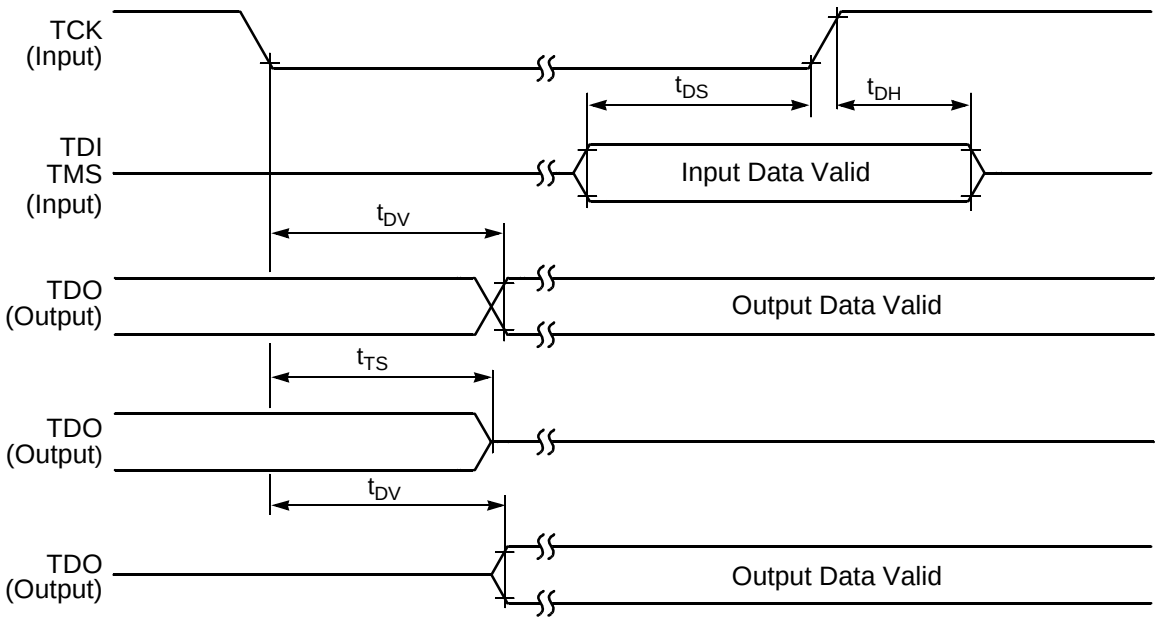


Figure 32. Test Access Port Timing Diagram

Figure 33. $\overline{\text{TRST}}$ Timing Diagram

Figure 34. OnCE—Debug Event

Part 4 Packaging

4.1 Package and Pin-Out Information 56F805

This section contains package and pin-out information for the 144-pin LQFP configuration of the 56F805.

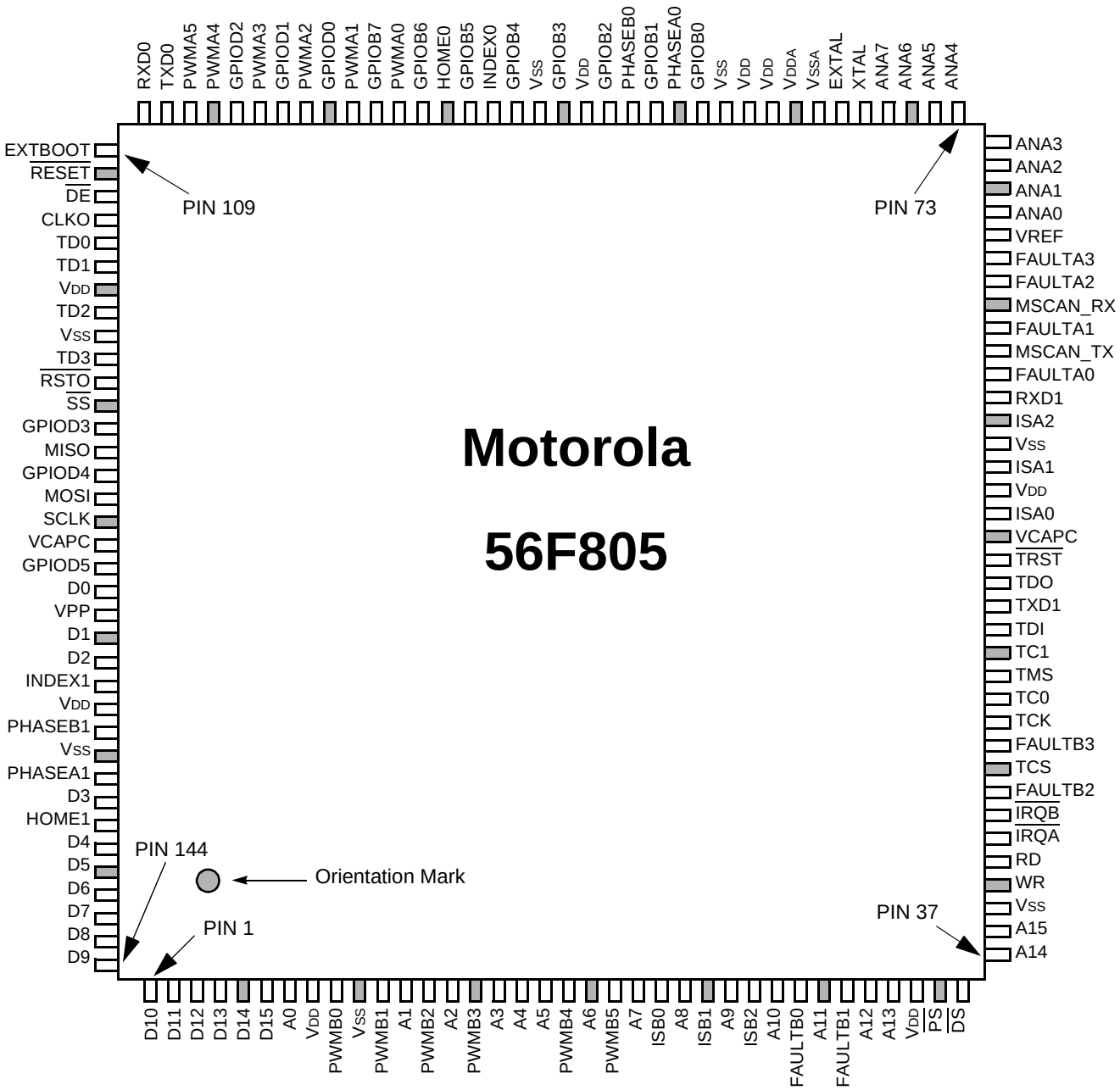


Figure 35. Top View, 56F805 144-pin LQFP Package

Table 38. 56F805 Pin Identification by Pin Number

Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name
1	D10	37	A14	73	ANA4	109	EXTBOOT
2	D11	38	A15	74	ANA5	110	$\overline{\text{RESET}}$
3	D12	39	V_{SS}	75	ANA6	111	$\overline{\text{DE}}$
4	D13	40	WR	76	ANA7	112	CLKO
5	D14	41	RD	77	XTAL	113	TD0
6	D15	42	$\overline{\text{IRQA}}$	78	EXTAL	114	TD1
7	A0	43	$\overline{\text{IRQB}}$	79	V_{SSA}	115	V_{DD}
8	V_{DD}	44	FAULTB2	80	V_{DDA}	116	TD2
9	PWMB0	45	TCS	81	V_{DD}	117	V_{SS}
10	V_{SS}	46	FAULTB3	82	V_{DD}	118	TD3
11	PWMB1	47	TCK	83	V_{SS}	119	$\overline{\text{RSTO}}$
12	A1	48	TC0	84	GPIOB0	120	$\overline{\text{SS}}$
13	PWMB2	49	TMS	85	PHASEA0	121	GPIOD3
14	A2	50	TC1	86	GPIOB1	122	MISO
15	PWMB3	51	TDI	87	PHASEB0	123	GPIOD4
16	A3	52	TXD1	88	GPIOB2	124	MOSI
17	A4	53	TDO	89	V_{DD}	125	SCLK
18	A5	54	$\overline{\text{TRST}}$	90	GPIOB3	126	VCAPC
19	PWMB4	55	VCAPC	91	V_{SS}	127	GPIOD5
20	A6	56	ISA0	92	GPIOB4	128	D0
21	PWMB5	57	V_{DD}	93	INDEX0	129	VPP
22	A7	58	ISA1	94	GPIOB5	130	D1
23	ISB0	59	V_{SS}	95	HOME0	131	D2
24	A8	60	ISA2	96	GPIOB6	132	INDEX1
25	ISB1	61	RXD1	97	PWMA0	133	V_{DD}
26	A9	62	FAULTA0	98	GPIOB7	134	PHASEB1
27	ISB2	63	MSCAN_TX	99	PWMA1	135	V_{SS}

Table 38. 56F805 Pin Identification by Pin Number (Continued)

Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name
28	A10	64	FAULTA1	100	GPIOD0	136	PHASEA1
29	FAULTB0	65	MSCAN_RX	101	PWMA2	137	D3
30	A11	66	FAULTA2	102	GPIOD1	138	HOME1
31	FAULTB1	67	FAULTA3	103	PWMA3	139	D4
32	A12	68	VREF	104	GPIOD2	140	D5
33	A13	69	ANA0	105	PWMA4	141	D6
34	V_{DD}	70	ANA1	106	PWMA5	142	D7
35	$\overline{PS}$	71	ANA2	107	TXD0	143	D8
36	$\overline{DS}$	72	ANA3	108	RXD0	144	D9

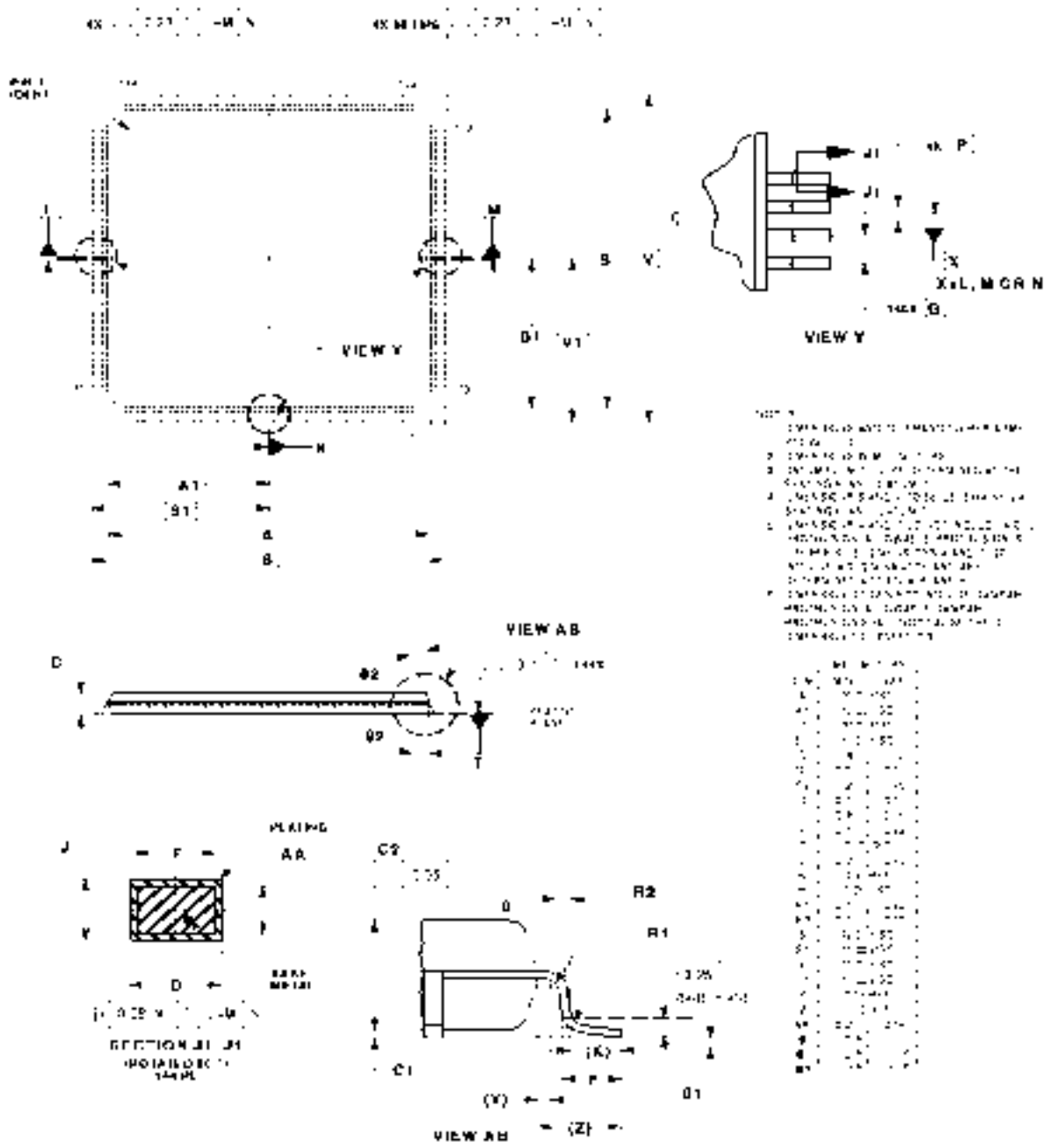


Figure 36. 144-pin LQFP Mechanical Information

Part 5 Design Considerations

5.1 Thermal Design Considerations

An estimation of the chip junction temperature, T_J, in °C can be obtained from the equation:

Equation 1: $$T_J = T_A + (P_D \times R_{\theta JA})$$

Where:

T_A = ambient temperature °C
$R_{\theta JA}$ = package junction-to-ambient thermal resistance °C/W
P_D = power dissipation in package

Historically, thermal resistance has been expressed as the sum of a junction-to-case thermal resistance and a case-to-ambient thermal resistance:

Equation 2: $$R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$$

Where:

$R_{\theta JA}$ = package junction-to-ambient thermal resistance °C/W
$R_{\theta JC}$ = package junction-to-case thermal resistance °C/W
$R_{\theta CA}$ = package case-to-ambient thermal resistance °C/W

$R_{\theta JC}$ is device-related and cannot be influenced by the user. The user controls the thermal environment to change the case-to-ambient thermal resistance, $R_{\theta CA}$. For example, the user can change the air flow around the device, add a heat sink, change the mounting arrangement on the Printed Circuit Board (PCB), or otherwise change the thermal dissipation capability of the area surrounding the device on the PCB. This model is most useful for ceramic packages with heat sinks; some 90% of the heat flow is dissipated through the case to the heat sink and out to the ambient environment. For ceramic packages, in situations where the heat flow is split between a path to the case and an alternate path through the PCB, analysis of the device thermal performance may need the additional modeling capability of a system level thermal simulation tool.

The thermal performance of plastic packages is more dependent on the temperature of the PCB to which the package is mounted. Again, if the estimations obtained from $R_{\theta JA}$ do not satisfactorily answer whether the thermal performance is adequate, a system level model may be appropriate.

Definitions:

A complicating factor is the existence of three common definitions for determining the junction-to-case thermal resistance in plastic packages:

- Measure the thermal resistance from the junction to the outside surface of the package (case) closest to the chip mounting area when that surface has a proper heat sink. This is done to minimize temperature variation across the surface.
- Measure the thermal resistance from the junction to where the leads are attached to the case. This definition is approximately equal to a junction to board thermal resistance.

- Use the value obtained by the equation $(T_J - T_T)/P_D$ where T_T is the temperature of the package case determined by a thermocouple.

The thermal characterization parameter is measured per JESD51-2 specification using a 40-gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over about 1mm of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by cooling effects of the thermocouple wire.

When heat sink is used, the junction temperature is determined from a thermocouple inserted at the interface between the case of the package and the interface material. A clearance slot or hole is normally required in the heat sink. Minimizing the size of the clearance is important to minimize the change in thermal performance caused by removing part of the thermal interface to the heat sink. Because of the experimental difficulties with this technique, many engineers measure the heat sink temperature and then back-calculate the case temperature using a separate measurement of the thermal resistance of the interface. From this case temperature, the junction temperature is determined from the junction-to-case thermal resistance.

5.2 Electrical Design Considerations

CAUTION

This device contains protective circuitry to guard against damage due to high static voltage or electrical fields. However, normal precautions are advised to avoid application of any voltages higher than maximum rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate voltage level.

Use the following list of considerations to assure correct operation:

- Provide a low-impedance path from the board power supply to each V_{DD} pin on the hybrid controller, and from the board ground to each V_{SS} pin.
- The minimum bypass requirement is to place 0.1µF capacitors positioned as close as possible to the package supply pins. The recommended bypass configuration is to place one bypass capacitor on each of the V_{DD}/V_{SS} pairs, including $V_{DDA}/V_{SSA.}$ Ceramic and tantalum capacitors tend to provide better performance tolerances.
- Ensure that capacitor leads and associated printed circuit traces that connect to the chip V_{DD} and V_{SS} pins are less than 0.5 inch per capacitor lead.
- Bypass the V_{DD} and V_{SS} layers of the PCB with approximately 100µF, preferably with a high-grade capacitor such as a tantalum capacitor.
- Because the DSP output signals have fast rise and fall times, PCB trace lengths should be minimal.

- Consider all device loads as well as parasitic capacitance due to PCB traces when calculating capacitance. This is especially critical in systems with higher capacitive loads that could create higher transient currents in the V_{DD} and V_{SS} circuits.
- Take special care to minimize noise levels on the V_{REF}, V_{DDA} and V_{SSA} pins.
- Designs that utilize the $\overline{\text{TRST}}$ pin for JTAG port or OnCE module functionality (such as development or debugging systems) should allow a means to assert $\overline{\text{TRST}}$ whenever $\overline{\text{RESET}}$ is asserted, as well as a means to assert $\overline{\text{TRST}}$ independently of $\overline{\text{RESET}}$. $\overline{\text{TRST}}$ must be asserted at power up for proper operation. Designs that do not require debugging functionality, such as consumer products, $\overline{\text{TRST}}$ should be tied low.
- TRST must be externally asserted even when the user relies on the internal power on reset for functional test purposes.
- Because the Flash memory is programmed through the JTAG/OnCE port, designers should provide an interface to this port to allow in-circuit Flash programming.

Part 6 Ordering Information

Table 39 lists the pertinent information needed to place an order. Consult a Motorola Semiconductor sales office or authorized distributor to determine availability and to order parts.

Table 39. 56F805 Ordering Information

Part	Supply Voltage	Package Type	Pin Count	Frequency (MHz)	Order Number
56F805	3.0–3.6 V	Low Profile Plastic Quad Flat Pack (LQFP)	144	80	DSP56F805FV80

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