Product List

SM59264C25, 25 MHz 128KB internal flash MCU
SM59264C40, 40 MHz 128KB internal flash MCU

Description

The SM59264 series product is an 8 - bit single chip microcontroller with 128KB on-chip flash which including 64KB program flash & 64KB data flash and 1K byte RAM embedded. It has In-System Programming (ISP) function and is a derivative of the 8052 microcontroller family. It has 4-channel SPWM build-in. User can access on-chip expanded RAM with easier and faster way by its 'bank mapping direct addressing mode' scheme. With its hardware features and powerful instruction set, it's straight forward to make it a versatile and cost effective controller for those applications which demand up to 32 I/O pins for PDIP package or up to 36 I/O pins for PLCC/QFP package, or applications which need up to 64K byte flash memory for program and/or for data.

To program the on-chip flash memory, a commercial writer is available to do it in parallel programming method. The on-chip flash memory can be programmed in either parallel or serial interface with its ISP feature.

Ordering Information

yywwv
SM59264ihhk

yy: year, ww:week
v: version identifier { , A, B, ...}
i: process identifier
hh: working clock in MHz {25, 40}
k: package type postfix {as below table}

Postfix	Package	Pin/Pad Configuration	Dimension
P	40L PDIP	page 2	page 28
J	44L PLCC	page 2	page 29
Q	44L QFP	page 2	page 30

Features

- Working voltage:4.5V through 5.5V
- General 8052 family compatible
- 12 clocks per machine cycle
- 64K byte on chip program flash with In-System Programming (ISP) capability
- 64K byte on-chip data flash with ISP capability
- 1024 byte on-chip RAM
- Three 16 bit Timers/Counters
- One Watch Dog Timer
- Four 8-bit I/O ports for PDIP package
- Four 8-bit I/O ports + one 4-bit I/O ports for PLCC or QFP package
- Full duplex serial channel
- Bit operation instruction
- Page free jumps
- 8-bit Unsigned Division
- 8-bit Unsigned Multiply
- BCD arithmetic
- Direct Addressing
- Indirect Addressing
- Nested Interrupt
- Two priority level interrupt
- A serial I/O port
- Power save modes: Idle mode and Power down mode
- Code protection function
- Low EMI (inhibit ALE)
- Reset with address $0000 blank initiate ISP service program
- ISP service program space configurable in N*512 byte (N=0 to 8) size
- Bank mapping direct addressing mode for access on-chip RAM
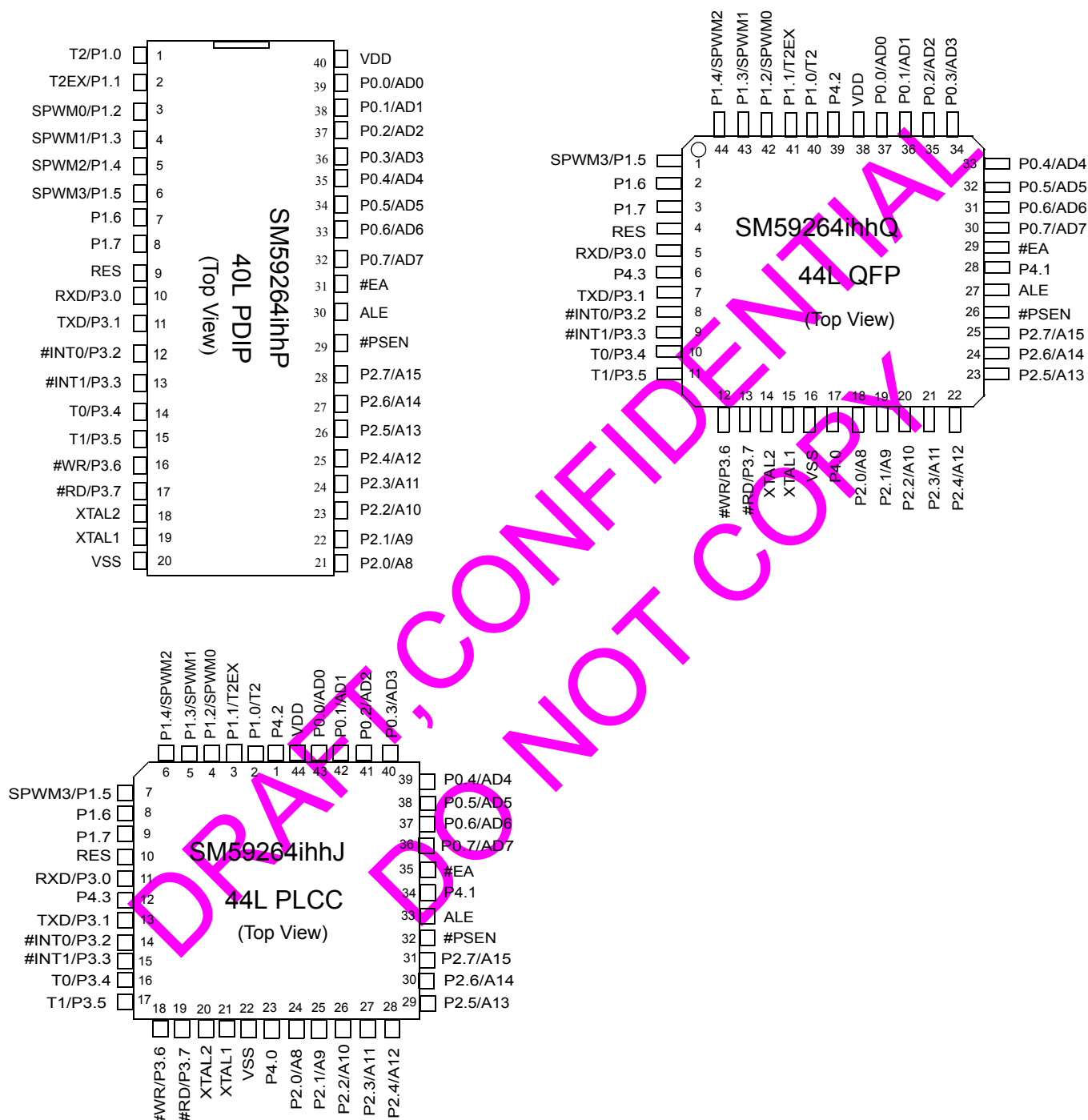- 4 channel SPWM function

Website: http://www.syncmos.com.tw

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Pin Configurations

SM59264ihhP
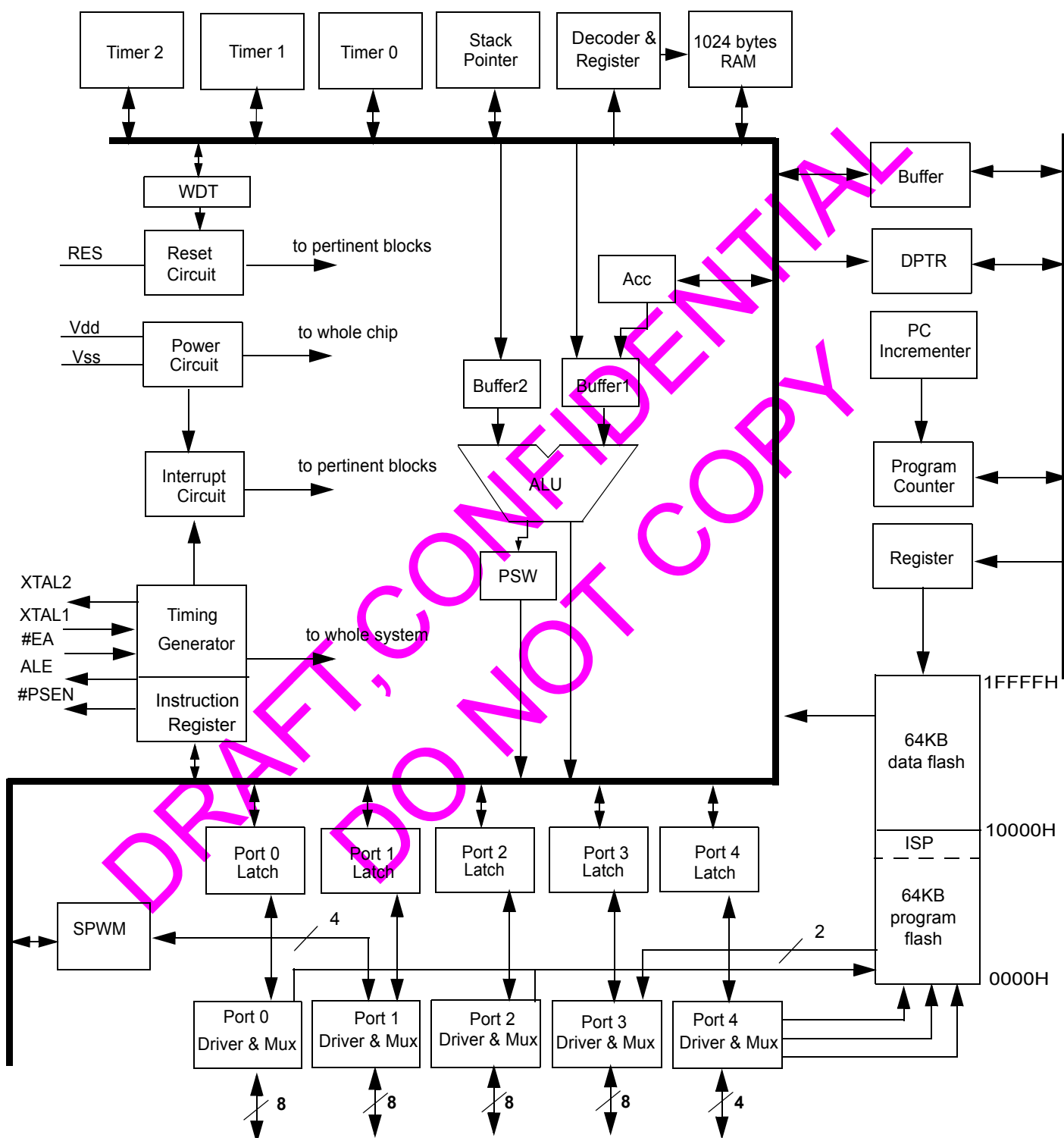**40L PDIP**
(Top View)

Pin	Left		Pin	Right
1	T2/P1.0		40	VDD
2	T2EX/P1.1		39	P0.0/AD0
3	SPWM0/P1.2		38	P0.1/AD1
4	SPWM1/P1.3		37	P0.2/AD2
5	SPWM2/P1.4		36	P0.3/AD3
6	SPWM3/P1.5		35	P0.4/AD4
7	P1.6		34	P0.5/AD5
8	P1.7		33	P0.6/AD6
9	RES		32	P0.7/AD7
10	RXD/P3.0		31	#EA
11	TXD/P3.1		30	ALE
12	#INT0/P3.2		29	#PSEN
13	#INT1/P3.3		28	P2.7/A15
14	T0/P3.4		27	P2.6/A14
15	T1/P3.5		26	P2.5/A13
16	#WR/P3.6		25	P2.4/A12
17	#RD/P3.7		24	P2.3/A11
18	XTAL2		23	P2.2/A10
19	XTAL1		22	P2.1/A9
20	VSS		21	P2.0/A8

SM59264ihhQ
44L QFP
(Top View)

Top pins (44–34): P1.4/SPWM2, P1.3/SPWM1, P1.2/SPWM0, P1.1/T2EX, P1.0/T2, P4.2, VDD, P0.0/AD0, P0.1/AD1, P0.2/AD2, P0.3/AD3

Left pins (1–11): SPWM3/P1.5, P1.6, P1.7, RES, RXD/P3.0, P4.3, TXD/P3.1, #INT0/P3.2, #INT1/P3.3, T0/P3.4, T1/P3.5

Right pins (33–23): P0.4/AD4, P0.5/AD5, P0.6/AD6, P0.7/AD7, #EA, P4.1, ALE, #PSEN, P2.7/A15, P2.6/A14, P2.5/A13

Bottom pins (12–22): #WR/P3.6, #RD/P3.7, XTAL2, XTAL1, VSS, P4.0, P2.0/A8, P2.1/A9, P2.2/A10, P2.3/A11, P2.4/A12

SM59264ihhJ
44L PLCC
(Top View)

Top pins (6–40): P1.4/SPWM2, P1.3/SPWM1, P1.2/SPWM0, P1.1/T2EX, P1.0/T2, P4.2, VDD, P0.0/AD0, P0.1/AD1, P0.2/AD2, P0.3/AD3

Left pins (7–17): SPWM3/P1.5, P1.6, P1.7, RES, RXD/P3.0, P4.3, TXD/P3.1, #INT0/P3.2, #INT1/P3.3, T0/P3.4, T1/P3.5

Right pins (39–29): P0.4/AD4, P0.5/AD5, P0.6/AD6, P0.7/AD7, #EA, P4.1, ALE, #PSEN, P2.7/A15, P2.6/A14, P2.5/A13

Bottom pins (18–28): #WR/P3.6, #RD/P3.7, XTAL2, XTAL1, VSS, P4.0, P2.0/A8, P2.1/A9, P2.2/A10, P2.3/A11, P2.4/A12

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Block Diagram

Specifications subject to change without notice,contact your sales representatives for the most recent information.

Pin Descriptions

40L PDIP Pin#	44L QFP Pin#	44L PLCC Pin#	Symbol	Active	I/O	Names
1	40	2	T2/P1.0		i/o	timer 2 clock out & bit 0 of port 1
2	41	3	T2EX/P1.1		i/o	timer 2 control & bit 1 of port 1
3	42	4	SPWM0/P1.2		i/o	SPWM channel 0, bit 2 of port 1
4	43	5	SPWM1/P1.3		i/o	SPWM channel 1, bit 3 of port 1
5	44	6	SPWM2/P1.4		i/o	SPWM channel 2, bit 4 of port 1
6	1	7	SPWM3/P1.5		i/o	SPWM channel 3, bit 5 of port 1
7	2	8	P1.6		i/o	bit 6 of port 1
8	3	9	P1.7		i/o	bit 7 of port 1
9	4	10	RES	H	i	Reset
10	5	11	RXD/P3.0		i/o	Receive data & bit 0 of port 3
11	7	13	TXD/P3.1		i/o	Transmit data & bit 1 of port 3
12	8	14	#INT0/P3.2	L/ -	i/o	low true interrupt 0 & bit 2 of port 3
13	9	15	#INT1/P3.3	L/ -	i/o	low true interrupt 1 & bit 3 of port 3
14	10	16	T0/P3.4		i/o	Timer 0 & bit 4 of port 3
15	11	17	T1/P3.5		i/o	Timer 1 & bit 5 of port 3
16	12	18	#WR/P3.6		i/o	ext. memory write & bit 6 of port 3
17	13	19	#RD/P3.7		i/o	ext. mem. read & bit 7 of port 3
18	14	20	XTAL2		o	Crystal out
19	15	21	XTAL1		i	Crystal in
20	16	22	VSS			Sink Voltage, Ground
21	18	24	P2.0/A8		i/o	bit 0 of port 2 & bit 8 of ext. memory address
22	19	25	P2.1/A9		i/o	bit 1 of port 2 & bit 9 of ext. memory address
23	20	26	P2.2/A10		i/o	bit 2 of port 2 & bit 10 of ext. memory address
24	21	27	P2.3/A11		i/o	bit 3 of port 2 & bit 11 of ext. memory address
25	22	28	P2.4/A12		i/o	bit 4 of port 2 & bit 12 of ext. memory address
26	23	29	P2.5/A13		i/o	bit 5 of port 2 & bit 13 of ext. memory address
27	24	30	P2.6/A14		i/o	bit 6 of port 2 & bit 14 of ext. memory address
28	25	31	P2.7/A15		i/o	bit 7 of port 2 & bit 15 of ext. memory address
29	26	32	#PSEN		o	program storage enable
30	27	33	ALE		o	address latch enable
31	29	35	#EA	L	i	external access & VPP
32	30	36	P0.7/AD7		i/o	bit 7 of port 0 & data/address bit 7 of ext. memory
33	31	37	P0.6/AD6		i/o	bit 6 of port 0 & data/address bit 6 of ext. memory
34	32	38	P0.5/AD5		i/o	bit 5 of port 0 & data/address bit 5 of ext. memory
35	33	39	P0.4/AD4		i/o	bit 4 of port 0 & data/address bit 4 of ext. memory
36	34	40	P0.3/AD3		i/o	bit 3 of port 0 & data/address bit 3 of ext. memory
37	35	41	P0.2/AD2		i/o	bit 2 of port 0 & data/address bit 2 of ext. memory
38	36	42	P0.1/AD1		i/o	bit 1 of port 0 & data/address bit 1 of ext. memory
39	37	43	P0.0/AD0		i/o	bit 0 of port 0 & data/address bit 0 of ext. memory
40	38	44	VDD			Drive Voltage, +5 Vcc
	17	23	P4.0		i/o	bit 0 of Port 4
	28	34	P4.1		i/o	bit 1 of Port 4
	39	1	P4.2		i/o	bit 2 of Port 4
	6	12	P4.3		i/o	bit 3 of Port 4

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Special Function Register (SFR)

The address $80 to $FF can be accessed by direct addressing mode only.
Address $80 to $FF is SFR area.
The following table lists the SFRs which are identical to general 8052, as well as SM59264 Extension SFRs.

Special Function Register (SFR) Memory Map

$F8								$FF
$F0	B				**ISPFAH**	**ISPFAL**	**ISPFD**	**ISPC**	$F7
$E8								$EF
$E0	ACC							$E7
$D8	**P4**							$DF
$D0	PSW							$D7
$C8	T2CON	T2MOD	RCAP2L	RCAP2H	TL2	TH2		$CF
$C0								$C7
$B8	IP						**SCONF**	$BF
$B0	P3							$B7
$A8	IE							$AF
$A0	P2		**SPWMC**	**SPWMD0**	**SPWMD1**	**SPWMD2**	**SPWMD3**	$A7
$98	SCON	SBUF	**P1CON**				**WDTC**	$9F
$90	P1						**WDTKEY**	$97
$88	TCON	TMOD	TL0	TL1	TH0	TH1		$8F
$80	P0	SP	DPL	DPH	(Reserved)	**RCON**	**DBANK**	PCON	$87

Note: The text of SFRs with bold type characters are Extension Special Function Registers for SM59264

Addr	SFR	Reset	7	6	5	4	3	2	1	0
85H	**RCON**	00H	RAMS7	RAMS6	RAMS5	RAMS4	RAMS3	RAMS2	RAMS1	RAMS0
86H	**DBANK**	0***0001	BSE				BS3	BS2	BS1	BS0
97H	**WDTKEY**	********	WDTKEY7	WDTKEY6	WDTKEY5	WDTKEY4	WDTKEY3	WDTKEY2	WDTKEY1	WDTKEY0
9BH	**P1CON**	**0000**			SPWME3	SPWME2	SPWME1	SPWME0		
9FH	**WDTC**	0*0**000	WDTE		CLEAR			PS2	PS1	PS0
A3H	**SPWMC**	******00							SPFS1	SPFS0
A4H	**SPWMD0**	00H	SPWMD04	SPWMD03	SPWMD02	SPWMD01	SPWMD00	BRM02	BRM01	BRM00
A5H	**SPWMD1**	00H	SPWMD14	SPWMD13	SPWMD12	SPWMD11	SPWMD10	BRM12	BRM11	BRM10
A6H	**SPWMD2**	00H	SPWMD24	SPWMD23	SPWMD22	SPWMD21	SPWMD20	BRM22	BRM21	BRM20
A7H	**SPWMD3**	00H	SPWMD34	SPWMD33	SPWMD32	SPWMD31	SPWMD30	BRM32	BRM31	BRM30
BFH	**SCONF**	0***_0000	WDR				DFEN	ISPE	OME	ALEI
C8H	**T2CON**	00H	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/T2	CP/RL2
C9H	**T2MOD**	******00	*	*	*	*	*	*	T2OE	DCEN
D8H	**P4**	****1111					P4.3	P4.2	P4.1	P4.0

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Addr	SFR	Reset	7	6	5	4	3	2	1	0
F4H	**ISPFAH**	00H	FA15	FA14	FA13	FA12	FA11	FA10	FA9	FA8
F5H	**ISPFAL**	00H	FA7	FA6	FA5	FA4	FA3	FA2	FA1	FA0
F6H	**ISPFD**	00H	FD7	FD6	FD5	FD4	FD3	FD2	FD1	FD0
F7H	**ISPC**	0*0***00	START		FAU0				ISPF1	ISPF0

Extension Function Description

1. Memory Structure

The SM59264 is the general 8052 hardware core to integrate the expanded 768 byte data RAM, 64KB flash program memory with ISP function module and 64KB data flash as a single chip microcontroller. Its memory structure follows general 8052 structure plus SM59264 propriatary external RAM structure.

1.1 Program Memory

The SM59264 has 64K byte on-chip flash memory which used as general program memory, on which include up to 4K byte specific ISP service program memory space. The address range for the 64K byte is $0000 to $FFFF. The address range for the ISP service program is $F000 to $FFFF. The ISP service program size can be partitioned as N blocks of 512 byte (N=0 to 8). When N=0 means no ISP service program space available, total 64K byte memory used as program memory. When N=1 means memory address $FE00 to $FFFF reserved for ISP service program. When N=2 means memory address $FC00 to FFFF reserved for ISP service program,...etc. Value N can be set and programmed into SM59264 by writer.

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6/32   Preliminary   Ver 0.1   PID 59264   05/02
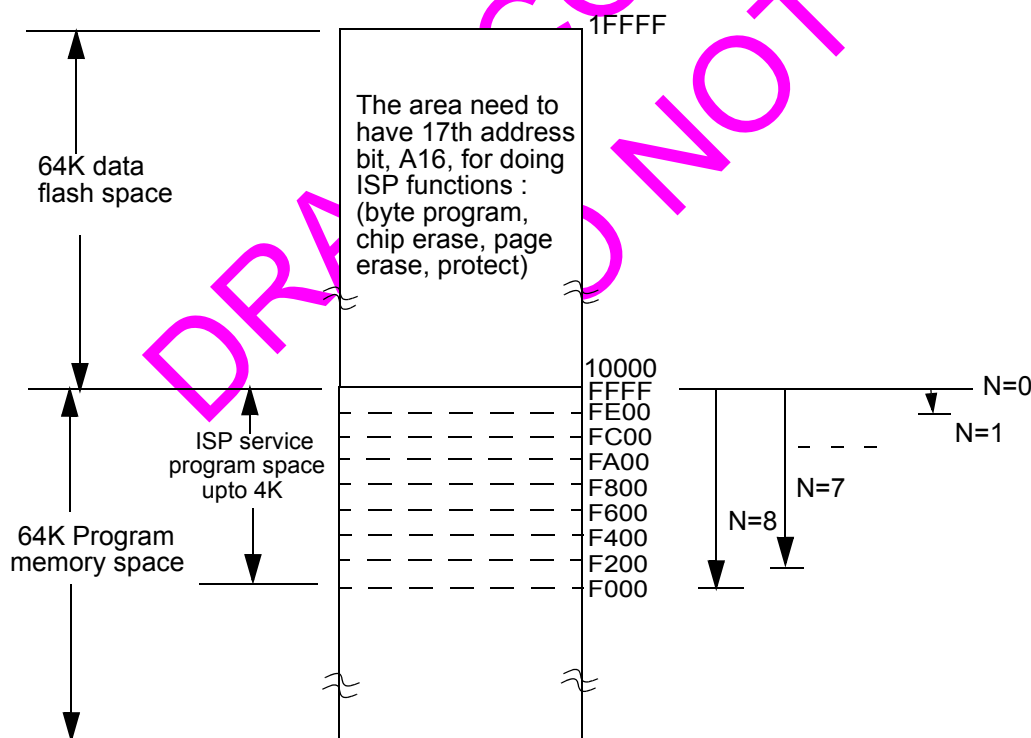
Note: The single flash block address structure for doing the ISP function to the on-chip data flash as well as program ROM flash.

1.2 Data Memory

The SM59264 has 1K bytes on-chip RAM, 256 bytes of it are the same as general 8052 internal memory structure while the expanded 768 bytes on-chip RAM can be accessed by external memory addressing method (by instruction MOVX), or by 'Bank mapping direct addressing mode' as described in page 9. The SM59264 also has 64K bytes data flash embedded in. The contents of data flash can be erased or programmed by software control and can be read by MOVX instruction. User can use MOVX instruction to access internal RAM, internal data flash or external memory by setting OME and DFEN. The different setting of OME and DFEN will map to different memory block.

```
                                                              02FF

                                              Expanded 768 bytes RAM
                                              (Accessed by direct external
                                              addressing mode, by instruction
                                              MOVX, or by Bank mapping
                                        FF    direct addressing mode)
  FF  Higher 128 bytes (Access by     SFR (Accessed by direct
  80  indirect addressing mode only)  addressing mode only)
  7F  Lower 128 bytes  (Accessed by                  80
  00  direct & indirect addressing mode)                          0000
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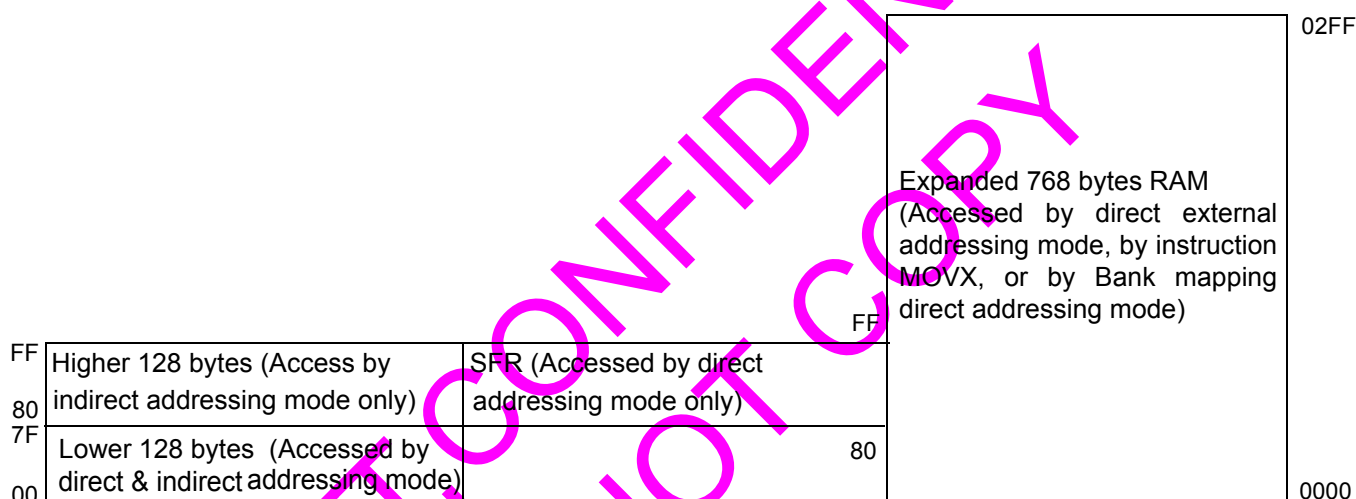
On-chip expanded RAM address structure.

DFEN	OME	address of MOVX below 768	address of MOVX over 768
0	0	external memory	external memory
0	1	internal RAM	external memory
1	0	internal data flash	internal data flash
1	1	internal RAM	internal data flash
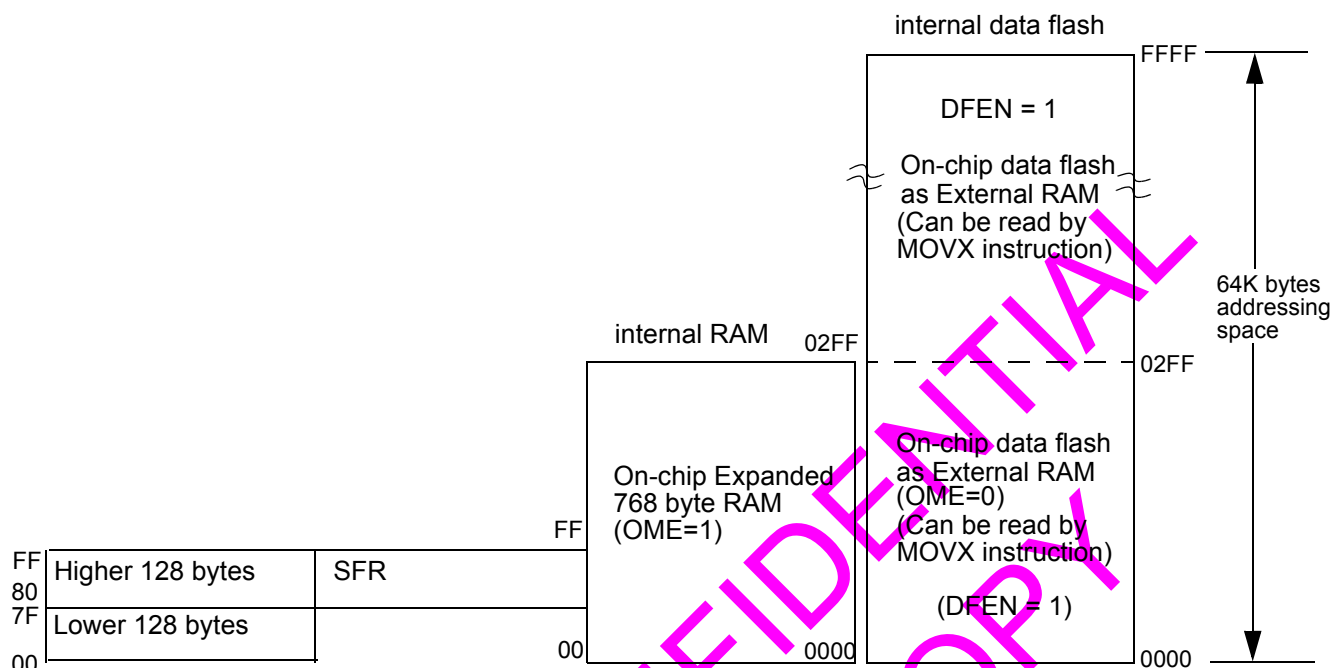
Note: External RAM address structure for reading the on-chip data flash.

1.2.1 Data Memory - Lower 128 byte ($00 to $7F, Bank 0 & Bank 1)

Data Memory $00 to $FF is the same as 8052.

The address $00 to $7F can be accessed by direct and indirect addressing modes.

Address $00 to $1F is register area.

Address $20 to $2F is memory bit area.

Address $30 to $7F is for general memory area.

1.2.2 Data Memory - Higher 128 byte ($80 to $FF, Bank 2 & Bank 3)

The address $80 to $FF can be accessed by indirect addressing mode or by bank mapping direct addressing mode.

Address $80 to $FF is data area.

1.2.3 Data Memory - Expanded 768 bytes ($0000 to $02FF, Bank 4 ~ Bank 15)

From external address $0000 to $02FF is the on-chip expanded RAM area, total 768 bytes. This area can be accessed by external direct addressing mode (by instruction MOVX) or by bank mapping direct addressing mode as described below:

1.3 Bank mapping direct addressing mode:

We provide RAM bank address '40H~7FH' as mapping window which allow user access all the 1K on-chip RAM through this RAM bank address.

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BS3	BS2	BS1	BS0	040h~07fh mapping address	Note
0	0	0	0	000h~03fh	lower 128 byte RAM
0	0	0	1	040h~07fh	lower 128 byte RAM
0	0	1	0	080h~0bfh	higher 128 byte RAM
0	0	1	1	0c0h~0ffh	higher 128 byte RAM
0	1	0	0	0000h~003fh	on-chip expanded 768 byte RAM
0	1	0	1	0040h~007fh	"
0	1	1	0	0080h~00bfh	"
0	1	1	1	00c0h~00ffh	"
1	0	0	0	0100h~013fh	"
1	0	0	1	0140h~017fh	"
1	0	1	0	0180h~01bfh	"
1	0	1	1	01c0h~01ffh	"
1	1	0	0	0200h~023fh	"
1	1	0	1	0240h~027fh	"
1	1	1	0	0280h~02bfh	"
1	1	1	1	02c0h~02ffh	"

With this bank mapping scheme, user can access entire 1k byte on-chip RAM with direct addressing method. That means using the window area ($040~$07F), user can access any bank (64 byte) data of 1k byte on-chip RAM space which is selected by BS[3:0] of data bank control register (DBANK, $86).

For example, user write #30h to $101 address :
MOV   DBANK, #88H   ; set bank mapping $040~$07f to $0100~$013f
MOV   A, #30H   ; store #30H to A
MOV   41H, A   ; write #30H to $0101 address

Data Bank Control Register (DBANK, $86)

	bit-7						bit-0
Read : Write :	BSE	Unused	Unused	Unused	BS3	BS2	BS1	BS0
Reset value :	0	*	*	*	0	0	0	1

Data bank select enable bit BSE = 1 enables the data bank select function
Data bank select enable bit BSE = 0 disables the data bank select function
BS[3:0] setting will map $040~$07F RAM space to entire 1k byte on-chip RAM space.

1.4 Data Flash - ($0000 to $ FFFF)

SM59264 has 64K byte on-chip data flash embedded. The 64KB on-chip data flash can be read by direct external addressing mode (by MOVX instruction) which means user does not need to care about 17th flash address bit (FA16). To read 64KB on-chip data flash is similiar to read 64KB external RAM. However, to write (program) data flash is much different from to read data flash. User need to use SyncMOS preprietary ISP function, such as byte program/chip erase/page erase/protect, to the data flash. To do ISP function to data flash need to set FAU0 bit of ISPC ($F7) at first. User has to recognize 64K program ROM flash and 64KB data flash as combined one single 128KB flash area for ISP function. 64K byte data flash resides on top of the 64K byte program ROM flash. Please see ISP function description on page 14 for detail.

Read data flash : Using direct external addressing mode (by instruction MOVX). Reading on-chip data flash will be the same as reading external RAM with MOVX instruction.
For example,　　MOVX A, @DPTR　or　MOVX A, @Ri　; i=0,1

instruction with 16-bit addressing space.

Write data flash : Using ISP 'byte program' function will have to set the FAU0 bit at first.

Erase data flash : Including ISP 'chip erase' function and 'page erase' function. When using 'chip erase' function, it will erase all the 64K byte data flash plus 64K byte program ROM flash except the ISP service program space if lock bit 'N' been configured.

Chip protect flash : Using ISP 'chip protect' function will protect the 64K byte data flash plus 64K byte program ROM flash from read out. Once flash been protected, the content read will be all '00'.

For 'byte program' and 'page erase' flash-address-dependent ISP functions, user need to specify the FAU0 bit (=FA16) of ISPC ($F7) at first for doing with data flash space. The 64K data flash also can be programmed or erased on writer.

1.4.1 Second Data Pointer Register - RCON ($85) and MOVX @Ri, i=1,2 with read function

Using RCON register with MOVX @Ri, i=0,1 instruction enables SM59264 has second Data Pointer Register (DPTR) with read function only. The content of RCON register determines high byte address of 64KB data flash while content of MOVX @Ri instruction determines low byte address. This feature similiar to DPH and DPL register of MOVX @ DPTR instruction but with read function only. Using MOVX @Ri instruction to write data to the data flash will have no effect.

Internal RAM Control Register (RCON, $85)

	bit-7							bit-0
Read : Write :	RAMS7	RAMS6	RAMS5	RAMS4	RAMS3	RAMS2	RAMS1	RAMS0
Reset value :	0	0	0	0	0	0	0	0

RAMS[7:0] setting will map on-chip RAM and/or data flash space by pages which accessed by MOVX @Ri

instruction, i=0,1

The address space of instruction MOVX @Ri is determined by RAMS[7:0] of RCON. The default setting of RAMS[7:0] is 00H (page 0).

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One page of data RAM is 256 bytes.

The port 0, port2, port3.6 and port3.7 can be used as general purpose I/O pin while port0 is open-drain structure.

System Control Register (SCONF, $BF)

	bit-7							bit-0
Read : Write :	WDR	Unused	Unused	Unused	DFEN	ISPE	OME	ALEI
Reset value :	0	*	*	*	0	0	0	0

WDR : Watch Dog Timer Reset. When system reset by Watch Dog Timer overflow, WDR will be set to 1, The bit 7 (WDR) of SCONF is Watch Dog Timer Reset bit. It will be set to 1 when reset signal generated by WDT overflow. User should check WDR bit whenever unpredicted reset happened.

DFEN: 64K Data Flash enable bit. The default setting of DFEN bit is 0 (disable).

ISPE : ISP enable bit

OME : 768 bytes on-chip RAM enable bit, The bit 1 (OME) of SCONF can enable or disable the on-chip expanded 768 byte RAM. The default setting of OME bit is 0 (disable).

ALEI : ALE output inhibit bit, to reduce EMI, Setting bit 0 (ALEI) of SCONF can inhibit the clock signal in Fosc/6Hz output to the ALE pin.

1.5 I/O Pin Configuration

The ports 1, 2 and 3 of standard 8051 have internal pull-up resistor, and port 0 has open-drain outputs. Each I/O pin can be used independently as an input or an output. For I/O ports to be used as an input pin, the port bit latch must contain a '1' which turns off the output driver FET. Then for port 1, 2 and 3 port pin is pulled high by a weak internal pull-up, and can be pulled low by an external source. The port 0 has open-drain outputs which means its pull-ups are not active during normal port operation. Writing '1' to the port 0 bit latch will causing bit floating so that it can be used as a high-impedance input.

The port 4 used as GPIO will has the same function as port 1, 2 and 3.

output data → ▷ → pin port 0 standard 8051
input data ←

output data → ▷ → pin port 1, 2 and 3 standard 8051
input data ←

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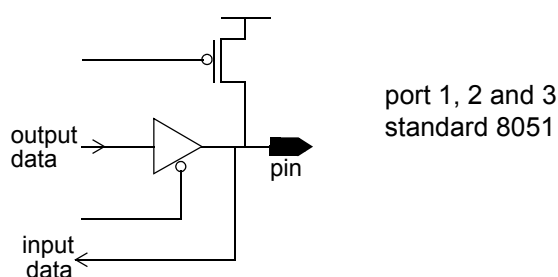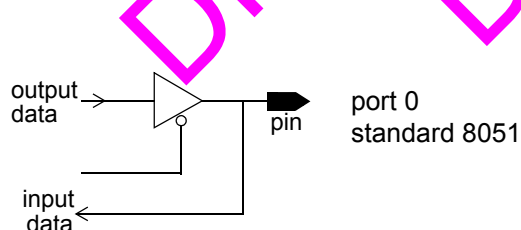
2. Port 4 for PLCC or QFP package :

The bit addressable port 4 is available with PLCC or QFP package. The port 4 has only 4 pins and its port address is located at 0D8H. The function of port 4 is the same as the function of port 1, port 2 and port 3.

Port4 (P4, $D8)

	bit-7							bit-0
Read : Write :	Unused	Unused	Unused	Unused	P4.3	P4.2	P4.1	P4.0
Reset value :	*	*	*	*	1	1	1	1

The bit 3, bit 2, bit 1, bit 0 output the setting to pin P4.3, P4.2, P4.1, P4.0 respectively.

3. In-System Programming (ISP) Function

The SM59264 can generate flash control signal by internal hardware circuit. User utilize flash control register, flash address register and flash data register to perform the in-system programming (ISP) function without removing the SM59264 from the system.

The SM59264 provides internal flash control signal which can do flash progam/chip erase/page erase/protect functions. User need to design and use any kind of interface which SM59264 can input data. User then utilize ISP service program to perform the flash program/chip erase/page erase/protect functions.

3.1 ISP Service Program

The ISP service program is a user developed firmware program which resides in the ISP service program space. After user developed the ISP service program, user then determine the size of the ISP service program. User need to program the ISP service program in the SM59264 for the ISP purpose.
The ISP service program were developed by user so that it should includes any features which relates to the flash memory programming function as well as communication protocol between SM59264 and host device which output data to the SM59264. For example, if user utilize UART interface to receive/transmit data between SM59264 and host device, the ISP service program should include baut rate, checksum or parity check or any error-checking mechanism to avoid data transmission error.
The ISP service program can be initiated under SM59264 active or idle mode. It can not be initiated under power down mode.

3.2 Lock Bit (N)

The Lock Bit N has two functions: one is for service program size configuration and the other is to lock the ISP service program space from flash erase function.

The ISP service program space address range from $F000 to $FFFF. It can be divided as blocks of N*512 byte. (N=0 to 8). When N=0 means no ISP function, all of 64K byte flash memory can be used as program memory. When N=1 means ISP service program occupies 512 byte while the rest of 63.5K byte flash memory can be used as program memory. The maximum ISP service program allowed is 4K byte for N=8. Under such configuration, the usable program memory space is 60K byte.

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After N determined, SM59264 will reserve the ISP service program space downward from the top of the program address $FFFF. The start address of the ISP service program located at $Fx00 while x is an even number, depending on the lock bit N. Please see page 7 program memory diagram for this ISP service program space structure.

The lock bit N function is different from the flash protect function. The chip erase function can erase all of the flash memory space including 64KB program flash & 64KB data flash, except for the locked ISP service program space. If the flash not been protected, the content of flash program still can be read. If the flash been protected, the overall content of flash program memory space including ISP service program space can not be read.

3.3 Program the ISP Service Program

After Lock Bit N is set and ISP service program been programmed, the ISP service program memory will be protected (locked) automatically. The lock bit N has its own program/erase timing. It is different from the flash memory program/erase timing so the locked ISP service program can not be erased by flash erase function. If user need to erase the locked ISP service program, he can do it by writer only. User can not change ISP service program when SM59264 was in system.

3.4 Initiate ISP Service Program

To initiate the ISP service program is to load the program counter (PC) with start address of ISP service program and execute it. There are three ways to do so:
(1) Blank reset. Hardware reset with first flash address blank ($0000=#FFH) will load the PC with start address of ISP service program.
(2) Execute 'JUMP' instruction can load the start address of the ISP service program to PC.
(3) Enter's ISP service program by hardware setting. User can force SM59264 enter ISP service program by setting P2.6, P2.7 "low or P4.3 "low" during hardware reset period. In application system design, user should take care of the setting of P2.6, P2.7 and P4.3 at reset period to prevent SM59264 from entering ISP service program.

Enters ISP service program by hardware setting :
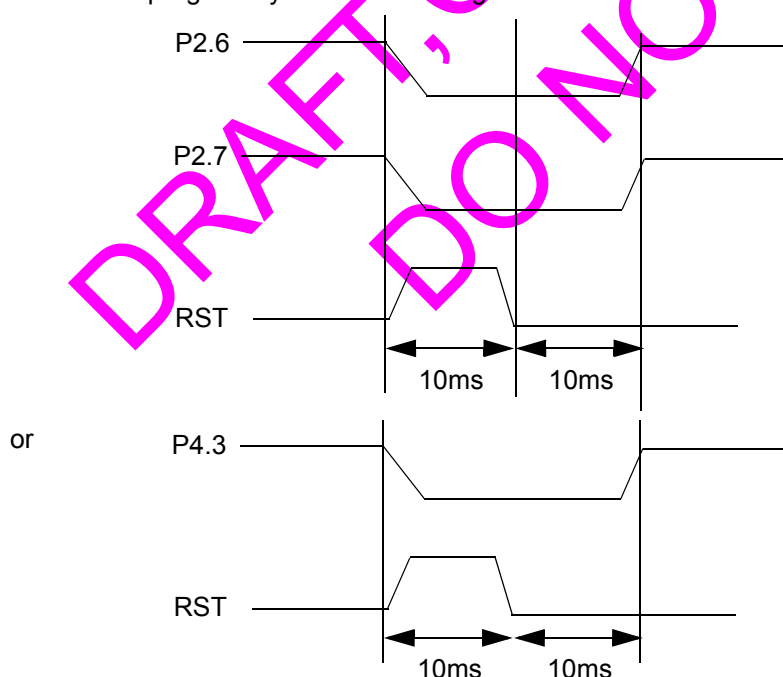
User can initiate general 8052 UART function to initiate the ISP service program. After ISP service program executed, user need to reset the SM59264, either by hardware reset or by WDT, or jump to the address $0000 to re-start the firmware program.

3.5 ISP Registers - System Control Register (SCONF, $BF)

	bit-7							bit-0
Read : Write :	WDR	Unused	Unused	Unused	DFEN	ISPE	OME	ALEI
Reset value :	0	0	0	0	0	0	0	0

The bit 2 (ISPE) of SCONF is ISP enable bit. User can enable overall ISP function by setting ISPE bit to 1, setting ISPE to 0 will disable overall ISP function.

The function of ISPE behaves like a security key. User can disable overall ISP function to prevent software program be erased accidentally.

3.6 ISP Registers : ISPFAH, ISPFAL, ISPFD and ISPC registers

The ISPFAH & ISPFAL provide the 16-bit flash memory address for ISP function. The flash memory address should not include the ISP service program space address. If the flash memory address indicated by ISPFAH & ISPFAL registers overlay with the ISP service program space address, the flash program/page erase of ISP function executed thereafter will have no effect.

When performing byte program ISP function, the content of ISPFD register will be programmed to the flash address which indicated by ISPFAH and ISPFAL registers.

ISP Registers- Flash Address-High Register (ISPFAH, $F4)

	bit-7							bit-0
Read : Write :	FA15	FA14	FA13	FA12	FA11	FA10	FA9	FA8
Reset value :	0	0	0	0	0	0	0	0

FA15 ~ FA8 : flash address-high for ISP function

ISP Registers - Flash Address-Low Register (ISPFAL, $F5)

	bit-7							bit-0
Read : Write :	FA7	FA6	FA5	FA4	FA3	FA2	FA1	FA0
Reset value :	0	0	0	0	0	0	0	0

FA7 ~ FA0 : flash address-low for ISP function

The ISPFAH & ISPFAL provide the 16-bit flash memory address for ISP function. The flash memory address should not include the ISP service program space address. If the flash memory address indicated by ISPFAH & ISPFAL registers overlay with the ISP service program space address, the flash program/page erase of ISP function executed thereafter will have no effect.

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ISP Registers - Flash Data Register (ISPFD, $F6)

	bit-7							bit-0
Read : Write :	FD7	FD6	FD5	FD4	FD3	FD2	FD1	FD0
Reset value :	0	0	0	0	0	0	0	0

FD7 ~FD0 : flash data for ISP function

The ISPFD provide the 8-bit data for ISP function

ISP Registers - Flash Control Register (ISPC, $F7)

	bit-7							bit-0
Read : Write :	START	Unused	FAU0	Unused	Unused	Unused	ISPF1	ISPF0
Reset value :	0	0	0	0	0	0	0	0

ISPF[1:0] : ISP function select bit

ISPF [1:0]	ISP function
00	Byte program
01	Chip protect
10	Page erase (512Byte)
11	Chip erase

START : ISP function start bit
     = 1 : start ISP function which indicated by bit 1, bit 0 (ISPF1, ISPF0)
     = 0 : no operation
FAU0 : 64K program Flash or 64K Data Flash select bit
     = 1 : selected 64K data flash
     = 0 : selected 64K program flash

Note: The START bit is read-only by default, software must write three specific values 55H, AAH and 55H sequentially to the ISPFD register to enable the START bit write attribute. That is :
    MOV ISPFD, #55H
    MOV ISPFD, #AAH
    MOV ISPFD, #55H

Any attempt to set START bit will not be allowed without the procedure above.

After START bit set to 1 then the SM59264 hardware circuit will latch flash address and data bus and hold the program counter until the START bit reset to 0 when ISP function finished. The program counter (PC) will point to next instruction after START bit reset to 0. User does not need to check START bit status by software method.

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To perform byte program/page erase ISP function, user need to specify flash address at first. When performing page erase function, SM59264 will erase entire page which flash address indicated by ISPFAH & ISPFAL registers located within the page.

e.g. flash address: $XYMN
    page erase function will erase from $XY00 to $X(Y+1)FF (Y : even number), or
    page erase function will erase from $X(Y-1)00 to $XYFF (Y : odd number)

To perform the chip erase ISP function, SM59264 will erase all the flash program memory and data flash memory except the ISP service program space if lock bit N been configured. Also, SM59264 will un-protect the flash memory automatically. To perform chip protect ISP function, all the flash memory will be read #00H.

e.g. ISP service program to do the byte program - to program #22H to the address $1005H

```
MOV ISPFD, #55H
MOV ISPFD, #AAH
MOV ISPFD, #55H
MOV $BF, #04H      ; enable SM59264 ISP function
MOV $F4, #10H      ; set flash address-high, 10H
MOV $F5, #05H      ; set flash address-low, 05H
MOV $F6, #22H      ; set flash data to be programmed, data = 22H
MOV $F7, #80H      ; start to program #22H to the flash address $1005H
                   ; after byte program finished, START bit of FCR will be reset to 0 automatically
                   ; program counter then point to the next instruction
```

4. Watch Dog Timer

The Watch Dog Timer (WDT) is a 16-bit free-running counter that generate reset signal if the counter overflows. The WDT is useful for systems which are susceptible to noise, power glitches, or electronics discharge which causing software dead loop or runaway. The WDT function can help user software recover from abnormal software condition. The WDT is different from Timer0, Timer1 and Timer2 of general 8052. To prevent a WDT reset can be done by software periodically clearing the WDT counter. User should check WDR bit of SCONF register whenever unpredicted reset happened

The purpose of the secure procedure is to prevent the WDTC value from being changed when system runaway.

There is a 250KHz RC oscillator embedded in chip. Set WDTE = "1" will enable the RC oscillator and the frequency is independent to the system frequency.

To enable the WDT is done by setting 1 to the bit 7 (WDTE) of WDTC. After WDTE set to 1, the 16-bit counter starts to count with the RC oscillator. It will generate a reset signal when overflows. The WDTE bit will be cleared to 0 automatically when SM59264 been reset, either hardware reset or WDT reset.

To reset the WDT is done by setting 1 to the CLEAR bit of WDTC before the counter overflow. This will clear the content of the 16-bit counter and let the counter re-start to count from the beginning.

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4.1 Watch Dog Timer Registers:

Watch Dog Timer Registers - WDT Control Register (WDTC, $9F)

	bit-7							bit-0
Read : Write :	WDTE	Unused	CLEAR	Unused	Unused	PS2	PS1	PS0
Reset value :	0	*	0	*	*	0	0	0

 WDTE : Watch Dog Timer enable bit
 CLEAR : Watch Dog Timer reset bit
 PS[2:0] : Overflow period select bits

PS [2:0]	Overflow Period (ms)
000	2.048
001	4.096
010	8.192
011	16.384
100	32.768
101	65.536
110	131.072
111	262.144

Watch Dog Key Register - (WDTKEY, $97H)

	bit-7							bit-0
Read : Write :	WDT KEY7	WDT KEY6	WDT KEY5	WDT KEY4	WDT KEY3	WDT KEY2	WDT KEY1	WDT KEY0
Reset value :	*	*	*	*	*	*	*	*

By default, the WDTC is read only. User need to write values 1EH, E1H sequentially to the WDTKEY($97H) register to enable the WDTC write attribute, That is

                MOV WDTKEY, # 1EH
                MOV WDTKEY, # E1H

When WDTC is set, user need to write another values E1H, 1EH sequentially to the WDTKEY($97H) register to disable the WDTC write attribute, That is

                MOV WDTKEY, # E1H
                MOV WDTKEY, # 1EH

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Watch Dog Timer Register - System Control Register (SCONF, $BF)

	bit-7							bit-0
Read : Write :	WDR	Unused	Unused	Unused	DFEN	ISPE	OME	ALEI
Reset value :	0	*	*	*	0	0	0	0

The bit 7 (WDR) of SCONF is Watch Dog TImer Reset bit. It will be set to 1 when reset signal generated by WDT overflow. User should check WDR bit whenever unpredicted reset happened

5. Reduce EMI Function

The SM59264 allows user to reduce the EMI emission by setting 1 to the bit 0 (ALEI) of SCONF register. This function will inhibit the clock signal in Fosc/6Hz output to the ALE pin.

6. Specific Pulse Width Modulation (SPWM)

The Specific Pulse Width Modulation (SPWM) module contains 1 kind of PWM submodule: SPWM (Specific PWM). SPWM has four 8-bit channels.

6.1 SPWM Function Description:

The 8-bit SPWM channel is composed of an 8-bit register which contains a 5-bit SPWM in MSB portion and a 3-bit binary rate multiplier (BRM) in LSB portion. The value programmed in the 5-bit SPWM portion will determine the pulse length of the output. The 3-bit BRM portion will generate and insert certain narrow pulses among an 8-SPWM-cycle frame. The number of pulses generated is equal to the number programmed in the 3-bit BRM portion. The usage of the BRM is to generate equivalent 8-bit resolution SPWM type DAC with reasonably high repetition rate through 5-bit SPWM clock speed. The SPFS[1:0] settings of SPWMC ($A3) register are divident of Fosc to be SPWM clock, $Fosc/2^{(SPFS[1:0]+1)}$. The SPWM output cycle frame repetition rate (frequency) equals (SPWM clock)/32 which is $[Fosc/2^{(SPFS[1:0]+1)}]/32$.

6.2 SPWM Registers - P1CON, SPWMC, SPWMD[3:0]

SPWM Registers - Port1 Configuration Register (P1CON, $9B)

	bit-7							bit-0
Read: Write:	Unused	Unused	SPWME3	SPWME2	SPWME1	SPWME0	Unused	Unused
Reset value:	*	*	0	0	0	0	*	*

SPWME[3:0] : When the bit set to one, the corresponding SPWM pin is active as SPWM function. When the bit reset to zero, the corresponding SPWM pin is active as I/O pin. Four bits are cleared upon reset.

SPWM Registers - SPWM Control Register (SPWMC, $A3)

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	bit-7							bit-0
Read: Write:	Unused	Unused	Unused	Unused	Unused	Unused	SPFS1	SPFS0
Reset value:	*	*	*	*	*	*	0	0

SPFS[1:0] : These two bits is 2's power parameter to form a frequency divider for input clock.

SPFS1	SPFS0	Divider	SPWM clock, Fosc=20MHz	SPWM clock, Fosc=24MHz
0	0	2	10MHz	12MHz
0	1	4	5MHz	6MHz
1	0	8	2.5MHz	3MHz
1	1	16	1.25MHz	1.5MHz

SPWM Registers - SPWM Data Register (SPWMD[3:0], $A7 ~$A4)

	bit-7							bit-0
Read: Write:	SPWMD [4:0]4	SPWMD [4:0]3	SPWMD [4:0]2	SPWMD [4:0]1	SPWMD [4:0]0	BRM [2:0]2	BRM [2:0]1	BRM [2:0]0
Reset value:	0	0	0	0	0	0	0	0

SPWMD[4:0] : content of SPWM Data Register. It determines duty cycle of SPWM output waveform.

BRM[2:0] : will insert certain narrow pulses among an 8-SPWM-cycle frame

N = BRM[2:0]	Number of SPWM cycles inserted in an 8-cycle frame
000	0
001	1
010	2
011	3
100	4
101	5
110	6
111	7

Example of SPWM timing diagram :

```
MOV  SPWMD0 , #83H      ; SPWMD0[4:0]=10h (=16T high, 16T low), BRM[2:0] = 3
MOV  P1CON , #08H       ; Enable P1.3 as SPWM output pin
```

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1st cycle frame	2nd cycle frame	3rd cycle frame	4th cycle frame	5th cycle frame	6th cycle frame	7th cycle frame	8th cycle frame

(narrow pulse inserted by BRM0[2:0] setting, here BRM0[2:0]=3)
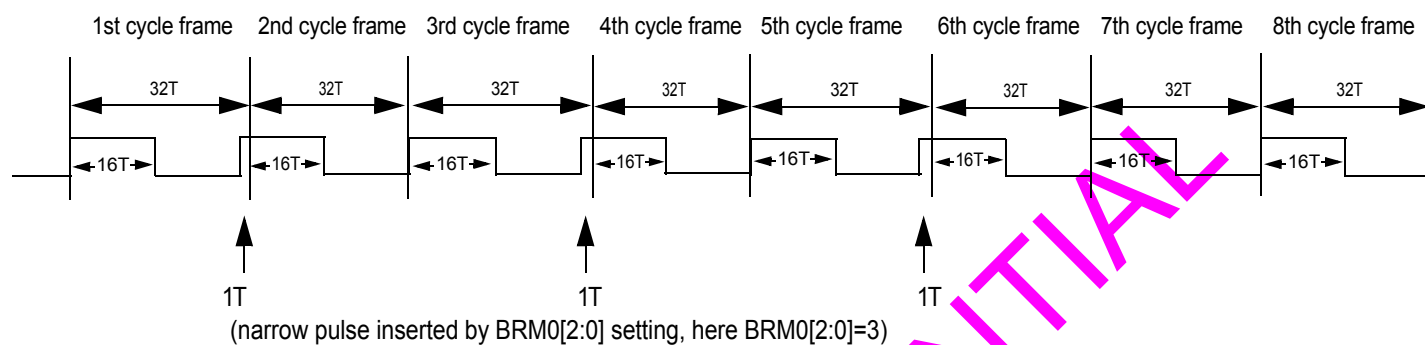
SPWM clock = 1 / T = Fosc / $2^{(SPFS[1:0]+1)}$
The SPWM output cycle frame frequency = SPWM clock / 32 = [Fosc/$2^{(SPFS[1:0]+1)}$]/32

If user use Fosc=20MHz, SPFS[1:0] of SPWMC=#03H, then
SPWM clock = 20MHz/2^4 = 20MHz/16 = 1.25MHz
SPWM output cycle frame frequency = (20MHz/2^4)/32=39.1KHz

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Operating Conditions

Symbol	Description	Min.	Typ.	Max.	Unit.	Remarks
TA	Operating temperature	0	25	70	°C	Ambient temperature under bias
TS	Storage temperature	-55	25	155	°C	
VCC5	Supply voltage	4.5	5.0	5.5	V	
Fosc 16	Oscillator Frequency	3.0	16	16	MHz	For 5V application
Fosc 25	Oscillator Frequency	3.0	25	25	MHz	For 5V application
Fosc 40	Oscillator Frequency	3.0	40	40	MHz	For 5V application

DC Characteristics

(16/25/40 MHZ, typical operating conditions, valid for SM59264 series)

Symbol	Parameter	Valid	Min.	Max.	Unit	Test Conditions
VIL1	Input Low Voltage	port 0,1,2,3,4,#EA	-0.5	0.8	V	Vcc=5V
VIL2	Input Low Voltage	RES, XTAL1	0	0.8	V	"
VIH1	Input High Voltage	port 0,1,2,3,4,#EA	2.0	Vcc+0.5	V	"
VIH2	Input High Voltage	RES, XTAL1	70%Vcc	Vcc+0.5	V	"
VOL1	Output Low Voltage	port 0, ALE, #PSEN		0.45	V	IOL=3.2mA
VOL2	Output Low Voltage	port 1,2,3,4		0.45	V	IOL=1.6mA
VOH1	Output High Voltage	port 0	2.4		V	IOH=-800uA
			90%Vcc		V	IOH=-80uA
VOH2	Output High Voltage	port 1,2,3,4,ALE,#PSEN	2.4		V	IOH=-60uA
			90%Vcc		V	IOH=-10uA
IIL	Logical 0 Input Current	port 1,2,3,4		-75	uA	Vin=0.45V
ITL	Logical Transition Current	port 1,2,3,4		-650	uA	Vin=2.0V
ILI	Input Leakage Current	port 0, #EA		± 10	uA	0.45V<Vin<Vcc
R RES	Reset Pulldown Resistance	RES	50	300	Kohm	
C IO	Pin Capacitance			10	pF	Freq=1MHz, Ta=25°C
I CC	Power Supply Current	Vdd		20	mA	Active mode, 40MHz
				15	mA	Active mode, 25MHz
				10	mA	Active mode, 16MHz
				10	mA	Idle mode, 40MHz
				7.5	mA	Idle mode, 25MHz
				6	mA	Idle mode, 16MHz
				150	uA	Power down mode

ICC Active mode test circuit
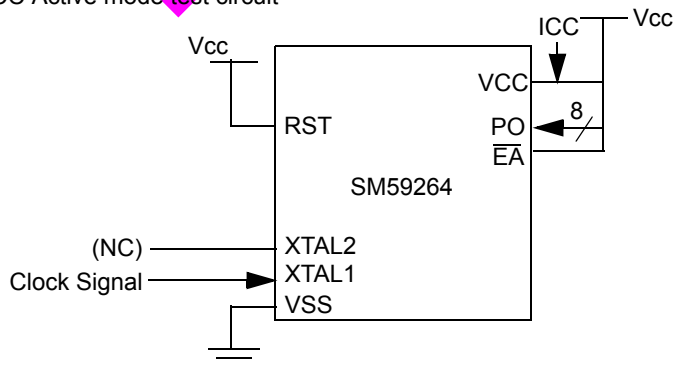
ICC Idle mode test circuit
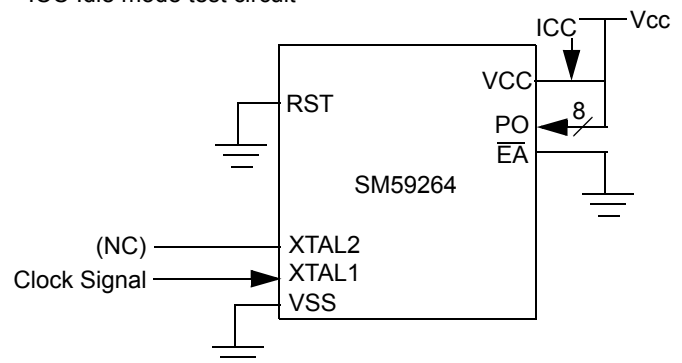
AC Characteristics

(16/25/40 MHZ, operating conditions; CL for Port 0, ALE and PSEN Outputs=150PF; CL for all Other Output=80pF)

Symbol	Parameter	Valid Cycle	f osc 16 Min.	f osc 16 Typ.	f osc 16 Max	Variable f osc Min.	Variable f osc Typ.	Variable f osc Max	Unit	Remarks
T LHLL	ALE pulse width	RD/WRT	115			2xT - 10			nS	
T AVLL	Address Valid to ALE low	RD/WRT	43			T - 20			nS	
T LLAX	Address Hold after ALE low	RD/WRT	53			T - 10			nS	
T LLIV	ALE low to Valid Instruction In	RD			240			4xT - 10	nS	
T LLPL	ALE low to #PSEN low	RD	53			T - 10			nS	
T PLPH	#PSEN pulse width	RD	173			3xT - 15			nS	
T PLIV	#PSEN low to Valid Instruction In	RD			177			3xT - 10	nS	
T PXIX	Instruction Hold after #PSEN	RD	0			0			nS	
T PXIZ	Instruction Float after #PSEN	RD			87			T + 25	nS	
T AVIV	Address to Valid Instruction In	RD			292			5xT - 20	nS	
T PLAZ	#PSEN low to Address Float	RD			10			10	nS	
T RLRH	#RD pulse width	RD	365			6xT - 10			nS	
T WLWH	#WR pulse width	WRT	365			6xT - 10			nS	
T RLDV	#RD low to Valid Data In	RD			302			5xT - 10	nS	
T RHDX	Data Hold after #RD	RD	0			0			nS	
T RHDZ	Data Float after #RD	RD			145			2xT + 20	nS	
T LLDV	ALE low to Valid Data In	RD			590			8xT - 10	nS	
T AVDV	Address to Valid Data In	RD			542			9xT - 20	nS	
T LLYL	ALE low to #WR High or #RD low	RD/WRT	178		197	3xT - 10		3xT + 10	nS	
T AVYL	Address Valid to #WR or #RD low	RD/WRT	230			4xT - 20			nS	
T QVWH	Data Valid to #WR High	WRT	403			7xT - 35			nS	
T QVWX	Data Valid to #WR transition	WRT	38			T - 25			nS	
T WHQX	Data hold after #WR	WRT	73			T + 10			nS	
T RLAZ	#RD low to Address Float	RD						5	nS	
T YALH	#WR or #RD high to ALE high	RD/WRT	53		72	T -10		T + 10	nS	
T CHCL	clock fall time								nS	
T CLCX	clock low time								nS	
T CLCH	clock rise time								nS	
T CHCX	clock high time								nS	
T, TCLCL	clock period			63			1/fosc		nS	

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ISP Test Conditions

(40 MHZ, typical operating conditions, valid for SM59264 serires)

Symbol	MAX	Remark
Chip erase	3000ms	Vcc = 5V
Page erase	10ms	"
Program	400us	"
Protect	30us	"

Application Reference

Valid for SM59264			
X'tal	3MHz	6MHz	9MHz	12MHz
C1	30 pF	30 pF	30 pF	30 pF
C2	30 pF	30 pF	30 pF	30 pF
R	open	open	open	open

X'tal	16MHz	25MHz	40MHz
C1	30 pF	15 pF	2 pF
C2	30 pF	15 pF	2 pF
R	open	62KΩ	4.7KΩ
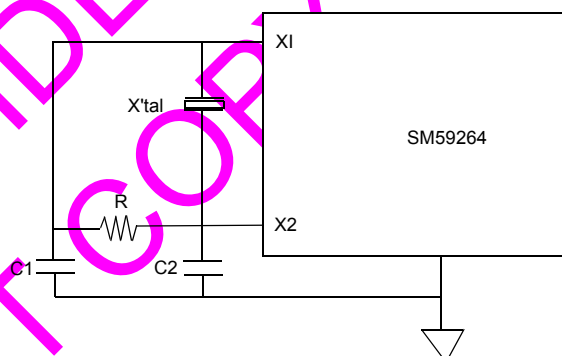
Note : Oscillation circuit may differs with different crystal or ceramic
resonator in higher oscillation frequency which was due to
each crystal or ceramic resonator has its own characteristics.
User should check with the crystal or ceramic resonator
manufacture for appropriate value of external components.
Please see SM59264 application note for details.

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Data Memory Read Cycle Timing

Program Memory Read Cycle Timing

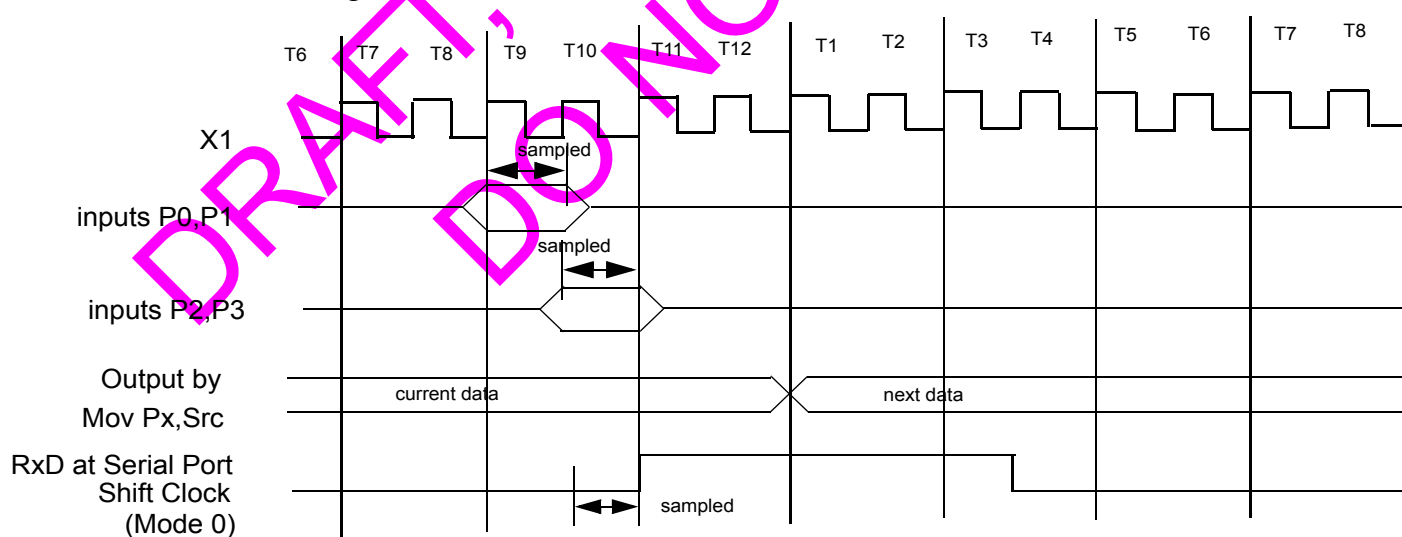Specifications subject to change without notice,contact your sales representatives for the most recent information.
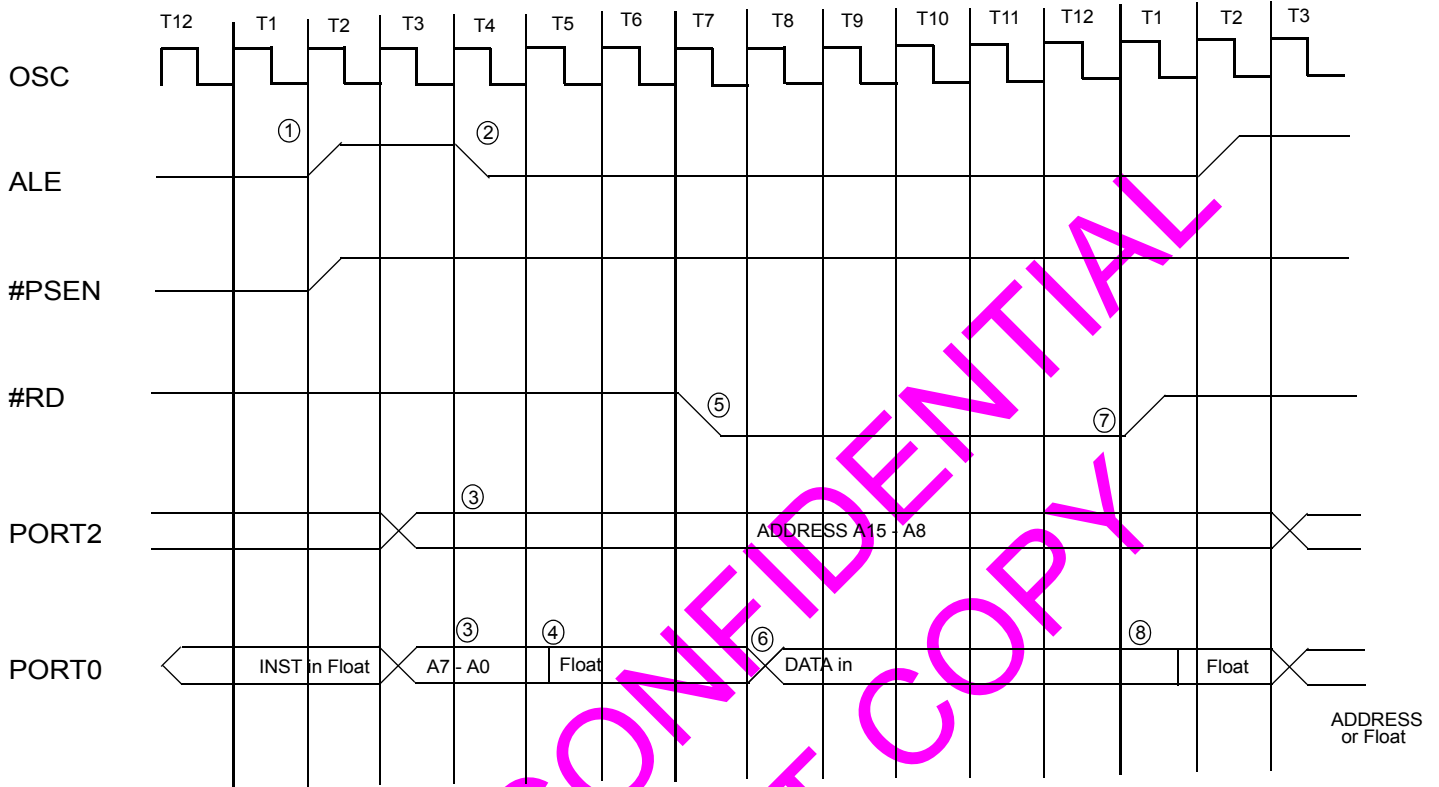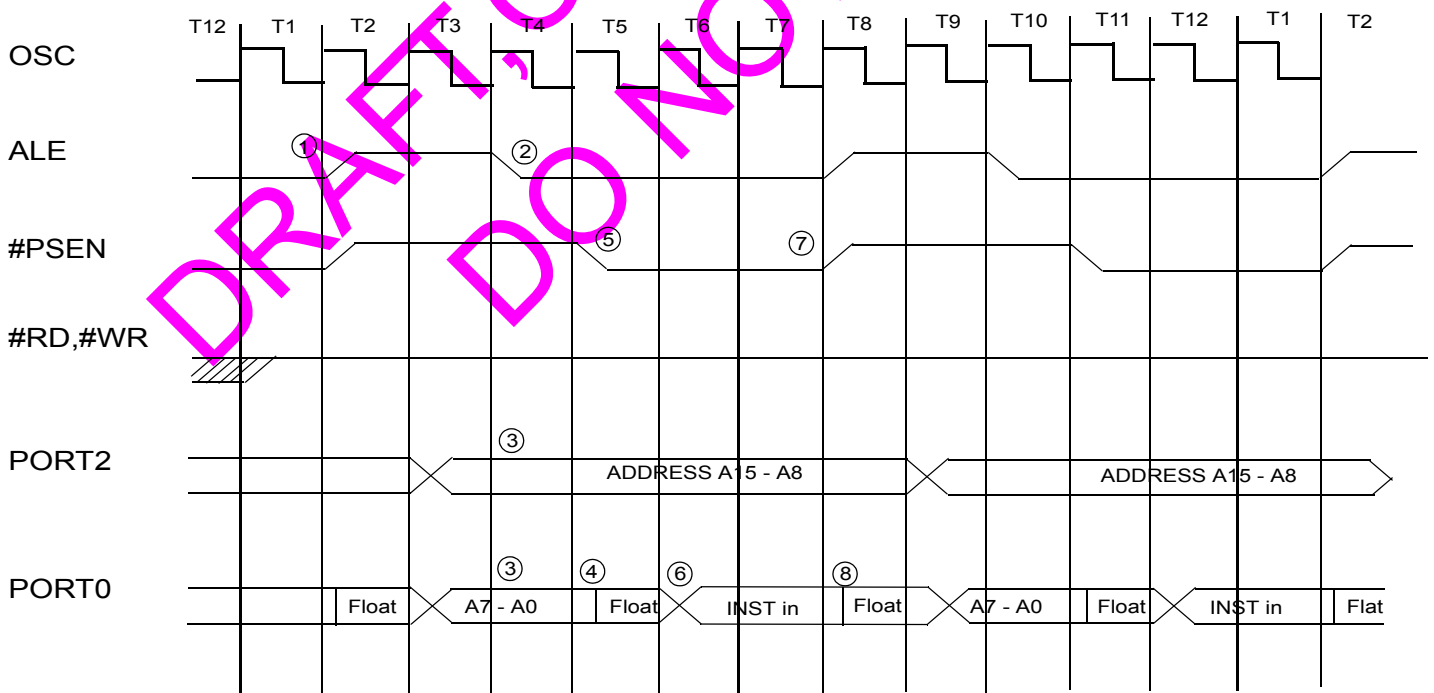
Data Memory Write Cycle Timing

I/O Ports Timing

Specifications subject to change without notice,contact your sales representatives for the most recent information.
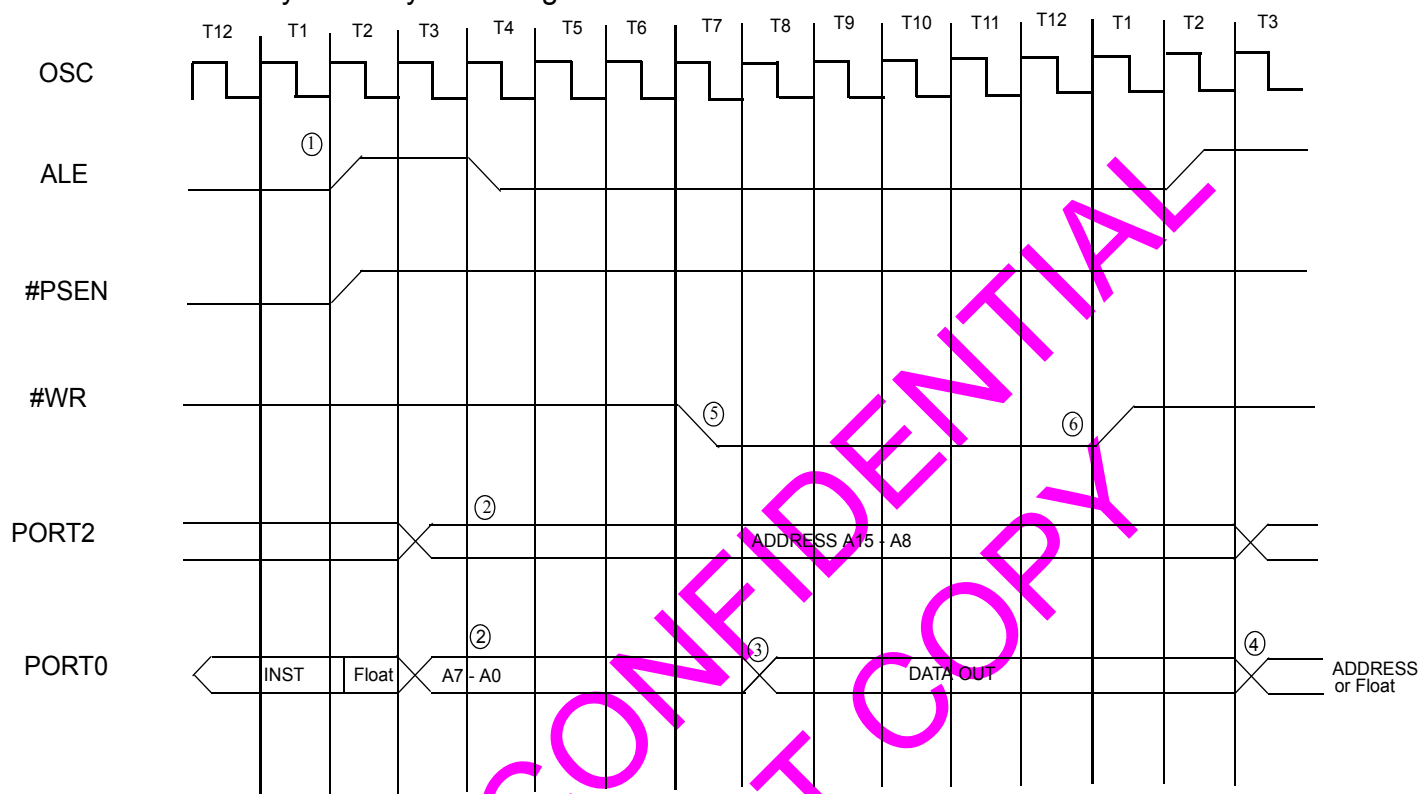
Timing Critical, Requirement of External Clock   (Vss=0.0V is assumed)
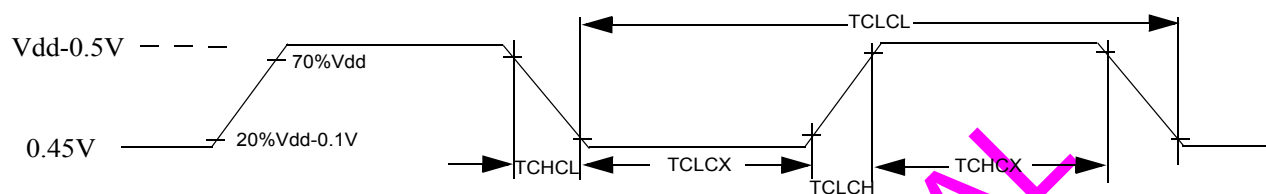
Tm.I   External Program Memory Read Cycle
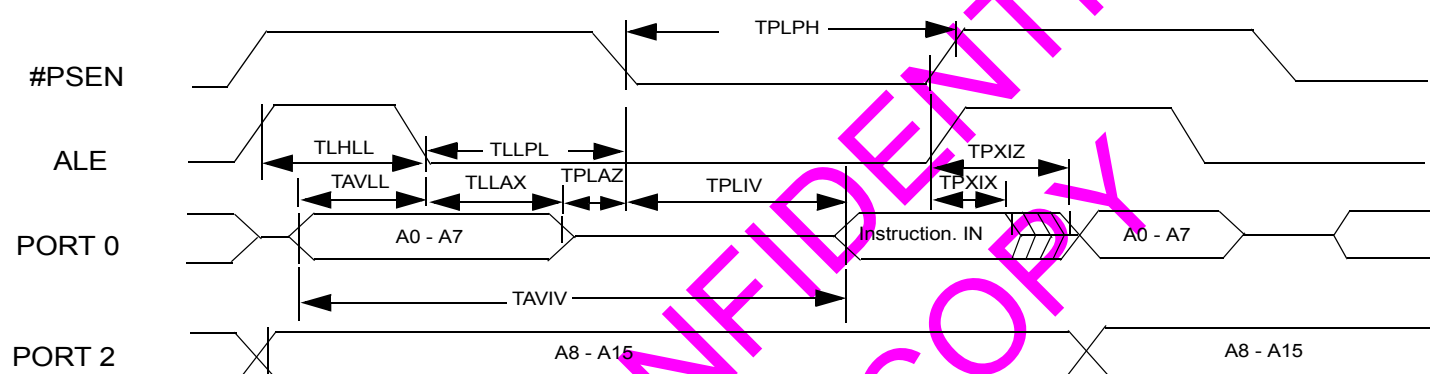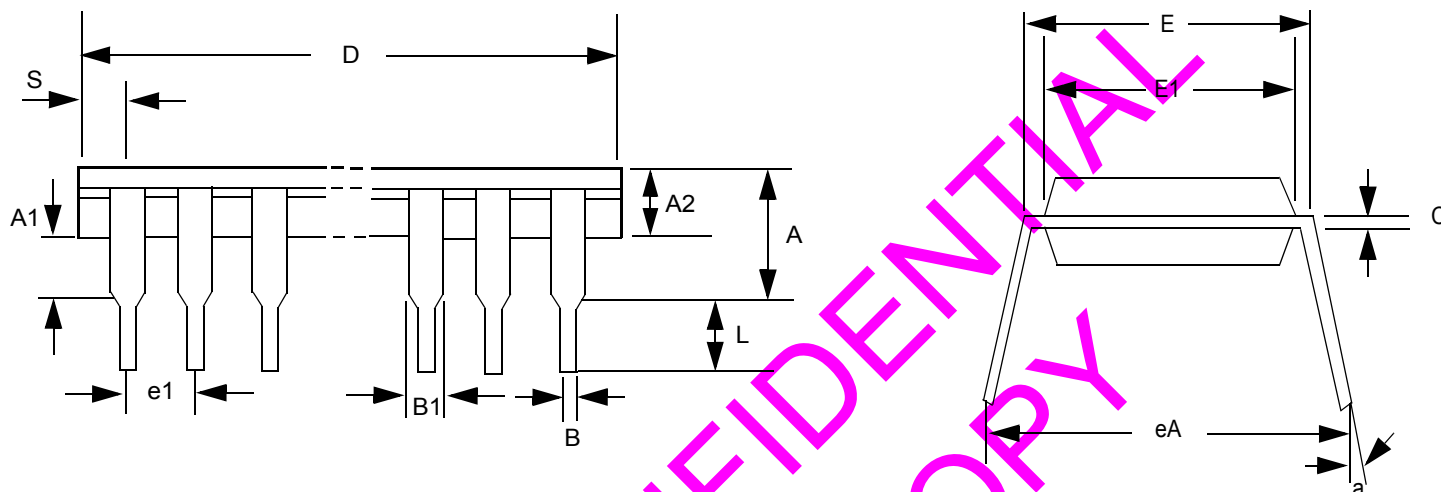

Tm.II   External Data Memory Read Cycle

Specifications subject to change without notice,contact your sales representatives for the most recent information.
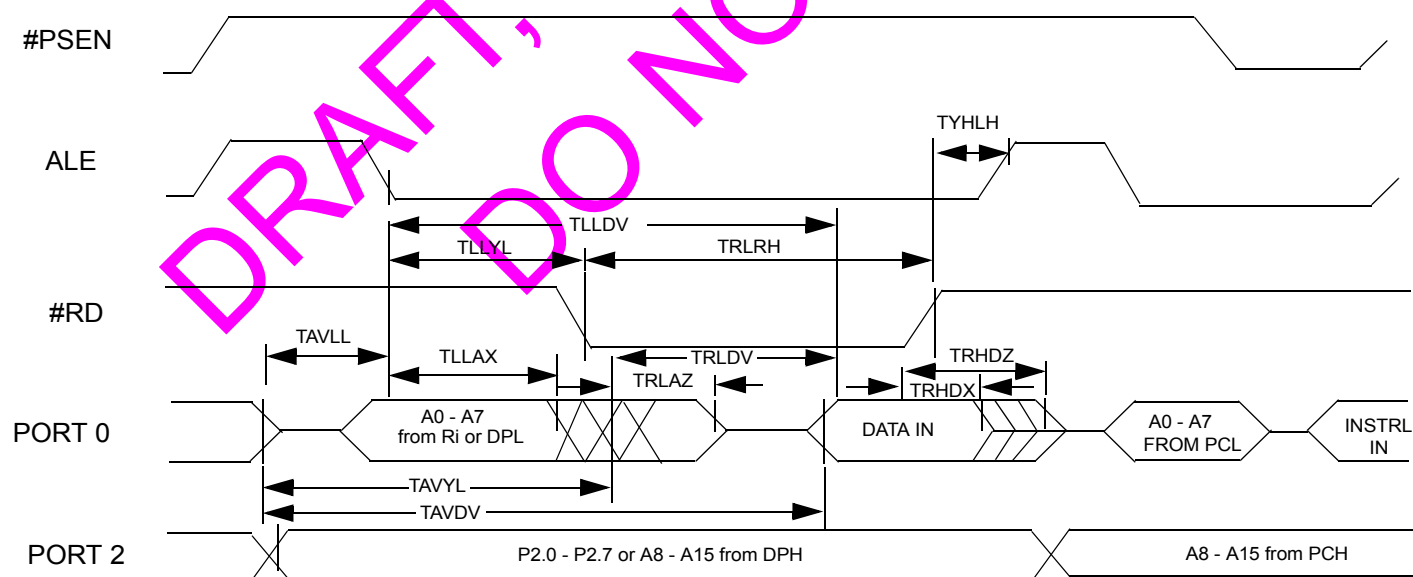
Tm.III External Data Memory Write Cycle

Specifications subject to change without notice,contact your sales representatives for the most recent information.
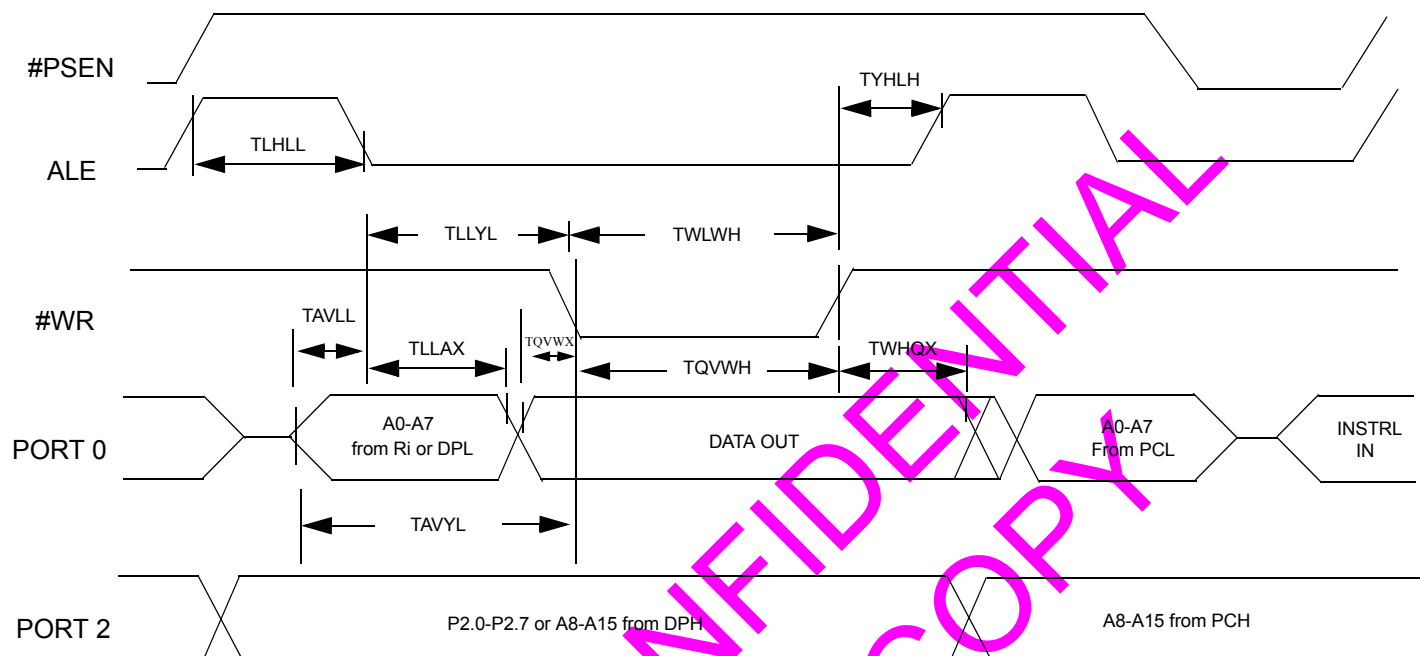
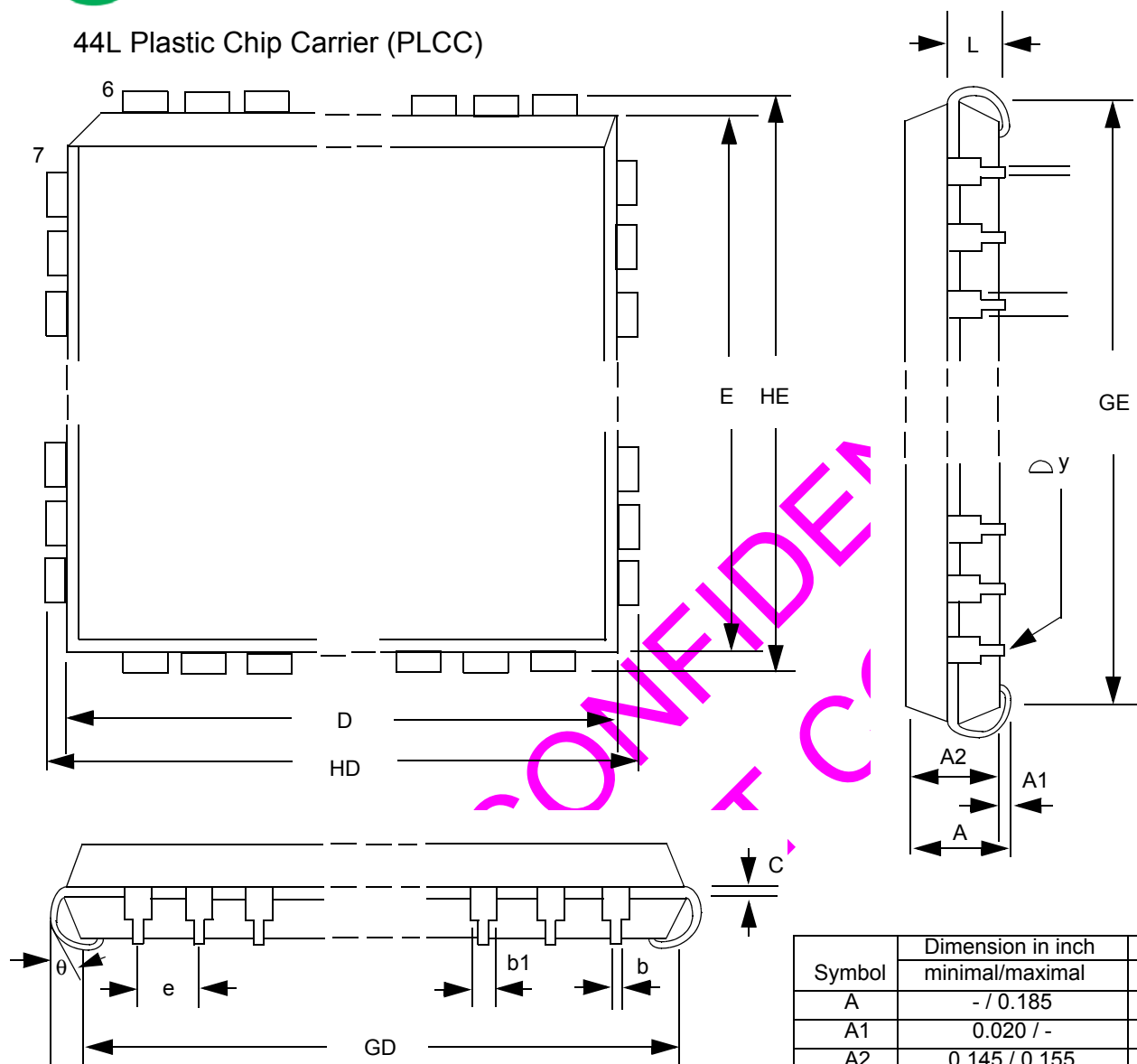27/32 Preliminary Ver 0.1 PID 59264 05/02

40L 600mil PDIP Information

Note:
1. Dimension D Max & include mold flash or tie bar burrs.
2. Dimension E1 does not include interlead flash.
3. Dimension D & E1 include mold mismatch and are determined at the mold parting line.
4. Dimension B1 does not include dambar protrusion/infrusion.
5. Controlling dimension is inch.
6. General appearance spec. should base on final visual inspection spec.

Symbol	Dimension in inch minimal/maximal	Dimension in mm minimal/maximal
A	- / 0.210	- / 5.33
A1	0.010 / -	0.25 / -
A2	0.150 / 0.160	3.81 / 4.06
B	0.016 / 0.022	0.41 / 0.56
B1	0.048 / 0.054	1.22 / 1.37
C	0.008 / 0.014	0.20 / 0.36
D	- / 2.070	- / 52.58
E	0.590 / 0.610	14.99 / 15.49
E1	0.540 / 0.552	13.72 / 14.02
e1	0.090 / 0.110	2.29 / 2.79
L	0.120 / 0.140	3.05 / 3.56
a	0˚ / 15˚	0˚ / 15˚
eA	0.630 / 0.670	16.00 / 17.02
S	- / 0.090	- / 2.29

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44L Plastic Chip Carrier (PLCC)

Note:

1. Dimension D & E does not include interlead flash.
2. Dimension b1 does not include dambar protrusion/
   intrusion.
3. Controlling dimension:Inch
4. General appearance spec. should base on final visual
   inspection spec.

Symbol	Dimension in inch minimal/maximal	Dimension in mm minimal/maximal
A	- / 0.185	- / 4.70
A1	0.020 / -	0.51 / -
A2	0.145 / 0.155	3.68 / 3.94
b1	0.026 / 0.032	0.66 / 0.81
b	0.016 / 0.022	0.41 / 0.56
C	0.008 / 0.014	0.20 / 0.36
D	0.648 / 0.658	16.46 / 16.71
E	0.648 / 0.658	16.46 / 16.71
e	0.050 BSC	1.27 BSC
GD	0.590 / 0.630	14.99 / 16.00
GE	0.590 / 0.630	14.99 / 16.00
HD	0.680 / 0.700	17.27 / 17.78
HE	0.680 / 0.700	17.27 / 17.78
L	0.090 / 0.110	2.29 / 2.79
θ	- / 0.004	- / 0.10
◠y	/	/

44L Plastic Quad Flat Package
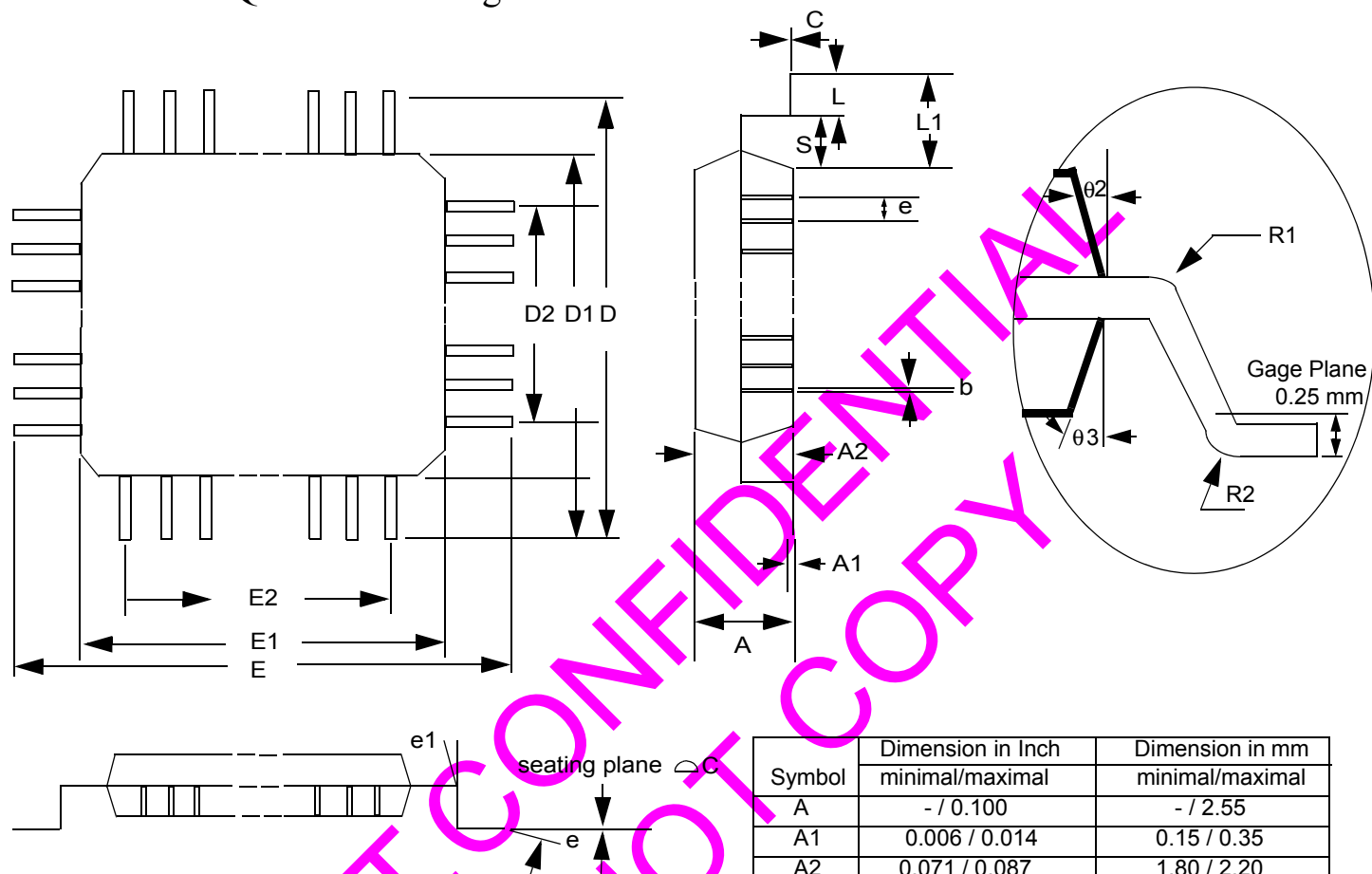
Note:

Dimension D1 and E1 do not include mold protrusion.

Allowance protrusion is 0.25mm per side.

Dimension D1 and E1 do include mold mismatch

and are determined datum plane.

Dimension b does not include dambar protrusion.

Allowance dambar protrusion shall be 0.08 mm total

in excess of the b dimension at maximum material

condition. Dambar cannot be located on the lower

radius or the lead foot.

Symbol	Dimension in Inch minimal/maximal	Dimension in mm minimal/maximal
A	- / 0.100	- / 2.55
A1	0.006 / 0.014	0.15 / 0.35
A2	0.071 / 0.087	1.80 / 2.20
b	0.012 / 0.018	0.30 / 0.45
c	0.004 / 0.009	0.09 / 0.20
D	0.520 BSC	13.20 BSC
D1	0.394 BSC	10.00 BSC
D2	0.315	8.00
E	0.520 BSC	13.20 BSC
E1	0.394 BSC	10.00 BSC
E2	0.315	8.00
e	0.031 BSC	0.80 BSC
L	0.029 / 0.041	0.73 / 1.03
L1	0.063	1.60
R1	0.005 / -	0.13 / -
R2	0.005 / 0.012	0.13 / 0.30
S	0.008 / -	0.20 / -
θ	0° / 7°	as left
θ1	0° / -	as left
θ2	10° REF	as left
θ3	7° REF	as left
⌒C	0.004	0.10

eMCU writer list		
Company	Contact info	Programmer Model Number
Advantech 7F, No.98, Ming-Chung Rd., Shin-Tien City, Taipei, Taiwan, ROC Website: http://www.aec.com.tw	Tel:02-22182325 Fax:02-22182435 E-mail: aecwebmaster@advantech.com.tw	LabTool - 48 (1 * 1) LabTool - 848 (1*8)
Caprilion P.O. Box 461 KaoHsiung, Taiwan, ROC Website: http://www.market.net.tw/ ~ cap/	Tel:07-3865061 Fax:07-3865421 E-mail: cap@market.net.tw	UNiV2000
_Hi-Lo_ 4F, No. 20, 22, LN, 76, Rui Guang Rd., Nei Hu, Taipei, Taiwan, ROC. Website: http://www.hilosystems.com.tw	Tel:02-87923301 Fax:02-87923285 E-mai: support@hilosystems.com.tw	All - 11 (1*1) Gang - 08 (1*8)
Leap 6th F1-4, Lane 609, Chunghsin Rd., Sec. 5, Sanchung, Taipei Hsien, Taiwan, ROC Website: http://www.leap.com.tw	Tel:02-29991860 Fax:02-29990015 E-mail: service@leap.com.tw	ChipStation (1*1) SU - 2000 (1*8)
Xeltek Electronic Co., Ltd 338 Hongwu Road, Nanjing, China 210002 Website: http://www.xeltek-cn.com	Tel:+86-25-4408399, 4543153-206 E-mail: xelclw@jlonline.com, xelgbw@jlonline.com	Superpro/2000 (1*1) Superpro/680 (1*1) Superpro/280 (1*1) Superpro/L+(1*1)

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Feedback / Inquiry

To : SyncMOS Technologies, Inc.	From : _____
Attn : MKT / Customer Service Dept.	Company : _____
Fax : 886-3-5792960	Dept, Section : _____
: 886-3-5780493	Position Title : _____
Tel : 886-3-5792988	Inquiry Date : _____
: 886-3-5792926	Ref No : _____

☐ Request customer logo as below :

Description :

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