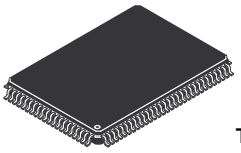
MCM69P536C

32K x 36 Bit Pipelined BurstRAM Synchronous Fast Static RAM



TQ PACKAGE
TQFP
CASE 983A–01

The MCM69P536C is a 1M–bit synchronous fast static RAM designed to provide a burstable, high performance, secondary cache for the 68K Family, PowerPC™, 486, i960™, and Pentium™ microprocessors. It is organized as 32K words of 36 bits each. This device integrates input registers, an output register, a 2–bit address counter, and high speed SRAM onto a single monolithic circuit for reduced parts count in cache data RAM applications. Synchronous design allows precise cycle control with the use of an external clock (K). BiCMOS circuitry reduces the overall power consumption of the integrated functions for greater reliability.

Addresses (SA), data inputs (DQx), and all control signals except output enable (G) and Linear Burst Order (LBO) are clock (K) controlled through positive–edge–triggered noninverting registers.

Bursts can be initiated with either ADSP or ADSC input pins. Subsequent burst addresses can be generated internally by the MCM69P536C (burst sequence operates in linear or interleaved mode dependent upon the state of LBO) and controlled by the burst address advance (ADV) input pin.

Write cycles are internally self–timed and are initiated by the rising edge of the clock (K) input. This feature eliminates complex off–chip write pulse generation and provides increased timing flexibility for incoming signals.

Synchronous byte write (SBx), synchronous global write (SGW), and synchronous write enable SW are provided to allow writes to either individual bytes or to all bytes. The four bytes are designated as “a”, “b”, “c”, and “d”. SBa controls DQa, SBb controls DQb, etc. Individual bytes are written if the selected byte writes SBx are asserted with SW. All bytes are written if either SGW is asserted or if all SBx and SW are asserted.

For read cycles, pipelined SRAMs output data is temporarily stored by an edge–triggered output register and then released to the output buffers at the next rising edge of clock (K).

The MCM69P536C operates from a 3.3 V power supply and all inputs and outputs are LVTTL compatible.

- MCM69P536C–4 = 4 ns Access / 7.5 ns Cycle
  MCM69P536C–4.5 = 4.5 ns Access / 8 ns Cycle
  MCM69P536C–5 = 5 ns Access / 10 ns Cycle
  MCM69P536C–6 = 6 ns Access / 12 ns Cycle
  MCM69P536C–7 = 7 ns Access / 13.3 ns Cycle
- Single 3.3 V + 10%, – 5% Power Supply
- ADSP, ADSC, and ADV Burst Control Pins
- Selectable Burst Sequencing Order (Linear/Interleaved)
- Internally Self–Timed Write Cycle
- Byte Write and Global Write Control
- 5 V Tolerant on all Pins (Inputs and I/Os)
- 100–Pin TQFP Package

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i960 and Pentium are trademarks of Intel Corp.

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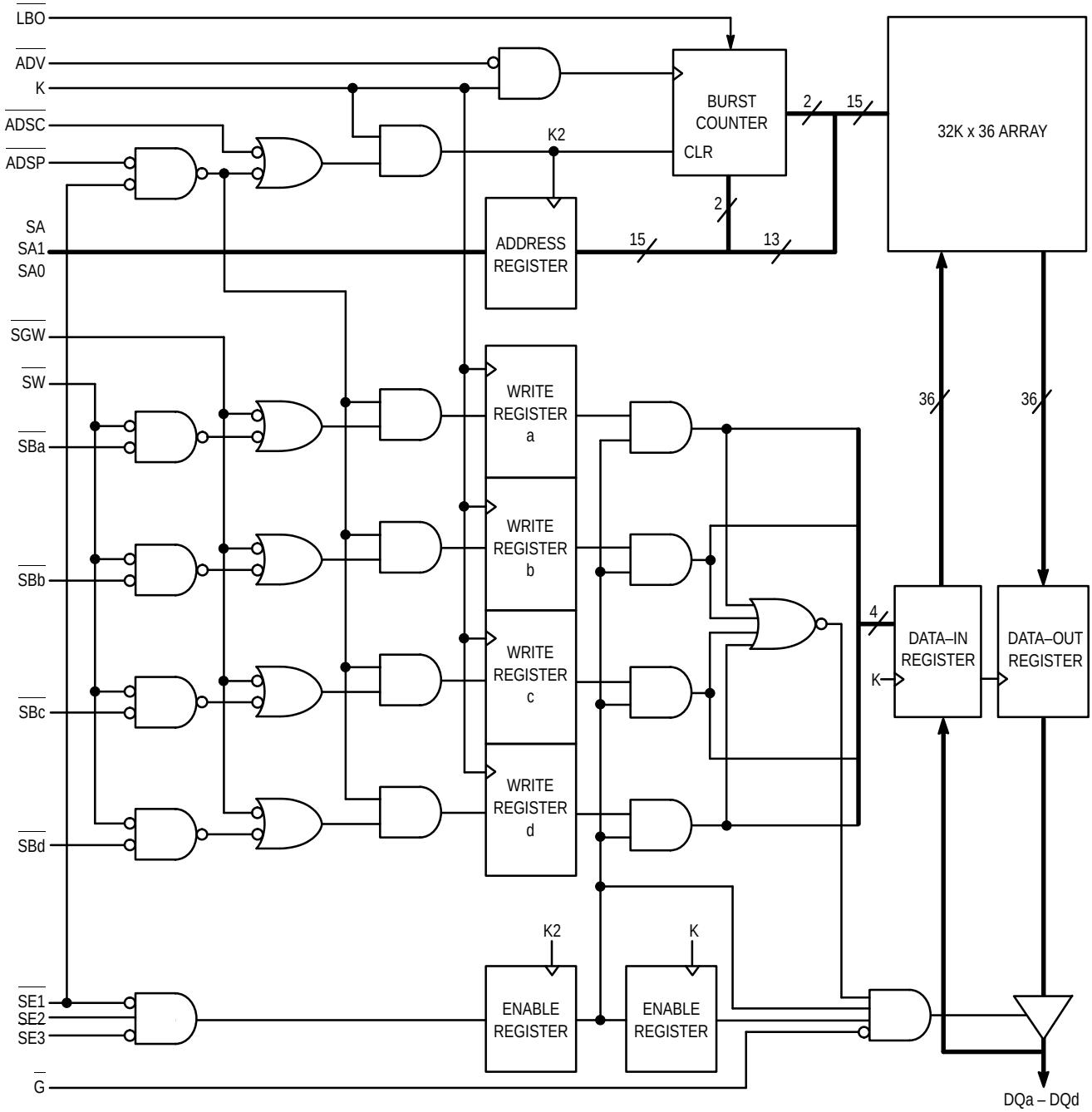
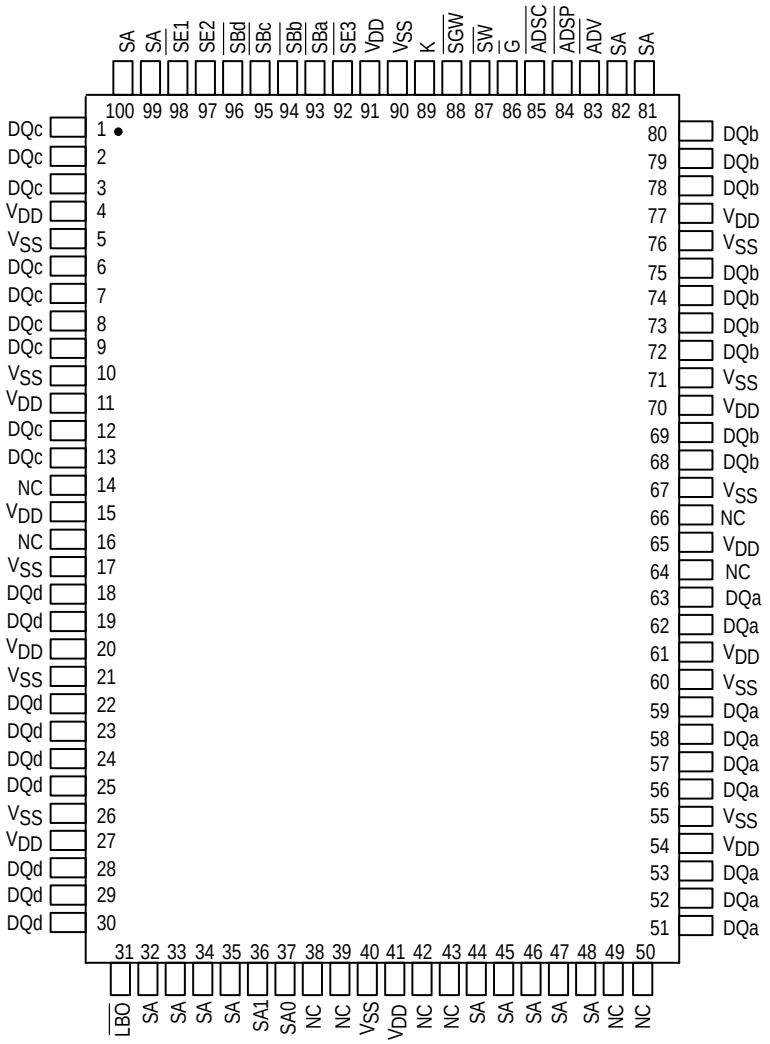
FUNCTIONAL BLOCK DIAGRAM



PIN ASSIGNMENT



PIN DESCRIPTIONS

Pin Locations	Symbol	Type	Description
85	$\overline{\text{ADSC}}$	Input	Synchronous Address Status Controller: Initiates READ, WRITE, or chip deselect cycle.
84	$\overline{\text{ADSP}}$	Input	Synchronous Address Status Processor: Initiates READ, WRITE, or chip deselect cycle (exception — chip deselect does not occur when ADSP is asserted and SE1 is high).
83	$\overline{\text{ADV}}$	Input	Synchronous Address Advance: Increments address count in accordance with counter type selected (linear/interleaved).
(a) 51, 52, 53, 56, 57, 58, 59, 62, 63 (b) 68, 69, 72, 73, 74, 75, 78, 79, 80 (c) 1, 2, 3, 6, 7, 8, 9, 12, 13 (d) 18, 19, 22, 23, 24, 25, 28, 29, 30	DQx	I/O	Synchronous Data I/O: “x” refers to the byte being read or written (byte a, b, c, d).
86	$\overline{\text{G}}$	Input	Asynchronous Output Enable Input: Low — enables output buffers (DQx pins). High — DQx pins are high impedance.
89	K	Input	Clock: This signal registers the address, data in, and all control signals except G and LBO.
31	$\overline{\text{LBO}}$	Input	Linear Burst Order Input: This pin must remain in steady state (this signal not registered or latched). It must be tied high or low. Low — linear burst counter (68K/PowerPC). High — interleaved burst counter (486/i960/Pentium).
32, 33, 34, 35, 44, 45, 46, 47, 48, 81, 82, 99, 100	SA	Input	Synchronous Address Inputs: These inputs are registered and must meet setup and hold times.
36, 37	SA1,SA0	Input	Synchronous Address Inputs: These pins must be wired to the two LSBs of the address bus for proper burst operation. These inputs are registered and must meet setup and hold times.
93, 94, 95, 96 (a) (b) (c) (d)	$\overline{\text{SBx}}$	Input	Synchronous Byte Write Inputs: “x” refers to the byte being written (byte a, b, c, d). SGW overrides SBx.
98	SE1	Input	Synchronous Chip Enable: Active low to enable chip. Negated high–blocks ADSP or deselects chip when ADSC is asserted.
97	SE2	Input	Synchronous Chip Enable: Active high for depth expansion.
92	$\overline{\text{SE3}}$	Input	Synchronous Chip Enable: Active low for depth expansion.
88	$\overline{\text{SGW}}$	Input	Synchronous Global Write: This signal writes all bytes regardless of the status of the SBx and SW signals. If only byte write signals SBx are being used, tie this pin high.
87	$\overline{\text{SW}}$	Input	Synchronous Write: This signal writes only those bytes that have been selected using the byte write SBx pins. If only byte write signals SBx are being used, tie this pin low.
4, 11, 15, 20, 27, 41, 54, 61, 65, 70, 77, 91	V_{DD}	Supply	Power Supply: 3.3 V + 10%, – 5%.
5, 10, 17, 21, 26, 40, 55, 60, 67, 71, 76, 90	V_{SS}	Supply	Ground.
64	NC	Input	No Connection: There is no connection to the chip. For compatibility reasons, it is recommended that this pin be tied low for system designs that do not have a sleep mode associated with the cache/memory controller. Other vendors’ RAMs may have implemented the Sleep Mode (ZZ) feature.
14, 16, 38, 39, 42, 43, 49, 50, 66	NC	—	No Connection: There is no connection to the chip.

TRUTH TABLE (See Notes 1 through 4)

Next Cycle	Address Used	$\overline{SE1}$	SE2	$\overline{SE3}$	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{G}$ [3]	DQx	Write [2, 4]
Deselect	None	1	X	X	X	0	X	X	High–Z	X
Deselect	None	0	X	1	0	X	X	X	High–Z	X
Deselect	None	0	0	X	0	X	X	X	High–Z	X
Deselect	None	X	X	1	1	0	X	X	High–Z	X
Deselect	None	X	0	X	1	0	X	X	High–Z	X
Begin Read	External	0	1	0	0	X	X	X	High–Z	READ
Begin Read	External	0	1	0	1	0	X	X	High–Z	READ
Continue Read	Next	X	X	X	1	1	0	1	High–Z	READ
Continue Read	Next	X	X	X	1	1	0	0	DQ	READ
Continue Read	Next	1	X	X	X	1	0	1	High–Z	READ
Continue Read	Next	1	X	X	X	1	0	0	DQ	READ
Suspend Read	Current	X	X	X	1	1	1	1	High–Z	READ
Suspend Read	Current	X	X	X	1	1	1	0	DQ	READ
Suspend Read	Current	1	X	X	X	1	1	1	High–Z	READ
Suspend Read	Current	1	X	X	X	1	1	0	DQ	READ
Begin Write	Current	X	X	X	1	1	1	X	High–Z	WRITE
Begin Write	Current	1	X	X	X	1	1	X	High–Z	WRITE
Begin Write	External	0	1	0	1	0	X	X	High–Z	WRITE
Continue Write	Next	X	X	X	1	1	0	X	High–Z	WRITE
Continue Write	Next	1	X	X	X	1	0	X	High–Z	WRITE
Suspend Write	Current	X	X	X	1	1	1	X	High–Z	WRITE
Suspend Write	Current	1	X	X	X	1	1	X	High–Z	WRITE

NOTES: 1. X = Don't Care. 1 = logic high. 0 = logic low.
2. Write is defined as either 1) any SBx and SW low or 2) $\overline{SGW}$ is low.
3. G is an asynchronous signal and is not sampled by the clock K. G drives the bus immediately (t_{GLQX}) following $\overline{G}$ going low.
4. On write cycles that follow read cycles, G must be negated prior to the start of the write cycle to ensure proper write data setup times. G must also remain negated at the completion of the write cycle to ensure proper write data hold times.

LINEAR BURST ADDRESS TABLE ($\overline{LBO} = V_{SS}$)

1st Address (External)	2nd Address (Internal)	3rd Address (Internal)	4th Address (Internal)
X . . . X00	X . . . X01	X . . . X10	X . . . X11
X . . . X01	X . . . X10	X . . . X11	X . . . X00
X . . . X10	X . . . X11	X . . . X00	X . . . X01
X . . . X11	X . . . X00	X . . . X01	X . . . X10

INTERLEAVED BURST ADDRESS TABLE ($\overline{LBO} = V_{DD}$)

1st Address (External)	2nd Address (Internal)	3rd Address (Internal)	4th Address (Internal)
X . . . X00	X . . . X01	X . . . X10	X . . . X11
X . . . X01	X . . . X00	X . . . X11	X . . . X10
X . . . X10	X . . . X11	X . . . X00	X . . . X01
X . . . X11	X . . . X10	X . . . X01	X . . . X00

WRITE TRUTH TABLE

Cycle Type	SGW	SW	SBa	SBb	SBc	SBd
Read	H	H	X	X	X	X
Read	H	L	H	H	H	H
Write Byte a	H	L	L	H	H	H
Write Byte b	H	L	H	L	H	H
Write Byte c	H	L	H	H	L	H
Write Byte d	H	L	H	H	H	L
Write All Bytes	H	L	L	L	L	L
Write All Bytes	L	X	X	X	X	X

ABSOLUTE MAXIMUM RATINGS (See Note 1)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{DD}	– 0.5 to + 4.6	V
Voltage Relative to V_{SS} for Any Pin Except V_{DD}	V_{in}, V_{out}	– 0.5 to 6.0	V
Output Current (per I/O)	I_{out}	± 20	mA
Package Power Dissipation (See Note 2)	P_D	1.6	W
Temperature Under Bias	T_{bias}	– 10 to 85	°C
Storage Temperature	T_{stg}	– 55 to 125	°C

NOTES:
1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.
2. Power dissipation capability is dependent upon package characteristics and use environment. See Package Thermal Characteristics.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high–impedance circuit.

PACKAGE THERMAL CHARACTERISTICS

Rating		Symbol	Max	Unit	Notes
Thermal Resistance Junction to Ambient (@ 200 lfm)	Single–Layer Board Four–Layer Board	$R_{\theta JA}$	40 25	°C/W	1, 2
Thermal Resistance Junction to Board (Bottom)		$R_{\theta JB}$	17	°C/W	1, 3
Thermal Resistance Junction to Case (Top)		$R_{\theta JC}$	9	°C/W	1, 4

NOTES:
1. Junction temperature is a function of on–chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, board population, and board thermal resistance.
2. Per SEMI G38–87.
3. Indicates the average thermal resistance between the die and the printed circuit board.
4. Indicates the average thermal resistance between the die and the case top surface via the cold plate method (MIL SPEC–883 Method 1012.1).

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{DD} = 3.3 V + 10%, – 5%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (Voltages Referenced to V_{SS} = 0 V)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{DD}	3.135	3.3	3.6	V
Input Low Voltage	V_{IL}	– 0.5*	—	0.8	V
Input High Voltage	V_{IH}	2	—	5.5**	V

* $V_{IL} \geq -2$ V for $t \leq t_{KHKH}/2$.
** $V_{IH} \leq 6$ V for $t_{KHKH}/2$.

DC CHARACTERISTICS AND SUPPLY CURRENTS

Parameter		Symbol	Min	Max	Unit	Notes
Input Leakage Current (0 V ≤ V_{in} ≤ V_{DD}) (Excluding LBO)		$I_{lkg(I)}$	—	± 1	µA	
Output Leakage Current (0 V ≤ V_{in} ≤ V_{DD})		$I_{lkg(O)}$	—	± 1	µA	
AC Supply Current (Device Selected, All Outputs Open, Cycle Time ≥ t_{KHKH} min)	MCM69P536C–4	I_{DDA}	—	420	mA	1, 2, 3
	MCM69P536C–4.5			410		
	MCM69P536C–5			380		
	MCM69P536C–6			360		
	MCM69P536C–7			350		
CMOS Standby Supply Current (Deselected, Clock (K) Cycle Time ≥ t_{KHKH}, All Inputs Toggling at CMOS Levels $V_{in} \leq V_{SS}$ + 0.2 V or ≥ V_{DD} – 0.2 V)	MCM69P536C–4	I_{SB1}	—	170	mA	4
	MCM69P536C–4.5			170		
	MCM69P536C–5			150		
	MCM69P536C–6			140		
	MCM69P536C–7			130		
Clock Running Supply Current (Deselected, Clock (K) Cycle Time ≥ t_{KHKH}, All Other Inputs Held to Static CMOS Levels $V_{in} \leq V_{SS}$ + 0.2 V or ≥ V_{DD} – 0.2 V)	MCM69P536C–4	I_{SB2}	—	60	mA	4
	MCM69P536C–4.5			60		
	MCM69P536C–5			55		
	MCM69P536C–6			50		
	MCM69P536C–7			45		
Output Low Voltage (I_{OL} = 8 mA)		V_{OL}	—	0.4	V	
Output High Voltage (I_{OH} = – 4 mA)		V_{OH}	2.4	—	V	

NOTES:
1. Reference AC Operating Conditions and Characteristics for input and timing.
2. All addresses transition simultaneously low (LSB) and then high (HSB).
3. Data states are all zero.
4. Device in deselected mode as defined by the Truth Table.

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Parameter	Symbol	Min	Typ	Max	Unit
Input Capacitance	C_{in}	—	4	6	pF
Input/Output Capacitance	$C_{I/O}$	—	7	9	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{DD} = 3.3 V + 10%, – 5%, T_A = 0 to 70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level . . . . . 1.5 V
Input Pulse Levels . . . . . 0 to 3.0 V
Input Rise/Fall Time . . . . . 1 V/ns (20% to 30%)

Output Timing Reference Level . . . . . 1.5 V
Output Load . . . . . See Figure 1 Unless Otherwise Noted

READ/WRITE CYCLE TIMING (See Notes 1, 2, and 3)

Parameter	Symbol	69P536C–4		69P536C–4.5		69P536C–5		69P536C–6		69P536C–7		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Cycle Time	t_{KHKH}	7.5	—	8	—	10	—	12	—	13.3	—	ns	
Clock High Pulse Width	t_{KHKL}	3	—	3	—	3	—	4	—	4.5	—	ns	
Clock Low Pulse Width	t_{KLKH}	3	—	3	—	3	—	4	—	4.5	—	ns	
Clock Access Time	t_{KHQV}	—	4	—	4.5	—	5	—	6	—	7	ns	
Output Enable to Output Valid	t_{GLQV}	—	4	—	4.5	—	5	—	5	—	6	ns	
Clock High to Output Active	t_{KHQX1}	1.5	—	1.5	—	0	—	0	—	0	—	ns	4
Clock High to Output Change	t_{KHQX2}	1.5	—	1.5	—	2	—	2	—	2	—	ns	4
Output Enable to Output Active	t_{GLQX}	0	—	0	—	0	—	0	—	0	—	ns	4
Output Disable to Q High–Z	t_{GHQZ}	—	4	—	4.5	—	5	—	5	—	5	ns	4, 5
Clock High to Q High–Z	t_{KHQZ}	2	4	2	4.5	2	5	2	5	2	5	ns	4, 5
Setup Times: Address ADSP, ADSC, ADV Data In Write Chip Enable	t_{ADKH} t_{ADSKH} t_{DVKH} t_{WVKH} t_{EVKH}	2	—	2.5	—	2.5	—	2.5	—	2.5	—	ns	
Hold Times: Address ADSP, ADSC, ADV Data In Write Chip Enable	t_{KHAX} t_{KHADSX} t_{KHDX} t_{KHWX} t_{KHEX}	0.5	—	0.5	—	0.5	—	0.5	—	0.5	—	ns	

NOTES:
1. Write is defined as either any $\overline{SBx}$ and $\overline{SW}$ low or $\overline{SGW}$ is low. Chip Enable is defined as $\overline{SE1}$ low, SE2 high and $\overline{SE3}$ low whenever $\overline{ADSP}$ or ADSC is asserted.
2. All read and write cycle timings are referenced from K or $\overline{G}$.
3. G is a don't care after write cycle begins. To prevent bus contention, $\overline{G}$ should be negated prior to start of write cycle.
4. This parameter is sampled and not 100% tested.
5. Measured at ± 200 mV from steady state.

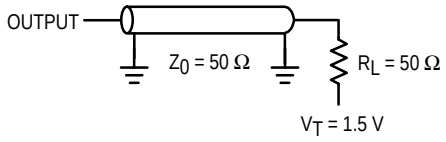
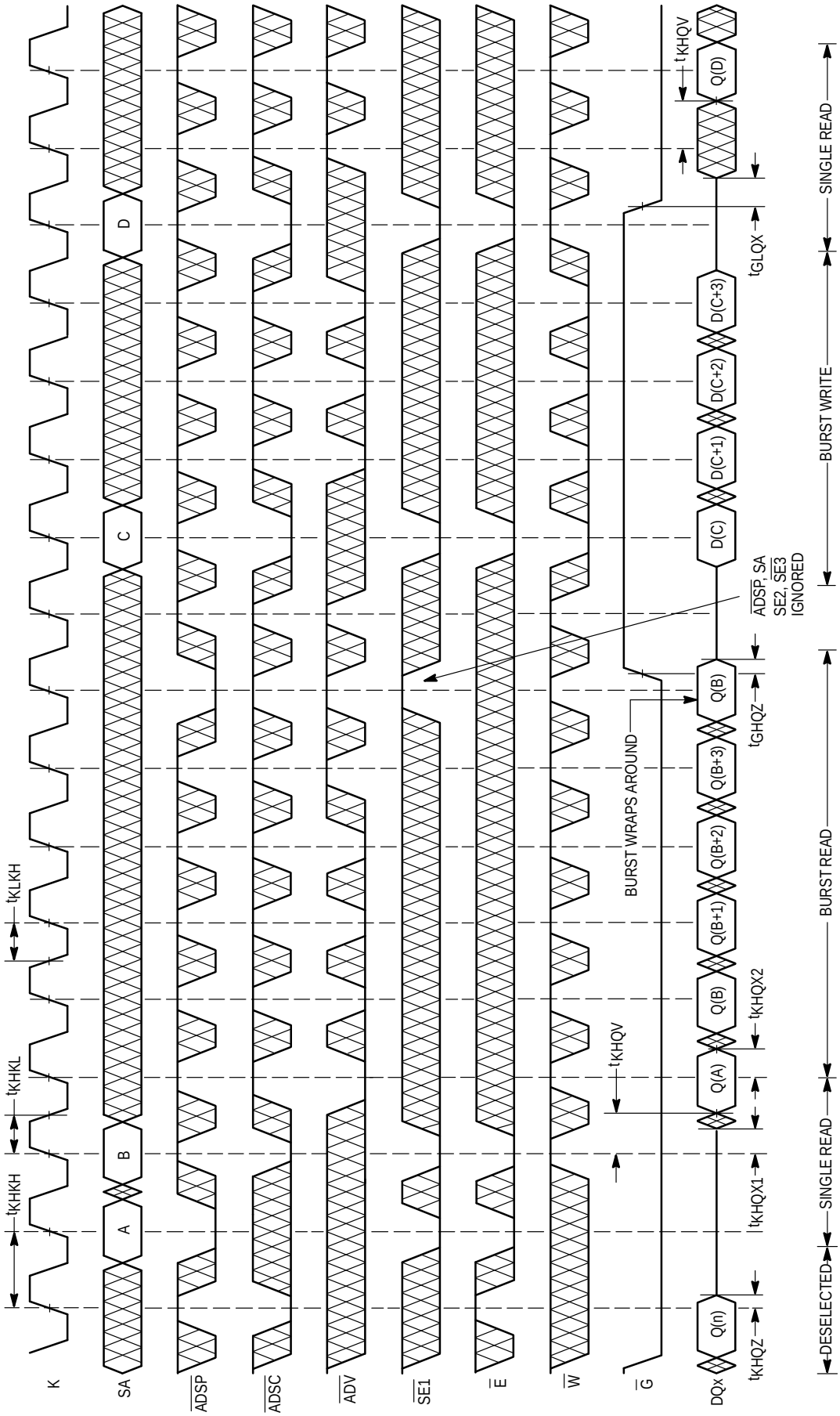


Figure 1. AC Test Load

READ/WRITE CYCLES



NOTE: $\overline{E}$ low = SE2 high and $\overline{SE3}$ low.
$\overline{W}$ low = $\overline{SGW}$ low and/or $\overline{SW}$ and $\overline{SBx}$ low.

APPLICATION INFORMATION

The MCM69P536C BurstRAM is a high speed synchronous SRAM that is intended for use primarily in secondary or level two (L2) cache memory applications. L2 caches are found in a variety of classes of computers — from the desktop personal computer to the high–end servers and transaction processing machines. For simplicity, the majority of L2 caches today are direct mapped and are single bank implementations. These caches tend to be designed for bus speeds in the range of 33 to 66 MHz. At these bus rates, non–pipelined (flow–through) BurstRAMs can be used since their access times meet the speed requirements for a minimum–latency, zero–wait state L2 cache interface. Latency is a measure (time) of "dead" time the memory system exhibits as a result of a memory request.

For those applications that demand bus operation at greater than 66 MHz or multi–bank L2 caches at 66 MHz, the pipelined (register/register) version of the 32Kx36 BurstRAM (MCM69P536C) allows the designer to maintain zero–wait state operation. Multiple banks of BurstRAMs create additional bus loading and can cause the system to otherwise miss its timing requirements. The access time (clock–to–valid–data) of a pipelined BurstRAM is inherently faster than a non–pipelined device by a few nanoseconds. This does not come without cost. The cost is latency — "dead" time.

Since most L2 caches are tied to the processor bus and bus speeds continue to increase over time, pipelined (R/R) BurstRAMs are the best choice in achieving zero–wait state L2 cache performance. At bus speeds ranging from 66 MHz to 100 MHz, pipelined BurstRAMs are able to provide fast clock to valid data times required of these high speed buses.

NON–BURST SYNCHRONOUS OPERATION

Although this BurstRAM has been designed for 68K–, PowerPC–, 486–, i960–, and Pentium–based systems, these SRAMs can be used in other high speed L2 cache or memory applications that do not require the burst address feature. Most L2 caches designed with a synchronous interface can make use of the MCM69P536C. The burst counter feature of the BurstRAM can be disabled, and the SRAM can be configured to act upon a continuous stream of addresses. See Figure 2.

CONTROL PIN TIE VALUES EXAMPLE ($H \geq V_{IH}$, $L \leq V_{IL}$)

Non–Burst	ADSP	ADSC	ADV	SE1	SE2	LBO
Sync Non–Burst, Pipelined SRAM	H	L	H	L	H	X

NOTE: Although X is specified in the table as a don't care, the pin must be tied either high or low.

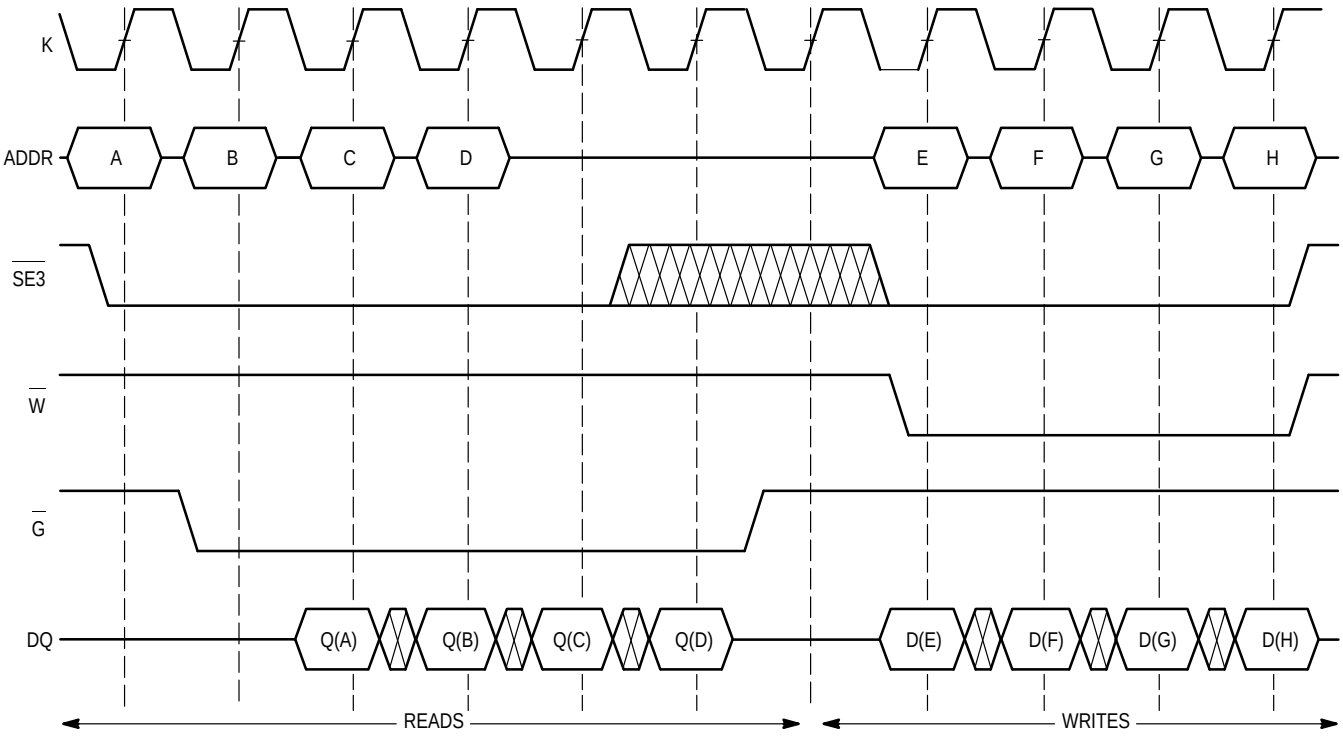
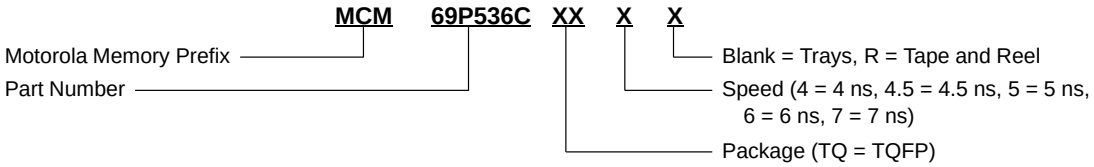


Figure 2. Example Configuration as Non–Burst Synchronous SRAM

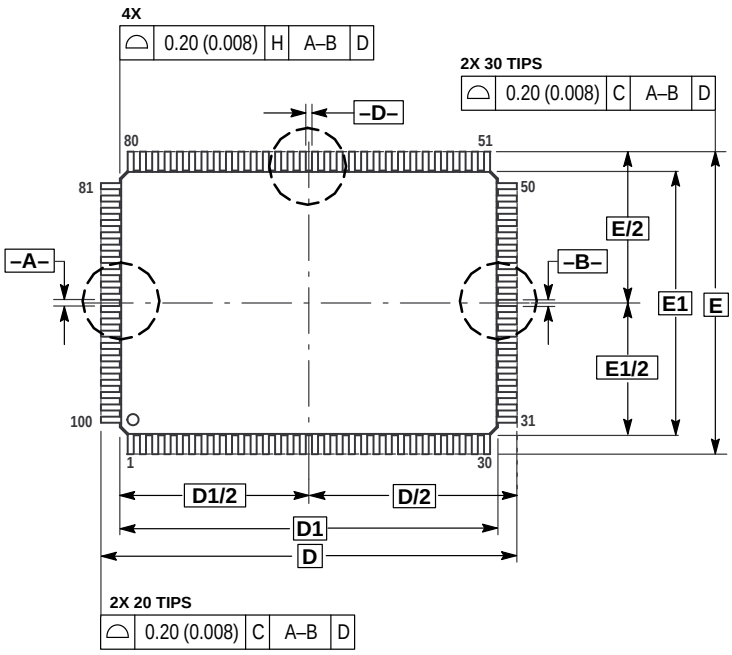
ORDERING INFORMATION
(Order by Full Part Number)

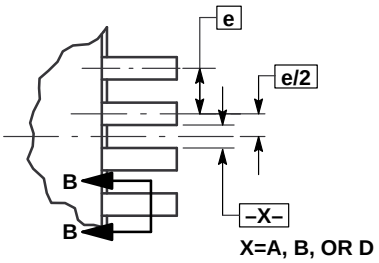


Full Part Numbers —		
	MCM69P536CTQ4	MCM69P536CTQ4R
	MCM69P536CTQ4.5	MCM69P536CTQ4.5R
	MCM69P536CTQ5	MCM69P536CTQ5R
	MCM69P536CTQ6	MCM69P536CTQ6R
	MCM69P536CTQ7	MCM69P536CTQ7R

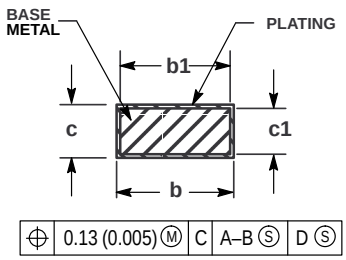
PACKAGE DIMENSIONS

TQ PACKAGE
TQFP
CASE 983A–01

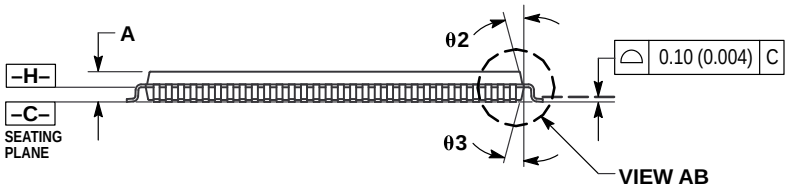


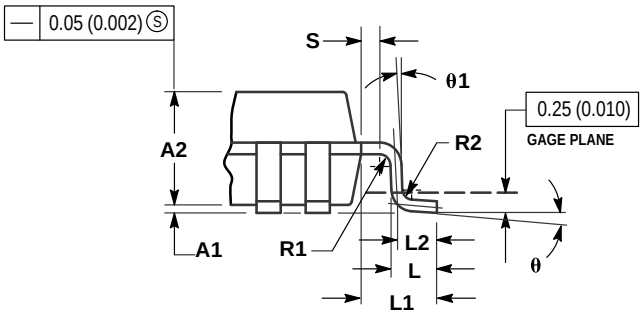


VIEW Y



SECTION B–B





VIEW AB

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE –H– IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS –A–, –B– AND –D– TO BE DETERMINED AT DATUM PLANE –H–.
5. DIMENSIONS D AND E TO BE DETERMINED AT SEATING PLANE –C–.
6. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 (0.010) PER SIDE. DIMENSIONS D1 AND B1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE –H–.
7. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE b DIMENSION TO EXCEED 0.45 (0.018).

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	—	1.60	—	0.063
A1	0.05	0.15	0.002	0.006
A2	1.35	1.45	0.053	0.057
b	0.22	0.38	0.009	0.015
b1	0.22	0.33	0.009	0.013
c	0.09	0.20	0.004	0.008
c1	0.09	0.16	0.004	0.006
D	22.00 BSC		0.866 BSC	
D1	20.00 BSC		0.787 BSC	
E	16.00 BSC		0.630 BSC	
E1	14.00 BSC		0.551 BSC	
e	0.65 BSC		0.026 BSC	
L	0.45	0.75	0.018	0.030
L1	1.00 REF		0.039 REF	
L2	0.50 REF		0.020 REF	
S	0.20	—	0.008	—
R1	0.08	—	0.003	—
R2	0.08	0.20	0.003	0.008
θ	0 °	7 °	0 °	7 °
θ1	0 °	—	0 °	—
θ2	11 °	13 °	11 °	13 °
θ3	11 °	13 °	11 °	13 °

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