M5M5408BFP/TP/RT/KV/KR

PRELIMINARY

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Some parametric limits are subject to change

4194304-BIT (524288-WORD BY 8-BIT) CMOS STATIC RAM

DESCRIPTION

The M5M5408B is a family of 4-Mbit static RAMs organized as 524,288-words by 8-bit, fabricated by Mitsubishi's high-performance 0.25µm CMOS technology.

The M5M5408B is suitable for memory applications where a simple interfacing , battery operating and battery backup are the important design objectives.

M5M5408B is packaged in 32-pin plastic SOP, 32-pin plastic TSOP and 32-pin 8mm x 13.4mm STSOP packages. Two types of TSOPs and two types of STSOPs are available , M5M5408BTP (normal-lead-bend TSOP) , M5M5408BRT (reverse-lead-bend TSOP) , M5M5408BKV (normal-lead-bend STSOP) and M5M5408BKR (reverse-lead-bend STSOP). These two types TSOPs and two types STSOPs are suitable for a surface mounting on double-sided printed circuit boards.

From the point of operating temperature, the family is divided into three versions; "Standard", "W-version", and "I-version". Those are summarized in the part name table below.

FEATURES

- Single +5V power supply
- Small stand-by current: 0.4µA(3V,typ.)
- No clocks, No refresh
- Data retention supply voltage=2.0V to 5.5V
- All inputs and outputs are TTL compatible.
- Easy memory expansion by $\overline{S}$
- Common Data I/O
- Three-state outputs: OR-tie capability
- $\overline{OE}$ prevents data contention in the I/O bus
- Process technology: 0.25µm CMOS
- Package:
  M5M5408BFP: 32 pin 525 mil SOP
  M5M5408BTP/RT: 32 pin 400 mil TSOP(II)
  M5M5408BKV/KR: 32 pin 8mm x 13.4mm STSOP

PART NAME TABLE

Version, Operating temperature	Part name (## stands for "FP","TP", "RT","KV"or"KR")	Power Supply	Access time max.	Stand-by current $I_{CC(PD)}$, Vcc=3.0V			Active current Icc1 (5.0V, typ.)
				typical *	Ratings (max.)		
				25°C	70°C	85°C	
Standard 0 ~ +70°C	M5M5408B## -55L	5.0V	55ns	---	50µA	---	50mA (10MHz) 25mA (1MHz)
	M5M5408B## -70L		70ns				
	M5M5408B## -10L		100ns				
	M5M5408B## -55H	5.0V	55ns	0.4µA	10µA	---	
	M5M5408B## -70H		70ns				
	M5M5408B## -10H		100ns				
W-version -20 ~ +85°C	M5M5408B## -55LW	5.0V	55ns	---	---	100µA	
	M5M5408B## -70LW		70ns				
	M5M5408B## -10LW		100ns				
	M5M5408B## -55HW	5.0V	55ns	0.4µA	---	20µA	
	M5M5408B## -70HW		70ns				
	M5M5408B## -10HW		100ns				
I-version -40 ~ +85°C	M5M5408B## -55LI	5.0V	55ns	---	---	100µA	
	M5M5408B## -70LI		70ns				
	M5M5408B## -10LI		100ns				
	M5M5408B## -55HI	5.0V	55ns	0.4µA	---	20µA	
	M5M5408B## -70HI		70ns				
	M5M5408B## -10HI		100ns				

* "typical" parameter is sampled, not 100% tested.

M5M5408BFP/TP/RT/KV/KR

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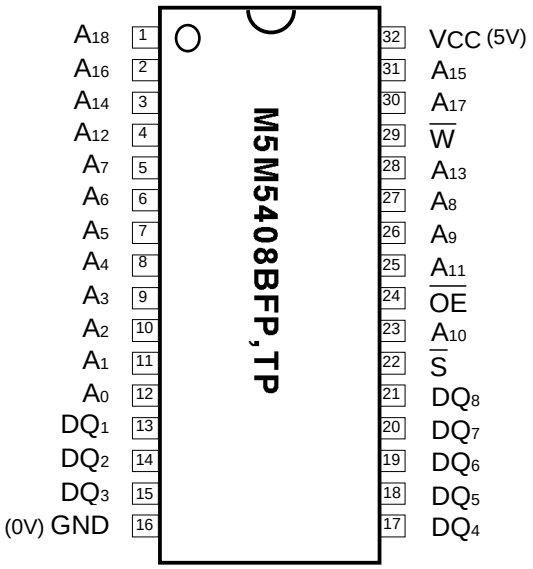
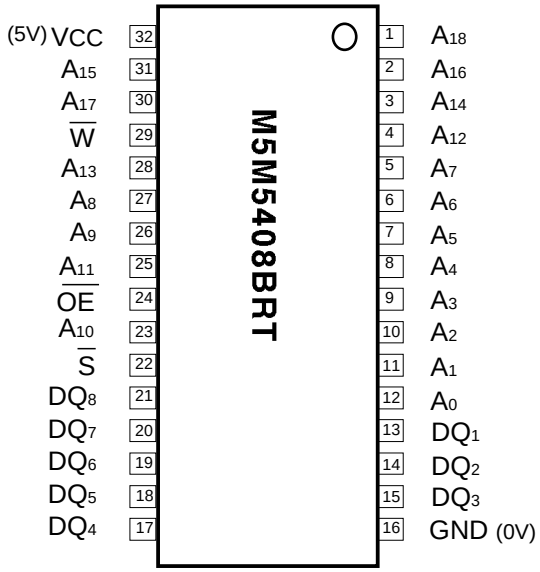
4194304-BIT (524288-WORD BY 8-BIT) CMOS STATIC RAM

PIN CONFIGURATION (TOP VIEW)

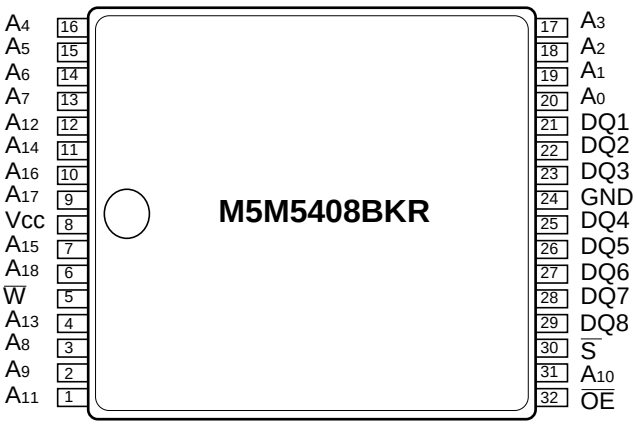


Outline 32P2M-A (FP)
32P3Y-H (TP)



Outline 32P3Y-J (RT)

Outline 32P3K-B



Outline 32P3K-C

M5M5408BFP/TP/RT/KV/KR

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4194304-BIT (524288-WORD BY 8-BIT) CMOS STATIC RAM

FUNCTION

The M5M5408BFP,TP,RT,KV,KR is organized as 524,288-words by 8-bit. These devices operate on a single +5.0V power supply, and are directly TTL compatible to both input and output. Its fully static circuit needs no clocks and no refresh, and makes it useful.

A write operation is executed during the $\overline{S}$ low and $\overline{W}$ low overlap time. The address(A0~A18) must be set up before the write cycle

A read operation is executed by setting $\overline{W}$ at a high level and $\overline{OE}$ at a low level while S are in an active state($\overline{S}$=L).

When setting $\overline{S}$ at a high level, the chips are in a non-selectable mode in which both reading and writing are disabled. In this mode, the output stage is in a high-impedance state, allowing OR-tie with other chips. Setting the $\overline{OE}$ at a high level,the output stage is in a high-impedance state, and the data bus contention problem in the write cycle is eliminated.

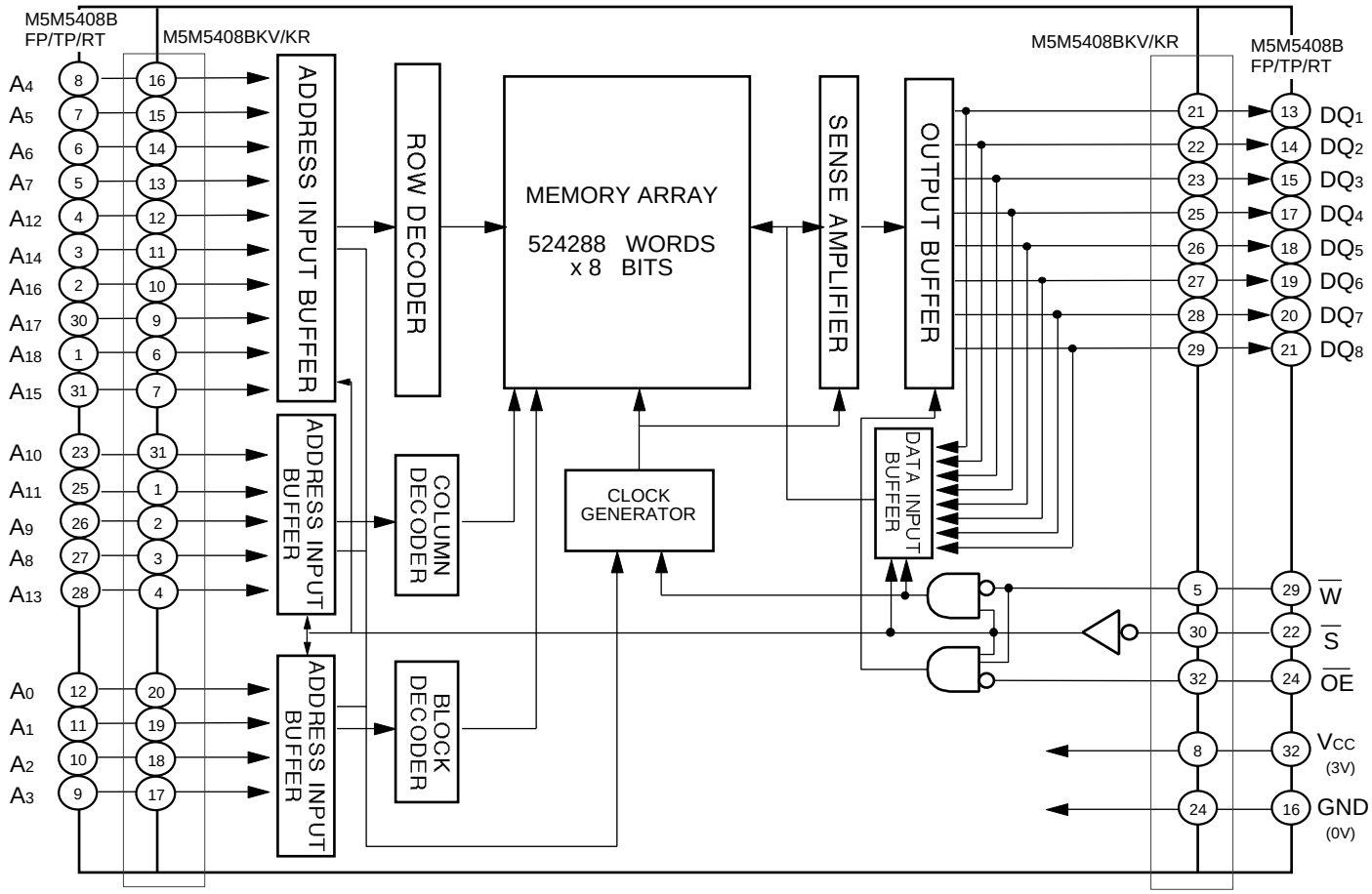
The power supply current is reduced as low as 0.4μA(25°C, typical), and the memory data can be held at +2V power supply, enabling battery back-up operation during power failure or power-down operation in the non-selected mode.

FUNCTION TABLE

$\overline{S}$	$\overline{W}$	$\overline{OE}$	Mode	DQ	Icc
H	X	X	Non selection	High-impedance	Standby
L	L	X	Write	Data input (D)	Active
L	H	L	Read	Data output (Q)	Active
L	H	H	Read	High-impedance	Active

Pin	Function
A0 ~ A18	Address input
DQ1 ~ DQ8	Data input / output
$\overline{S}$	Chip select input
$\overline{W}$	Write control input
$\overline{OE}$	Output inable input
Vcc	Power supply
GND	Ground supply

BLOCK DIAGRAM



M5M5408BFP/TP/RT/KV/KR

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4194304-BIT (524288-WORD BY 8-BIT) CMOS STATIC RAM

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Units
V_{CC}	Supply voltage	With respect to GND	-0.3* ~ +7	V
V_I	Input voltage	With respect to GND	-0.3* ~ Vcc + 0.3	
V_O	Output voltage	With respect to GND	0 ~ Vcc	
P_d	Power dissipation	Ta=25°C	700	mW
T_a	Operating temperature	Standard (-L, -H)	0 ~ +70	°C
		W-version (-LW, -HW)	-20 ~ +85	
		I-version (-LI, -HI)	-40 ~ +85	
T_{stg}	Storage temperature		-65 ~150	°C

* -3.0V in case of AC (Pulse width ≤ 30ns)

DC ELECTRICAL CHARACTERISTICS

(Vcc=5V±10%, unless otherwise noted)

Symbol	Parameter	Conditions		Limits Min	Limits Typ	Limits Max	Units
V_{IH}	High-level input voltage			2.2		Vcc+0.3V	V
V_{IL}	Low-level input voltage			-0.3 *		0.8	
V_{OH1}	High-level output voltage 1	I_{OH}= -1mA		2.4			
V_{OH2}	High-level output voltage 2	I_{OH}= -0.1mA		Vcc-0.5V			
V_{OL}	Low-level output voltage	I_{OL}=2mA				0.4	
I_I	Input leakage current	V_I =0 ~ Vcc				±1	µA
I_O	Output leakage current	$\overline{S}$=V_{IH} or $\overline{OE}$=V_{IH}, $V_{I/O}$=0 ~ Vcc				±1	
Icc1	Active supply current (AC,MOS level)	$\overline{S}$ ≤0.2V Output-open Other inputs ≤0.2V or ≥Vcc-0.2V	minimum cycle	-	50	80	mA
			f= 1MHz	-	25	30	
Icc2	Active supply current (AC,TTL level)	$\overline{S}$=VIL Output-open Other inputs=V_{IH} or V_{IL}	minimum cycle	-	60	90	
			f= 1MHz	-	30	40	
Icc3	Stand by supply current (AC,MOS level)	$\overline{S}$ ≥Vcc-0.2V Other inputs=0~Vcc	-LW, -LI	-	-	200	µA
			-L	-	-	100	
			-HW, -HI	-	0.4	40	
			-H	-	0.4	20	
Icc4	Stand by supply current (AC,TTL level)	$\overline{S}$=V ,Other inputs= 0 ~ Vcc		-	-	3	mA

Note 1: Direction for current flowing into IC is indicated as positive (no mark)
Note 2: Typical value is for Vcc=5.0V and Ta=25°C

* -3.0V in case of AC (Pulse width ≤ 50ns)

CAPACITANCE

(Vcc=5.0V±10%, unless otherwise noted)

Symbol	Parameter	Conditions	Limits Min	Limits Typ	Limits Max	Units
C_I	Input capacitance	V_I=GND, V_I=25mVrms, f=1MHz			8	pF
C_O	Output capacitance	V_O=GND,V_O=25mVrms, f=1MHz			10	

M5M5408BFP/TP/RT/KV/KR

PRELIMINARY

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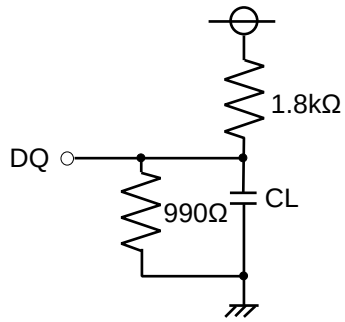
AC ELECTRICAL CHARACTERISTICS (Vcc=5.0V±10%, unless otherwise noted)

(1) TEST CONDITIONS

Supply voltage	5.0V
Input pulse	VIH=2.4V,VIL=0.6V (FP,TP,RT,KV,KR-70,-10) VIH=3.0V,VIL=0V (FP,TP,RT,KV,KR-55)
Input rise time and fall time	5ns
Reference level	VOH=VOL=1.5V Transition is measured ±500mV from steady state voltage.(for ten,tdis)
Output loads	Fig.1, CL=100pF (FP,TP,RT,KV,KR-70,-10) CL=30pF (FP,TP,RT,KV,KR-55) CL=5pF (for ten,tdis)



CL Including scope and jig capacitance

Fig.1 Output load

(2) READ CYCLE

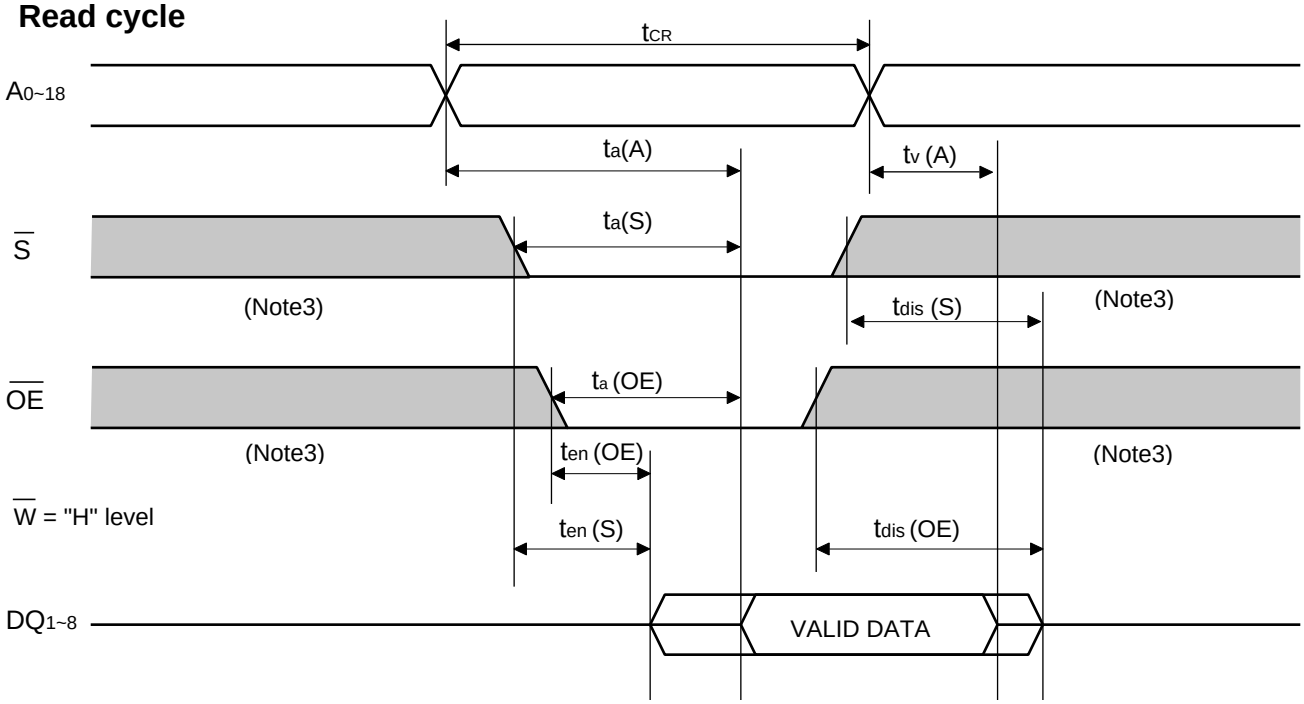
Symbol	Parameter	Limits						Units
		M5M5408BFP,TP,RT, KV,KR-55		M5M5408BFP,TP,RT, KV,KR-70		M5M5408BFP,TP,RT, KV,KR-10		
		Min	Max	Min	Max	Min	Max	
t_{CR}	Read cycle time	55		70		100		ns
t_a(A)	Address access time		55		70		100	ns
t_a(S)	Chip select access time		55		70		100	ns
t_a(OE)	Output enable access time		25		35		50	ns
t_{dis}(S)	Output disable time after $\overline{S}$ high		20		25		35	ns
t_{dis}(OE)	Output disable time after $\overline{OE}$ high		20		25		35	ns
t_{en}(S)	Output enable time after $\overline{S}$ low	10		10		10		ns
t_{en}(OE)	Output enable time after $\overline{OE}$ low	5		5		5		ns
t_v(A)	Data valid time after address	10		10		10		ns

(3) WRITE CYCLE

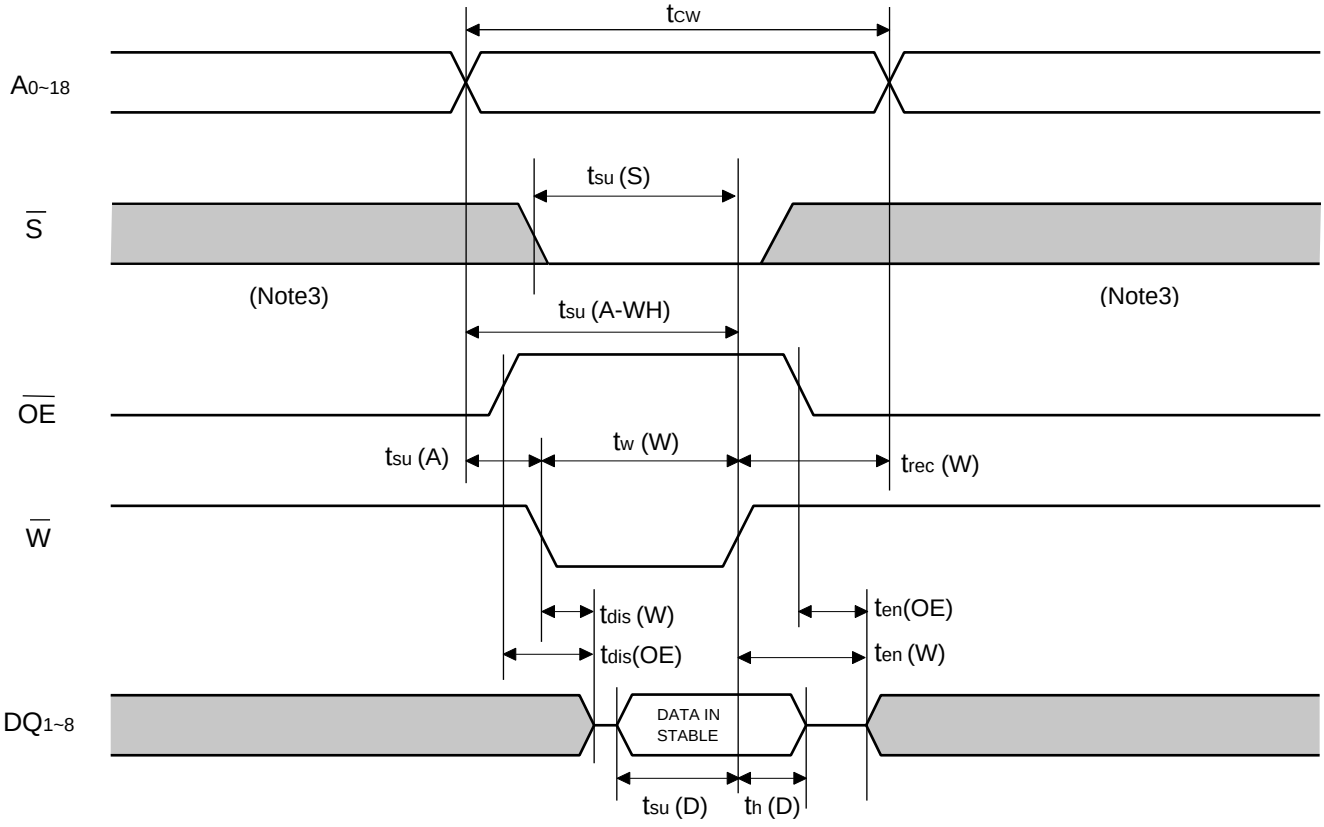
Symbol	Parameter	Limits						Units
		M5M5408BFP,TP,RT, KV,KR-55		M5M5408BFP,TP,RT, KV,KR-70		M5M5408BFP,TP,RT, KV,KR-10		
		Min	Max	Min	Max	Min	Max	
t_{CW}	Write cycle time	55		70		100		ns
t_w(W)	Write pulse width	40		50		60		ns
t_{su}(A)	Address set up time	0		0		0		ns
t_{su}(A-WH)	Address set up time with respect to $\overline{W}$ high	50		60		80		ns
t_{su}(S)	Chip select set up time	50		60		80		ns
t_{su}(D)	Data set up time	25		30		35		ns
t_h(D)	Data hold time	0		0		0		ns
t_{rec}(W)	Write recovery time	0		0		0		ns
t_{dis}(W)	Output disable time after $\overline{W}$ low		20		25		35	ns
t_{dis}(OE)	Output disable time after $\overline{OE}$ high		20		25		35	ns
t_{en}(W)	Output enable time after $\overline{W}$ high	5		5		5		ns
t_{en}(OE)	Output enable time after $\overline{OE}$ low	5		5		5		ns

(4)TIMING DIAGRAMS

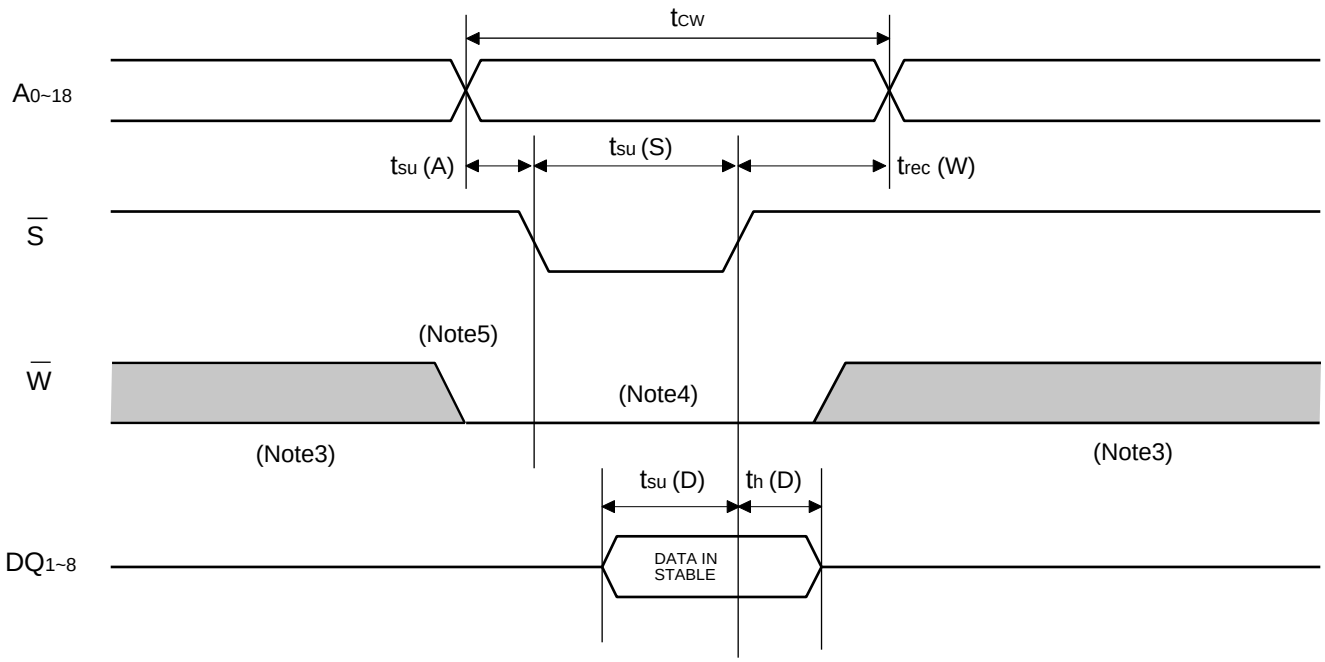
Read cycle



Write cycle (W control mode)



Write cycle ($\overline{S}$ control mode)



Note 3: Hatching indicates the state is "don't care".

Note 4: A Write occurs during the overlap of a low $\overline{S}$ and a low $\overline{W}$.

Note 5: If $\overline{W}$ goes low simultaneously with or prior to $\overline{S}$,the output remains in the high impedance state.

Note 6: Don't apply inverted phase signal externally when DQ pin is in output mode.

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POWER DOWN CHARACTERISTICS

(1) ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		Limits			Units
				Min	Typ.	Max	
V_{CC} (PD)	Power down supply voltage			2	-	-	V
V_I ($\overline{S}$)	Chip select input $\overline{S}$	Vcc(PD) ≥ 2.2V		2.2	-	-	V
		2.2V ≥ Vcc(PD) ≥ 2.0V		-	Vcc(PD)	-	V
I_{CC} (PD)	Power down supply current	Vcc=3.0V, $\overline{S}$≥Vcc-0.2V, Other inputs=0 ~ Vcc	-LW, -LI	-	-	100	µA
			-L	-	-	50	µA
			-HW, -HI	-	0.4	20	µA
			-H	-	0.4	10	µA

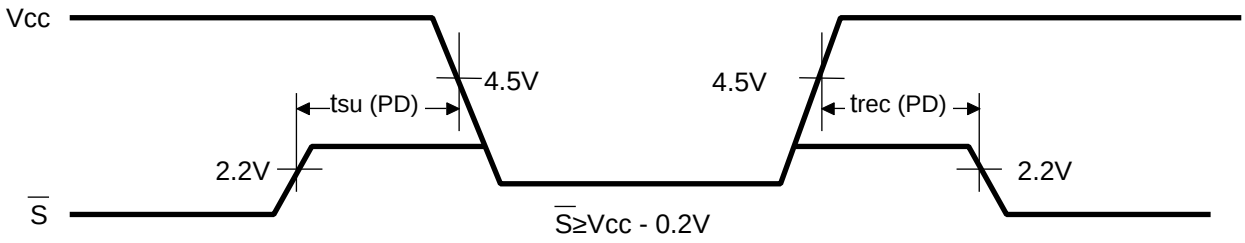
Typical value is for Ta=25°C

(2) TIMING REQUIREMINTS

Symbol	Parameter	Test conditions	Limits			Units
			Min	Typ	Max	
t_{su} (PD)	Power down set up time		0			ns
t_{rec} (PD)	Power down recovery time		5			ms

(3) TIMING DIAGRAM

$\overline{S}$ control mode



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Revision History

Revision No.	History	Date	
K0.1e	The first edition	'98.7.30	Preliminary